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An Integrated Chip High-Voltage Power Receiver for Wireless Biomedical Implants

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Abstract: In near-field wireless-powered biomedical implants, the receiver voltage largely overrides the compliance of low-voltage power receiver systems. To limit the induced voltage, generally, low-voltage topologies utilize limiter circuits, voltage clippers or shunt regulators, which are power-inefficient methods. In order to overcome the voltage limitation and improve power efficiency, we propose an integrated chip high-voltage power receiver based on the step down approach. The topology accommodates voltages as high as 30 V and comprises a high-voltage semi-active rectifier, a voltage reference generator and a series regulator. Further, a battery management circuit that enables safe and reliable implant battery charging based on analog control is proposed and realized. The power receiver is fabricated in 0.35-µm high-voltage Bipolar-CMOS-DMOStechnology based on the LOCOS0.35-µm CMOS process. Measurement results indicate 83.5% power conversion efficiency for a rectifier at 2.1 mA load current. The low drop-out regulator based on the current buffer compensation and buffer impedance attenuation scheme operates with low quiescent current, reduces the power consumption and provides good stability. The topology also provides good power supply rejection, which is adequate for the design application. Measurement results indicate regulator output of 4 \pm 0.03 V for input from 5 to 30 V and 10 \pm 0.05 V output for input from 11 to 30 V with load current 0.01–100 mA. The charger circuit manages the charging of the Li-ion battery through all if the typical stages of the Li-ion battery charging profile.

Keywords: high-voltage bridge rectifier; low drop-out voltage; regulator; battery charger circuit; power efficiency; wireless power receiver

1. Introduction

Wireless power transmission (WPT) technology has significantly developed in the field of consumer electronics and implantable biomedical devices in recent years. To ensure long-term reliability and to improve device portability, these devices demand for power-efficient and compact physical design. In biomedical devices, such as neural stimulator aiding nerve repair and cochlear implant, power is transmitted by inductive links to enhance the operational lifetime of the implant batteries [1-4]. The inductive near-field link supplies essential power to the bio-microsystem, which requires high stimulation currents for the large cuff-electrode interface nerve impedance (cuff-electrode nerve interface impedance at time of implant: 0.7 K Ω [4], 4.5 K Ω [5], 0.35 K Ω [6], 0.4 K Ω [7]). Therefore, the received voltage at the receiver end (Rx) will be high in magnitude and exceeds the compliance of low-voltage (LV) integrated chips (IC). Generally, to overcome the high-voltage (HV) limitation, voltage limiters or Zener diodes, as in [2,8-10], or shunt regulators, as in [11], are employed. These approaches limit the supply voltage to 5 V, but the power efficiency of the system decreases, as the excess power is heat dissipated or grounded. Moreover, the cuff electrode-nerve interface impedance gradually increases after the time of implant. Table 1 shows monitored cuff electrode-nerve interface impedance variations published in prior artworks. Therefore, to meet the necessary system requirements, typically a 0.03–2 mA [12,13] stimulation current for an interface impedance of 1–8 K Ω , the supply voltage is increased correspondingly. For example; to source 2-mA current through a 5-K Ω resistor, a supply of 10 V is required. Hence, prior LV approaches become unsuitable for implementation and, thus, the HV approach is recommended.

Table 1. Monitore	d cuff nerve-ele	ectrode interface i	mpedance in prior	works.
Ref [3]	Ref [4]	Ref [5]	Ref [6]	Ref [7

	Ref [3]	Ref [4]	Ref [5]	Ref [6]	Ref [7]
Monitored Time Period	8 months	Day 1–Day 40	Day 1–Day 10	Day 7–Day 28	Minute 1– Minute 10000
Resultant Impedance	greater than 4 KΩ	0.7 ΚΩ–1.2 ΚΩ	4.5 ΚΩ–8 ΚΩ	0.35 ΚΩ–0.49 ΚΩ	0.4 ΚΩ–1.5 ΚΩ

In consideration of a real-time system for a neural stimulator (current >800 μ A from 3.7 V for a control system, 2-mA stimulation pulses from 10 V for nerve stimulation [14]), a dual supply is necessary for the system. Generally, there are two approaches to generate dual supplies for inductive power receivers employing a shunt regulator topology: (1) the step down and (2) the step up approach [3]. Referring to the theoretical studies published in [15] and the system requirements [14], the step down approach proves to be more efficient, if the converter preceding the rectifier has more than 40% efficiency and the output impedance of the DC-DC converter is less than 10 K Ω . Thus, an approach based on IC that do not limit Rx voltage may be a more effective solution for neural stimulator application. A power receiver IC, realized in HV technology, includes a high input voltage rectifier and step down buck converter [11], which stores the excess power in a filter capacitor, leading to higher rectified voltage, and omits prior voltage-limiting circuits [2,8–10]. However, for the on-chip buck converter, it is difficult to maintain good power efficiency and regulation quality. Besides, it is not suitable to integrate a large inductor and capacitor on the chip. An alternate and suitable technique may be to integrate a linear voltage regulator.

In [3,16], IC based on the HV process for receivers in implantable device showed improved power efficiency based on simulation results. An HV IC power recovery system for contact-less memory card [17] reported 50% power efficiency at a higher supply voltage. However, the system feature size and its low power efficiency made it unsuitable for biomedical implantation. An IC with HV compliance was fabricated for epi-retinal and neural prostheses [18], consisting of HV half-bridge rectifiers, but the efficiency of the half bridge structure is comparatively less and not advisable for a power-efficient design.

This paper propose the design fabrication of an IC for power recovery in the HV process based on the step down voltage approach and a battery management circuit for safe and reliable charging of the implant battery. The paper is detailed as follows. Section 2 briefly describes the system architecture. Section 3 describes the methodology and design specification. Section 4 explains the conventional and proposed circuit techniques. Section 5 presents the simulation and experimental results, and Section 6 concludes the paper. The chip is fabricated with a 5060BD35BA BCD0.35 μ m 60-V process at the Dongbu Hitek foundry.



Figure 1. Block diagram of the wireless power and data transfer chain for the neurostimulator.

2. Architectural Overview of the System

The neural stimulator comprises an external power transmission module and an internal power receiver module (body implant). The conventional system block of the neural-stimulator system is illustrated in Figure 1 [13,14]. Using inductively-coupled coils, energy is transmitted from the external module to the implant with an operating frequency of 13.56 MHz within the Industrial Scientific Medical (ISM) band specifications. To control and monitor the sequence of wireless power transmission and reception between the modules, data modules are also incorporated in the system. The external

power amplifier module generates the necessary power for the implant based on the feedback from the internal module. The user interface enables the user to systematically monitor, interrupt and control the power transmission process with the aid of a micro-controller unit, the data transceiver, the data modulator/demodulator and the power amplifier unit. The class-E-type power amplifier generates the signal based on load requirements, and the impedance matching network assists the system to obtain maximum power transfer efficiency [19]. The power and data are transferred through separate coils, with the data coil performing an additional task of receiving the feedback signals from the internal module.

The internal module constitutes the high-voltage power recovery circuits and low-voltage data receiver circuits. The HV receiver provides essential power to the high stimulation current stages directly, to meet the load current requirements for cuff-electrode nerve interface impedance. The rest of the circuits operates at low-voltage conditions, which is powered from the implant battery. The battery is charged with the aid of a control circuitry after the voltage is stepped down to the required level, which is discussed in the following sections. The data receiver unit collects the data signal, processes it and provides it to the control unit and field programmable logic device (FPGA) for interpretation. The control and FPGA unit monitor and control the current stimulation process based on user commands and feedback, through signal de-multiplexer stages integrated with bipolar cuff-electrodes. The emitter and antenna within the implant are responsible for sending feedback to the user for continuous monitoring of the operation. The oscillator provides the necessary clock signals for the FPGA and the monitoring stage. The neural stimulator consists of two stimulation stages for neural regeneration, a high current stimulation stage powered directly by the high-voltage receiver and the continuous low-current stimulator powered by the battery.

3. Design Approach and System Specification

3.1. Implementation Method

The system focuses on the design and integration of an HV power recovery scheme for neural stimulator application. The topology includes a rectifier, voltage and current references, a linear voltage regulator and a battery charger for the implant system. The rectifier rectifies the inductive voltage and stores in the filter capacitor. The rectified voltage supplied to the series regulator provides for stable and regulated output voltage. The regulator, based on the switch control, directs the output towards the high voltage and current stimulus generator or towards the battery charger circuit. The start-up circuit coupled with the reference circuit generates the essential bias current and voltage for the regulator and charger circuit. The implemented power recovery topology is shown in Figure 2. In general, for biomedical system applications, the power efficiency is of high significance. Therefore, the total system efficiency constituted by the sub-circuits is the main constraint of the design. The total system efficiency (η_{totsys}) is given by:

$$\eta_{totsys} = \eta_{Source} * \eta_{coillink} * \eta_{recti} * \eta_{LDO} * \eta_{charger} \tag{1}$$

where η_{source} is efficiency of the RF source, $\eta_{coillink}$ is the efficiency of the wireless link, η_{recti} is the power conversion efficiency of the rectifier (PCE), η_{LDO} is the regulator efficiency and η_{cont} is the efficiency of the battery charger.



Figure 2. Schematic block of the power recovery topology in the neurostimulator.

3.2. Design Specification

For neural stimulator implants, pulse current waveforms are supplied for nerve repair. Based on the availability of the supply power, the magnitude of the stimulus current varies with time intervals. A continuous low current stimuli in the magnitude of order 30 μ A at 100 Hz [4,12,13] is provided for longer intervals of time powered from the battery. The high stimulation current of magnitude range 0.8–2 mA [3,4,12,13] is supplied for shorter time intervals. Though conventional LV schemes are favorable for high current stimulation at the initial stages of implant, over the course of time, the cuff-nerve electrode interface impedance of the implant rises [3,4,12,13] and the LV schemes become unsuitable. Thus, to essentially supply the high stimulation currents for implants with increasing cuff-nerve electrode interface impedance, the supply voltage is raised gradually. The voltage at the initial stage of the implant in the range of 3.3–5 V is raised to 10–20 V. This requirement is met by the design of the IC based on HV technology in the BCD process. The rest of the system functions from the power supplied from the lithium-ion (Li-ion) battery used in the system. The battery has a rating of 3.7 V and 20 mAh and is used because of its compact size and cost effectiveness.

4. Circuit Design Methodology

4.1. High-Voltage Bridge Rectifier

In general, diode bridges constitute rectifiers. However, due to the large voltage drops of the diode and low PCE, they are not suitable for on-chip rectification. To compensate the voltage drop, low threshold voltage transistors are employed that involve higher fabrication costs. A more effective and less expensive solution to the problem is provided by utilizing active diodes, threshold cancellation techniques, cross-coupled bridge techniques and comparator-based techniques. The prior rectifiers based on threshold cancellation techniques suffer from low PCE [20]. The cross-coupled bridge rectifier [21,22] improves the PCE, but was confined to less than 70%, due to the reverse leakage current in the non-conducting phase of the rectifier. Further, a series of works based on comparator techniques [1,2,9,23] showed higher PCE at lower frequencies. However, the speed of the comparator plays a crucial role to achieve high PCE, and for higher frequencies, the comparator design is a challenging task.

The earlier works are unsuitable for the proposed application due to the input voltage constraint, comparably low PCE, the operating frequencies and complicated circuit calibration. In the HV process, the technology library offers limited design flexibility for HV transistors. Besides this, our technology also limits the gate to source voltage (V_{GS}) for all HV transistors to 13.2 V, which prevents earlier works from being implemented for the HV application. In [3], the designed HV rectifier indicated 93% PCE based on the simulation results, but measurement results indicate heavy loading of the rectifier above a 1-mA load current and resulted in latch-up and breakdown of the rectifier. Later, the work in [16] showed the implementation of a half wave rectifier structure to prevent latch-up for higher load current conditions. However, since the rectifier was a half wave structure, the PCE obtained is low.

To accommodate high input voltage and to obtain high PCE for higher load currents in neural stimulator application, an HV bridge rectifier technique is proposed. The circuit schematic of the designed rectifier is shown in Figure 3. The rectifier is based on a partial and adaptive threshold cancellation technique of the N-type HV LDMOStransistor switches (HVM3, HVM4). The gates of HVM3 and HVM4 are biased to an average voltage of approximately 68% of the threshold voltage (V_{th}). The bias circuits are formed with cross-coupled resistors (Rb1, Rb2), diode connected transistors (HVM5, HVM6) and capacitors (Cb1, Cb2). To attain the suitable bias voltage for conducting and non-conducting phases, the bias network components are effectively sized. The dynamic bias voltage tracks the V_{th} of HVM3 and HVM4 for various temperature and process conditions. For bridge transistors in the conduction phase, but increases the leakage current in the non-conduction phase. Thus, the bias voltage should be effectively determined without complete cancellation of V_{th} . In this design, the bias voltage increases to 94% in the conduction phase and decreases to 41% in the non-conduction phase of the V_{th} .

Bi-directional P-type switches HVM1 and HVM2 are connected with the gate cross-coupled as in Figure 3, with a unique set of HV P-type transistors offered by technology that does not have the V_{GS} limitation. This allows one to obtain higher PCE in comparison to the diode connected transistor configuration reported in [14], but at the cost of area consumption. Since the default length of the HVM1 and HVM2 used is high compared to other HV transistors, to reduce the on-resistance, the width of the transistor is increased. Furthermore, the bulk biasing scheme employed helps to reduce the substrate leakage current and effectively increase the PCE [9].



Figure 3. Circuit schematic of the proposed high-voltage rectifier.

4.2. High-Voltage Reference and Bias Current Generator

The voltage reference and bias current generators are designed in reference to the sub-threshold MOSFET technique [24]. Prior work published is for low-voltage applications below 1.8 V. However, the proposed design includes an LV-HV cascading [25] scheme to overcome the input voltage limitation and contain a higher supply voltage. The implemented circuit schematic of the reference voltage and bias current generator [14] is shown in Figure 4. Transistors LVM13 and LVM14 operated in the sub-threshold region generate supply voltage independently, proportional to absolute temperature (PTAT) current I_A . Further, a complimentary to the absolute temperature (CTAT) current I_B is independent of the supply voltage fluctuations generated by LVM5, also operated in the sub-threshold regime. In addition, to compensate for channel length modulation effects that reflect the reference voltage, current I_A is mirrored (K_8/K_9) times and subtracted from $(V_{GSLVM4})/R1$ to form I_B . The desired independent supply voltage, and the zero temperature coefficient reference voltage is obtained by mirroring the currents I_A and I_B over transistors LVM15 and LVM16 and allowing the summed currents to pass over resistor R_a $(R_a = R3 + R4 + R5)$. The summed current is expressed as I_{REF} , and the reference voltage is given by:

$$V_{REF} = \left(\frac{K_{LVM15}}{K_{LVM10}}I_A + \frac{K_{LVM16}}{K_{LVM6}}I_B\right)R_a \tag{2}$$

where,

$$I_{A} = \frac{V_{GSLVM13} - V_{GSLVM14}}{R2} = \frac{\zeta V_{T} ln\left(\frac{K_{LVM13}}{K_{LVM14}}\right)}{R2}; \quad I_{B} = \frac{V_{GSLVM4}}{R1} - \frac{K_{LV8}}{K_{LV9}}I_{A}$$
(3)

Additionally, K is the aspect ratio of the transistors, Ris the resistor, V_{GS} is the gate to source voltage, $\zeta > 1$ is a non-ideal factor and $V_T = \text{KT/q}$ is the thermal voltage. A startup circuitry is also included for the initial excitation of the reference generator.



Figure 4. Circuit schematic of voltage and current reference generator with the startup circuit.

4.3. High Input Voltage Linear Regulator

The HV low drop-out (LDO) voltage regulator is designed to provide 4-V and 10-V output with a maximum input voltage of 30 V and delivers a maximum output current of 100 mA. The LDO comprises a p-type LDMOS pass transistor, an error amplifier, a resistance feedback network, a buffer and an output capacitor. The conventional LDO with an intermediate driver stage is depicted in Figure 5a for which the poles and zeros are represented by the following equations.

$$P_{1:Node1} = \frac{1}{r_{o1}C_{1}}; \quad P_{2:Node2} = \frac{1}{r_{obuff}C_{pass}}; \quad P_{3:Node3} = \frac{1}{R_{oLDO}C_{out}}; \quad z_{1:Node1} = \frac{1}{R_{ESR}C_{out}}$$
(4)

where r_{o1} is the output resistance of the amplifier, C_1 the effective capacitance at Node 1, r_{obuff} is the buffer output resistance, C_{pass} the input capacitance of pass transistor, R_{oLDO} is the effective output resistance of the LDO, C_{out} is the output capacitor and R_{ESR} is the ESR of the output capacitor.

For LDOs that source high load current, the pass transistor is large in size to reduce the dropout voltage [26]. Therefore, in stability analysis, a pole P_2 , is generated by the large gate capacitance of the pass transistor in addition to the low-frequency pole P_1 , created by the output capacitance, which degrades the stability. Various approaches have been employed to address the issue [3,10,14,25–30]. In [26–28], large quiescent current consumption is required in the intermediate buffer stage to ensure stability, thereby degrading the current efficiency of the LDO under low load conditions. Current buffer compensation techniques reported in [14,29] showed good stability, but the results indicated comparatively low PSRR. Besides this, prior works [26,28–30] are for low-voltage supply fabrication.

HV input voltage LDOs are reported in [3,10,14,25,27] for operating voltages in the range of 10–50 V. In [10], the input operating voltage is in the range of 10–30 V, but the design utilizes a pre-regulator module to initially step down the voltage for supplying power to the error amplifier stage.

The pre-regulator, designed with Zener diodes, dissipates energy, which makes it unsuitable for our low-power application. Besides, the n-type pass transistor involves higher dropout voltage, and large output capacitors (10–25 μ F), used to ensure stability, make the system bulky. Further, an HV LDO fabricated in BCD technology [3] showed improved PSRR response and input voltage up to 50 V. The design of the LDO in [3] is based on a current buffer compensation technique with r_{obuff} in the order of $1/g_m$. However, as the load current increases, the system turns unstable as r_{obuff} is constant [30].



Figure 5. (a) Block schematic of conventional low drop-out (LDO); (b) source follower buffer; (c) source follower with shunt feedback.

The proposed LDO uses a current buffer compensation topology, with a low impedance buffer, to attain stability for varying load conditions; Figure 6. The error amplifier is realized by a folded-cascode structure, with cascaded LV-HV transistors to contain high input voltage [25]. The pass device is a p-type HV transistor with a rated maximum voltage of 45 V. The resistor feedback network is constituted by R_{FB1} and R_{FB2} , with capacitors C1 and C2 connected in parallel to R_{FB1} and R_{FB2} , respectively, for reducing high frequency noise [29]. Transistor HVM6 with C_{CAS} forms the current buffer for frequency compensation. The necessary bias current and reference voltage are obtained from the high-voltage reference and bias current generator.

The proposed buffer is based on a dynamically-biased shunt feedback scheme, as in [30]. The circuit schematic of the implemented buffer is depicted in Figure 6. As in Equation (4), pole frequency P_2 is dependent on r_{obuff} . Lowering r_{obuff} will push P_2 towards a higher frequency, ensuring the stability of the LDO. The buffer stage with the source-follower, the source-follower with the npntransistor-based shunt feedback and dynamically-biased npn transistor-based shunt feedback are analyzed in [30]. Our design uses the dynamically-biased n-type MOSFET-based shunt feedback buffer.

Under light load conditions, for the source follower buffer in Figure 5b, the r_{obuff} (= $1/g_{M1}$) can be only decreased by increasing the feature size of the source follower (M1) or by increasing the current passing through M1 [30]. This pushes pole P_2 towards higher frequency, but increases the quiescent current. For a design that involves the source-follower with n-type MOSFET shunt feedback (Figure 5c), r_{obuff} is reduced by a factor of $g_{m2}r_{o1}$ where $r_{obuff} = 1/(g_{MS1}r_{oMS1}g_{MS2})$. Thus, the quiescent current required to attain a given r_{obuff} in the source-follower with shunt feedback is less, in comparison to a simple source-follower. In a similar way, the feature size of the source-follower is also reduced, which, in turn, reduces the buffer input capacitance. The reduction of input buffer capacitance allows pole P_1 to be located at higher frequency. Additionally, the buffer in our design includes diode connected transistor M4 and M5 to realize dynamically-biased shunt feedback [30] to decrease r_{obuff} for varying load conditions. The output resistance of the proposed buffer is given by:

$$r_{obuff} = \frac{1}{g_{mHVM10}g_{mHVM12}r_{oHVM10} + g_{mHVM11}}$$
(5)

where g_m and r_o are the transconductance and output resistance of each transistor, respectively. As load current increases, the voltage at Node 1 and Node 2 decreases. The V_{GS} of HVM11 increases, which allows more current through HVM11. HVM9 mirrors the current of HVM11, which aids the source-follower (HVM10) current to dynamically increase with load current. An increase in M1 current increases the g_{mHVM10} and reduces the r_{obuff} Equation (5). Further, g_{HVM11} and g_{HVM12} also increase due to the rise in current flowing through HVM11 and HVM12, which also adds to the reduction of r_{obuff} Equation (5). Thus, the reduction in r_{obuff} places pole P_2 towards higher frequencies, ensuring the stability of the LDO. The stability analysis of the LDO is referenced from [30].



Figure 6. Schematic diagram of the implemented high-voltage LDO.

The final loop gain transfer function of the implemented LDO is given by:

$$T_{s} = \frac{Bg_{mLVM4}g_{mpass}r_{oLVM4}R_{oLDO}(1 + s\frac{C_{CAS}}{g_{mHVM6}})}{1 + as + bs^{2} + cs^{3}}$$
(6)

$$a = R_{oLDO}(C_{out} + g_{mpass}r_{oLVM4}C_{CAS}); \quad b = C_1 C_{out}r_{oLVM4}R_{oLDO}; \quad c = \frac{C_1 C_{CAS}C_{out}r_{oLVM4}R_{oLDO}}{g_{mHVM6}}$$
(7)

where g_m and r_o are the transconductance and output resistance of each transistor, B is the feedback factor $(R_{FB2}/(R_{FB1}+R_{FB2}))$ and C_{CAS} the feedback capacitor. The frequency response plot of the LDO is depicted in Figure 7 for various load currents. The plot indicates the phase margin above 55 degrees for currents in the range of 0–100 mA with a 1-µF output load capacitor.



Figure 7. Loop gain frequency response of the proposed high-voltage (HV) LDO.

4.4. Battery Charger Circuit

Battery management circuits are inevitable in the design implementation of biomedical devices to extend the battery lifetime. The battery charger circuit plays a significant role in battery management, to ensure safe and reliable charging and, thus, prolonging the battery life expectancy. Earlier works [31–36] show various control schemes based on digital and analog techniques. In [34,35], LDO-based Li–ion battery chargers are reported. These chargers' ICs provide good stability performance, but are characterized by their low efficiency at the start of the charging process [31]. To compensate for the low efficiency, switched mode converter-based chargers are proposed in [31,32]. Though they achieved high efficiency, the system required large off-chip inductors, transistor switches and driver circuits that occupied a large area of the chip. An integrated chip, the analog control-based charger reported in [33], minimized the implementation area, but expensive precision sensingresistors are employed in the design.

The proposed charger IC design based on an analog control scheme intends to minimize the implementation area, achieve higher power efficiency and ensure safe and reliable battery charging. The analog control is based on the work in [36]. The design addresses all of the typical charge regimes of Li–ion batteries, namely trickle charging, constant current (CC), constant voltage (CV) and end of charge (EOC). The simplified block diagram of our charger is shown in Figure 8. The

operational transconductance amplifier (OTA) compares the battery voltage (V_{Bat}) to a reference voltage ($V_{Ref1} = 3.7 \text{ V}$) and generates an output current supplied to the current gain stage. The current gain stage consists of two stages, which allows the battery to be charged for maximum current (10 mA) in the CC regime and 1 mA in the trickle charging regime. The gain stages are activated based on the comparator output, which compares V_{Bat} to a reference voltage ($V_{Ref2} = 2.4 \text{ V}$). Finally, the EOC detector detects the end of the charging process.



Figure 8. Block schematic of the proposed charger circuit. OTA, operational transconductance amplifier; EOC, end of charge.

The OTA in Figure 9a generates a tanh function-based output current curve based on the instantaneous V_{Bat} and the reference voltage inputs. The OTA, operated in the saturated regime, is designed to have a linear range of 160 mV. This feature allowed our design to automatically transform the CC regime of operation to the CV regime. In prior work [36], based on sub-threshold OTA control for low power consumption, the linear range is directly dependent on the thermal voltage that gives rise to the uncertainty of the linear range during temperature fluctuations. Besides this, the OTA was biased with a current of order in nanoamperes, which would require large current gain stages to source a current of a magnitude of 10 mA, as per our design specification. Our design compensates for the prior design by implementing saturated regime transistor-based OTA, with an adaptively controlled linear range [37]. The linear range of the implemented OTA is given by:

$$V_L = \frac{V_{B1} - V_{th}}{k_s \sqrt{2}} \tag{8}$$

where V_{B1} is the bias voltage used to adaptively control the linear range of the OTA and k_s is the sub-threshold exponential slope parameter. The linear range signifies that, for $V_{Bat} < 3.54$ V, the OTA output is saturated, and the maximum current passes through the power device, indicating the CC regime of operation. For V_{Bat} greater than or equal to 3.54 V, the OTA output shifts to the linear regime of operation, and gradually, the output current decreases as the battery voltage approaches the reference threshold. The output current of the OTA I_{out} is given by:

$$I_{out} = I_{B1} tanh(\frac{k_s(V_{in+} - V_{in-})}{2U_T})$$
(9)

where I_{B1} is the bias current of the OTA, k_s is the subthreshold exponential slope parameter, V_{in+}, V_{in-} are the input voltages and U_T is the thermal voltage. The necessary reference and bias voltages are realized from Section 4.2. The current gain constituted by two stages, as in Figure 10a, facilitates CC and trickle charging. The output current of the OTA in microamps is mirrored to pass the transistor to enable the charging process. When the comparator (Figure 10b) detects the V_{Bat} greater than or equal to V_{Ref2} , both the high and low gain stages are activated to source maximum current to the battery. However, while $V_{Bat} < V_{Ref2}$, only the lower current gain stage is activated with a 1-mA charging current. The comparator-based approach is devised in the system in comparison to the trickle charge threshold detector [36], as it proves to be more effective at start up for an over-discharged battery. Besides, in [36], there is the possibility that the threshold charge detector may run out the battery. The EOC detector is based on the current comparator technique, where a reference current is compared to the output current of the OTA to determine the end of the charging process. The schematic circuit of the current comparator for EOC detection is depicted in Figure 9b.



Figure 9. Schematic diagram of: (a) the implemented OTA; (b) the EOC detector.



Figure 10. Schematic diagram of: (a) the implemented current gain; stages (b) the comparator.

5. Simulation and Experimental Results

The design is simulated in the Cadence Spectre environment and realized with the 0.35- μ m Dongbu-Hitek BCD process for test purposes. The rectifier is supplied with a maximum input voltage of 20 V_{peak} at 13.56 MHz and a maximum load current of 10 mA. In general, rectifiers are characterized by their PCE. For our work, the PCE of the rectifier is calculated based on Equation (10).

To attain maximum PCE, the bias voltage is varied approximately between 40% and 94% of V_{th} (Dongbu-Hitek 60-V LDNMOS $V_{th} = 1.2$ V typical). The bias voltage varies marginally with the varying input voltage, owing to the resistor, diode connected transistor and capacitor biasing. However, this results only in minor variations of the bias voltage and could be neglected. Figure 11(a) shows the post-layout simulation results of PCE for the implemented rectifier with varying load current and input voltage. The plot indicates that with increasing load current and voltage, PCE tends to rise and reach up to 91%. It is evident that the reverse leakage current is greatly reduced with the adaptive and partial threshold cancellation technique. The transient simulation response for an input voltage of 16 V at a 13.56-MHz input frequency and 5-mA load current is depicted in Figure 11(b).

$$\eta_{PCE} = \frac{V_{OUT} * I_{OUT}}{P_{in}} = \frac{V_{OUT}^2 * T}{R_L \int_0^T V_{in}(t) * I_{in}(t) \,\mathrm{d}t}$$
(10)

The experimental results of PCE for varying the input voltage and load current are shown in Figure 12(a). Discrete resistors were used to replicate the increasing cuff-nerve electrode interface impedance. IC is tested with the value of discrete resistors ranging from $0.5-10 \text{ K}\Omega$. The results in Figure 12(a) indicate that, at low load currents, the experimental results closely follow the simulation results. For high load currents and supply voltages, the PCE curve deviates from the simulation results. This is due to substrate leakage current within the chip. The existence of high gain parasitic bipolar junction transistors (BJT) that are not modeled during the simulation process of the design conducts current when the reverse voltage exceeds a certain limit [38]. Parasitic BJT modeling has been explored in prior works [38], but a consistent and generalized model is yet to be developed. The major restriction for developing a generalized parasitic BJT model is the variation of the process in the technologies. The development of the model is beyond the scope of our design. The captured transient oscilloscope waveforms of rectifier input and output node voltages at a 13.56-MHz input frequency and 1.2-mA output load current are shown in Figure 12(b).

For high voltages and load currents, the substrate leakage current increases and results in latch-up, which finally breaks down the chip. The results shown in Figure 12(a) are based on operating points where latch-up does not occur. In Figure 12(b), we notice that the substrate leakage current is negligible as the rectifier input node AC does not peak the DC voltage [3]. For high input voltages and load currents, the rectifier is abnormally loaded, and the input AC node voltages become higher than the output DC [3,16]. However, in our application for a neural stimulator, the current required is less than 2 mA, with input voltages ranging from 10–20 V_{peak}, the design proves to be effective. Further, for the purpose of charging the implant battery, as the load resistance is low, the system is operated in a voltage range of input 5–7 V sourcing a maximum current of 10 mA. A comparison of the proposed rectifier to prior works is shown in Table 2.



Figure 11. Simulated: (**a**) power conversion efficiency (PCE) with varying input voltage and load current; (**b**) transient response of the proposed rectifier.



Figure 12. Experimental: (a) PCE with varying input voltage and load current; (b) oscilloscope capture of the transient response of the proposed rectifier.

Publication	2009 [1]	2011 [2]	2011 [3]	2012 [23]	This work
µltirow2*Technology	0.35 μm CMOS	0.5 μm CMOS	DALSA C08G-C08E	0.18 μm CMOS	0.35 μm BCD
$V_{in,peak}(V)$	2.4	3.8	16.8	1.5	20.0
$V_{REC}(V)$	2.28	3.12	15.5	1.33	17.54
Frequency (MHz)	0.2-1.5	13.56	13.56	13.56	13.56
\mathbf{R}_{Load} (K Ω)	0.1	0.5	5.0	1.0	0.5-10.0
Load current $I_L(mA)$	20	NA	10	NA	0.5–10
PCE (%)	82-87	80.20	93.10 (Simulated)	81.90	83.5

Table 2. Performance comparison with prior rectifiers.

The fabricated reference current and voltage references generated independent supply voltage and zero temperature coefficient bias current and voltage for the LDO and charger circuit. The implemented LDO provided an adjustable output voltage of 4 V and 10 V with a maximum load current of 100 mA. For the 4-V and 10-V output, the input voltage range is from 4.5–30 V and 11–30 V, respectively. For the purpose of the experiment, the resistor network was implemented with discrete resistors, even though the BCD technology provided on-chip resistors. A 1- μ F capacitor was used for testing purposes of the fabricated LDO. The oscilloscope capture of the transient response of the LDO at start-up for a 10-V output and 5-mA current is shown in Figure 13(a). The transient response curve for a 4-V output with 10-V step input is shown in Figure 13(b). The experimental results of the LDO for a 4-V and a 10-V output are summarized in Table 3.



Figure 13. Oscilloscope capture of the transient response of the LDO: (**a**) at start-up for a 10-V output; (**b**) with a step input of 10 V for a 4-V output.

Parameter	Value	Conditions	Value	Conditions
Output	4 ± 0.02 V	Vin = 5 - 30 V;	10 + 0.05 V	Vin = 11–30 V;
Voltage	4 ± 0.03 V	Io = 0.01 - 100 mA	10 ± 0.03 V	Io = 0.01 - 100 mA
Dropout	320 mV Mean	Io = 1 mA, Vo = 4.02 V;	240 mV Mean	Io = 1 mA, Vo = 10.03 V;
Voltage	370 mV Mean	Io = 5 0 mA, Vo = 4.03 V	290 mV Mean	Io = 50 mA, Vo = 10.04 V
Line	$42\pm20\ mV$	Vin = 4.8–30 V	$54 \pm 20 \text{ mV}$	Vin = 11.05–30 V
Regulation		Io = 5 mA	$34 \pm 20 \text{ mV}$	Io = 5 mA
Load	30 mV	Vin = 10 V;	49 m V	Vin = 20 V;
Regulation		Io = 1-50 mA	48 III v	Io = 1-50 mA
DCDD	(-65.2) dB -	100 Hz 1 KHz	(-64.9) dB -	100 Hz–1 KHz
PSKK	(-54.35) dB	100 HZ-1 KHZ	(-54.2) dB	
Quiescent Current	94 µA	Vo = 4 V	98 μA	Vo = 10 V
Maximum I_O	100 mA	Vin = 530 V	100 mA	Vin = 11–30 V

Table 3. Performance summary of the HV regulator.

The battery management circuit facilitates the battery charging process under the typical Li-ion battery charging profile. Figure 14(a) and 14(b) show the simulated charging current and instantaneous battery voltage for the entire charging process. For the simulation setup, the battery is represented as a capacitor in series with a resistor. The values of the capacitor and resistor used for the simulation process are 0.25 mF and 0.5 Ω , respectively. The plot in Figure 14, depicts all four regimes of the Li-ion charging process. For $V_{Battery} < 2.4$ V, the battery is charged with a 1-mA current, implying trickle charging. When V_{Bat} greater than or equal to 2.4 V and V_{Bat} less than or equal to 3.54 V, the battery is directed to CC charging with a 10-mA current. Followed by the CC regime, when $V_{Bat} > 3.54$ V, the charging current begins to decrease until 0.3 mA, which indicates the CV regime. Further, after the CV regime, the charging current drops from 0.3 mA to zero magnitude, which illustrates the EOC regime and the battery to be completely charged.



Figure 14. Simulated: (a) charging current; (b) instantaneous battery voltage with charging current.

For experimental verification, a 3.7-V, 20-mAh Li-ion battery is used. In the CC regime, the battery is charged with 9.8 mA, and in the trickle charging regime, a 1-mA current charged the battery. The threshold below 2.4 V is stated to be the trickle charge regime as per the experimental result and is shown in Figure 15. The measured charging current and instantaneous battery voltage for the EOC regime of charging is depicted in Figure 15(a). Figure 15(b) indicates the measured battery voltage and charging current in the CC, CV and EOC regimes of charging. When the battery reaches a threshold voltage of 2.4 V, high current is sourced into the circuit, indicating the CC regime. As the voltage of the battery reaches 3.54 V, approximately, the charge current starts to reduce, indicating the CV charging regime. The charging current reduces until 0.15 mA, where the final battery threshold voltage of 3.7 V is reached. As the charging current reaches 0.15 mA, the battery is charged completely, and the charging current drops to zero, indicating the EOC regime. The die-micrograph of the fabricated chip is shown in Figure 16c,d shows the packaged chips mounted on the socket for test purposes.



Figure 15. Measured charging current and voltage when charging a 20-mAh, 3.7-V battery. (a) Trickle charging regime; (b) constant current (CC), constant voltage (CV) and EOC regime.



Figure 16. (a) Die-micrograph of the fabricated LDO and charger circuit; (b) die-micrograph of the fabricated rectifier; (c,d) packaged chip mounted on to the socket for testing.

6. Conclusions

In this paper, we propose and implement a power-efficient design of an HV power receiver for WPT systems in biomedical devices. The topology is based on the step down approach, accommodates input voltage as high as 30 V and integrated on a 2.5 mm \times 5 mm chip for the purpose of stimulus generation and battery recharging application. The rectifier attains a maximum PCE 83.5% for a 12-V input and 2.1-mA load current. The PCE decreases for higher load currents and input voltages, but the obtained PCE for a 2.1-mA and 15 V_{peak} input proves effective for our system specifications. Even though the design was focused on protecting the rectifier from substrate leakage current and latch-up, at high input voltages and load currents, the efficiency deviated from the post-layout simulation results, indicating the

increased substrate leakage current. The integrated linear voltage regulator provides stable 10-V output for the purpose of generating a high stimulus current and a 4-V output for the purpose of implant Li-ion battery charging. The LDO fabricated operated for a wide range of load currents (1 μ A–100 mA). The battery charger circuit enabled the implanted Li-ion battery to be charged through the typical battery charging profile and ensured a safe and reliable charging process to extend the battery lifetime.

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Author Contributions

Vijith Vijayakumaran Nair designed and tested the system. Jun Rim Choi provided guidance and key suggestions for the system design and test.

Conflicts of Interest

The authors declare no conflict of interest.

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