

Article

Three-Phase High-Power and Zero-Current-Switching OBC for Plug-In Electric Vehicles

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Abstract: In this paper, an interleaved high-power zero-current-switching (ZCS) onboard charger (OBC) based on the three-phase single-switch buck rectifier is proposed for application to plug-in electric vehicles (EVs). The multi-resonant structure is used to achieve high efficiency and high power density, which are necessary to reduce the volume and weight of the OBC. This study focuses on the border conditions of ZCS converting with a battery load, which means the variation ranges of the output voltage and current are very large. Furthermore, a novel hybrid control method combining pulse frequency modulation (PFM) and pulse width modulation (PWM) together is presented to ensure a driving frequency higher than 10 kHz, and this will reduce the unexpected inner resonant power flow and decrease the total harmonic distortion (THD) of the input current under a light load at the end of the charging process. Finally, a prototype is established, and experiments are carried out. According to the experimental results, the conversion efficiency is higher than 93.5%, the THD about 4.3% and power factor (PF) 0.98 under the maximum power output condition. Besides, a three-stage charging process is also carried out the experimental platform.

Keywords: onboard charger; buck converter; zero-current-switching; electric vehicle

1. Introduction

Due to the environmental and energy crises, more and more researchers are paying attention to novel energy vehicles, such as electric vehicles (EVs) and hybrid electric vehicles (HEVs). It is widely known that battery chargers play a critical role in the development of EVs, and the charging time and lifetime of batteries are closely related to the characteristics of the chargers. A battery charger must be efficient and reliable, with low cost, low volume and low weight, as well as high-power output capability [1–5]. Most of the chargers can be divided into two types: onboard chargers (OBCs) and off-board chargers (FBCs). Generally, FBCs are located in charging station, which are suitable for fast charging. However, the expensive construction cost and limited locations (mostly in big cities) have limited the wide application of FBCs. Different from FBCs, OBCs mean taking the chargers with the vehicles and thus having relatively higher flexibility, which makes it possible to get charged through a socket. Thereby, the OBCs are supposed to be a better alternative for customers. However, OBCs have some specific limitations, since the added charger will increase the volume, weight and cost, as well as the charging time, which is too long for normal usage. Therefore, novel OBCs with low volume, high efficiency, high power density and high power capability are needed [3].

From the perspective of structure, OBCs are classified into two types: a single-stage topology and a multi-stage topology. The multi-stage (mostly two-stage) structures are commonly used at present due to their favorable features. A simplified structure of the two-stage OBC using digital signal processor (DSP) or microcontroller unit (MCU) as controller is shown in Figure 1. The two-stage structure has the advantages of a wide adjustable output voltage range and high flexibility of the output load. To satisfy the requirements of the conversion efficiency, soft switching technology is widely used in the DC/DC converter. The most commonly-used topologies are the phase shifted zero-voltage-switching (ZVS) topology [6–10] and the resonant tank with two inductors and a capacitor (LLC) resonant topology [11–13]. The shifted ZVS topology can achieve a relatively high output power level, which is more than a dozen kilowatts with an efficiency between 95% and 97%. However, it also has some drawbacks, such as a limited soft switching range and being sensitive to the parasitic parameters of switch devices and the leakage inductance of the transformer. All of these problems will increase the design difficulty. The LLC resonant topology has disadvantages, such as a low power rating and a rigorous design of the transformer and inductor because of the parasitic parameters. In addition, the wide frequency range of the LLC structure increases the difficulty of the design process for the input electromagnetic interference (EMI) filter.

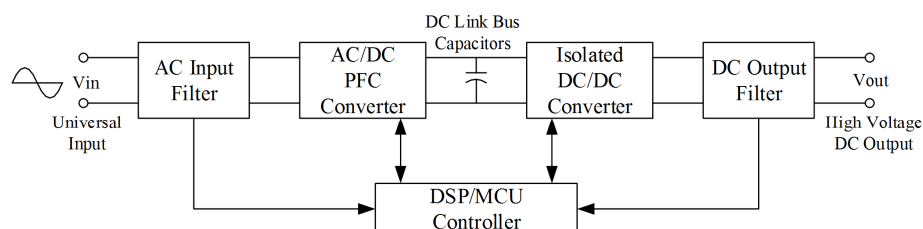


Figure 1. Simplified block diagram of a universal single-phase onboard charger (OBC); power factor correction (PFC).

Compared with the two-stage structure, the single-stage structure will reduce the number of devices and circuit complexity, so it is easier to get low volume, high efficiency and high power density. Furthermore,

to realize rapid charging for EVs, three-phase AC/DC converters are widely used in the single-stage charging structure.

A large number of three-phase AC-DC converters have been developed to improve power factor correction (PFC), to reduce THD and EMI of the AC input and to regulate DC output, which are addressed as the three-phase improved power quality AC-DC converters (IPQCs). Concerning topologies, these circuits can be classified into five categories: buck, boost, buck-boost, multilevel and multi-pulse [14].

The output voltage of the boost IPQCs is higher than the peak input voltage, which will result in a high output voltage or a decrease of the input voltage to satisfy the output requirement. Therefore, this kind of converter is usually used to provide a constant, regulated DC output voltage [14,15]. Furthermore, there are many problems hindering the buck-boost IPQCs from high-power applications, such as the storage capacitor selection and the reversed output voltage polarity. Therefore, the boost and buck-boost IPQCs are not suitable for the single-stage OBC application.

The buck IPQCs with high-frequency switching devices are extensively used in battery charging for automotive applications [16]. These circuits can reduce the filter size and weight and enhance the efficiency of the system. Several topologies, such as using a single switch with a diode bridge rectifier [17], three switches with a dual diode, shown in Figure 2a [18], and six switches with free-wheeling diodes, shown in Figure 2b [19], are used to improve the power factor, to reduce the harmonic currents of AC input and to get a well-filtered output DC voltage.

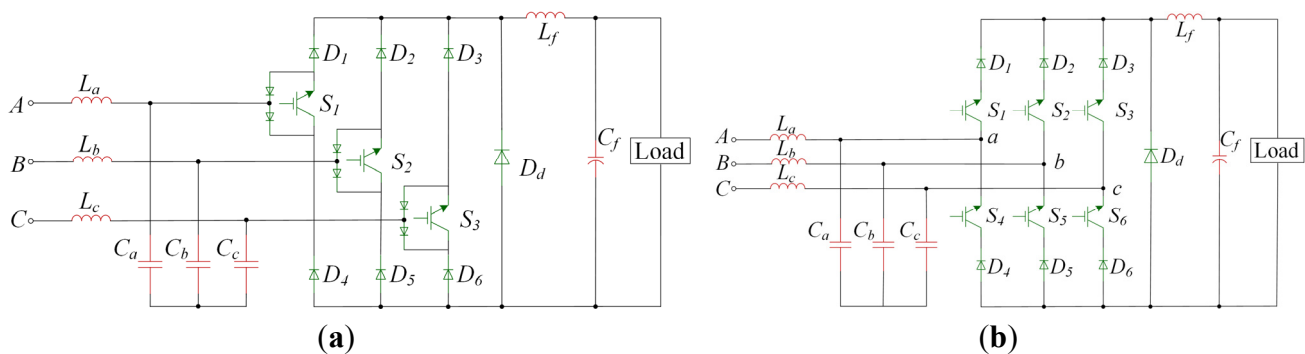


Figure 2. Three-phase AC-DC buck converters: (a) three-switch buck converter; (b) six switch with free-wheeling diode buck converter.

To enhance the efficiency and switching frequency of buck IPQCs, Robert W. Erickson and Yungtaek Jang proposed a new zero-current-switching (ZCS) three-phase high quality rectifier, which is illustrated in Figure 3 [15,20,21]. In this three-phase ZCS buck circuit, continuous input and output currents, a high power factor and low harmonic rectification are achieved. By the usage of a multi-resonant scheme, the switch operates in ZCS mode, and the diodes operate in ZVS mode; therefore, this circuit is suitable for the high-frequency implementation with insulated gate bipolar transistor (IGBT) [21].

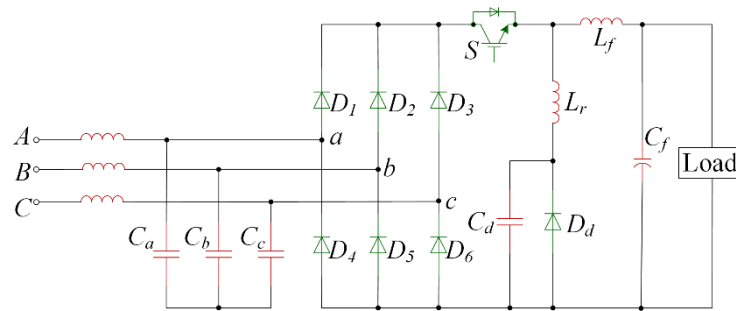


Figure 3. New three-phase multi-resonant zero-current-switching buck rectifier.

In view of the aforementioned advantages, this three-phase ZCS buck topology is adopted and optimized in this article. Although this topology can satisfy the requirement of single-stage OBC in general, the battery characteristics and the ZCS boundary condition of the multi-resonant tank, as well as their influence on each other have to be considered. Moreover, the output voltage and current fluctuations should be carefully considered for different battery statuses. Many charging strategies for EV batteries have been proposed [22–26]. Comprehensively considering the life cycle of batteries and the feasibility of the control methods, the three-stage charging strategy is selected in this article. Then, this article studies the influence between the realization of ZCS and the battery parameters or status changes and solves the problem of the large input current ripple and the useless large resonant current within the tank when the driving frequency is extremely low under light load conditions.

In addition, an interleaved structure is used to improve the power level of the OBC system in this paper, which can reduce the charging current ripple and inductor size, and it also reduces the current stress on output capacitors [1,27,28]. Finally, a prototype platform was built to verify the feasibility of the proposed topology. Besides, the SiC Schottky diodes were applied to promote the power level and the system efficiency [29,30].

The structure of this article is organized as follows. The operating states and principles are shown in Section 2. Section 3 explains the process of the system design, the ZCS border conditions, the impact caused by the battery load and the novel PWM and PFM combined control strategy. Section 4 presents the simulation and experimental results to evaluate the proposed converter. Finally, Section 5 concludes the work carried out in this article.

2. System Introduction

The proposed interleaved three-phase multi-resonant ZCS OBC is shown in Figure 4. It is composed of the input filter inductors $L_a, L_b, L_c, L_{as}, L_{bs}, L_{cs}$, input resonant capacitors $C_{r1}, C_{r2}, C_{r3}, C_{rs1}, C_{rs2}, C_{rs3}$, uncontrolled rectifier bridges D_1 – D_6 and D_{s1} – D_{s6} , resonant inductors L_r and L_{rs} , output resonant capacitors C_d and C_{ds} , fly-wheel diodes D_d and D_{ds} , output filter inductor L_f and L_{fs} and output filter capacitor C_f . In this topology, C_{r1} – C_{r3} , C_d and L_r constitute a resonant tank, and the resonance cycle of this is fixed. Therefore, the PFM control strategy with a constant turn on time is adopted, and the output voltage will increase with the driving frequency increasing while other circuit parameters remain the same.

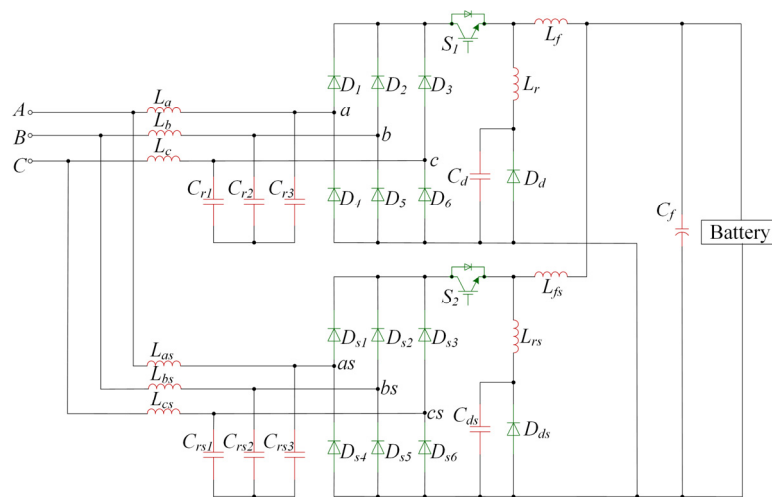


Figure 4. The proposed OBC.

Due to the structures of the two interleaved channels being completely the same, the following analysis is based on the single-channel structure. This topology is established on the basis of the three-phase single-switch rectifier [16], in which the output voltage is controllable from zero to the peak AC input line voltage. Only one IGBT in each channel needs to be controlled in this structure. In the proposed topology, C_{r1} – C_{r3} , C_d and L_r constitute a multi-resonant tank, which can guarantee the IGBTs S_1 and S_2 working in ZCS mode and diodes D_d and D_{ds} operating in ZVS mode. Moreover, by the usage of the multi-resonant scheme and the interleaved structure, this converter can improve the power level and achieve high quality input current and almost unity power factor; which can reduce the input and output side ripples and decrease the volume of the circuit.

The operating waveforms of the input side resonant capacitor v_{cr} and IGBT current i_s are shown in Figure 5. The voltage v_{cr} can be divided into four parts: during T_1 , IGBT is turned off, and C_r is charged with input current; during T_2 , C_r , L_r and C_d form a resonant tank, until v_{cr} decreases to zero; v_{cr} remains zero during T_3 ; during T_4 , C_r is charged with a current of input line current i_{in} minus the IGBT current i_s . While the average value of v_{cr} is the same as the input voltage during each switching cycle, and peak value of v_{cr} is proportional to the input current. If interval T_1 is much longer than the sum of T_2 , T_3 and T_4 , the input current will follow the input voltage waveform. The details of the working process and control strategy will be analyzed below.

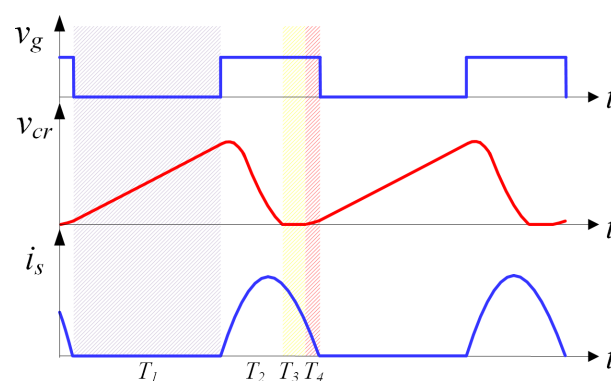


Figure 5. The waveforms of the input side capacitor voltage v_{cr} and insulated gate bipolar transistor (IGBT) current i_s .

2.1. Operating States

Both of the interleaved channels adopt same control strategy, but hold a phase shift of π in driving signal from each other. Assuming that the three-phase input voltages are symmetrical and balanced, it is sufficient to consider a 30-degree interval of the AC input. The 30-degree interval where $v_a > 0 > v_c > v_b$ is introduced. In order to simplify the algorithm, we choose the operating point at $\pi/2$ to analyze the operating process of each period.

V_{PM} and I_{PM} represent the peak input phase voltage and current, respectively. At the point of $\pi/2$, both v_a and i_a reach the peak value of the phase voltage and current, and $v_b = v_c = -0.5v_a$, $v_a = V_{PM}$. Similarly, $i_b = i_c = -0.5i_a$, $i_a = I_{PM}$. At this point, the input side resonant capacitor C_{r2} and C_{r3} are charged and discharged entirely synchronously, and diodes of phase B and C of the uncontrolled rectifier are turned on and off synchronously, too. Therefore, the following analysis of C_{r3} is neglected.

Since the driving frequency is much higher than the input voltage frequency, so during one switching cycle the input voltage and current can be considered as a constant value. The ideal operating waveforms of the OBC is shown in Figure 6, and the equivalent circuits of each interval are shown in Figure 7.

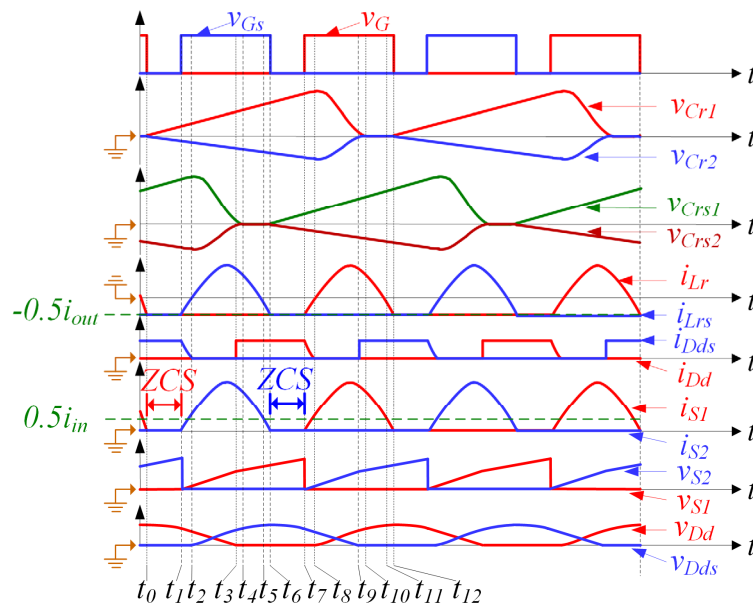


Figure 6. Ideal waveforms of the charger mode.

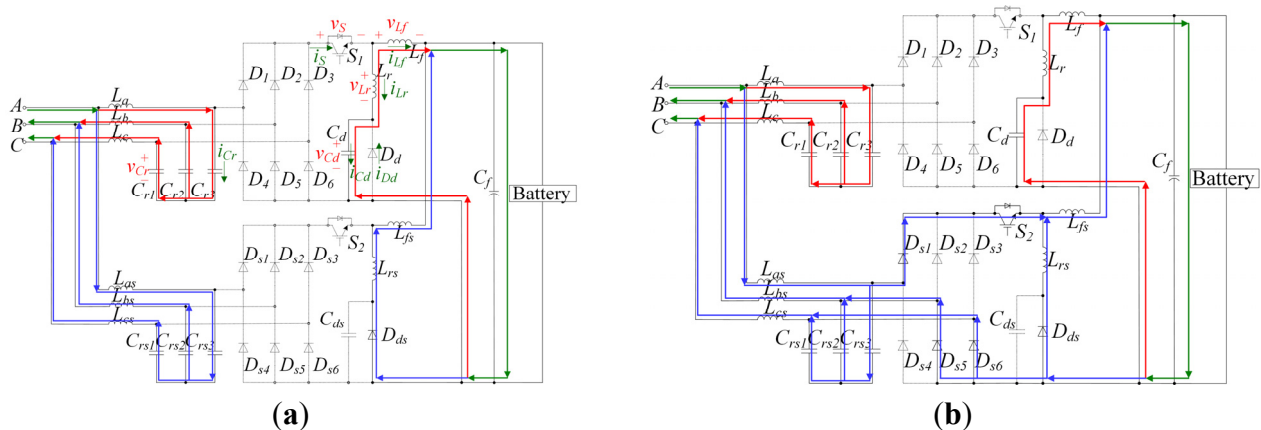


Figure 7. Cont.

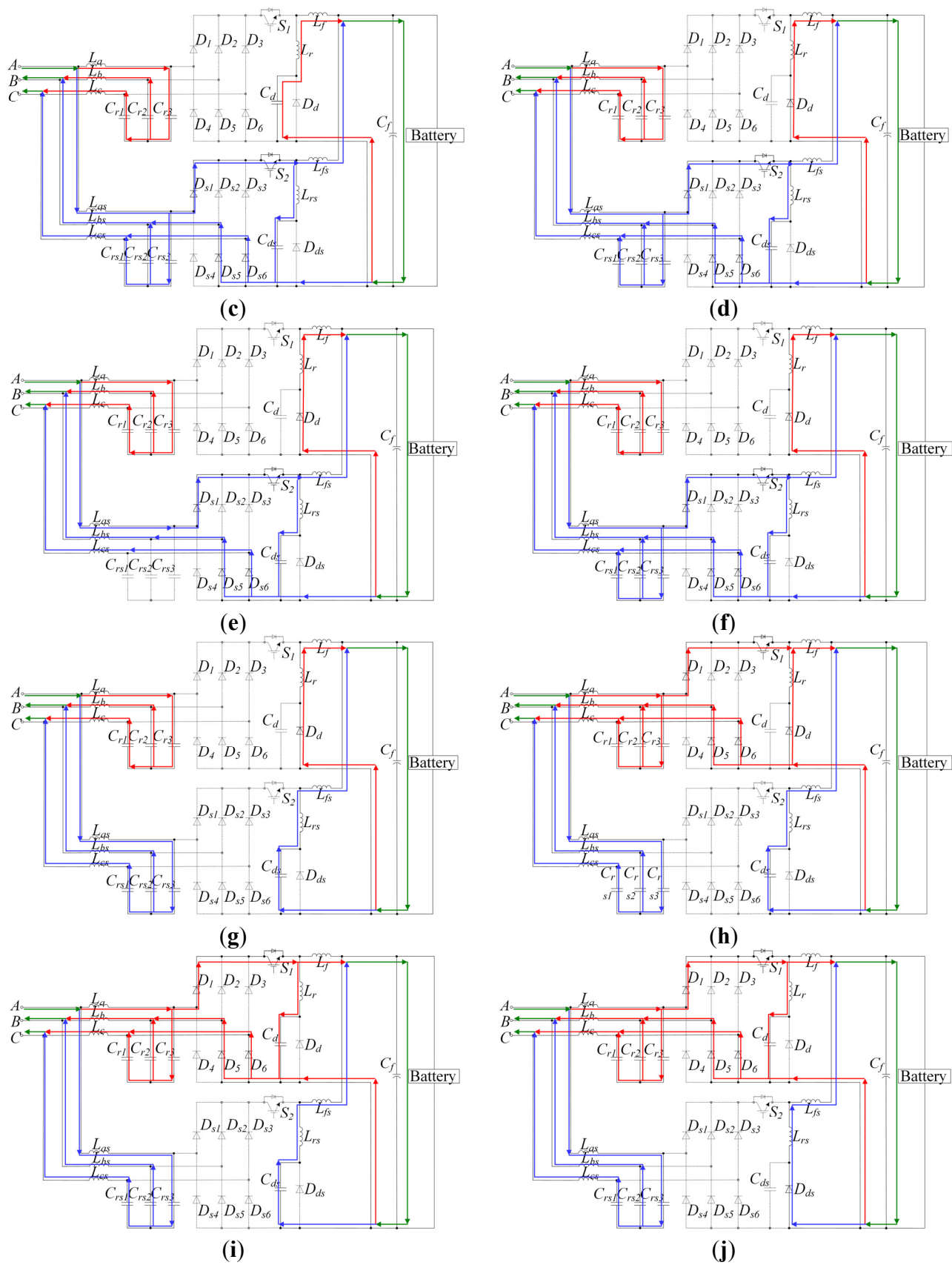


Figure 7. Cont.

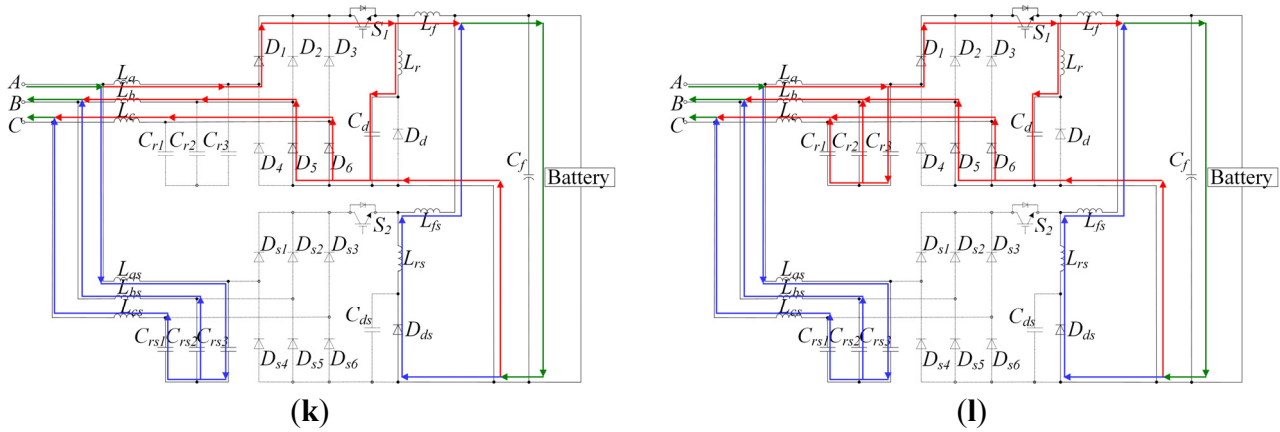


Figure 7. Equivalent circuits of each interval. (a) t_0-t_1 ; (b) t_1-t_2 ; (c) t_2-t_3 ; (d) t_3-t_4 ; (e) t_4-t_5 ; (f) t_5-t_6 ; (g) t_6-t_7 ; (h) t_7-t_8 ; (i) t_8-t_9 ; (j) t_9-t_{10} ; (k) $t_{10}-t_{11}$; (l) $t_{11}-t_{12}$.

The parameters are defined as follows: $v_{Cr1}-v_{Cr3}$ and $i_{Cr1}-i_{Cr3}$ are the voltage and current of resonant capacitors $C_{r1}-C_{r3}$, respectively; v_{Cd} and i_{Cd} are the voltage and current of the resonant capacitor C_d , respectively; v_{Lr} and i_{Lr} are the voltage and current of the resonant inductor L_r , respectively; I_{out} is the output current; V_{out} is the output voltage; i_{Cf} is the current of C_f . Since the two paralleled channels use the same control strategy, the single channel will be introduced in the following theoretical analysis and calculation parts. The input and output current for each channel are the half of the total circuit and can be defined as $0.5I_{PM}$ and $0.5I_{out}$. The capacitance values of $C_{r1}-C_{r3}$ are the same and can be represented as C_r . Figure 7a illustrates the voltage and current reference directions of the devices for the following analysis, and the reference directions of $C_{r1}-C_{r3}$ are exactly the same.

Interval I (t_0-t_3): D_1-D_6 , S_1 and D_d are off. $C_{r1}-C_{r3}$ are charged by the input current. During this interval, L_r provides the output current. C_d is discharged with i_{Lr} , and C_f is also charged. This interval ends when v_{Cd} decreases to zero and D_d is turned on. The state equations of this interval are:

$$\begin{cases} C_r \frac{dv_{Cr1}(t)}{dt} = 0.5I_{PM} \\ C_r \frac{dv_{Cr2}(t)}{dt} = -0.25I_{PM} \\ C_d \frac{dv_{Cd}(t)}{dt} = i_{Cd}(t) \\ V_{Lf}(t) = L_f \frac{di_{Lf}(t)}{dt} \\ i_{Cd}(t) = i_{Lr}(t) = -i_{Lf}(t) = -0.5I_{out} + i(t) \\ v_{Cd}(t) + v_{Lr}(t) = v_{Lf}(t) + V_{out} \\ v_s(t) + v_{Cd}(t) = v_{Cr1}(t) - v_{Cr2}(t) \end{cases} \quad (1)$$

In Equation (1), $i(t)$ represents the fluctuation component of the freewheel current through C_d , L_r and L_f . From the perspective of the current analysis, $i(t)$ can be ignored, while in the voltage analysis, $i(t)$ will cause a decided change of $V_{Lf}(t)$. Moreover, $V_{Lr}(t)$ can be considered as a constant value in this interval, in view of the fact that compared to L_f , the value of L_r is very small.

Interval II ($t_3 \sim t_7$): D_d is on, and $D_1 \sim D_6$ and S_1 are off. The output current is still supplied by L_r . The only difference between Interval I and Interval II is that the current flows through D_d , rather than

the resonant capacitor C_d . This interval ends when the switch S_1 is turned on. The state equations of this interval are:

$$\begin{cases} C_r \frac{dv_{Cr1}(t)}{dt} = 0.5I_{PM} \\ C_r \frac{dv_{Cr2}(t)}{dt} = -0.25I_{PM} \\ i_{Lr}(t) = -i_{Dd}(t) = -i_{Lf}(t) = -0.5I_{out} + i(t) \\ v_s(t) = v_{Cr1}(t) - v_{Cr2}(t) \end{cases} \quad (2)$$

Interval III (t_7 – t_8): D_1 , D_5 , D_6 , S_1 and D_d are on, and the other diodes are off. C_{r1} – C_{r3} and L_r form a resonant tank, until the inductor current increases to zero. The state equations of this interval are:

$$\begin{cases} C_r \frac{dv_{Cr1}(t)}{dt} = i_{Cr1}(t) \\ C_r \frac{dv_{Cr2}(t)}{dt} = i_{Cr2}(t) \\ L_r \frac{di_{Lr}(t)}{dt} = v_{Lr}(t) \\ i_{Cr1}(t) = -2i_{Cr2}(t) \\ i_s(t) = i_{Lf}(t) + i_{Lr}(t) \\ v_{Lr}(t) = v_{Cr1}(t) - v_{Cr2}(t) \\ i_{Cr1}(t) + i_s(t) = 0.5I_{PM} \end{cases} \quad (3)$$

Interval IV (t_8 – t_{10}): D_1 , D_5 , D_6 and S_1 are on, and D_2 – D_4 and D_d are off. C_d , C_r and L_r form a resonant tank. This interval ends until the voltage of C_r decreases to zero. The state equations of this interval are:

$$\begin{cases} C_r \frac{dv_{Cr1}(t)}{dt} = i_{Cr1}(t) \\ C_r \frac{dv_{Cr2}(t)}{dt} = i_{Cr2}(t) \\ i_{Cr1}(t) = -2i_{Cr2}(t) \\ i_s(t) = i_{Lf}(t) + i_{Lr}(t) \\ L_r \frac{di_{Lr}(t)}{dt} + v_{Cd}(t) = L_f \frac{di_{Lf}(t)}{dt} + V_{out} = v_{Cr1}(t) - v_{Cr2}(t) \\ 0.5I_{PM} = i_{Cr1}(t) + i_s(t) \end{cases} \quad (4)$$

Interval V (t_{10} – t_{11}): D_1 – D_6 and S_1 are on, and D_d is off. L_r and C_d form a resonant tank. This interval ends when the current i_{S1} reduces to the input current $0.5I_{PM}$. If $i_{S1} < 0.5I_{PM}$, then the current $i_{Cr1} > 0$, and the input capacitor begins to charge, indicating that this interval ends. The state equations of this interval are:

$$\begin{cases} L_r \frac{di_{Lr}(t)}{dt} + v_{Cd}(t) = 0 \\ C_d \frac{dv_{Cd}(t)}{dt} = i_{Cd}(t) = i_{Lr}(t) \\ i_s(t) = i_{Lf}(t) + i_{Lr}(t) \\ L_f \frac{di_{Lf}(t)}{dt} + V_{out} = 0 \end{cases} \quad (5)$$

Interval VI (t_{11} – t_{12}): D_1 , D_5 , D_6 and S_1 are on, and D_2 – D_4 and D_d are off. C_r , C_d and L_r form a resonant tank. This interval ends when the current i_{S1} decreases to zero. After this ending point, S_1 can realize turning on of ZCS. The state equations of this interval are:

$$\begin{cases} C_r \frac{dv_{Cr1}(t)}{dt} = i_{Cr1}(t) \\ C_r \frac{dv_{Cr2}(t)}{dt} = i_{Cr2}(t) \\ i_{Cr1}(t) = -2i_{Cr2}(t) \\ i_S(t) = i_{Lf}(t) + i_{Lr}(t) \\ L_r \frac{di_{Lr}(t)}{dt} + v_{Cd}(t) = v_{Cr1}(t) - v_{Cr2}(t) \\ 0.5I_{PM} = i_{Cr1}(t) + i_S(t) \end{cases} \quad (6)$$

2.2. Operating Analysis

This section will carry out a further analysis of the operating principle during each interval. From the state Equations (1)–(6), the current and voltage expressions of S_1 , L_r , C_r and C_d can be calculated. Then, the starting and ending point of each interval are confirmed, which will be used to determine the ZCS boundary and to provide the basis for the circuit design.

By solving Equation (1), the expressions of the main power devices of Interval I are listed as:

$$\begin{cases} v_{Cr1}(t) = \frac{I_{PM}}{2C_r} t \\ v_{Cr2}(t) = v_{Cr3}(t) = -\frac{I_{PM}}{4C_r} t \\ v_{Cd}(t) = V_{Cd}|_{T0} - \frac{I_{out}}{2C_d} t \\ i_{Lf}(t) = \frac{I_{out}}{2} + \frac{V_{Cd}|_{T0} - V_{out}}{L_f} t - \frac{I_{out}}{4L_f C_d} t^2 + C_{11} \\ i_{Cd}(t) = i_{Lr}(t) = -i_{Lf}(t) \\ v_{Lf}(t) = V_{Cd}|_{T0} - V_{out} - \frac{I_{out}}{2L_f C_d} t \\ v_S(t) = \frac{3I_{PM}}{4C_r} t - V_{Cd}|_{T0} + \frac{I_{out}}{2C_d} t \end{cases} \quad (7)$$

As analyzed above, Interval I will end when v_{Cd} decreases to zero, so the ending moment T_1 and C_{11} can be deduced as:

$$T_1 = \frac{2V_{Cd}|_{T0} C_d}{I_{out}} \quad (8)$$

$$C_{11} = I_{Lf}|_{T0} - \frac{I_{out}}{2} \quad (9)$$

Then, the value of each electric parameter at the ending time of Interval I can be derived as:

$$\left\{ \begin{array}{l} V_{Cd}|_{T_1} = 0 \\ V_{Cr1}|_{T_1} = \frac{I_{PM} V_{Cd}|_{T_0} C_d}{I_{out} C_r} \\ V_{Cr2}|_{T_1} = V_{Cr3}|_{T_1} = -\frac{I_{PM} V_{Cd}|_{T_0} C_d}{2I_{out} C_r} \\ V_S|_{T_1} = \frac{3I_{PM} V_{Cd}|_{T_0} C_d}{2I_{out} C_r} \\ I_{Lf}|_{T_1} = \frac{I_{out}}{4} + \frac{V_{Cd}|_{T_0} - V_{out}}{L_f} \frac{V_{Cd}|_{T_0} C_d}{I_{out}} - \frac{2I_{out}}{L_f C_d} \left(\frac{V_{Cd}|_{T_0} C_d}{I_{out}} \right)^2 + C_{11} \\ I_{Cd}|_{T_1} = I_{Lr}|_{T_1} = -I_{Lf}|_{T_1} \\ V_{Lf}|_{T_1} = -V_{out} \end{array} \right. \quad (10)$$

Similarly, by solving Equations (2)–(6), the expressions of Intervals II–VI can be obtained. For Interval II, the expressions of the main devices of can be listed as:

$$\left\{ \begin{array}{l} v_{Cr1}(t) = \frac{I_{PM}}{2C_r}(t+T_1) \\ v_{Cr2}(t) = v_{Cr3}(t) = -\frac{V_{Cr1}(t)}{2} \\ v_S(t) = \frac{3v_{Cr1}(t)}{2} \\ v_{Lf}(t) = -V_{out} \\ i_{Lf}(t) = \frac{I_{out}}{2} - \frac{V_{out}}{L_f}t + C_{21} \\ i_{Dd}(t) = i_{Lf}(t) = -i_{Lr}(t) \end{array} \right. \quad (11)$$

For the duration of Interval II, T_2 and the final value of each electric parameter can be inferred as:

$$T_2 = DT_s - T_1 \quad (12)$$

$$C_{21} = I_{Lf}|_{T_1} - \frac{I_{out}}{2} \quad (13)$$

$$\left\{ \begin{array}{l} V_{Cr1}|_{T_2} = \frac{I_{PM} DT_s}{2C_{r1}} \\ V_{Cr2}|_{T_2} = V_{Cr3}|_{T_2} = -\frac{I_{PM} DT_s}{4C_{r1}} \\ V_S|_{T_2} = \frac{3I_{PM} DT_s}{4C_{r1}} \\ I_{Lf}|_{T_2} = I_{Lf}|_{T_1} - \frac{V_{out}}{L_f}(DT_s - T_1) \\ I_{Dd}|_{T_2} = I_{Lf}|_{T_2} = -I_{Lr}|_{T_2} \end{array} \right. \quad (14)$$

For Interval III, the expressions of the main devices can be listed as:

$$\begin{cases} v_{Cr1}(t) = C_{31} \sin \alpha_3 t + C_{32} \cos \alpha_3 t \\ i_{Cr1}(t) = C_{31} C_r \alpha_3 \cos \alpha_3 t - C_{32} C_r \alpha_3 \sin \alpha_3 t \\ i_s(t) = \frac{I_{PM}}{2} - C_{31} C_r \alpha_3 \cos \alpha_3 t + C_{32} C_r \alpha_3 \sin \alpha_3 t \\ i_{Lr}(t) = \frac{I_{PM}}{2} - \frac{I_{out}}{2} - C_{31} C_r \alpha_3 \cos \alpha_3 t + C_{32} C_r \alpha_3 \sin \alpha_3 t \\ v_{Lr}(t) = L_r C_{31} C_r \alpha_3^2 \sin \alpha_3 t + L_r C_{32} C_r \alpha_3^2 \cos \alpha_3 t \end{cases} \quad (15)$$

By substituting the final value of Interval II into Equation (15), the parameters can be shown as:

$$\alpha_3 = \sqrt{\frac{3}{2L_r C_r}} \quad (16)$$

$$\begin{cases} C_{31} = \frac{I_{Cr1}|_{T2}}{C_r \alpha_3} \\ C_{32} = V_{Cr1}|_{T2} \end{cases} \quad (17)$$

For the duration of Interval III, T_3 and the final value of each parameter can be deduced as:

$$\begin{aligned} T_3 &= \arcsin[M_3] \\ M_3 &= \frac{\left(\frac{I_{out}}{2} - \frac{I_g}{2}\right) C_{32} C_r \alpha_3 + \sqrt{\left(\frac{I_{out}}{2} - \frac{I_g}{2}\right)^2 C_{31}^2 C_r^2 \alpha_3^2 + C_{31}^4 C_r^4 \alpha_3^4 + C_{31}^2 C_{32}^2 C_r^4 \alpha_3^4}}{C_r^2 \alpha_3^2 (C_{31}^2 + C_{32}^2)} \\ N_3 &= \sqrt{1 - M_3^2} \end{aligned} \quad (18)$$

$$\begin{cases} V_{Cr1}|_{T3} = C_{31} M_3 + C_{32} N_3 \\ I_{Cr1}|_{T3} = C_{31} C_r \alpha_3 N_3 - C_{32} C_r \alpha_3 M_3 \\ I_s|_{T3} = \frac{I_{PM}}{2} - C_{31} C_r \alpha_3 N_3 + C_{32} C_r \alpha_3 M_3 \\ I_{Lr}|_{T3} = \frac{I_{PM}}{2} - \frac{I_{out}}{2} - C_{31} C_r \alpha_3 N_3 + C_{32} C_r \alpha_3 M_3 \\ V_{Lr}|_{T3} = L_r C_{31} C_r \alpha_3^2 M_3 + L_r C_{32} C_r \alpha_3^2 N_3 \end{cases} \quad (19)$$

For Interval IV, the voltage and current expressions of the main devices can also be deduced by solving Equation (4). They can be listed as:

$$\begin{cases} i_{Lr}(t) = C_{41} \sin \alpha_4 t \\ i_{Cd}(t) = C_{41} \sin \alpha_4 t \\ v_{Lr}(t) = C_{41} L_r \alpha_4 \cos \alpha_4 t \\ v_{Cd}(t) = \frac{C_{41}}{C_d \alpha_4} (1 - \cos \alpha_4 t) \\ v_{Cr1}(t) = \frac{2}{3} \left[C_{41} L_r \alpha_4 \cos \alpha_4 t + \frac{C_{41}}{C_d \alpha_4} (1 - \cos \alpha_4 t) \right] \\ i_{Cr1}(t) = \left(\frac{2C_{41} C_{r1} - 2C_{41} C_{r1} L_r C_d \alpha_4^2}{3C_d} \right) \sin \alpha_4 t \\ i_s(t) = \frac{I_{PM}}{2} - \left(\frac{2C_{41} C_{r1} - 2C_{41} C_{r1} L_r C_d \alpha_4^2}{3C_d} \right) \sin \alpha_4 t \\ i_{Lr}(t) = \frac{I_{PM}}{2} - \left(\frac{2C_{41} C_{r1} - 2C_{41} C_{r1} L_r C_d \alpha_4^2 - 3C_{41} C_d}{3C_d} \right) \sin \alpha_4 t \end{cases} \quad (20)$$

The parameters of Equation (20) can be determined by the final value of Interval III.

$$\alpha_4 = \sqrt{\frac{L_r + 2L_f + \sqrt{4L_f^2 + L_r^2}}{2C_d L_f L_r}} \quad (21)$$

$$C_{41} = \frac{V_{Lr}|_{T3}}{L_r \alpha_4} \quad (22)$$

For the duration of Interval IV, T_4 and the final value of each electric parameter can be derived as:

$$\begin{aligned} T_4 &= \frac{\arccos[N_4]}{\alpha_4} \\ N_4 &= \frac{1}{1 - L_r C_d \alpha_4^2} \\ M_4 &= \sqrt{1 - N_4^2} \end{aligned} \quad (23)$$

$$\left\{ \begin{aligned} I_{Lr}|_{T4} &= C_{41} M_4 \\ I_{Cd}|_{T4} &= C_{41} M_4 \\ V_{Lr}|_{T4} &= C_{41} L_r \alpha_4 N_4 \\ V_{Cd}|_{T4} &= \frac{C_{41}}{C_d \alpha_4} (1 - N_4) \\ V_{Cr1}|_{T4} &= \frac{2}{3} \left[C_{41} L_r \alpha_4 N_4 + \frac{C_{41}}{C_d \alpha_4} (1 - N_4) \right] \\ I_{Cr1}|_{T4} &= \left(\frac{2C_{41} C_{r1} - 2C_{41} C_{r1} L_r C_d \alpha_4^2}{3C_d} \right) M_4 \\ I_S|_{T4} &= \frac{I_{PM}}{2} - \left(\frac{2C_{41} C_{r1} - 2C_{41} C_{r1} L_r C_d \alpha_4^2}{3C_d} \right) M_4 \\ I_{Lf}|_{T4} &= \frac{I_{PM}}{2} - \left(\frac{2C_{41} C_{r1} - 2C_{41} C_{r1} L_r C_d \alpha_4^2 - 3C_{41} C_d}{3C_d} \right) M_4 \end{aligned} \right. \quad (24)$$

For Interval V, according to the above operating states' analysis, we can deduce the expressions of the electrical parameters as:

$$\left\{ \begin{aligned} i_{Lr}(t) &= C_{51} \sin \alpha_5 t + C_{52} \cos \alpha_5 t \\ v_{Cd}(t) &= C_{51} L_r \alpha_5 \cos \alpha_5 t - C_{52} L_r \alpha_5 \sin \alpha_5 t \\ i_{Lr}(t) &= i_{Cd}(t) \\ i_{Lf}(t) &= -\frac{V_{out}}{L_f} t + C_{53} \\ v_{Lr}(t) &= C_{52} L_r \alpha_5 \sin \alpha_5 t - C_{51} L_r \alpha_5 \cos \alpha_5 t \\ i_S(t) &= C_{51} \sin \alpha_5 t + C_{52} \cos \alpha_5 t - \frac{V_{out}}{L_f} t + C_{53} \end{aligned} \right. \quad (25)$$

The parameters in Equation (25) are listed as:

$$\alpha_5 = \frac{1}{\sqrt{L_r C_d}} \quad (26)$$

$$\begin{cases} C_{51} = V_{Cd} \big|_{T_4} \\ C_{52} = \frac{I_{Cd} \big|_{T_4}}{C_d \alpha_5} \\ C_{53} = I_{Lf} \big|_{T_4} \end{cases} \quad (27)$$

Since this interval ends when i_{S1} reduces to $0.5I_{PM}$ and from Equations (25)–(27), the time length of this interval T_5 can be deduced as:

$$\begin{aligned} T_5 &= \arcsin[M_5] \\ M_5 &= \frac{C_{51} \left(\frac{I_{PM}}{2} - \frac{I_{out}}{2} \right) + \sqrt{C_{51}^2 C_{52}^2 + C_{52}^4 - C_{52}^2 \left(\frac{I_{out}}{2} - \frac{I_{PM}}{2} \right)^2}}{(C_{51}^2 + C_{52}^2)} \\ N_5 &= \sqrt{1 - M_5^2} \end{aligned} \quad (28)$$

Then, we can get the final value of each electric parameter as:

$$\begin{cases} I_{Lr} \big|_{T_5} = C_{51} M_5 + C_{52} N_5 \\ V_{Cd} \big|_{T_5} = C_{51} L_r \alpha_5 N_5 - C_{52} L_r \alpha_5 M_5 \\ I_{Cd} \big|_{T_5} = C_{51} M_5 + C_{52} N_5 \\ I_{Lf} \big|_{T_5} = -\frac{V_{out}}{L_f} T_5 + I_{Lf} \big|_{T_4} \\ V_{Lr} \big|_{T_5} = C_{52} L_r \alpha_5 M_5 - C_{51} L_r \alpha_5 N_5 \\ I_S \big|_{T_5} = C_{51} M_5 + C_{52} N_5 - \frac{V_{out}}{L_f} T_5 + I_{Lf} \big|_{T_4} \end{cases} \quad (29)$$

For Interval VI, we can deduce the expressions of the electrical parameters as:

$$\begin{cases} i_{Cr1}(t) = C_{61} \alpha_6 t \\ v_{Cr1}(t) = \frac{C_{61} \alpha_6}{2C_{r1}} t^2 \\ i_{Lf}(t) = \frac{C_{61} \alpha_6}{6L_f C_d} t^3 - V_{out} t + C_{62} \\ i_S(t) = \frac{I_{PM}}{2} - C_{61} \alpha_6 t \end{cases} \quad (30)$$

$$\begin{cases} i_{Lr}(t) = i_{Cd}(t) = \frac{I_{PM}}{2} - \frac{C_{61} \alpha_6}{6L_f C_d} t^3 + V_{out} t - C_{61} \alpha_6 t - C_{62} \\ v_{Lr}(t) = L_r (V_{out} - C_{61} \alpha_6 - \frac{C_{61} \alpha_6}{2L_f C_d} t^2) \\ v_{Cd}(t) = \frac{C_{61} \alpha_6}{2C_d} t^2 - L_r (V_{out} - C_{61} \alpha_6 - \frac{C_{61} \alpha_6}{3L_f C_d} t^2) \end{cases}$$

$$\alpha_6 = \sqrt{\frac{L_r + 2L_f + \sqrt{4L_f^2 + L_r^2}}{2C_d L_f L_r}} \quad (31)$$

$$\begin{cases} C_{61} = -\frac{V_{Lr} \big|_{T_5}}{L_r \alpha_6} \\ C_{62} = I_{Lf} \big|_{T_5} \end{cases} \quad (32)$$

From Equations (30)–(32), the time length of this interval T_6 is:

$$T_6 = \frac{I_{PM}}{2C_{61}\alpha_6} \quad (33)$$

Then, we can get the final value of each parameter as:

$$\begin{cases} I_{Cr1}|_{T_6} = \frac{I_{PM}}{2} \\ V_{Cr1}|_{T_6} = \frac{C_{61}\alpha_6}{2C_{r1}}t^2 \\ I_{Lf}|_{T_6} = \frac{C_{61}\alpha_6}{6L_fC_d}T_6^3 - V_{out}T_6 + C_{62} \\ I_S|_{T_6} = 0 \\ I_{Lr}|_{T_6} = I_{Cd}|_{T_6} = \frac{I_{PM}}{2} - \frac{C_{61}\alpha_6}{6L_fC_d}T_6^3 + V_{out}T_6 - C_{61}\alpha_6T_6 - C_{62} \\ V_{Lr}|_{T_6} = L_r(V_{out} - C_{61}\alpha_6 - \frac{C_{61}\alpha_6}{2L_fC_d}T_6^2) \\ V_{Cd}|_{T_6} = \frac{C_{61}\alpha_6}{2C_d}T_6^2 - L_r(V_{out} - C_{61}\alpha_6 - \frac{C_{61}\alpha_6}{3L_fC_d}T_6^2) \end{cases} \quad (34)$$

3. System Design

In this section, based on the analysis above and the battery charging requirements, the hardware parameters and control strategy are designed. The design mainly focuses on the ZCS realization when considering the differences of battery parameters and charging conditions.

3.1. ZCS Condition Analysis

The system cannot realize ZCS under two conditions, which are:

- (1) The circuit parameters do not satisfy the ZCS requirement.
- (2) The circuit parameters are appropriate, but the driving signal is mismatched.

3.1.1. Mismatch of Circuit Parameters

To realize ZCS, the previous stage should provide the conditions to obtain the next stage. From the ideal waveforms in Figure 6 and the operating analysis above, we can deduce the constraint expressions.

Interval I and II should be long enough to guarantee energy storage, for the resonant inductor current to be positive. This can be expressed as, at the end of Interval III, the voltage of v_{Cr} is positive.

$$V_{Cr1}|_{T_3} = C_{31}M_3 + C_{32}N_3 > 0 \quad (35)$$

C_r must be completely discharged when the resonant inductor current is positive. This can be expressed as:

$$I_{Lr}|_{T_4} = C_{41}M_4 > 0 \quad (36)$$

During Interval V and Interval VI, L_r and C_d form a resonant tank. Only if C_d have enough energy, the resonant inductor current can reach output current $0.5I_{out}$, and i_S can reach zero to realize ZCS. It can be described as:

$$V_{cd}|_{T_5} = C_{s1}L_r\alpha_5N_5 - C_{s2}L_r\alpha_5M_5 > 0 \quad (37)$$

$$V_{cd}|_{T_6} = \frac{C_{61}\alpha_6}{2C_d}T_6^2 - L_r(V_{out} - C_{61}\alpha_6 - \frac{C_{61}\alpha_6}{3L_fC_d}T_6^2) > 0 \quad (38)$$

Figure 8 shows the working waveforms with mismatched circuit parameters, where the converter cannot realize ZCS. We can see that the output side resonant capacitor is entirely discharged before i_S decreases to zero. Thus, i_S fails to drop down to zero, and ZCS cannot be realized.

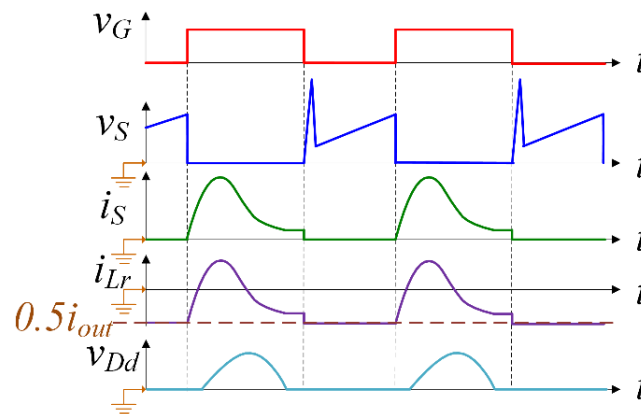


Figure 8. Typical waveforms with mismatch circuit parameters.

3.1.2. Mismatch of the Driving Signal

ZCS can only be realized when the circuit and the driving signal are matched. The condition that optimizes the circuit parameters with an improper driving signal is discussed below, and the typical waveforms are shown in Figure 9. Figure 9a shows the waveforms when T_{on} is shorter than the minimum allowable value, and Figure 9b shows the waveforms when T_{on} is longer than the maximum allowable value.

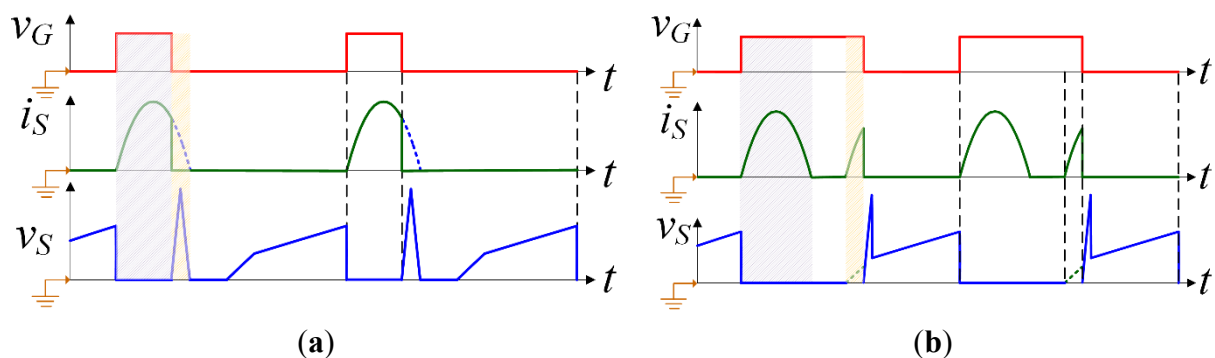


Figure 9. Theoretical waveforms with mismatch driving signal. (a) T_{on} is too short and (b) T_{on} is too long

Regarding the ideal waveforms of the proposed converter, which are shown in Figure 6, ZCS can only be realized during a specified period. Additionally, if the drive signal turns to zero before i_{S1} decreases to zero, ZCS will not be realized obviously, and this constraint is expressed as Equation (39).

Besides, if the drive signal remains on after the voltage v_{S1} increases to zero, S_1 will be turned on again, and ZCS will not be realized either; the constraint expression is shown in Equation (40).

$$T_{on} \geq T_6 \quad (39)$$

$$\begin{cases} T_{on} \leq T_6 + T_\delta \\ \frac{3I_g}{2C_r} T_\delta - (V_{out} - \frac{I_{out}}{C_d} T_\delta) = 0 \end{cases} \quad (40)$$

3.1.3. ZCS Boundary

Based on the above analysis and the constraints shown in Equations (35)–(40), the T_{on} range and ZCS boundary can be obtained, when the parameters of the resonant devices vary under the maximum power output condition (380-V input line voltage, 400-V output voltage, 8-Ohm load resistance). Figure 10a,b illustrates the minimum and maximum T_{on} value to realize ZCS, respectively. The driving frequency to satisfy the maximum output power with resonant device parameters changing is shown in Figure 11.

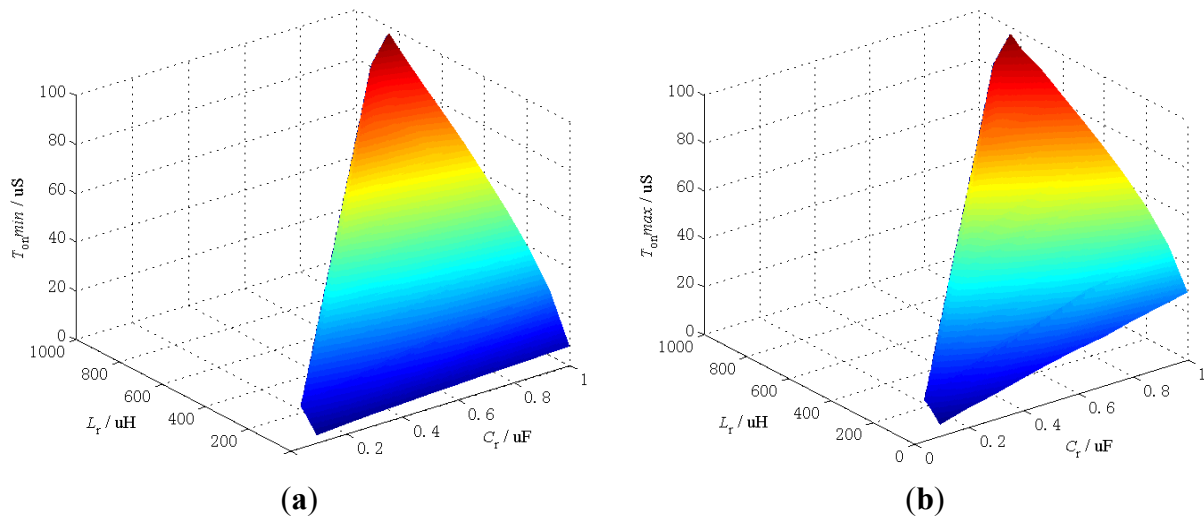


Figure 10. Minimum and maximum T_{on} value to realize zero-current-switching (ZCS). (a) minimum T_{on} and (b) maximum T_{on} .

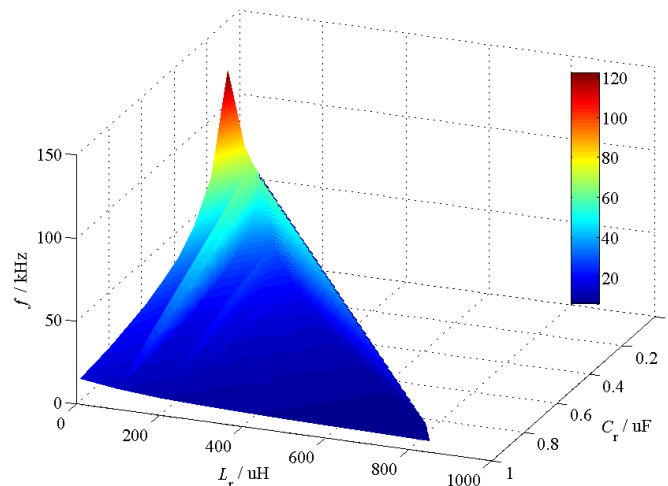


Figure 11. Driving frequency f to realize maximum output power.

3.2. ZCS and Battery

In this section, the cooperative control between ZCS realization and the three-stage battery charging method is studied, and the negative influence of battery charging status on ZCS realization is analyzed. Furthermore, a new method is presented to limit the minimum driving frequency when the battery is in a different status of charging.

In order to optimize the charge cycles and lifetime of EV batteries, we adopt the three-stage charging method. The three stages are: constant current stage, constant voltage stage and floating voltage stage. During the constant current stage, the open-circuit voltage of the battery is about 300 V, and it is charged by a constant current of 50 A. The battery voltage increases with the charging process. When the voltage increases to 400 V, this stage ends, and the constant voltage stage begins. In the constant voltage stage, the charging voltage is 400 V, and the charging current will decrease; this stage ends when the current is below 5 A. The floating voltage stage is actually a low constant voltage stage to ensure a small charging current, to make sure that the battery is truly saturated to extend the service time. During this stage, the charging voltage is 350 V. The charging process and parameter settings are shown in Figure 12 and Table 1. Restricted by the experimental conditions, we use resistor load to simulate the batteries, and the equivalent resistor value is also shown in Figure 12 and Table 1.

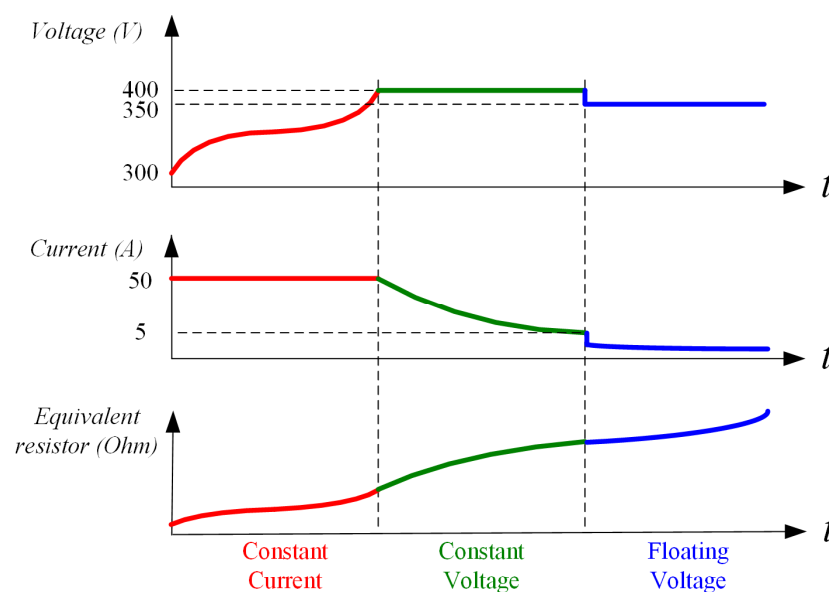


Figure 12. Three-stage charging process.

Table 1. Three-stage charging parameters.

Stage	I_{out} (A)	V_{out} (V)	R_{load} (Ohm)
Constant current	50	300–400	6–8
Constant voltage	50–5	400	8–80
Floating voltage	4.4–2	350	80–175

During the whole process of charging, the fluctuation range of the load equivalent resistance is very large. Just as the parameters shown in Table 1, at the end of the constant current stage, the charging power is the greatest at 20 kW. At the end of the floating voltage process, the minimum charging power

is 0.7 kW. If we use the PFM control strategy during the whole process, the driving frequency variation range is very large. We select a point of the floating voltage stage as an example. If the equivalent resistor is 100 Ohm, the driving frequency should be 5.5 kHz to get a voltage output of 350 V. The simulation waveforms are shown in Figure 13. From Figure 13c, it can be seen that at this working point, the power switch S works under the ZCS condition, while, the driving frequency is very low, so the turn off time is much longer than the resonant period of the resonant tank: L_r , C_r and C_d . Therefore, before S_1 turns on, the resonant components will begin the next resonant cycle. Reactive power will be circulating in the tank, which will reduce the system efficiency and increase the THD of the input current.

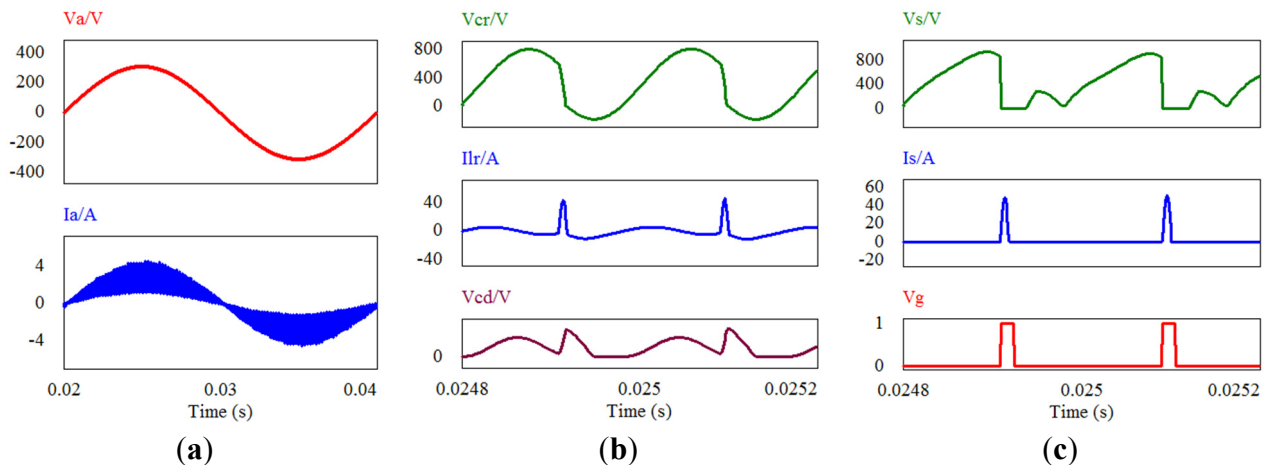


Figure 13. Simulation waveforms of the floating voltage charging stage. (a) input phase voltage and input phase current; (b) resonant capacitors voltage and resonant inductor current and (c) voltage and current of IGBT and gate signal.

To solve the mentioned problem, we proposed a new control strategy. The complete control method of the system should be as follows: take the PFM control strategy at the beginning of the charging process (the conduction time is constant), and satisfy the output requirements by adjusting the frequency. If the PFM frequency is lower than 10 kHz, convert it to the PWM control strategy, keep the fixed driving frequency at 10 kHz and satisfy the output requirements by adjusting the conduction time T_{on} . The charging process control flow chart is shown in Figure 14.

By using the proposed control strategy, the minimum frequency is set at 10 kHz, and the frequency fluctuation will be reduced. Although the PWM strategy cannot guarantee ZCS realization, under the condition of a light load, the conduction losses increase greatly, are greater than the switching losses and seriously affect the system efficiency. Thus, using the PWM control strategy can contribute to the improvement of the system's efficiency. What is more, this strategy can reduce the unexpected resonance on the resonant devices and power switches caused by a sharp drop of the driving frequency under a light load, which will lead to the increase of the input current THD.

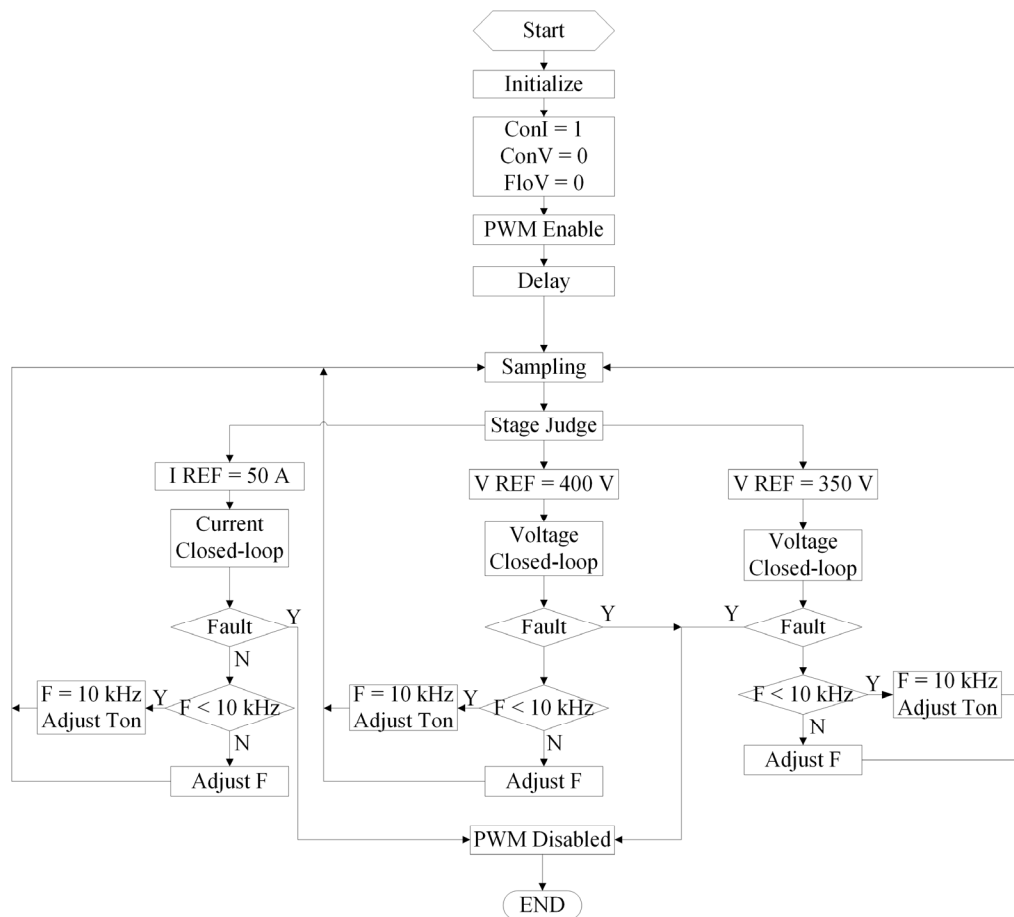


Figure 14. Charging process control flow chart.

3.3. Optimized Parameters

Considering the fact that the output voltage and current are changing during the whole charging process, we chose a set of circuit parameters that can ensure ZCS in the whole load range, as shown in Table 2.

Table 2. Main components of the prototype.

Component	Value
Input filter inductors L_a – L_c	2 mH
Resonant inductor L_r	50 μ H
Output filter inductor L_f	800 μ H
Input side resonant capacitors C_{r1} – C_{r3}	0.65 μ F
Output side resonant capacitor C_d	0.44 μ F
Output filter capacitor C_f	860 μ F
Uncontrolled rectifier diodes D_1 – D_6	C3D25170H
Fly-wheel diode D_d	C3D25170H
Power switch S_1	IGW25T120 3 in parallel

As shown in Table 3, the power devices are selected at the maximum output current and voltage, which are 50 A and 400 V, respectively. From the interval analysis and Equations (7)–(34), we can

calculate the voltage and current stresses of the main power devices in the circuit and finally determine the device type as follows.

Table 3. Voltage and current stress of the main power devices.

Component	Peak Voltage (V)	Voltage RMS (V)	Peak Current (A)	Current RMS (A)	Value
D_1 – D_6	1170	440	95	20	C3D25170H
D_d	900	500	25	7	C3D25170H
S_1	1100	470	30	12	IXBH42N170A 3 in parallel
L_a – L_c	-	-	23	16	-
L_r	-	-	65	32	-
L_f	-	-	27	25	-
C_d	900	500	65	31	-
C_{r1} – C_{r3}	650	270	75	25	-

3.4. Design of the Inductors

Besides the power switches and diodes selected above, the design of the inductors is very critical for the system design.

Through the theoretical analysis above, the currents of input filter inductors L_a – L_c and the output filter inductor L_f are sine wave shaped input current and non-oscillatory DC output current, respectively. Thus, the FeSi circular magnetic rings (PPF306060) are chosen to be the magnetic cores of the input and output filter inductors. Since the currents of the resonant inductors are a high-frequency resonant current with an extremely high peak value, a specially designed air gap is needed for the high frequency peak energy storage, and E-shaped magnetic cores (EE110) are selected for the resonant inductors.

3.4.1. Input Filter Inductor

According to the theoretical analysis and simulation results, the input filter inductance is 2 mH; the peak inductor current is 23 A; and the RMS current is 16 A. We choose the magnetic core PPF306060 and use three cores in parallel. The inductance can be determined by the relative permeability and the effective core parameters as:

$$L = \frac{4\pi\mu N^2 A}{e} \quad (41)$$

In Equation (41), μ represents relative permeability; N represents the number of turns; A represents the effective cross-section area; e represents the mean magnetic path length. From the parameters shown in the datasheet of PPF306060, it can be computed that $N = 84$.

3.4.2. Resonant Inductor

According to the theoretical analysis and simulation results, the resonant inductance is 50 μ H, and the peak inductor current and RMS current are 65 A and 32 A, respectively. The inductor core is selected as EE110, and the material is PC-40 (MnZn power ferrite material). The turns of this inductor can be calculated as:

$$N = \frac{LI_p}{A_e B_{\max}} \quad (42)$$

From the datasheet, $A_e = 1296 \text{ mm}^2$ and $B_{\max} = 0.39 \text{ T}$. Thus, the turns can be deduced: $N = 7$.

3.4.3. Output Filter Inductor

According to the simulation results, the output filter inductance is $800 \mu\text{H}$; the peak inductor current is 27 A ; and the RMS current is 25 A . We also choose the magnetic core PPF306060 and use three cores in parallel. The number of turns can be calculated in the same way as Equation (41), and the parameters of this core are exactly the same as those of the input filters; finally, $N = 54$.

3.5. Loss Distribution

In this section, the power losses of the power switches, power diodes, inductors and capacitors at 50 A and 400 V output are estimated.

3.5.1. Power Switches

When calculating the power switch losses in the maximum power output condition, in view of the ZCS status of the power switches, we ignore the switching losses and only consider the conduction losses. The losses can be calculated by the following expression.

$$P_{\text{cond}} = D \times V_{\text{CESAT}} \times I_C \quad (43)$$

In Equation (43), D represents the duty ratio, V_{CESAT} represents the drop voltage of the switch and I_C represents the average current flow through the switch.

In the maximum power output condition, the driving frequency is about 35 kHz , so D is about 0.53 . The current of each switch can be approximated to a sine wave, shown in Equation (44), from zero to π . According to the datasheet of the switch, V_{CESAT} at this point is 2.1 V .

$$I_C = \frac{(0.5I_{\text{out}} + C_{41})}{3} \sin \frac{t}{2\pi\sqrt{L_r C_d}} \quad (43)$$

From Equations (43) and (44), the power loss of each power switch is:

$$P_{\text{cond}} = 0.525 \times 2.1 \times \int_0^{15} I_C dt = 60 \text{ W} \quad (44)$$

Thus, the total power loss of the 6 IGBTs is: $P_S = 6 \times P_{\text{cond}} = 360 \text{ W}$.

3.5.2. Uncontrolled Rectifier Bridge Diodes

Just like the IGBTs, only conduction losses of the uncontrolled rectifier bridge diodes are considered:

$$P_f = D \times V_f \times I_f \quad (45)$$

$$\begin{cases} V_f = V_T + I_f \times R_T \\ R_T = 0.03 + (T \times 0.5 \times 10^{-3}) \\ V_T = 0.99 - (T \times 1.5 \times 10^{-3}) \end{cases} \quad (46)$$

According to the parameters shown in the datasheet and the operating point of the diodes, we can get that the power loss of each diode in the uncontrolled rectifier is 25 W.

Therefore, the total power losses of 12 uncontrolled rectifier diodes in the maximum power output condition can be shown as: $P_{DBir} = 12 \times P_f = 300\text{ W}$.

3.5.3. Fly-Wheel Diodes

The calculating formula of fly-wheel diodes is the same as those of the rectifier diodes shown in Equations (46) and (47). Based on the interval analysis above, the current of the fly-wheel diodes is half of the output current. Thus, we can calculate the power loss for each fly-wheel diode to be about 7 W.

The total power loss of the two fly-wheel diodes in the maximum power output condition is 14 W.

The power dissipation of all the diodes in the OBC is: $P_D = P_{DBir} + P_{DFly} = 314\text{ W}$.

3.5.4. Resonant and Filter Capacitors

The losses of the capacitors include two parts: dielectric loss and metal loss. The calculating expression is shown in Equations (48) and (49).

$$P = UI \sin \theta \quad (47)$$

$$\tan \theta = \tan \theta_0 + 2\pi f \times C_n \times R_{ESR} \quad (48)$$

In Equations (48) and (49), R_{ESR} represents equivalent series resistance, $\tan \theta_0$ represents the dielectric dissipation factor and $\tan \theta$ represents the dissipation factor.

For the input side resonant capacitors, the datasheet gives that the $\tan \theta$ is lower than 0.001, so we select the maximum value 0.001 as the dissipation factor. Considering that the dissipation angle is too small, the sine value can be approximated to the tangent value. Consequently, the power losses of the six input side resonant capacitors can be calculated as: $P_{Cr} = 6 \times (270\text{ V} \times 25\text{ A} \times 0.001) = 40.5\text{ W}$.

The output side resonant capacitors use the same calculation and approximation method as the input side resonant capacitors. We use two 0.22- μF capacitors in parallel for each channel. The dissipation factor is lower than 0.006. Thus, the power losses of the four output side resonant capacitors can be calculated as: $P_{Cd} = 4 \times (500\text{ V} \times 5\text{ A} \times 0.0006) = 6\text{ W}$.

Using the same calculation and approximation method, the power losses of the output filter capacitors can be calculated. We use two 430- μF capacitors in parallel for each channel, and the datasheet gives that the dissipation factor is lower than 0.002 at the operating point. Therefore, the power loss of the output filter capacitors is: $P_{Cf} = 2 \times (400\text{ V} \times 10\text{ A} \times 0.002) = 16\text{ W}$.

Therefore, the total power losses of the capacitors in the OBC can be calculated as: $P_C = P_{Cd} + P_{Cr} + P_{Cf} = 62.5\text{ W}$.

3.5.5. Resonant and Filter Inductors

The power losses of the inductor can be divided into two parts: core loss and winding loss.

For the magnetic core PPF306060, the core loss can be decided by the flux density and working frequency. The flux density can be calculated by the following expression.

$$B = \frac{0.4\pi\mu NI}{l} \quad (50)$$

$$P_{core} = 0.42B^{2.2}f^{1.87} \times V \quad (51)$$

where B represents flux density (kG); μ represents relative permeability; N represents the number of turns; l means magnetic path length (cm); I represents peak magnetic current (A); f represents the working frequency (kHz) and V represents the volume of the magnetic core (cm³).

The winding loss is the heat loss caused by the coil resistance, and it can be calculated by Ohm's law, shown in following expression.

$$P_{wind} = I^2 R \quad (52)$$

From Equations (50)–(52), we can get the power losses of the six input filter inductors and the two output filter inductors, respectively, as: $P_{Lin} = 6 \times (P_{core} + P_{wire}) = 72$ W; $P_{Lf} = 2 \times (P_{core} + P_{wire}) = 24$ W.

For the resonant inductor, the winding loss is very small compared to the core loss. The core is designed as PC-40 EE110, where $V_e = 336,420$ mm³. According to the datasheet, the core loss per volume is obtained as: $P_{cv} = 0.0004$ W/mm³ at 60 °C. As a result, the core losses of two resonant inductors are:

$$P_{Lr} = 2 \times (V_e \cdot P_{cv}) = 269$$
 W (53)

Thus, the total power losses of the inductors in the system can be shown as: $P_L = P_{Lr} + P_{Lin} + P_{Lf} = 365$ W.

Finally, based on the calculation results shown in Equations (43)–(53), the conversion efficiency at the 20-kW output condition can be deduced as:

$$\eta_{\%} = \frac{P_{out}}{P_{out} + P_S + P_D + P_C + P_L} \times 100\% = 94.8\% \quad (54)$$

A power loss distribution under a 20-kW load is shown in Figure 15. It can be concluded that the dissipation of this OBC mainly centralizes at the IGBTs, resonant inductors and bridge diodes. Additionally, this will be verified in the experiment section.

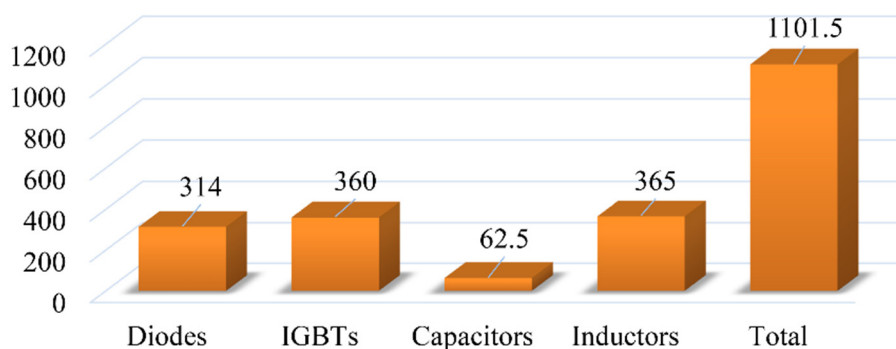


Figure 15. Power loss distribution.

4. Simulation and Experiment

In order to verify the efficiency, PFC and THD of the proposed topology and the accuracy of the theoretical analysis above, we established a simulation model. Furthermore, a hardware platform was built for the experimental research.

4.1. Simulation Result

4.1.1. Simulation at Maximum Output Power

Figure 16 illustrates the simulation waveforms of the proposed topology at the maximum output power (50-A current and 400-V voltage). There are two parallel interleaved channels in the circuit, and the driving signals have a 180-degree phase shift from each other. Figure 16a shows the waveforms of the input line current with its AC phase voltage and output voltage. Figure 16b shows the details of the IGBT voltage and current. Figure 16c shows the voltage waveforms of the resonant capacitors C_r and C_d and the current of the resonant inductor L_r .

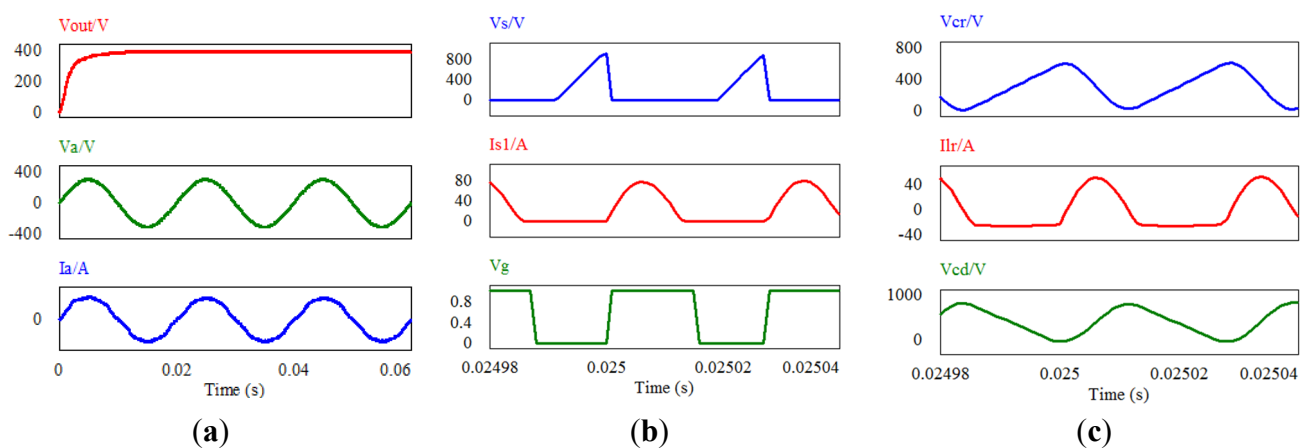


Figure 16. Simulated waveforms under 20-kW maximum output power: (a) input current, input and output voltage; (b) voltage and current of IGBT; (c) voltage of resonant devices.

The simulation results indicate that the proposed topology can realize the maximum output power at 34.5 kHz; the measured THD of the input current is 3.5%, and PF is 0.998. Besides, the detailed waveforms of the resonant components are consistent with the theoretical analysis results. The voltage and current waveforms of the IGBT show that the buck switches can realize ZCS at the maximum output power.

4.1.2. Simulation of the Proposed Control Strategy

In order to verify the effectiveness of the proposed control strategy, two groups of simulations under a low-power condition with traditional PFM control and the proposed hybrid PFM control method are compared in Figure 18. Take the charging process ending point for example, for which the output voltage and current are 350 V and 2 A, respectively. For these two groups of simulations, the input and output conditions are the same: 380-V input line voltage, 350-V output voltage and 2-A output current.

Figure 17a shows the input voltage and current of phase a under a 5-kHz driving frequency and a 15- μ s turn on time. I_{a1} is the input current of a single channel, and I_a is the input current of phase a . The results indicate that the interleaved structure will reduce the input current ripple obviously. However, I_a under the PFM control strategy has a great fluctuation, and the THD is about 41.2%. Figure 17b shows the input voltage and current of phase a under a 10-kHz driving frequency and a 5.8- μ s turn on time. It can be seen that the proposed control strategy eliminates the phase shift between V_a and I_a , and the THD of

I_a decreases to 25.1%. Therefore, by adopting the new proposed hybrid PFM control method, the quality of the input current waveform can be improved obviously.

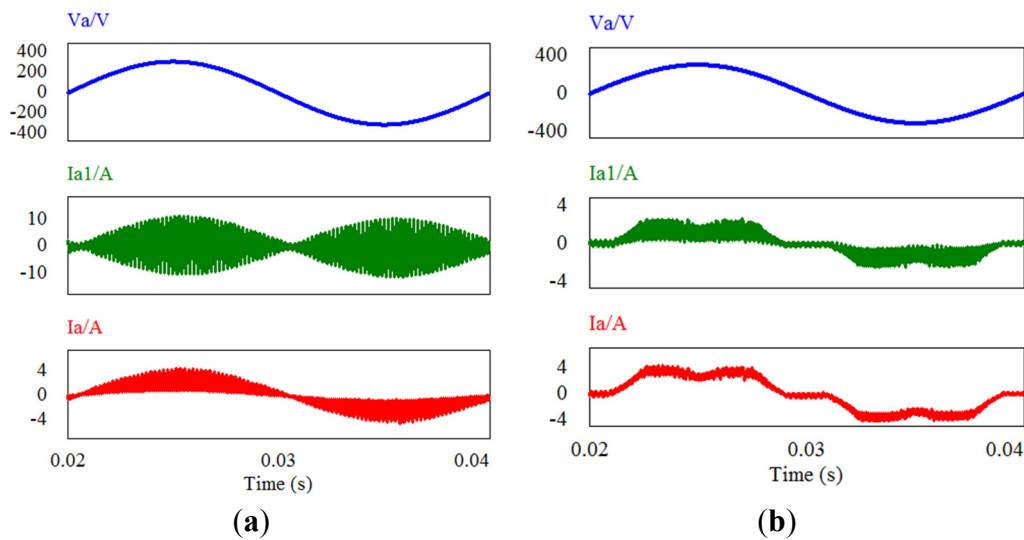


Figure 17. Simulated waveforms: (a) PFM; (b) the proposed hybrid PFM control strategy.

4.1.3. Simulation under Imbalanced Current Condition

Besides the simulations based on equally-shared input currents for the two parallel circuits above, the condition under an imbalanced current is also simulated. In this situation, the resonant inductors L_r and L_{rs} are set to be 50 μH and 20 μH separately, and the output is 20 kW.

The simulation waveforms of the two paralleled channels use the same driving signals with a 180-degree phase shift from each other and are shown in Figure 18a. At this time, the driving frequency of both channels is 35 kHz. In Figure 18a, $0.2 V_a$ and input current I_a are compared to illustrate PF of the system, V_{out} , and the contrast between I_{a1} and I_{a2} is also shown in Figure 18a. By calculation, we can get the RMS value, THD and PF of I_{a1} , I_{a2} and I_a , as shown in Table 4.

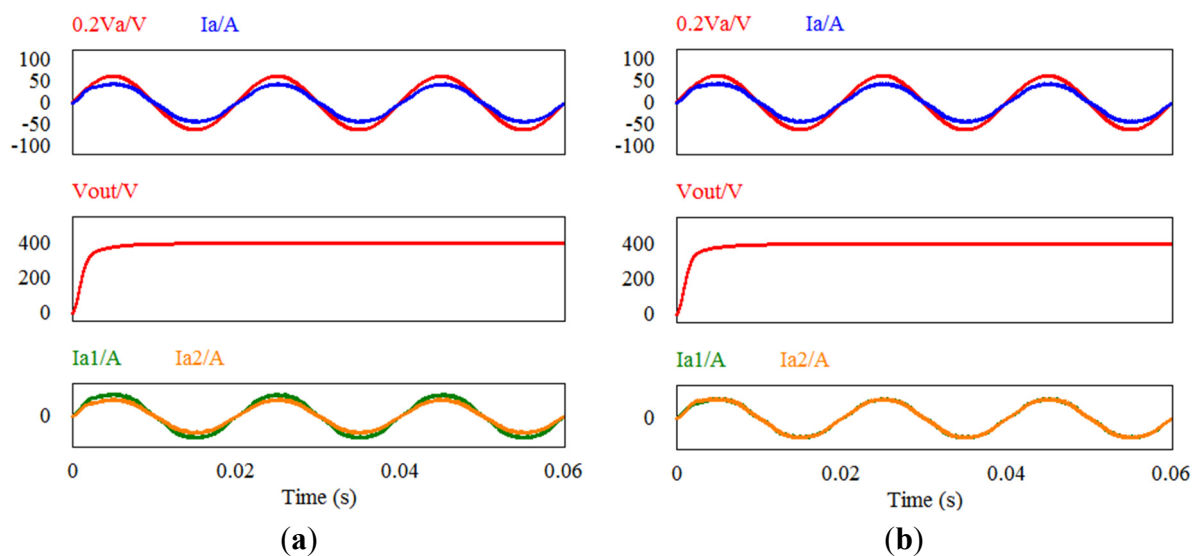


Figure 18. Simulated waveforms under the imbalanced current condition: (a) two channels with a synchronous drive; (b) the current sharing control strategy.

Although the current imbalance has no effect on the PF and THD of the circuit, it will cause the uneven distribution of heat, which will limit the increase of the system power. Therefore, a current sharing control strategy can be used: the current of two paralleled circuits can be equally shared by adjusting the driving frequency of the two paralleled circuits respectively when the circuit parameters are not exactly the same. The simulation results using the current sharing control strategy are shown in Figure 18b. Additionally, the statistic parameters are also shown in Table 4.

Table 4. Simulation results' contrast under balanced and imbalanced current.

Resonant Inductor (μH)		Driving Frequency (kHz)		Input Current RMS (A)			THD (%)			PF		
L_r	L_{rs}	f_1	f_2	I_a	I_{a1}	I_{a2}	I_a	I_{a1}	I_{a2}	I_a	I_{a1}	I_{a2}
50	50	33.0	33.0	31.2	15.6	15.6	3.46	4.13	4.13	0.998	0.998	0.998
50	20	35.0	35.0	30.9	17.5	13.3	3.08	4.30	3.00	0.998	0.998	0.998
50	20	32.9	38.2	31.0	15.5	15.5	3.46	4.13	3.43	0.998	0.998	0.998

4.2. Experiment Result

To verify the performance of the proposed topology, a prototype based on the previous study is built. Freescale MCU is used as the monolithic digital controller. Figure 19 is the photo of the prototype.



Figure 19. Prototype of the proposed topology.

4.2.1. Maximum Output Power Experiment

Restricted by experimental conditions, the maximum output power experiment can only be done at 8.5 kW. The experiment result of a 200-V output at a 6-Ohm load is presented in Figure 20. Figure 20a shows the input line voltage, input phase a current and output current. Figure 20b shows the envelope of the IGBT voltage v_s , IGBT current i_s , resonant inductor L_r current i_{Lr} and output current of the single channel $0.5i_{out}$. Figure 20c is the enlarged waveforms of Figure 20b, from which we can see that the IGBT realized ZCS and was completely consistent with the theoretical analysis waveforms shown in Section 3. Figure 20d is the thermal image, and the maximum temperature is about 46.8 degrees centigrade in the steady state. The concrete data of this experiment are as follows: input line voltage: 230 V; driving frequency: 30 kHz; turn on time T_{on} : 15 μs ; output voltage: 200 V; load resistance: 6 Ohm; input current THD: 4.3%; PF: 0.98 and efficiency: 93.7%.

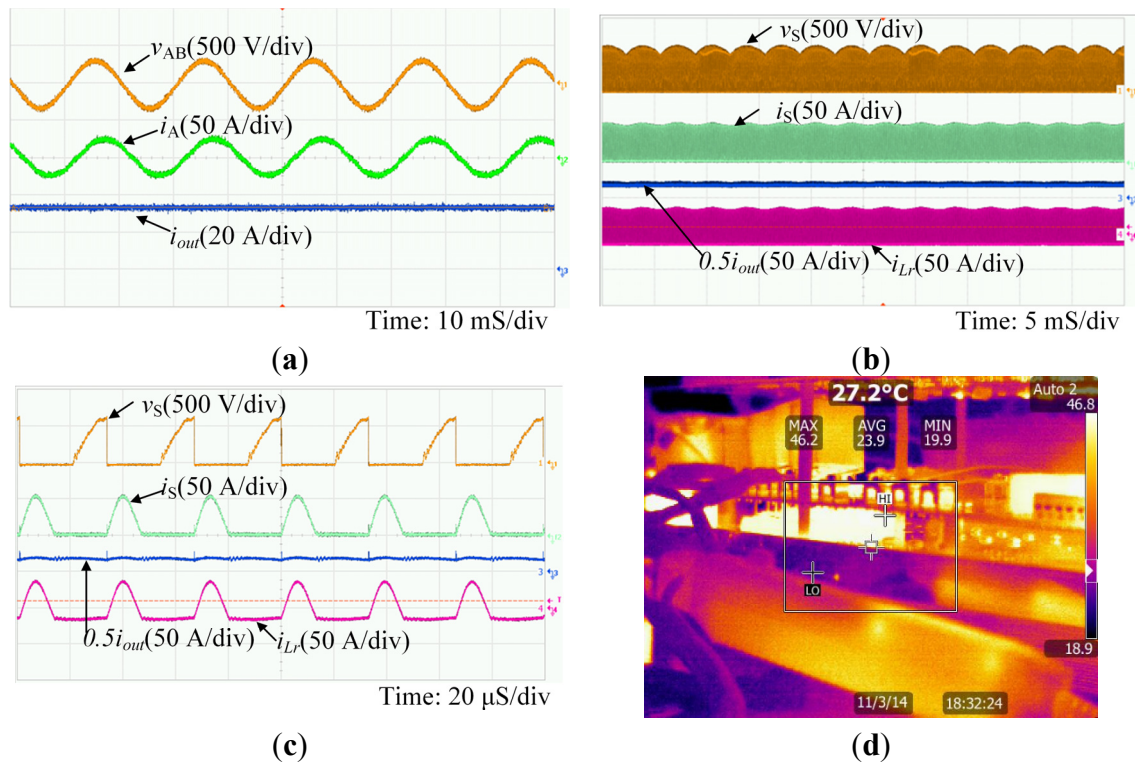


Figure 20. Experimental results (230-V input line voltage, 200-V output, 6-Ohm load resistance): (a) input voltage, input and output current; (b) envelop of resonant voltage and current; (c) enlarged waveform of resonant voltage and current; (d) thermal image.

4.2.2. Three-Stage Charging Process Experiment

The three-stage charging process is implemented by equivalent experiments, in which several variable high-power resistors are used as the load. In order to avoid overheating, the charging process is only fulfilled at the low-power level. The experimental parameters of three-stage charging are shown in Table 5.

Figure 21a shows the collector-emitter (C-E) voltage and current of the IGBT and the output current at a 70-V input line voltage. The driving frequency reached the upper limit of 40 kHz, and the output current is 9.2 A. Figure 21b shows the same parameters at a 90-V input line voltage; at this time, the driving frequency is 29 kHz, and the output current is 10 A. Comparing these experimental results, it can be concluded that the proposed control method can satisfy the requirements of constant current charging by adjusting the driving frequency, and even when the load or frequency changes, this circuit still can realize ZCS.

Table 5. Three-stage charging process parameter setting.

Stage	Output Voltage (V)	Output Current (A)	Load Resistance (Ohm)
Constant current	-	10	9
Constant voltage	120	-	15
Floating voltage	100	-	40

Note: In this table, “-” means that at that stage, this value is not a parameter that needs to be controlled.

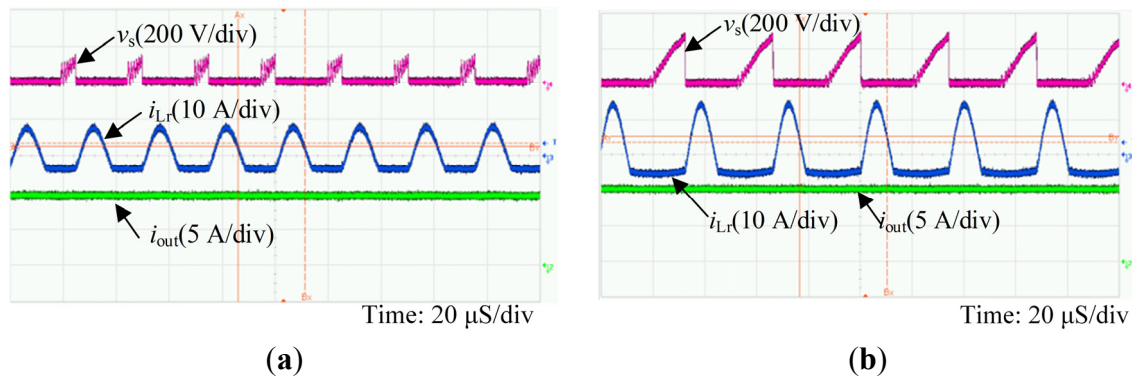


Figure 21. Experimental results under constant current charging: (a) 70-V line in; (b) 90-V line in.

Two groups of experimental results under the constant voltage stage are also compared in Figure 22. Figure 22a shows the C-E voltage and current of the IGBT and output current at a 90-V input line voltage. The driving frequency reached the upper limit of 40 kHz, and the output voltage is 106.8 V. Figure 22b shows the same parameters at a 110-V input line voltage. The driving frequency is 25 kHz, and the output voltage is 120.1 V. Constant voltage charging and ZCS are realized.

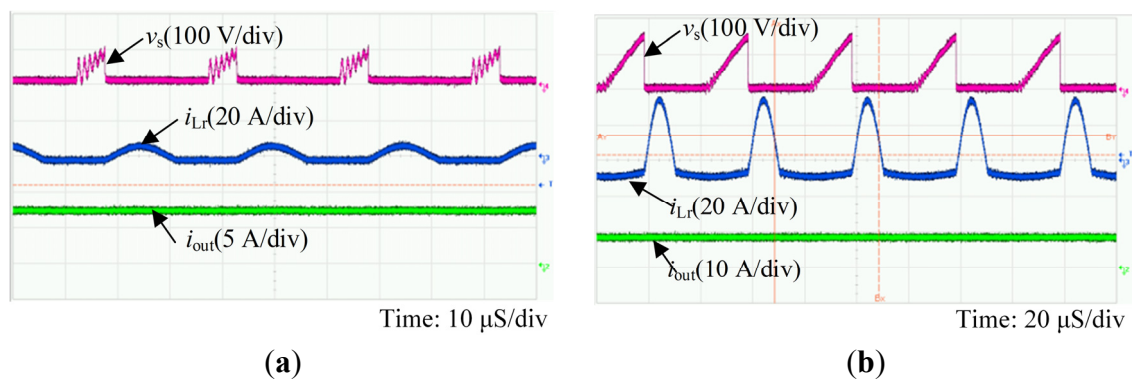


Figure 22. Experimental results under the constant voltage charging stage (a) 106.8 V out; (b) 110 V out.

The experimental results of floating charging stage are shown in Figure 23. Figure 23b is the enlarged waveforms of Figure 23a. It also shows the C-E voltage and current of the IGBT and output current at a 120-V input line voltage; at this condition, the driving frequency is 25 kHz and the output current 2.5 A, and the load resistance is 40 Ohm. In this case, ZCS is also realized in the possible load range.

Figure 24 shows the experimental waveforms in the process of charging state switching. Figure 24a shows the waveforms of the transformational transition from the constant current stage to the constant voltage stage. During this interval, the output current i_{out} turns to 8 A from 10 A in 2.5 ms. Figure 24b shows the switching point from the constant voltage charging stage to the floating voltage charging stage, where i_{out} turns from 8 A down to 2.5 A within 3.2 ms. It can be concluded that the built OBC platform can realize the switching of three charging stages smoothly without obvious overshoot and oscillation.

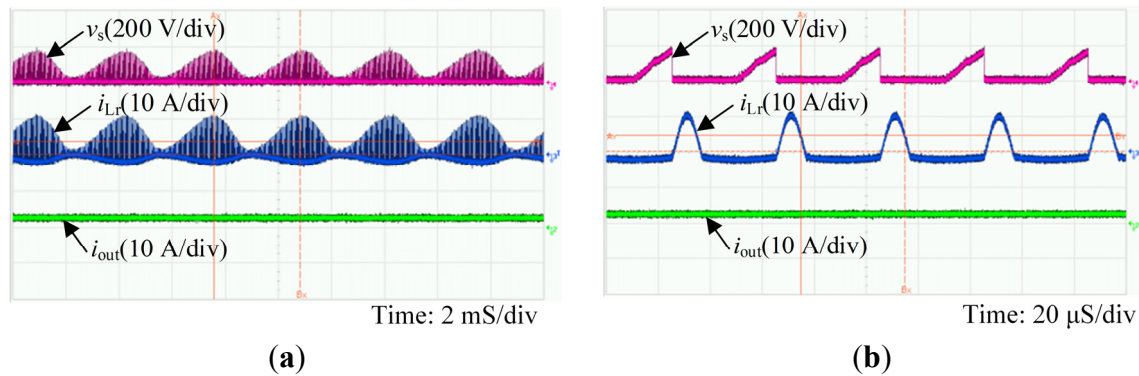


Figure 23. Experiment results under the floating voltage charging stage.

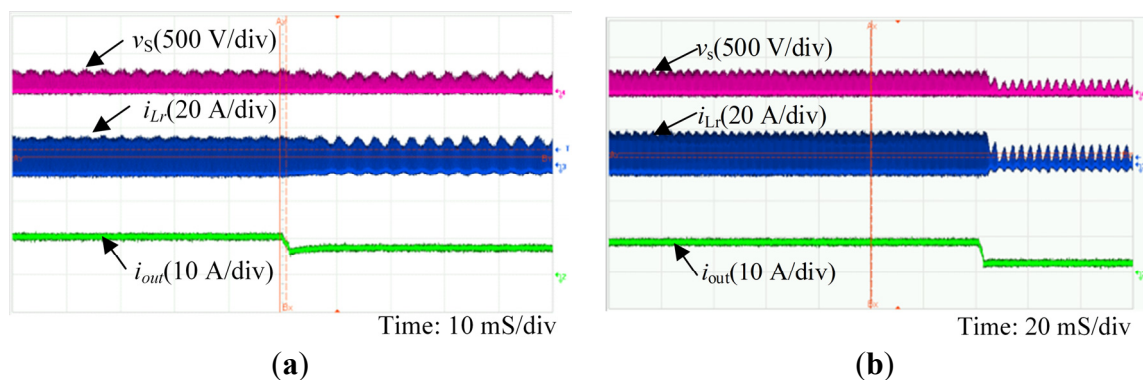


Figure 24. Experimental results under the mode transition point.

After a series of experiments, the efficiency, THD and PF of this OBC platform under different output powers are obtained and shown in Figure 25. It is shown that, with the power increases, the efficiency stays in a stable range between 93.5% and 94.0%. At the maximum output condition, the THD is about 4.3%, and PF is about 0.98.

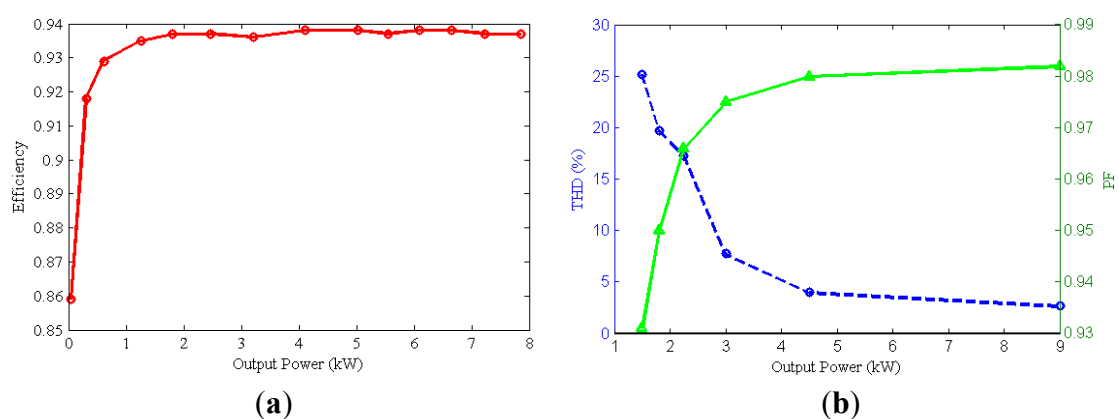


Figure 25. Measured efficiency, total harmonic distortion (THD) and PF curves: (a) efficiency; (b) THD and PF.

5. Conclusions

This paper proposed a three-phase interleaved high-efficiency and high power factor ZCS OBC for EV application. By using the multi-resonant structure, the buck switch can realize ZCS and can achieve

a high-quality input current waveform with high PF and low THD. The ZCS constraint conditions were deduced under a battery load. A hybrid PFM control method based on the battery load requirements during the three-stage charging process is also proposed. This method combines the PFM and PWM strategy and keeps the driving frequency in a range of 10 kHz–40 kHz, to avoid the power losses caused by the reactive power transmission and resonance at a low frequency.

The performance of the proposed charger has been verified through experimental results based on the built prototype platform. Due to the power upper limit of the AC source, the maximum output power experiment was done at 8.5 kW only. The efficiency is above 93.5%, and THD and PF remain around 4.3% and 0.98, respectively. Moreover, simulations and experimental results were verify the theoretical analysis. It is shown that the proposed interleaved three-phase high-power ZCS buck rectifier is suitable for high-frequency and high-efficiency OBC applications.

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Author Contributions

Cheng-Shan Wang, Wei Li and Yi-Feng Wang designed the main parts of the study, including the circuit simulation model, topology innovation and simulation development. Zhun Meng helped in the hardware development and experiment. Jie-Gui Zhou were also responsible for writing the paper.

Conflicts of Interest

The authors declare no conflict of interest.

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