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Design and Implementation of a High Efficiency, Low Component Voltage Stress, Single-Switch High Step-Up Voltage Converter for Vehicular Green Energy Systems

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Academic Editor: Ching-Ming Lai

Received: 30 June 2016; Accepted: 20 September 2016; Published: 25 September 2016

Abstract: In this study, a novel, non-isolated, cascade-type, single-switch, high step-up DC/DC converter was developed for green energy systems. An integrated coupled inductor and voltage lift circuit were applied to simplify the converter structure and satisfy the requirements of high efficiency and high voltage gain ratios. In addition, the proposed structure is controllable with a single switch, which effectively reduces the circuit cost and simplifies the control circuit. With the leakage inductor energy recovery function and active voltage clamp characteristics being present, the circuit yields optimizable conversion efficiency and low component voltage stress. After the operating principles of the proposed structure and characteristics of a steady-state circuit were analyzed, a converter prototype with 450 W, 40 V of input voltage, 400 V of output voltage, and 95% operating efficiency was fabricated. The Renesas MCU RX62T was employed to control the circuits. Experimental results were analyzed to validate the feasibility and effectiveness of the proposed system.

Keywords: cascade structure; coupled inductor; green energy; high step-up converter

1. Introduction

In response to climate change and global warming induced by heavy use of fossil fuels, energy conservation and carbon reduction techniques, such as developing clean energies and increasing energy use efficiency, have become a global focus. Major countries across the globe have endeavored to develop low-carbon economies based on high performance and low emissions and have adjusted various industry, energy, technology, and transaction-related policies [1,2] to encourage green industry development. Moreover, because fossil fuel supplies are overly concentrated in areas with social instability, fuel prices are typically volatile and affected by human factors (e.g., political schemes and policies). Thus, fossil fuel energy supplies become restricted, resulting in increased geopolitical risks for investors and hindering energy production, transportation, and infrastructure construction and maintenance. Typically, such adversity indirectly leads to social instability and volatile political developments in developing countries. To address these problems, green energies have been developed as the primary method to propel contemporary progression.

The reusability of green energies is unaffected by conventional energy shortages. Numerous applications of green energies have been developed in recent years, such as photovoltaics (PV), wind power, biomass energy, and tidal energy production. However, these green energies are highly dependent on natural conditions and require high investment and maintenance costs, resulting in low power efficiency and high total power generation cost. In addition, the output voltage of reusable energies is low and unstable. Such energy must be converted using a first-stage step-up power

converter before it can be used in households. The conversion process is shown in Figure 1. For instance, the input voltage (V_{in}) of photovoltaic ranges between 20 V and 45 V. To effectively feed the photovoltaic energy into the grid, the voltage must be increased to 380 ± 20 V to facilitate the grid connection for the rear inverter [3–5] or charge/discharge battery of an electric vehicle (EV) by a bidirectional DC/DC converter [6–8]. In the front-end structure, a boost converter is employed to generate a step-up ratio of at least 1:8. Thus, many high step-up converter structures have been recently researched and developed.

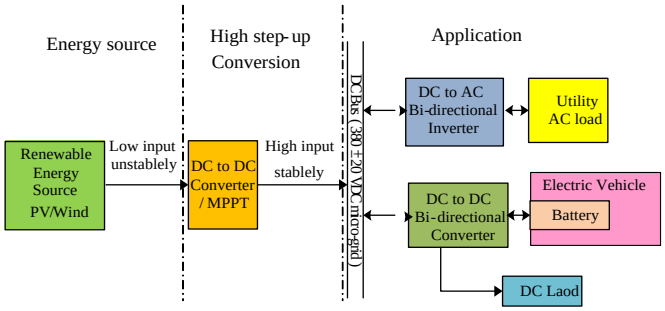

Figure 1. Block diagram of application of vehicular green energy systems. PV: photovoltaics; and MPPT: maximum power point tracking.

After previous studies have claimed that using a conventional, non-isolated boost converter to multiply voltage requires operating the system duty cycle at an extremely high ratio. Constrained by parasitic elements in the circuit, diodes have a reverse recovery time when equivalent series stray inductance and series impedance of the capacitor exist in the circuit or when switched between on and off transients. These factors restrain the step-up ratio and lower the conversion efficiency [9–11]. To achieve a high step-up ratio and conversion efficiency, while maintaining low development cost and compactness of electric power converters, many scholars have developed technical structures to improve boost converter-based step-up ratios. Applying a cascade type [12–14] boost converter can boost the voltage stepwise and raise the step-up ratio. However, in doing so, multistage cascade converters complicate the circuit and transmit energy indirectly through a capacitor [15,16], which causes unnecessary energy consumption. Therefore, scholars have proposed a voltage lift technique [17,18] to insert a voltage multiplier formed by a capacitor and diode in the boost pathway to substantially simplify the circuit compared with that of the cascade type. However, the voltage lift technique increases the size and cost of the circuit design and the voltage stress the switch bears remains overly high during high voltage output, thereby lowering the designers' flexibility in selecting components. Consequently, a concept of integrating coupled inductors [4,19,20] and a coupled inductor cascade [21–23] has been proposed to achieve a design with high step-up ratios. This coupled structure couples inductors with a method similar to how a transformer turns a ratio to form a voltage multiplier; thus, the size and cost of circuit design can be reduced considerably. However, when the switched-off leakage of coupled inductors lacks a pathway to release energy, it resonates with the parasitic capacitor of cascade switches, increases the switching voltage stress, and causes increased switching losses, thereby degrading the overall circuit efficiency [24]. To avoid the conversion efficiency deterioration resulting from leakage, scholars have proposed improved circuit designs [19,23] to fabricate a clamping circuit that combines a capacitor and diode, while compromising slight cost and size increases. The clamping circuit can recover leakage energy or increase the control complexity to add a soft-switching converter with zero-current switching (ZCS) and zero-voltage switching (ZVS), to improve the conversion efficiency [25–27].

In the present study, a high step-up converter structure for green energy systems was developed. By using integrated voltage multipliers of three groups of coupled inductors, the proposed converter structure can boost voltage and combine a capacitor and diode to produce a boost converter.

Additionally, a freewheeling current path is provided to recover leakage energy, reduce the voltage stress on critical components, largely reduce the circuit size, and increase the overall conversion efficiency. The proposed design satisfies the requirements of a high voltage gain ratio, high conversion efficiency, low component voltage stress, and simple control in green energy circuit systems.

2. Operating Principles of the Main Circuit

Figure 2 shows the proposed novel, non-isolated, cascade-type single-switch high step-up DC/DC converter. The main circuit components are composed of a switch (S), the primary magnetizing inductance (L_m), magnetizing leakage inductance (L_{k1}), and coupled inductors (turns ratio N_1:N_2:N_3). A voltage multiplier circuit is composed of diodes D_1 and D_2, capacitors C_1 and C_2, coupled inductor L_2, and coupled leakage inductance L_{k2}. Another circuit cascaded with capacitor C_3 is composed of diodes D_4 and D_5, capacitors C_4 and C_5, coupled inductor L_3, and coupled leakage inductance L_{k3}. A complete cycle of the circuits comprises five operating modes, which are analyzed as follows.

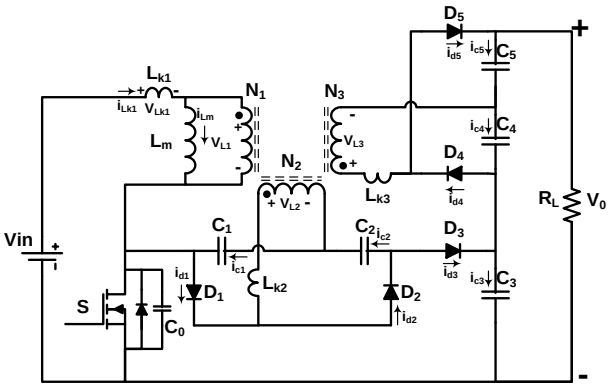

Figure 2. The novel, cascade-type single-switch, high step-up converter with coupled inductors.

To simplify the circuit analysis, the following assumptions were postulated:

(1) The capacitance values of C_1, C_2, C_3, C_4 and C_5 are high enough to be regarded as constant power sources; and

(2) The circuit is operated under the continuous conduction mode (CCM) and the magnetic inductance of each winding is substantially higher than the leakage.

In accordance with these assumptions, the steady-state waveform patterns of the primary operating signals of the converter were operated under the CCM and shown in Figure 3. Figure 4 shows the operating patterns of each mode.

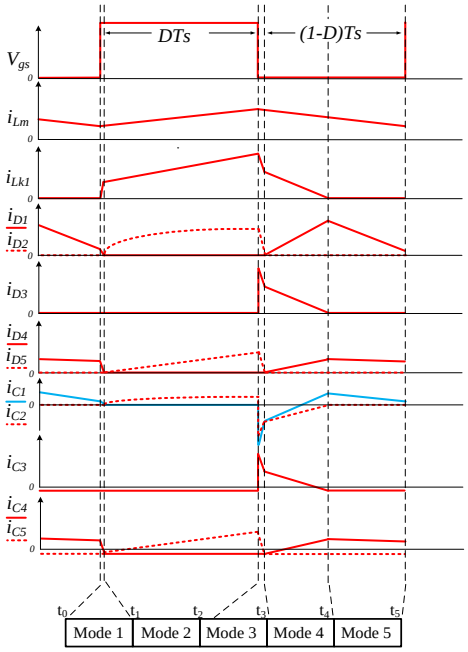

Figure 3. Operating waveform patterns in the continuous conduction mode (CCM).

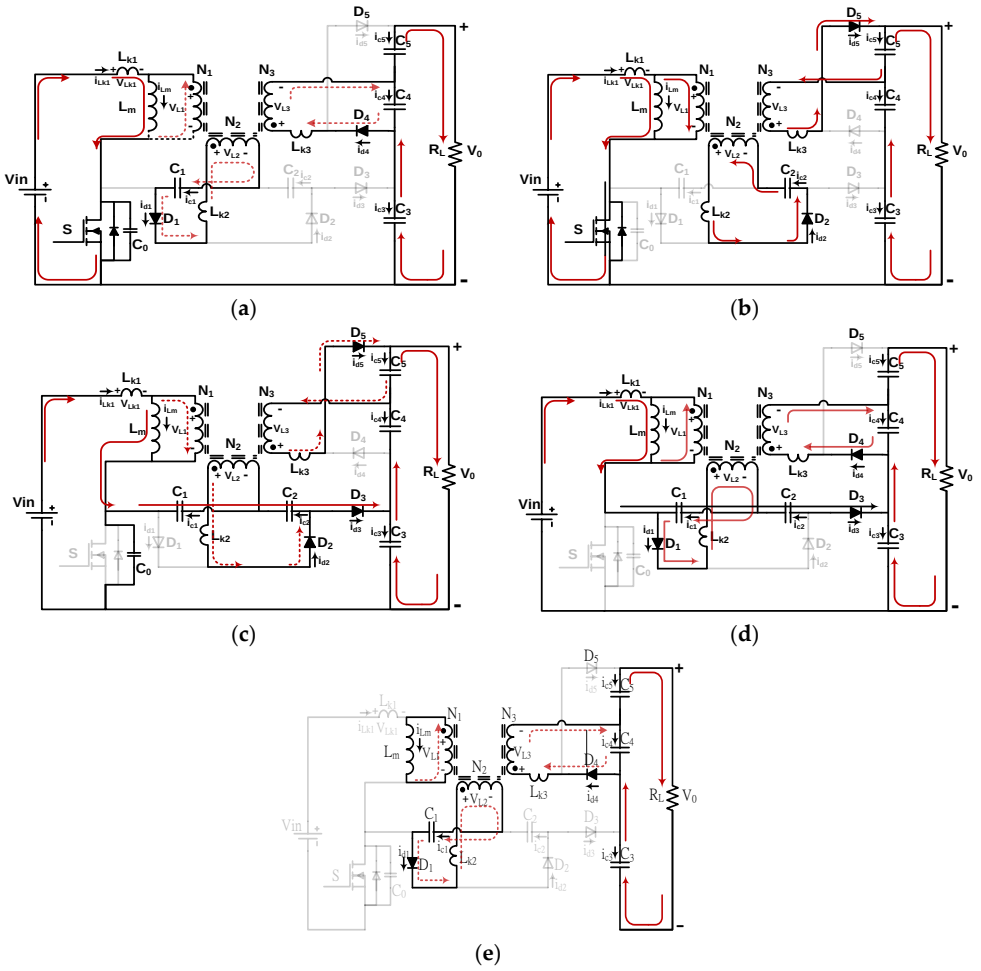

Figure 4. Mode operating under CCM: (**a**) Mode I; (**b**) Mode II; (**c**) Mode III; (**d**) Mode IV; and (**e**) Mode V.

2.1. Mode I ($t_0 \leq t < t_1$)

When $t = t_0$, the S, D_1 and D_4 are turned on, whereas D_2, D_3 and D_5 are turned off. The current pathway is depicted in Figure 4a. In this mode, the V_{in} stores energy through L_m and L_{k1}, yielding a linear rise of the inductive current. At the turn-on transient of S, L_{k2}, and L_{k3} of N_2 and N_3 continuously release energy to C_1 and C_4 through D_1 and D_4, the cascade of C_3, C_4 and C_5 transmits energy to the output load (R_L) until the currents i_{d1} and $i_{d4} = 0$. When $t = t_1$, this operating region ends and progresses into the next mode.

2.2. Mode II ($t_1 \leq t < t_2$)

In this operating region, the S, D_2 and D_5 are turned on continuously, whereas D_1, D_3 and D_4 are turned off. The current pathway is depicted in Figure 4b. In this mode, the V_{in} stores energy through L_m and L_{k1}, yielding a linear rise of the inductive current. Meanwhile, coupled inductors based on turns ratios N_{21} and N_{31} and through D_2 and D_5 release energy to C_2 and C_5 in a forward manner. The cascade of C_3, C_4 and C_5 transmits energy to the R_L. When $t = t_2$, this operating region ends and progresses into the next mode.

2.3. Mode III ($t_2 \leq t < t_3$)

In this operating region, when $t = t_2$, the S is turned off transiently. Since the inductive voltage has a continuous current characteristic and cannot be changed instantaneously, D_2, D_3 and D_5 are turned on, whereas D_1 and D_4 are turned off. The current pathway is depicted in Figure 4c. In this mode, the V_{in} is connected to V_{C1} and V_{C2} in series and transmits energy to C_3 through D_3. As D_2 and D_5 are switched on, the coupled inductors maintain leakage currents i_{Lk2}, i_{Lk3}, from which energy is continuously released to C_2 and C_5 as the means to recover leakage. The cascade of C_3, C_4 and C_5 transmits energy to the R_L. When the $t = t_3$, this operating region ends and enters the next mode.

2.4. Mode IV ($t_3 \leq t < t_4$)

When $t = t_3$, S is permanently turned off and D_1, D_3 and D_4 are turned on, whereas D_5 is turned off. The current pathway is depicted in Figure 4d. In this mode, because the preceding mode releases energy continuously until currents i_{Lk2} and i_{Lk3} reach zero, the polarity of the coupled inductors is reversed. The energy at N_1 is transmitted through a flyback method and switched on through D_1 and D_4 to C_1 and C_4, thereby increasing i_{d1} and i_{d4}. The V_{in} is continuously connected to V_{C1} and V_{C2} in series to transmit energy to C_3 through D_3. At the output end, similarly, the cascade of C_3, C_4 and C_5 transmits energy to the R_L until the i_{Lk1} current reaches zero. When $t = t_4$, this operating region ends and progresses into the next mode.

2.5. Mode V ($t_4 \leq t < t_5$)

In this operating region, the S is turned off permanently. The V_{in} becomes an open circuit because of the zero i_{Lk1} current. D_1 and D_4 are on, whereas D_2, D_3 and D_5 are off. The current pathway is depicted in Figure 4e. In this mode, the L_m couples energy into C_1 and C_4 through the coupled inductors. Since the magnetizing inductance is the only source that supplies the required energy, the magnetizing inductance current i_{Lm} and i_{d1} and i_{d2} continue to drop until $t = t_5$. Upon the conclusion of this operating region, a complete switching cycle T_S is achieved.

3. Steady-State Analysis

In this section, discussion and analysis of the voltage gain ratio and switching stress of components are provided. The results are then compared with those of previous studies. To simplify the circuit analysis, the following assumptions were postulated:

(1) The capacitance values of C_1, C_2, C_3, C_4 and C_5 are high enough to be regarded as constant power sources;

(2) The S, D_1, D_2, D_3, D_4 and D_5 are ideal circuit elements;
(3) The magnetizing inductance of each winding is substantially higher than the leakage, which can, thus, be ignored; and
(4) The converter is operated under the CCM.

3.1. Step-Up Conversion Ratio

With the S turned on, the node voltage analysis based on Kirchhoff's voltage law (KVL) applied to Mode II, shown in Figure 4b, yields the following equations of voltage stress of the inductance and capacitors:

$$V_{in} - V_{L1} = 0 \tag{1}$$

$$V_{C2} = N_{21} \times V_{L1} \tag{2}$$

$$V_{C5} = N_{31} \times V_{L1} \tag{3}$$

where $N_{21} = N_2{:}N_1$ and $N_{31} = N_3{:}N_1$.

When the S is off, KVL applied to Mode VI, shown in Figure 4e, can be used to determine the voltage stress of the inductance and capacitors as expressed in the following equations:

$$V_{C3} = V_{in} + V_{C1} + V_{C2} - V_{L1} \tag{4}$$

$$V_{C1} = N_2 \times V_{L1} \tag{5}$$

$$V_{C4} = N_{31} \times V_{L1} \tag{6}$$

In accordance with a voltage-second balance principle between the on-off transients of each inductance, the following equations were derived:

$$\int_0^{DTs} V_{L1}dt + \int_{DTs}^{Ts} V_{L1}dt = 0 \tag{7}$$

$$V_{c1} = \frac{N_{21} \times DV_{in}}{1-D} \tag{8}$$

$$V_{c2} = N_{21} \times V_{in} \tag{9}$$

$$V_{c3} = \frac{(1+D+N_{21}) \times V_{in}}{1-D} \tag{10}$$

$$V_{c4} = \frac{N_{31} \times DV_{in}}{1-D} \tag{11}$$

$$V_{c5} = N_{31} \times V_{in} \tag{12}$$

Since $V_O = V_{C3} + V_{C4} + V_{C5}$, substituting Equations (10)–(12) into the equation can render a voltage gain ratio of converters, as expressed in Equation (13):

$$\frac{V_O}{V_{in}} = \frac{1+D+(N_3/N_1)+(N_2/N_1)}{1-D} \tag{13}$$

The voltage gain ratio curve obtained from Equation (13) is shown in Figure 5. Under identical duty cycles, the proposed converter provided a higher step-up ratio than did conventional step-up converters at a turns ratio of $n = 1$.

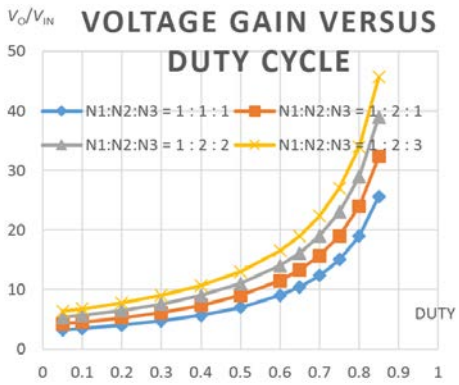

Figure 5. Converter voltage gain ratio curves with different turns ratios.

3.2. Component Voltage Stress

By using the on-off transients, the voltage stress on circuit elements can be calculated. The switch on-off state of Mode II in Figure 4b can be applied to calculate the voltage stress on the S and D_1, D_3, and D_4. The corresponding equations are expressed as follows:

$$V_{switch} = \frac{1}{1-D} V_{in} \tag{14}$$

$$V_{D1} = V_{C1} + V_{L2} = \frac{N_2}{1-D} \times V_{in} \tag{15}$$

$$V_{D3} = V_{C3} - V_{C2} - V_{C1} = \frac{1+D}{1-D} \times V_{in} \tag{16}$$

$$V_{D4} = V_{C4} + V_{L3} = \frac{N_3}{1-D} \times V_{in} \tag{17}$$

When the S of Mode VI in Figure 4d is off, the voltage stress on D_2 and D_5 are calculated using Equations (18) and (19), as follows:

$$V_{D5} = V_{C4} + V_{C5} = \frac{N_3}{1-D} \times V_{in} \tag{18}$$

$$V_{D2} = V_{C1} + V_{C2} = \frac{N_2}{1-D} \times V_{in} \tag{19}$$

3.3. Loss Analysis

Performing a loss analysis is a critical step in circuit design. By performing reasonable calculations and evaluations of the power loss characteristics of circuit elements, designers can efficiently design circuits without wasting time on wrong design directions. Loss analysis is discussed in two sections of this paper, separated into loss analysis of individual elements during operation and the estimated conversion efficiency of the entire system.

3.3.1. Switch Element (S)

The loss of the S primarily depends on conduction loss and switching loss, which involves driver loss, turn-on, and turn-off transient loss. The loss value is determined by summing Equations (20)–(23), where T_r represents the rise time of the switch and T_f represents the fall time of the switch.

$$P_{conduction\text{-}loss} = {I_{load}}^2 \times R_{DS}(on) \tag{20}$$

$$P_{driver\text{-}loss} = 16/3 \times C_{gs} \times V_{in} \times f_{sw} \tag{21}$$

$$P_{turn\_on\text{-}loss} = 1/2 \times T_r \times I_{load} \times V_{in} \times f_{sw} \quad (22)$$

$$P_{turn\_off\text{-}loss} = 1/2 \times T_f \times I_{load} \times V_{in} \times f_{sw} \quad (23)$$

3.3.2. Magnetic Energy Storage Element (*L*)

This element comprises copper and core losses. The copper losses refer to losses caused by current I flowing through wire equivalent impedance *R* on a transformer or inductor winding, as expressed in Equation (24). The core losses, or iron losses, can be categorized into hysteresis losses and eddy-current losses. Affected by varying magnetic fields, hysteresis losses cause partial energy losses inside the iron core through thermal dissipation. Eddy-current losses involve the cyclic current (i.e., eddy current) generated within a conductor caused by varying induction of the magnetic field. The energy of eddy currents dissipates through heat transference when passing through the resistance of iron core materials. The eddy-current loss and area of current cycle are positively correlated.

$$P_{copper\text{-}loss} = {I_{load}}^2 \times R \quad (24)$$

3.3.3. Capacitor (*C*)

The capacitor presents two major loss factors, namely, equivalent series resistance (ESR) and leakage current. When aluminum electrolytic capacitors are operated, leakage current definitely occurs. When the leakage current flows through the internal resistance *Rc* in the capacitor, losses are generated. The leakage current should be minimized. The equation to calculate leakage currents is expressed in Equation (25):

$$I_{leakage} = K \times C \times V \quad (25)$$

where *I* is the leakage current (μA) and *K* is the constant set for production.

3.3.4. Diode (*D*)

Although diodes are unidirectional conducted elements, power losses occur in forward conduction and reverse-bias blocking. In forward conduction, a junction potential barrier V_f occurs to lower the voltage; when current I_{load} flows through the potential barrier, power losses occur, as expressed in Equation (26):

$$P_{forward\text{-}loss} = V_f \times I_{load} \times D \quad (26)$$

where *D* represents a duty cycle. In addition, parasitic series resistance (R_d) exists in the diodes and can cause power losses when the I_{load} flows through it. The equation is expressed in Equation (27):

$$P_{Rd\text{-}loss} = {I_{load}}^2 \times R_d \times D \quad (27)$$

When the diodes are in the reverse-bias blocking state, they may have a reverse recovery that prevents the currents from returning to zero transiently during cut off; instead, the current maintains a reverse flow for a certain period before returning to zero. Such current is called reverse recover current (I_{rm}) and the period during which it occurs is called the reverse recovery time (T_{rr}). The area resembling an inverse triangle formed by I_{rm} and the T_{rr} is called the reverse storage charge (Q_{rr}). Without appropriate recycling mechanisms, the energy accumulates and cause losses, as expressed in Equation (28):

$$P_{drr-loss} = \frac{1}{2} T_{rr} \times I_{nn} \times V_R \times f_{sw} \quad (28)$$

where f_{sw} is the switching frequency and V_R is the reverse-bias voltage of the diode.

In the proposed structure, reverse recovery losses are absent because the capacitors in the circuit recycle and store the energy. Table 1 lists the expected loss assessment of components under a power loading of 450 W. The values were calculated without considering eddy-current losses, R_d, and capacitor losses. The total impedance of the winding was set to 60 mΩ, resistance of switching

conduction $R_{DS}(on)$ as 10 mΩ, diode V_f as 0.55 V, and f_s as 50 kHz for calculation. In this paper, the measurement device was limited, so component power losses were roughly estimated. We neglected some difficult evaluation parameters (for example. eddy-current, capacitance ESR, print circuit board (PCB) (parasitic impedance losses, and capacitance impedance losses, etc.), and the full load efficiency estimation compared with measurement can meet within ±1%. The total component power losses of the system were much smaller than the system power.

Table 1. Assessment of component power losses under 450 W power loading.

Component	Loss Calculation	Unit
Switch Conduction Loss	2.166	W
Switch Switching Loss	1.726	W
Inductor Copper Loss	12.612	W
Inductor Iron Loss	0.28	W
Total Diode Loss	7.324	W
Total	24.108	W
Calculated Efficiency	94.642%	-
Measured Efficiency	93.159%	-

3.3.5. Estimated Conversion Efficiency Analysis

In the analysis presented in this subsection, diode T_{rr}, coupled coefficient losses and leakage of coupled inductance, and equivalent series inductance of electrolytic capacitors were ignored. The parasitic effects of elements that were considered were the parasitic internal resistance of coupled inductance (r_{L1}, r_{L2} and r_{L3}), the forward conduction voltage drop of diodes (V_{D1}, V_{D2}, V_{D3}, V_{D4} and V_{D5}), the series internal resistance of diodes (r_{D1}, r_{D2}, r_{D3}, r_{D4} and r_{D5}), the ESR of capacitors (r_{C1}, r_{C2}, r_{C3}, r_{C4} and r_{C5}), and the internal R_{DS}, as depicted in Figure 6.

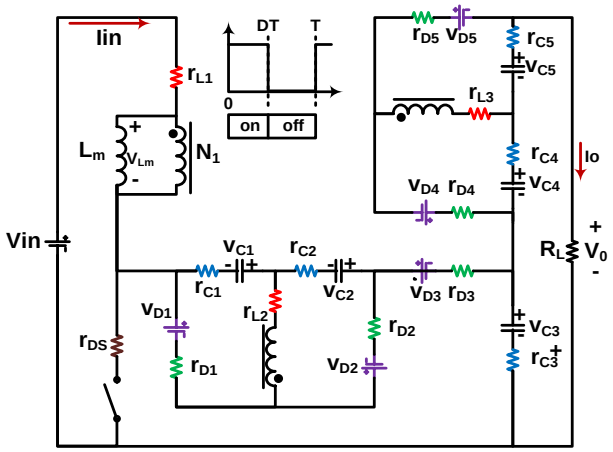

Figure 6. Equivalent model circuit of efficiency analysis.

To simplify the analysis, temporary recycle pathways caused by leakage and equivalent resistance of capacitors were ignored. Only the on and off states of the switch were considered. Subsequently, the voltage-second balance, small-ripple approximation, and capacitor-charge balance principles were applied to calculate the circuit conversion efficiency, as expressed in Equation (29). The efficiency was the ratio of the output power (P_o) to the input power, as expressed in Equation (30):

$$\frac{Vo}{V_{in}} = \frac{\left(n_2 D + \frac{2-n_3 D+D}{1-D}\right) - \frac{(V_{D1}+V_{D2}+V_{D3}+V_{D4}+V_{D5})}{V_{in}}}{1+\left(\frac{A}{R_L\times(1-D)^2}\right)+\left(\frac{B}{R_L\times(1-D)}\right)+\left(\frac{C}{R_L\times(1-D)}\right)+\left(\frac{D}{R_L}\right)} \quad (29)$$

$$\begin{gathered} A = (1 + n_2 D)\, r_{D3} + r_{C3}\,(1 + D) + (r_{C1} + r_{C5})\, D + (1 - D)\,(r_{C2} + r_{C4}) \\ B = n_3\,(1 - D)\, r_{L3} + (r_{D1+} r_{D5}) D + (1 - D) \\ C = (1 + n_2)\, D \times r_{L2} + (r_{D2+} r_{D4})\,(1 - D) \\ D = (1 + n_2 + n_3) \times (r_{ds} + r_{L1}) \\ \eta = \frac{(1-D)\left(n_2 + \frac{2 - n_3 D + D}{1-D}\right) - \frac{(V_{D1} + V_{D2} + V_{D3} + V_{D4} + V_{D5})}{V_{in}}}{(2 - n_3 D + D)[1 + \left(\frac{A}{R_L \times (1-D)^2}\right) + \left(\frac{B}{R_L \times (1-D)}\right) + \left(\frac{C}{R_L \times (1-D)}\right) + \left(\frac{D}{R_L}\right)]} \end{gathered} \tag{30}$$

where the values of r_{L1}–r_{L3} are assumed to be 50 mΩ, r_{D1}–r_{D5} as 20 mΩ, R_{DS} as 10 mΩ, r_{C1}–r_{C5} as 20 mΩ, diode conduction voltage drop as 0.55 V, V_{in} as 40 V, output voltage as 400 V, and R_L as 355.56 Ω. The relationship among efficiency, gain ratio, and duty cycle is shown in Figure 7.

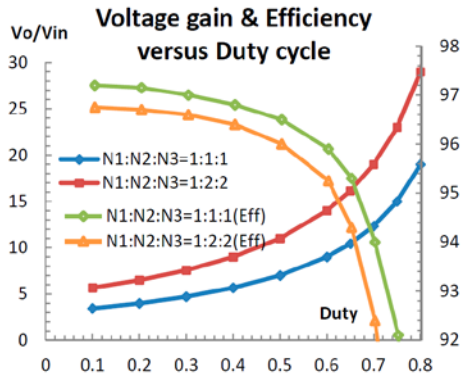

Figure 7. Relationship between efficiency and voltage gain vs. duty cycle.

A desirable step-up ratio was approximately 1:10. The curves in Figure 7 reveal that the turns ratio of n = 1:2:2 should be applied in consideration of optimal circuit design points. At this ratio, the duty cycle of the S is approximately 0.5, rendering an efficiency of 95% or higher.

3.4. Comparison of the Proposed Structure with Extant Structures

The aforementioned characteristics of the single-switch high step-up converter of the proposed structure were compared with those in [9,16,21], as tabulated in Table 2. In Table 2, n_2 represents the ratio of coils N_2 to N_1; n_3 represents the ratio of N_3 to N_1; and D represents the operating duty cycle ratio. The voltage gain comparison in Table 2 is depicted in Figure 5, where the turns ratio is N_1:N_2:N_3 = 1:2:2.

Table 2. Comparison of studies regarding the single-switch high step-up converters.

Comparison of Studies	Voltage Gain Ratio	Switch Voltage Stress	Diode Voltage Stress	Number of Capacitors	Number of Inductors	Number of Diodes
Proposed structure	$\frac{1+D+n_2+n_3}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{n_2 \times V_{in}}{1-D}$	5	3	5
Reference [9]	$\frac{2+n+nD}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{(1+n)V_{in}}{1-D}$	4	2	4
Reference [16]	$\frac{1+n_2 \times D}{(1-D)^2}$	$\frac{(1+n_2)V_{in}}{1-D}$	$Vo + n_3 V_{in}$	3	3	4
Reference [21]	$\frac{1+nD}{(1-D)^2}$	$\frac{Vo}{1+nD}$	$\frac{nVo}{1+nD}$	3	2	4

Figure 8 reveals that the systems of [9,16,21], and the proposed structure renders more than a 10-fold increase of voltage at D = 0.5–0.6. Although the step-up ratio of [9] exhibited an exponential increase with the increase in the control cycle, the cascade structure was unsuitable for overly high duty cycle ratios because of efficiency problems.

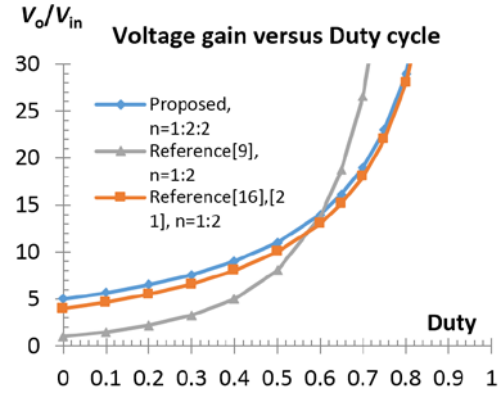

Figure 8. Comparison of voltage gains under identical turns ratios.

Figure 9 shows the comparison of switch voltage stresses of structures listed in Table 2. At D = 0.75 or lower, the proposed structure has lower switch voltage stresses compared with the other three structures.

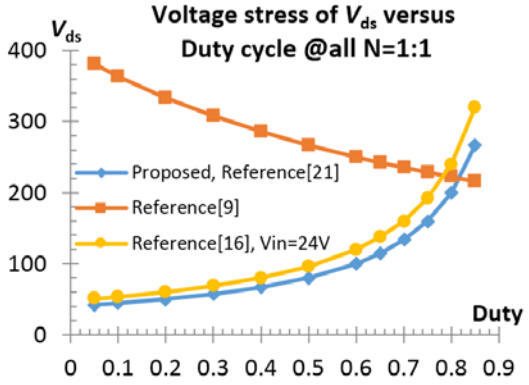

Figure 9. Comparison of switch voltage stresses (N_1:N_2:N_3 = 1:1:1).

Figure 10 depicts the comparison of diode voltage stresses. At D = 0.8 or lower, the proposed structure has lower voltage stress than do the other three structures.

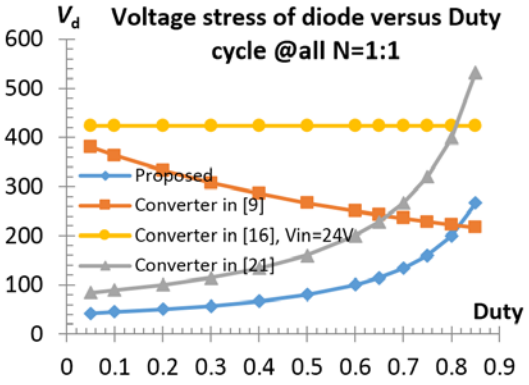

Figure 10. Comparison of diode voltage stresses (N_1:N_2:N_3 = 1:1:1).

4. Experiment Results

Figure 11 reveals a block diagram of system hardware and software planning. A microcontroller RX62T (Renesas, Santa Clara, CA, USA) was employed as the basis of system control. Through

digitized control, the problems of an overly complex hardware circuit and difficulty in designing the control circuit caused by the massive use of analog circuits can be avoided.

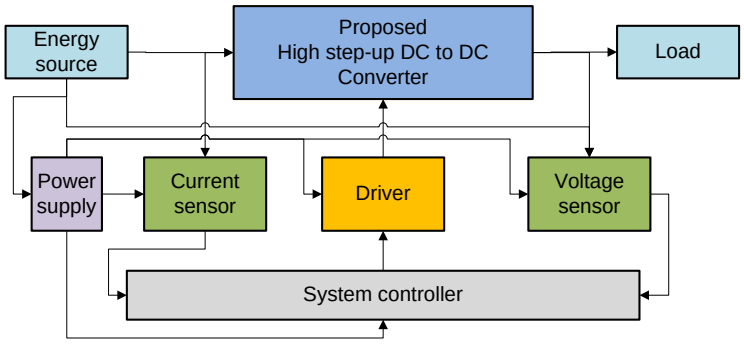

Figure 11. Block diagram of system hardware and software planning.

Figure 12 shows the picture of the experimental prototype circuit.

Figure 12. Picture of the experimental prototype circuit.

The electrical specification and element parameters of the circuit are tabulated in Table 3.

Table 3. Electrical specification and components of the experimental circuit.

Parameter		Specification
Input DC Voltage V_{in}		36–48 V
Output DC Voltage V_O		400 V
Max output power P_o		450 W
Switching frequency f_s		50 kHz
Coupled inductors turns ratio		N_1:N_2:N_3 = 1:2:2
Component	Model	Specification
S_1	IRFP4110	100 V, 120 A
D_1, D_2, D_4, D_5	MBR20200	200 V/20 A
D_3	NF020	200 V/40 A
L	MPPRing core	125 μH
C_1, C_2	MPP Film Capacitor	10 μF/100 V
C_3	Electrolytic Capacitor	300 μF/400 V
C_4, C_5	MPP Film Capacitor	22 μF/100 V

Figure 13 reveals the operating waveforms of each element measured under the power loading of 450 W: (a) S waveform and inductive current waveform; (b) D_1–D_3 voltage waveform; (c) D_4 and D_5 voltage waveform; (d) D_1–D_3 current waveform; (e) D_4 and D_5 current waveform; and (f) voltage waveform of C_1, C_3, C_4, and output. From the experimental waveforms of Figure 13 compared with the steady-state analysis before, the proposed converter had been proved that the component voltage stress of the active switch and diodes are less than 100 V, and was consistent with the results of steady-state analysis.

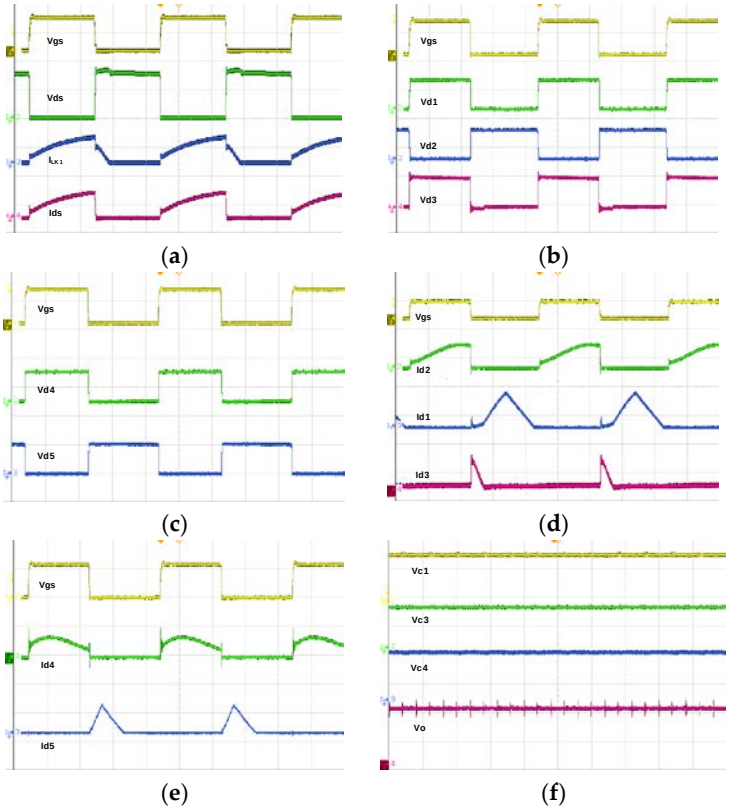

Figure 13. The operating waveforms of each element measured under the power loading of 450 W, (**a**) V_{gs}: 10 V/div, V_{ds}: 50 V/div, I_{LK1}: 25 A/div, I_{ds}: 25 A/div, time: 5 μs/div; (**b**) V_{gs}: 10 V/div, V_{D1}: 100 V/div, V_{D2}: 100 V/div, V_{D3}: 50 V/div, time: 5 μs/div; (**c**) V_{gs}: 10 V/div, V_{D4}: 100 V/div, V_{D5}: 100 V/div, time: 5 μs/div; (**d**) V_{gs}: 20 V/div, I_{D1}: 5 A/div, I_{D2}: 5 A/div, I_{D3}: 25 A/div, time: 5 μs/div; (**e**) V_{gs}: 20 V/div, I_{D4}: 5 A/div, I_{D5}: 5 A/div, time: 5 μs/div; and (**f**) V_{C1}: 50 V/div, V_{C3}: 250 V/div, V_{C4}: 50 V/div, V_O: 200 V/div, time: 25 μs/div.

Figure 14 shows the comparison of efficiency curves of the proposed converter and those presented in previous studies. The V_{in}, output voltage, and output power for the proposed converter were 40 V, 400 V and 450 W, respectively. The output power of [9,16,21] were only 200, 400 and 300 W, respectively. These curves were measured under a distinct P_o. Under a light-load P_o of 50 W, the proposed structure yielded a 94.511% efficiency. Under a full-load P_o of 450 W, the efficiency became 93.2%. The optimal efficiency (95.346%) was reached under a P_o of 250 W. The efficiency under all power conditions was higher than 93%.

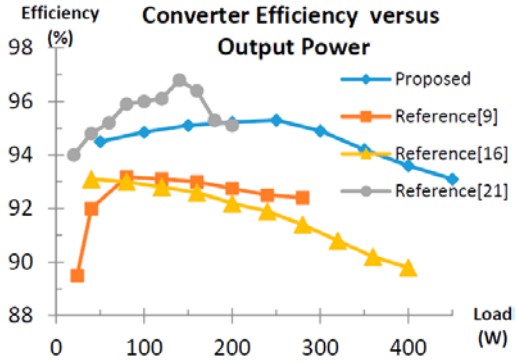

Figure 14. Comparison of converter efficiency curves.

Table 4 shows the weight efficiency of the proposed converter based on California Energy Commission (CEC) standard [28], the results show the converter reached 94.6% weight efficiency at the nominal input voltage.

Table 4. The weight efficiency of proposed converter.

V_{in}	Load						Weight Efficiency
	10%	20%	30%	50%	75%	100%	
36 V	94.018	94.287	94.441	94.608	93.983	92.648	94.119
40 V	94.447	94.768	95.086	95.268	94.375	93.159	94.610
48 V	94.836	95.322	95.482	95.712	94.898	93.541	95.090
-	4%	5%	12%	21%	53%	5%	-

5. Conclusions

In the present study, a high step-up DC/DC converter with coupled inductance and voltage multipliers was developed. Through operating principles, steady-state analysis, and final test results, the effectiveness and feasibility of the proposed converter were validated. Applying the design of a single switch and coupled inductance with an integrated common core can substantially simplify the control circuit and reduce costs, while maintaining the effect of high step-up ratios. In addition, the proposed converter can recycle leakage, thereby minimizing the reverse voltage stress of the switch and diodes. Consequently, the switching losses can be reduced. Meanwhile, low-conduction loss elements can be flexibly selected to lower the conduction losses and improve the converter efficiency. In accordance with the experiment results, the converter efficiency reached 93.16% and 95.35% under the output power conditions of 450 W and 250 W, respectively. Obviously the proposed converter is advantageous for integrating high efficiency, simple structure, and high voltage gain ratios.

Acknowledgments: The authors would like to thank their student, Kuo-Chan Huang, for his suggestions for this research.

Author Contributions: These authors contributed equally to this work.

Conflicts of Interest: The authors declare no conflict of interest.

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