

Article

Design and Optimization of an Efficient (96.1%) and Compact (2 kW/dm³) Bidirectional Isolated Single-Phase Dual Active Bridge AC-DC Converter

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Academic Editor: Ali M. Bazzi

Received: 14 August 2016; Accepted: 26 September 2016; Published: 3 October 2016

Abstract: The growing attention on plug-in electric vehicles, and the associated high-performance demands, have initiated a development trend towards highly efficient and compact on-board battery chargers. These isolated ac-dc converters are most commonly realized using two conversion stages, combining a non-isolated power factor correction (PFC) rectifier with an isolated dc-dc converter. This, however, involves two loss stages and a relatively high component count, limiting the achievable efficiency and power density and resulting in high costs. In this paper, a single-stage converter approach is analyzed to realize a single-phase ac-dc converter, combining all functionalities into one conversion stage and thus enabling a cost-effective efficiency and power density increase. The converter topology consists of a quasi-lossless synchronous rectifier followed by an isolated dual active bridge (DAB) dc-dc converter, putting a small filter capacitor in between. To show the performance potential of this bidirectional, isolated ac-dc converter, a comprehensive design procedure and multi-objective optimization with respect to efficiency and power density is presented, using detailed loss and volume models. The models and procedures are verified by a 3.7 kW hardware demonstrator, interfacing a 400 V dc-bus with the single-phase 230 V, 50 Hz utility grid. Measurement results indicate a state-of-the-art efficiency of 96.1% and power density of 2 kW/dm³, confirming the competitiveness of the investigated single-stage DAB ac-dc converter.

Keywords: ac-dc power converters; battery chargers; dual active bridge; DAB; optimal design; power metal oxide semiconductor field effect transistors (MOSFETs); single-stage

1. Introduction

1.1. Overview and Objectives

Single-phase utility-interfaced ac-dc converters with power factor correction (PFC) and galvanic isolation cover a wide range of applications such as chargers for plug-in hybrid electrical vehicles (PHEVs) and battery electric vehicles (BEVs) [1,2], interfaces for residential dc distribution systems and energy storage systems [3,4], and inverters for photovoltaic modules. Bidirectional power flow is increasingly required since the traditional electricity grid is evolving towards a smart interactive service network (customers/operators) in which energy systems play an active role in providing different types of support to the grid [5], e.g., vehicle-to-grid (V2G) concepts [6].

The above mentioned isolated ac-dc converters are most commonly realized using a dual-stage (2-S) approach, involving a non-isolated power factor correction (PFC) rectifier, followed by a dc-link to which a high-frequency (HF) isolated dc-dc converter is connected. An extensive review of uni- and bidirectional single-phase PFC rectifier topologies with improved power quality is presented in [7], including some variants with galvanic isolation. Examples of soft-switched, single-phase,

non-isolated, bidirectional PFC rectifiers are the boost-type PFC with passive snubber cell presented in [8] and the multi-cell totem-pole PFC described in [9,10], which employs a triangular current mode (TCM) modulation scheme. Extensive overviews, topology surveys, analyses, and comparative evaluations of common topologies used for the isolated dc-dc converter stage are presented in [11–18], inter alia including numerous (soft-switching) dual active bridge (DAB) topologies and resonant topologies, whether or not combined with active auxiliary snubber circuits and/or a second, typically hard-switched and non-isolated, dc-dc conversion stage.

Besides the 2-S approach, several single-stage (1-S), single-phase, isolated ac-dc PFC converter topologies have been proposed in literature, which combine all functionalities into one conversion stage and thus (potentially) enable a cost-effective efficiency and power density increase through the omission of a complete loss stage and through reduction of the component count. Moreover, due to the absence of an intermediate dc-link there is no need anymore for bulky, failure-prone electrolytic capacitors. This, however, is at the expense of an increased filtering effort at the dc output side due to the double line-frequency (i.e., 100 Hz) power pulsation that is seen by the output, where large low-frequency (LF) filter capacitors are required in case a low output voltage ripple is desired. An example of a 1-S, single-phase, bidirectional, isolated ac-dc converter is presented in [19,20], using a cyclo-converter at the primary side and a voltage source converter at the secondary side of a medium frequency transformer. Another well known example is the 1-S DAB ac-dc converter topology analyzed in [21–27], which is able to effectively obtain PFC while producing high-quality waveforms and complying to regulations on low- and high-frequency distortions of the mains ac power lines. The topology is shown in Figure 1 and is the subject of this paper. It consists of a quasi-lossless synchronous rectifier (SR) and an isolated full-bridge full-bridge DAB dc-dc converter, putting a small HF filter capacitor in between. Moreover, using advanced modulation schemes such as the one recently presented in [25], the DAB can be operated with minimum HF circulating currents and under full-operating-range zero voltage switching (ZVS) conditions, quasi completely eliminating the losses associated with the switching of the, in the case of this paper, MOSFET-type power switches.

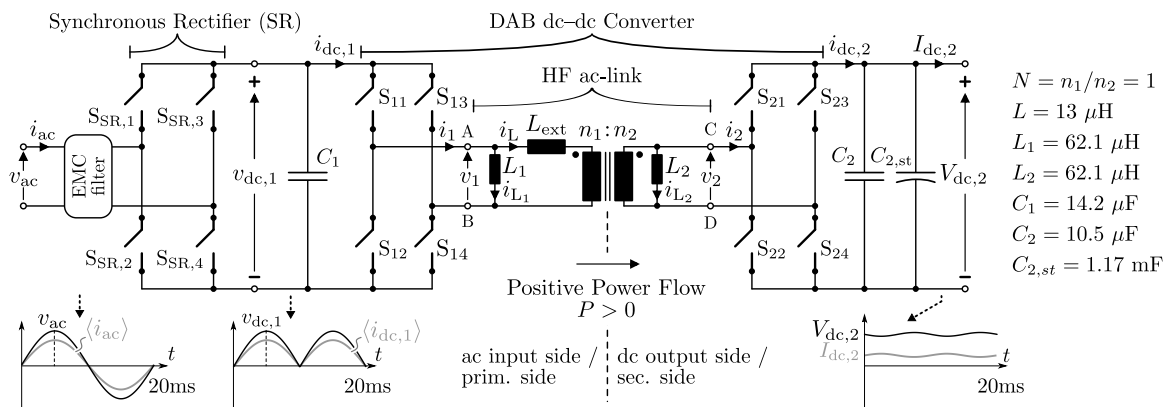


Figure 1. Schematic of the single-stage (1-S), single-phase, bidirectional, isolated dual active bridge (DAB) ac-dc converter topology. The nominal ac input voltage, input current, and power are respectively 230 V_{rms}, 16 A_{rms}, and 3.7 kW, while the specified output voltage range is $V_{dc,2} = 370\text{--}470 \text{ V}$, with $V_{dc,2,nom} = 400 \text{ V}$.

Whether or not used in a 1-S ac-dc converter, previous research on DAB converters has mainly been focused on the improvement of modulation schemes in order to facilitate increased converter efficiency and/or power density, e.g., as in [25,28]. This paper, on the other hand, presents a comprehensive design procedure and multi-objective optimization with respect to efficiency and power density, in particular for the 1-S, single-phase DAB ac-dc converter topology shown in Figure 1. Thereby it aims to show and prove the performance potential of this promising 1-S architecture, and the competitiveness with 2-S topologies [29], and therefore complements previous publications on DAB

converters. The operating conditions and converter specifications for the investigated ac-dc converter are summarized in Table 1 and are based on the requirements for future on-board electric vehicle battery chargers, interfacing the high-voltage battery (400 V) of the vehicle with the single-phase utility grid (230 V_{rms}, 50 Hz). The nominal ac input current of the converter is 16 A_{rms}, allowing domestic charging/discharging at a nominal power of 3.7 kW. Bidirectional power flow enables V2G functionality, while galvanic isolation ensures safety. The converter needs to have a very high conversion efficiency and power density, high power factor (PF), and low total harmonic distortion (THD) of the ac input current while complying to the CISPR 22 Class B standard for electromagnetic compatibility (EMC).

Table 1. Operating conditions and converter specifications.

Property		Value
ac-side	V_{ac} (V _{rms})	230 (nominal) $207 \leq V_{ac} \leq 253$
	$I_{ac,nom}$ (A _{rms})	16 (nominal)
	f_L (Hz)	50
dc-side	$V_{dc,2}$ (V)	$370 \leq V_{dc,2} \leq 470$
EMC compliance		CISPR 22 Class B
PF		> 0.9 (at $I_{ac} \geq 0.1 \times I_{ac,nom}$)
THD		IEC 61000-3-2 standard [30], and $THD \leq 5\%$ (at $I_{ac} \geq 0.3 \times I_{ac,nom}$)

Additional Requirements	
<ul style="list-style-type: none"> Galvanic isolation Bidirectional power flow capability High conversion efficiency ($\eta > 94\%$ within reasonable power range) High power density ($\rho \geq 2$ kW/L) Autonomous air cooling MOSFET-type power switches 	

1.2. Outline

At first, in Section 2 the general operating principle of the 1-S DAB ac-dc converter and the operating conditions of the DAB dc-dc converter, as core building block, are presented. Next, in Section 3 the operating principle, available modulation parameters, and relevant switching modes of the DAB are detailed and the method used for calculating an efficient full-operating-range ZVS modulation scheme is summarized. The selection of the high-level circuit variables such as the switching frequency, the inductance values, and the transformer's turns ratio is outlined as well. Based on the available degrees of freedom in the design of the 1-S DAB ac-dc converter, in Section 4 the modeling of the losses and volumes of the employed components is discussed and the corresponding optimization results are presented. Subsequently, in Section 5 the designed hardware demonstrator is shown and its performance, i.e., in terms of losses (and efficiency) and volume (and power density), is calculated. In order to verify the optimization results, different measurement results are presented in Section 6. Finally, conclusions are drawn in Section 7.

2. General Operating Principle of the 1-S Dual Active Bridge (DAB) AC-DC Converter

The investigated single-stage (1-S), single-phase ac-dc converter topology shown in Figure 1 consists of a synchronous rectifier (SR) and isolated full-bridge dual active bridge (DAB) dc-dc converter as the core building block, putting a small high-frequency (HF) filter capacitor C_1 in between. Also shown in Figure 1 are the principle current and voltage waveforms at the different converter ports. The SR switches at each zero-crossing of the ac line voltage v_{ac} , folding it into a dc voltage $v_{dc,1}$ that varies according to the absolute value of v_{ac} , i.e., at twice the 50 Hz line frequency ($2 \cdot f_L$), and that is directly fed to the input of the DAB dc-dc converter:

$$v_{dc,1} = |v_{ac}| = |\hat{V}_{ac} \sin(\omega_L t)|, \quad (1)$$

where \hat{V}_{ac} is the amplitude of v_{ac} and $\omega_L = 2\pi f_L$. The DAB performs the PFC by actively shaping the switching-cycle averaged value $\langle i_{dc,1} \rangle$ of its input current $i_{dc,1}$ in phase with $v_{dc,1}$:

$$\langle i_{dc,1} \rangle = dir \cdot |\hat{I}_{ac}^* \times \sin(\omega_L t)|, \quad (2)$$

where $\hat{I}_{ac}^* (= \sqrt{2} I_{ac}^*)$ is the amplitude set-point of ac input current i_{ac} and dir the power flow direction in accordance with Figure 1:

$$dir = \begin{cases} 1 & \text{if } P > 0: \text{prim. side} \rightarrow \text{sec. side}, \\ -1 & \text{if } P < 0: \text{sec. side} \rightarrow \text{prim. side}. \end{cases} \quad (3)$$

Since the differential mode (DM) EMC input filter capacitance C_{DM} (see Section 4.4.1), which includes capacitor C_1 , draws a small reactive current from the grid, this current should be compensated in order to achieve unity power factor. This is done by controlling $\langle i_{dc,1} \rangle$ slightly lagging on $v_{dc,1}$, as can be seen in Figure 2 which depicts $v_{dc,1}$, i_{ac} , and $\langle i_{dc,1} \rangle$ within a 10 ms half period of the grid voltage v_{ac} for ac line current values of $I_{ac}^* = I_{ac,nom} = 16 \text{ A}_{rms}$ and $I_{ac}^* = 0.2 \cdot I_{ac,nom} = 3.2 \text{ A}_{rms}$ (Note that around the zero crossing ($-30 \text{ V} \leq v_{ac} \leq 30 \text{ V}$) the bridges of the DAB are inactive ('dead zone') as zero voltage switching (ZVS) power conversion is quasi impossible when the input voltage of the DAB is close to zero [25]). These currents respectively correspond to 100% and 20% of the nominal ac input power of 3.7 kW. The exact control equation for $\langle i_{dc,1} \rangle$, which compensates for C_{DM} , is given by Equation (2) of [25] and is not shown here for brevity of this paper. For the same reason, in the following only positive power flow operation ($P > 0$) is discussed as, due to symmetry, the analysis and results for negative power flow are identical. It should be noted that the double line frequency (i.e., at $2 \times f_L$) component of the converter's ac input power is directly transferred to the dc output side, which is due to the absence of a large intermediate dc-link energy storage element within this single-stage converter architecture. As discussed in Section 4.3.1, an electrolytic capacitor $C_{2,st}$ is placed at the dc output to (partly) filter this 100 Hz power component and prevent low-frequency (LF) stress on the load (e.g., battery).

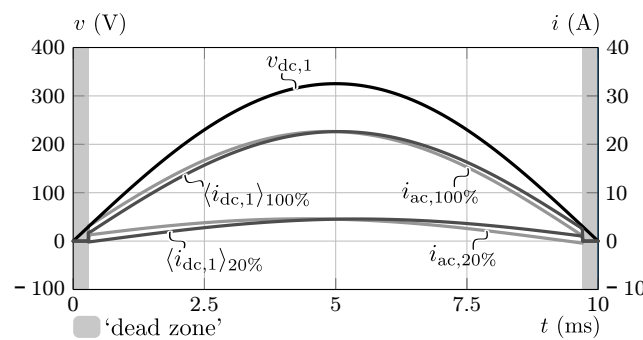


Figure 2. Ideal ac input-side quantities $v_{dc,1}$, i_{ac} , and $\langle i_{dc,1} \rangle$ within a 10 ms half period of the grid voltage v_{ac} for $I_{ac} = I_{ac,nom} = 16 \text{ A}_{rms}$ (100% power) and $I_{ac} = 0.2 \cdot I_{ac,nom} = 3.2 \text{ A}_{rms}$ (20% power).

3. Optimal Zero Voltage Switching (ZVS) Operation of the DAB DC-DC converter

3.1. Operating Principle, Available Modulation Parameters, and Relevant Switching Modes

Control of the switching-cycle averaged DAB input current $\langle i_{dc,1} \rangle$ according to (2) can be done by proper modulation of the full bridges ($S_{11...14}$ and $S_{21...24}$) of the DAB dc-dc converter [31] (see Figure 1). Thereby, the bridges produce phase-shifted edge-resonant square wave voltages v_1 and v_2 at the terminals of a HF ac-link. This link consists of a HF transformer (ratio $N = n_1/n_2$) and external series inductor L_{ext} . Also included in the ac-link are, so called, commutation inductances L_1 and L_2 which “inject” relatively small, purely reactive currents into the bridges of the DAB,

enhancing the commutation of the bridge legs without contributing to the power flow. In [25,26] they have been shown to be essential elements for achieving full-operating-range ZVS of the DAB with smooth modulation parameter trajectories. On the assumption of ideal components, the DAB can be represented by the primary-side referred equivalent model shown in Figure 3, where the main energy transfer inductance L consists of external inductance L_{ext} combined with the leakage inductances $L_{\sigma 1}$ and $L_{\sigma 2}$ (not shown in Figure 1) of the transformer:

$$L = L_{\text{ext}} + L_{\sigma 1} + N^2 \times L_{\sigma 2}. \quad (4)$$

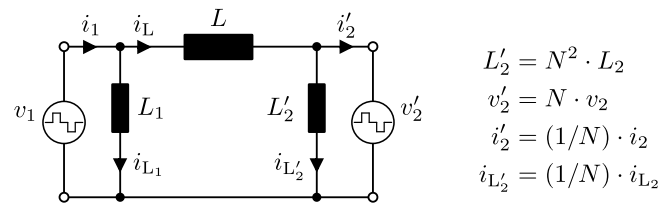


Figure 3. Simplified (lossless), primary-side referred equivalent model of the DAB dc-dc converter.

Figure 4, which depicts general waveforms of v_1 and v_2 for the two most appropriate switching modes, i.e., low-power mode 1 and high-power mode 2, for positive power flow of the DAB, defines the parameters available to modulate these voltages, being the phase-shift angle ϕ between v_1 and v_2 , the respective pulse-width modulation angles τ_1 and τ_2 , and the switching frequency f_s . As in the following it is assumed that the switching frequency value/pattern is predefined (see Section 3.3), this results in a total of three “free” modulation parameters: $\mathbf{x} = \{\phi, \tau_1, \tau_2\}$. The respective inductor currents, induced by voltages v_1 and v_2 , are also shown in Figure 4, whereby:

$$\frac{di_L(t)}{dt} = \frac{v_1(t) - N v_2(t)}{L}, \quad (5)$$

$$\frac{di_{L1}(t)}{dt} = \frac{v_1(t)}{L_1}, \quad (6)$$

$$\frac{di_{L2}(t)}{dt} = \frac{v_2(t)}{L_2}. \quad (7)$$

i_{L1} and i_{L2} , induced in commutation inductances L_1 and L_2 , are the purely reactive currents that are “injected” into the bridges of the DAB. As a result, the bridge currents i_1 and i_2 are calculated as:

$$i_1 = i_L + i_{L1}, \quad (8)$$

$$i_2 = N i_L - i_{L2}. \quad (9)$$

Both active bridges of the DAB act as ac-dc converters towards their respective dc side, transforming bridge currents i_1 and i_2 into net dc currents $i_{dc,1}$ and $i_{dc,2}$. Filter capacitors C_1 and C_2 bypass the HF components of $i_{dc,1}$ and $i_{dc,2}$. The dc component of $i_{dc,1}$ is thus the mentioned switching-cycle averaged DAB input current $\langle i_{dc,1} \rangle$, which is calculated by averaging $i_{dc,1}$ over one HF switching period $T_s = 1/f_s$, e.g. at a random instant kT_s :

$$\langle i_{dc,1} \rangle = \frac{1}{T_s} \int_{kT_s}^{(k+1)T_s} i_{dc,1}(t) dt. \quad (10)$$

Equations for $\langle i_{dc,1} \rangle$, regarding the two switching modes of Figure 4, can be found in [25].

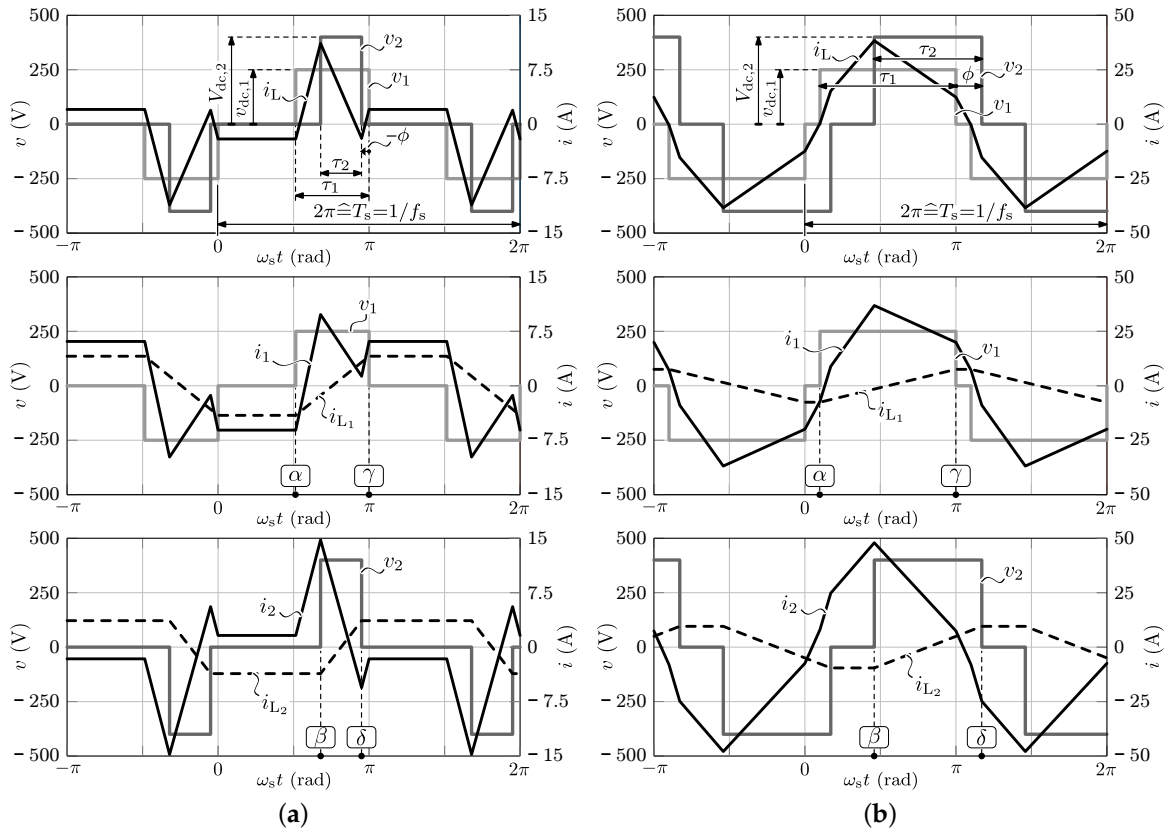


Figure 4. Ideal high-frequency (HF) ac-link voltage/current waveforms for (a) Switching mode 1: low input current/power intervals and (b) Switching mode 2: high input current/power intervals, being derived using: $v_{dc,1} = 250$ V, $V_{dc,2} = 400$ V, and $f_s = 120$ kHz. For mode 1 the selected modulation parameters are: $\tau_1 = 1.53$ rad., $\tau_2 = 0.85$ rad., $\phi = -0.16$ rad., resulting in $\langle i_{dc,1} \rangle = 2$ A. For mode 2 the selected modulation parameters are: $\tau_1 = 2.83$ rad., $\tau_2 = 2.24$ rad., $\phi = 0.54$ rad., resulting in $\langle i_{dc,1} \rangle = 22$ A.

3.2. Efficient ZVS Modulation Scheme

The method used to calculate an efficient, full-operating-range ZVS modulation scheme for the DAB is presented in [25]. It is based on a constrained numerical optimization algorithm that calculated the modulation parameters $\mathbf{x} = \{\phi, \tau_1, \tau_2\}$ in each DAB operating point $\{\langle i_{dc,1} \rangle, v_{dc,1}, V_{dc,2}\}$ based on a given switching frequency f_s ($v_{dc,1}$) and given circuit variables $\mathbf{h} = \{L, L_1, L_2, N\}$ (see next section). Through this algorithm, in each DAB operating point the most appropriate switching mode, i.e., mode 1 or mode 2 of Figure 4, is automatically selected. The resulting modulation scheme leads to quasi-lossless ZVS operation at near-minimum RMS values of the HF bridge currents i_1 and i_2 and thus minimum conduction losses. Thereby, ZVS at all switching instants $\theta_i = \{\alpha, \beta, \gamma, \delta\}$ of the DAB, which are defined in Figure 4, is ensured through incorporation of the charge $Q_{req}(V_{dc})$ that is required to charge/discharge the MOSFETs' non-linear parasitic output capacitances C_{oss} from 0 V to the corresponding dc-bus voltage V_{dc} (or vice versa) during commutation of the respective bridge legs. In Figure 4, switching instants α and β correspond with the positive rising edge of respectively v_1 and v_2 while γ and δ correspond with the respective positive falling edges. Consequently, the primary-side active bridge switches at $\theta_i = \{\alpha, \gamma\}$, while the secondary-side active bridge switches at $\theta_i = \{\beta, \delta\}$. $Q_{req}(V_{dc})$ for the used MOSFETs is depicted in Figure 5b (The selection of the FAIRCHILD

FCH76N60NF MOSFETs for the DAB is further detailed in Section 4.1.1), which is calculated using the characteristic of C_{oss} that is given in the data-sheet of the devices and shown in Figure 5a:

$$Q_{req}(V_{dc}) = \int_0^{V_{dc}} 2 C_{oss}(v) dv. \quad (11)$$

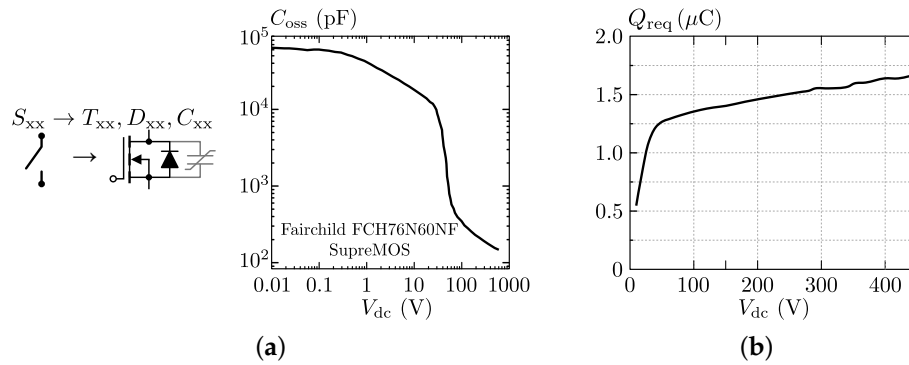


Figure 5. (a) Characteristic of the non-linear parasitic output capacitance of the used FAIRCHILD FCH76N60NF MOSFETs; (b) Charge required to charge/discharge the MOSFET's non-linear parasitic output capacitance C_{oss} from 0 V to V_{dc} (or vice versa) during commutation of a bridge leg.

For the primary-side active bridge (index 'p') this charge is function of the DAB's input voltage and is denoted $Q_{req,p}(v_{dc,1})$. For the secondary-side active bridge (index 's') this charge is function of the DAB's output voltage and is denoted $Q_{req,s}(V_{dc,2})$.

3.3. Selection of Circuit Variables

3.3.1. Switching Frequency $f_s(v_{dc,1})$

A nominal switching frequency of $f_{s,nom} = 120$ kHz is selected to accommodate a compact converter design without causing excessive switching frequency related losses. Moreover, thermal limitations apply at high switching frequencies, resulting in an increased total converter volume. The frequency of 120 kHz is chosen to stay well below these thermal limits. Furthermore, it has been shown in [25] that at both ends of the 10 ms half mains period, where the DAB input voltage $v_{dc,1}$ is low (see Figure 2), it is beneficial to linearly reduce f_s . In these regions, ZVS is hard to achieve without making commutation inductances L_1 and L_2 very small, which would result in unacceptably high circulating currents and thus a low conversion efficiency. This has led to the following predefined switching frequency pattern (see also Figure 6a of Section 3.4):

$$f_s \text{ (Hz)} = \begin{cases} 120,000 & \text{if } v_{dc,1} \geq 150 \text{ V,} \\ 75,000 + 375 \times (v_{dc,1} - 30) & \text{if } v_{dc,1} < 150 \text{ V.} \end{cases} \quad (12)$$

3.3.2. Transformer Turns Ratio N

With regard to ZVS considerations, a good design rule is to determine the turns ratio $N = n_1/n_2$ of the HF transformer such that $(N \times V_{dc,2,min}) > (v_{dc,1,max} + 10 \text{ V})$ [25]. Given the DAB's input and output voltage range, where $V_{dc,2,min} = 370$ V and $v_{dc,1,max} = \hat{v}_{ac} = 358$ V, this results in:

$$N > \left(\frac{v_{dc,1,max} + 10}{V_{dc,2,min}} = 0.9946 \right) \rightarrow N = 1. \quad (13)$$

As can be seen from Equation (13), a wider output voltage range with $V_{dc,2,min} < 370$ V is feasible by selecting $N > 1$. However, it was an initial design choice to take $N = 1$, limiting $V_{dc,2,min}$ to 370 V.

3.3.3. Main Energy Transfer Inductance L

The maximum achievable DAB input current $\langle i_{dc,1,max} \rangle$ is obtained at $\tau_1 = \tau_2 = \pi$ and $\phi = \pi/2$, mode 2, and is given by $\langle i_{dc,1,max} \rangle = N V_{dc,2} / (8 f_s L)$ [25]. This maximum current needs to be higher than the peak value of the ac input current at maximum power, which equal to $\hat{i}_{ac} (= \sqrt{2} I_{ac,nom} = \sqrt{2} \times 16 \approx 23 \text{ A})$. Therefore, the maximum allowable inductance value L_{max} is determined by:

$$L_{max} = \frac{N V_{dc,2,min}}{8 f_s \langle i_{dc,1,max} \rangle} = \frac{1 \times 370}{8 \times 120,000 \times 23} = 16.7 \mu\text{H}. \quad (14)$$

A good design guideline is to choose the value L in the range $L \approx (0.75 \dots 0.85) \times L_{max}$ [25], leaving sufficient margin for control purposes. This yields the final design value of $L = 13 \mu\text{H}$.

3.3.4. Commutation Inductances L_1 and L_2

As mentioned in Section 3.3.1, there is a strong correlation between the lower value of f_s (i.e., at low $v_{dc,1}$) and the maximum allowed values of commutation inductances L_1 and L_2 . Determination of these values requires some iteration. Assuming $L_1 = L_2$, the highest value for L_1 and L_2 that leads to full-operating-range ZVS, i.e., regarding the switching frequency pattern given by (12), has been found to be $L_1 = L_2 = 62.1 \mu\text{H}$, which is also the final design value.

3.4. Simulation Results

Figure 6 illustrates the relevant simulation results that are obtained using the constrained numerical optimization algorithm presented in [25] for a run through a half-cycle (i.e., $T_L/2 = 1/(2 f_L) = 10 \text{ ms}$) of the nominal ac input voltage ($V_{ac} = 230 \text{ V}_{rms}$, 50 Hz) at the nominal ac input current of $I_{ac} = 16 \text{ A}_{rms}$ (positive power flow) and the nominal dc output voltage of $V_{dc,2} = 400 \text{ V}$. Note that the values applied for $\langle i_{dc,1} \rangle$ correspond with line $\langle i_{dc,1} \rangle_{100\%}$ in Figure 2. The used circuit variables $\mathbf{h} = \{L, L_1, L_2, N\}$ are derived in the previous section and are listed in the right inset of Figure 1 while the predefined switching frequency pattern $f_s(v_{dc,1})$ is given by (12) and shown in Figure 6a. The modulation parameters $\mathbf{x} = \{\phi, \tau_1, \tau_2\}$ that result from the simulation are shown in Figure 6b, expectedly comprising only switching modes 1 and 2. From Figures 6c,d it can be seen that the available commutation charges $Q_{\alpha,A/B}$ and $Q_{\delta,A/B}$ at the two most critical switching instants $\theta_i = \{\alpha, \delta\}$ are higher than or equal to the minimum required commutation charges for achieving ZVS, i.e., respectively $Q_{req,p}$ (primary-side active bridge) and $Q_{req,s}$ (secondary-side active bridge). The same goes for the available commutation charges at the non-critical switching instants $\theta_i = \{\beta, \gamma\}$ which are not shown for brevity. This means that ZVS of all the semiconductor devices is guaranteed in all operating points of the simulation run.

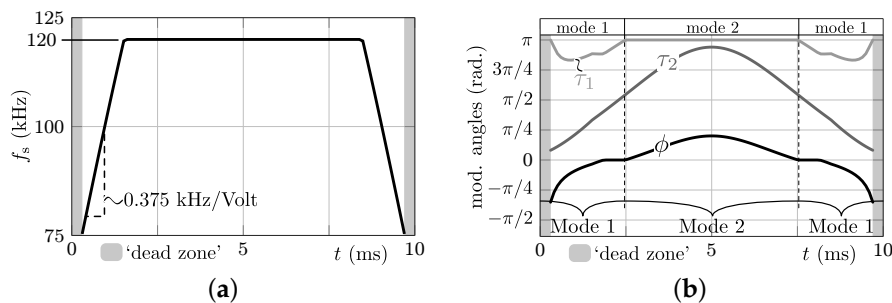


Figure 6. Cont.

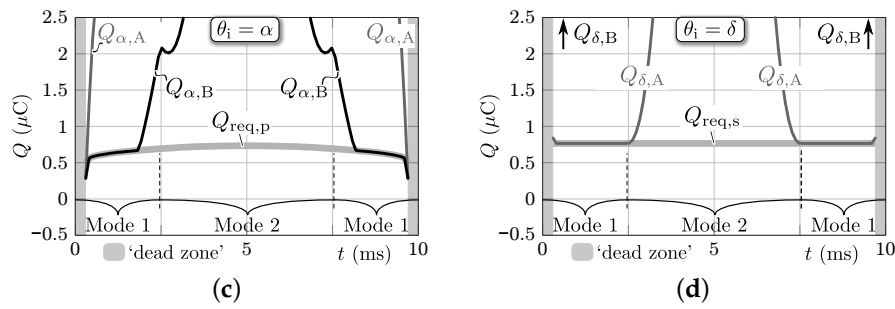


Figure 6. Resulting value trajectories of several quantities calculated for a half cycle of the nominal ac input voltage ($V_{ac} = 230 \text{ V}_{rms}$, 50 Hz) at the nominal ac input current of $I_{ac} = 16 \text{ A}_{rms}$ (positive power flow) and the nominal dc output voltage of $V_{dc,2} = 400 \text{ V}$.

4. Modeling and Optimization of the Main Functional Elements

Based on the ZVS modulation scheme, the switching frequency pattern $f_s(v_{dc,1})$, and circuit variables $\mathbf{h} = \{L, L_1, L_2, N\}$ derived in Section 3, in this section the main functional elements of the 1-S DAB ac-dc converter are designed and optimized. Each sub-section is dedicated to the design of the individual elements, combining state-of-the-art design methods/procedures, models for the component losses, and volume models with custom developed component-level optimization algorithms in order to obtain a high-efficiency and high-power-density converter design that is in compliance with the system requirements specified in Table 1.

4.1. Semiconductors and Heat Sinks

4.1.1. Semiconductor Selection

Each full-bridge of the DAB consists of four HF-switched MOSFETs, requiring characteristics that enable an excellent (soft-) switching performance and low conduction losses. The FCH76N60NF (FAIRCHILD) SupreMOS[®] high-voltage super-junction MOSFETs are selected, showing:

- A highly non-linear, not too big, parasitic output capacitance C_{oss} , enabling ZVS turn-off and turn-on. The C_{oss} characteristic of the FCH76N60NF MOSFETs is shown in Figure 5a;
- A low drain to source on-resistance $R_{DS(on)}$ and a low junction to case thermal resistance $R_{th,J-C}$, being beneficial regarding the DAB's conduction losses;
- A low total gate charge Q_g , leading to reduced turn-on and turn-off times, improved ZVS behavior (fast turn-off) [32], and reduced gate drive losses;
- An integrated fast body diode with low reverse recovery charge Q_{rr} and low reverse recovery time t_{rr} , ensuring that all the energy will timely leave the transistor after a ZVS commutation.

Of main importance for the four LF-switched MOSFETs of the SR are the characteristics that enable a reduction of the SR's conduction losses, being a low on-resistance $R_{DS(on)}$ and low junction to case thermal resistance $R_{th,J-C}$. The switching-performance related characteristics are of less importance since the SR's MOSFETs only change state two times per mains period. The STY112N65M5 (ST Microelectronics) MDmesh[™] V power MOSFETs are chosen. Table A1 of Appendix A.1 lists the most relevant device parameters of both the FCH76N60NF and the STY112N65M5 MOSFETs.

4.1.2. Loss Models

Since the modulation scheme derived in Section 3.2 results in full-operating-range ZVS of the DAB, switching losses can be neglected in the analysis [10,28]. Therefore, only conduction losses and the losses of the gate drive units are considered. For the SR also the gate drive losses can be neglected as the MOSFETs of the SR are low-frequency switched (100 Hz).

Conduction losses: The conduction losses of a MOSFET are proportional to the drain to source on-resistance $R_{DS(on)}$ and to the squared RMS value of the conducted current (The conduction losses of the internal body diodes can be neglected as they only conduct current during a very small interval of the switching period T_s). Assuming a negligible junction temperature change within a full line cycle T_L , the equivalent, line-cycle averaged conduction losses $P_{S,eq,c}$ of a single MOSFET are determined by:

$$P_{S,eq,c} = R_{DS(on)} \times I_{S,eq}^2 \quad (15)$$

$$\text{with: } I_{S,eq} = \sqrt{\frac{1}{T_L} \int_0^{T_L} I_S(t) dt}. \quad (16)$$

I_S is the local, switching-cycle averaged RMS value of the current conducted by the switch under consideration, and is used in (16) to calculate the equivalent, line-cycle averaged RMS value $I_{S,eq}$. In steady-state, each switch of the DAB conducts during half a switching cycle $T_s/2$. As a result, $I_{S,eq}$ for the switches of both active bridges are determined by:

$$I_{S_{S11-14},eq} = \sqrt{\frac{1}{T_L} \int_0^{T_L} \frac{I_1(t)}{\sqrt{2}} dt}, \quad (17)$$

$$I_{S_{S21-24},eq} = \sqrt{\frac{1}{T_L} \int_0^{T_L} \frac{I_2(t)}{\sqrt{2}} dt}. \quad (18)$$

I_1 and I_2 are the switching-cycle averaged RMS values of bridge currents i_1 and i_2 . Each SR switch conducts during half a mains period T_L . Assuming that the HF components of the DAB input current $i_{dc,1}$ are bypassed by HF filter capacitance C_1 , for each SR switch $I_{S,eq}$ can be approximated as:

$$I_{S_{SR1-4},eq} \approx \frac{I_{ac}}{\sqrt{2} \times PF}. \quad (19)$$

To calculate the resulting conduction losses using (15)–(19), the dependency of the MOSFET's on-resistance on the junction temperature T_J and on the switch current I_S has to be modeled. Figure 7 depicts these dependencies for the FCH76N60NF MOSFETs. The datasheet characteristics (gray lines) can be described by a second order approximation (Similarly, a second order approximation can be used to describe the characteristics of the SR's STY112N65M5 MOSFETs.) (black lines) according to:

$$R_{DS(on)}(T_J) |_{I_{S,ref}, V_{GS(on),ref}} = a_0 + a_1 T_{J,eq} + a_2 T_{J,eq}^2 \quad (20)$$

$$R_{DS(on)}(I_S) |_{T_{J,ref}, V_{GS(on),ref}} = b_0 + b_1 I_{S,eq} + b_2 I_{S,eq}^2 \quad (21)$$

where the equivalent, line-cycle averaged RMS values $I_{S,eq}$ for the switches of active bridge 1, active bridge 2, and the SR are respectively given by (17)–(19). $T_{J,eq}$ is the equivalent, line-cycle averaged junction temperature of the switch under consideration:

$$T_{J,eq} = \sqrt{\frac{1}{T_L} \int_0^{T_L} T_J(t) dt}, \quad (22)$$

which is calculated using the thermal network model that will be presented in Section 4.1.3. The coefficients (a_0, a_1, a_2 and b_0, b_1, b_2) required to evaluate (20) and (21) for both used MOSFET types are given in Table A2 of Appendix A.1 where $T_{J,ref}$, $I_{D,ref}$, and $V_{GS(on),ref}$ are the datasheet reference values. By combining (20) and (21), a generalized equation can be found which expresses $R_{DS(on)}$ as

a function of the deviations $\Delta T_J (= T_{J,eq} - T_{J,ref})$ and $\Delta I_S (= I_{S,eq} - I_{S,ref})$ of respectively the junction temperature $T_{J,eq}$ and the switch current $I_{S,eq}$ from the reference values $T_{J,ref}$ and $I_{S,ref}$:

$$R_{DS(on)} = \left[R_{DS(on)} |_{T_{J,ref}, I_{S,ref}, V_{GS(on),ref}} \times (1 + \alpha_1 \Delta T_J + \alpha_2 \Delta T_J^2) \times (1 + \beta_1 \Delta I_S + \beta_2 \Delta I_S^2) \right] + f_{V_{GS}}. \quad (23)$$

$R_{DS(on)} |_{T_{J,ref}, I_{S,ref}, V_{GS(on),ref}}$ is the reference datasheet value as listed in Table A1. The coefficients (α_1 , α_2 and β_1 , β_2) for both used MOSFETs are given in Table A3. In (23) a displacement term $f_{V_{GS}}$, determined using linear interpolation (see Figure 7a), is introduced in order to take into account the dependency of $R_{DS(on)}$ on the turn-on gate voltage $V_{GS(on)}$. For the FCH76N60NF MOSFET, and regarding the applied turn-on gate voltage of $V_{GS(on)} = 14$ V, $f_{V_{GS}}$ was found to be $f_{V_{GS}} = -2.247 \times 10^{-4} \Omega$. For the STY112N65M5, $f_{V_{GS}}$ could not be calculated due to the absence of information in the datasheet about the gate voltage dependency of $R_{DS(on)}$, and is assumed to be zero. This leads to a negligible overestimation of the SR's conduction losses.

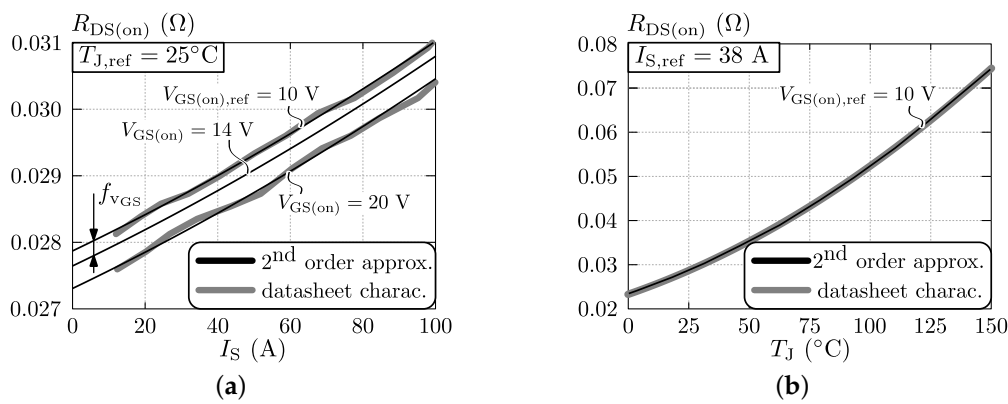


Figure 7. Dependency of the on-resistance $R_{DS(on)}$ on (a) the switch current I_S and (b) the junction temperature T_J , regarding the FAIRCHILD FCH76N60NF MOSFETs.

Gate drive losses: Assuming an efficiency of 90% for the gate drive units ($\eta_{gd} = 0.9$), the equivalent, line-cycle averaged gate drive losses $P_{S,eq,g}$ are:

$$P_{S11-24,eq,g} = \frac{1}{\eta_{gd}} \times \frac{Q_g \Delta V_{GS}^2}{\Delta V_{GS,ref}} \times \frac{1}{T_L} \int_0^{T_L} f_s(t) dt, \quad (24)$$

$$\text{whereas } P_{SRI-4,eq,g} \approx 0 \quad (25)$$

since the SR's gate drive losses can be neglected. ΔV_{GS} is the gate to source voltage swing which is 18 V ($-4 \dots +14$ V) for the custom designed gate drive circuits. Q_g is the total (typical) gate charge, measured for the reference gate voltage swing $\Delta V_{GS,ref}$ given in Table A1 of Appendix A.1.

4.1.3. Heat Sink Assembly and Thermal Network Model

Autonomous air cooling by means of forced convection is one of the system requirements defined in Table 1. Thereby the heat generated by the power devices is subtracted via a finned heat sink in combination with a fan. For the two active bridges of the DAB, a heat sink geometry with dual-sided base plate, as shown in Figure 8a, is considered. The four switches of the primary-side active bridge (active bridge 1; AB1) are mounted on the top-side base plate while the four switches of the secondary-side active bridge (active bridge 2; AB2) are mounted on the bottom-side base plate.

The four switches of the SR are mounted on a heat sink geometry with single-sided base plate, as shown in Figure 8b. The resulting stationary heat transfer models are depicted in Figure 9, where:

- $R_{th,J-C,S_{xx}}$ are the junction to case thermal resistances of the switches;
- $R_{th,C-S,S_{xx}}$ are the thermal resistances of the thermal pads (the Hi-Flow 300P thermal pads from Bergquist are used for all switches).;
- $R_{th,S-Am,AB1}$ and $R_{th,S-Am,AB2}$ ($=R_{th,S-Am,AB1}$) are the total thermal resistances between the surface of the heat sink (i.e., seen from one base plate) to the ambient, for the heat sink of the DAB;
- $R_{th,S-Am,SR}$ is the total thermal resistance between the surface of the heat sink (i.e., the surface of the base plate) to the ambient, for the heat sink of the SR.

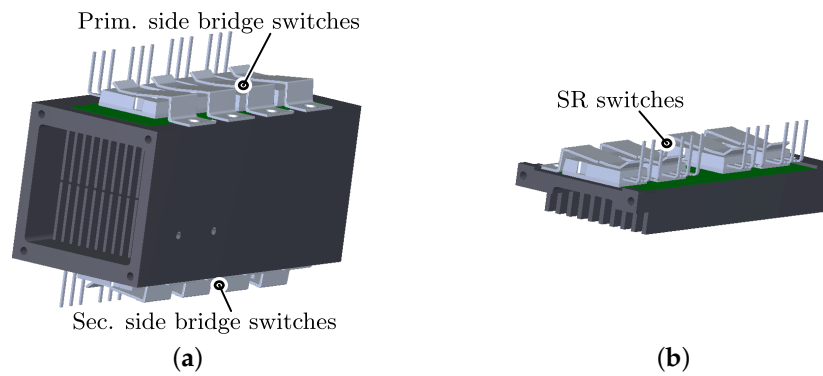


Figure 8. Heat sink-semiconductor assemblies for (a) the DAB and (b) the synchronous rectifier (SR).

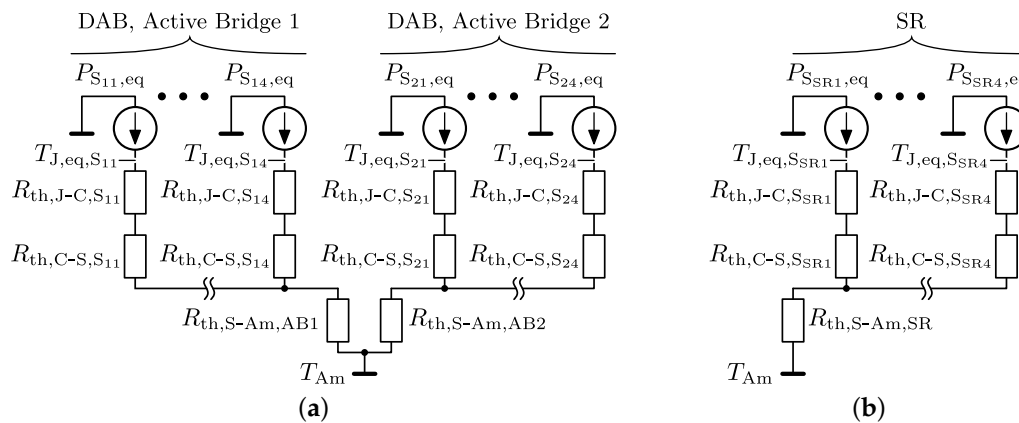


Figure 9. Stationary heat transfer model of the heat sink assembly of (a) the DAB and (b) the SR.

$R_{th,J-C,S_{xx}}$ for the used MOSFETs are given in Table A1 of Appendix A.1, while $R_{th,C-S}$ for all switches is defined by $R_{th,C-S} = h_{pad} / (\lambda_{pad} A_{pad})$ where h_{pad} is the thickness ($h_{pad} = 1.2 \times 10^{-4}$ m), λ_{pad} the thermal conductivity ($\lambda_{pad} = 1.6$ W/mK), and A_{pad} the cross section area of the thermal pads ($A_{pad} \approx A_{package} = 3.31 \times 10^{-4}$ m² for the FCH76N60NF MOSFETs and $A_{pad} \approx A_{package} = 3.22 \times 10^{-4}$ m² for the STY112N65M5 MOSFETs). $R_{th,S-Am,AB1}$ ($=R_{th,S-Am,AB2}$) and $R_{th,S-Am,SR}$ are obtained from the heat sink optimizations performed in Section 4.1.4. Referring to Figure 9, the equivalent junction temperature $T_{J,eq}$ of a switch can now be expressed as:

$$T_{J,eq} = T_{Am} + P_{S,eq} \times (R_{th,J-C} + R_{th,C-S} + 4 \cdot R_{th,S-Am}), \quad (26)$$

where, under the assumption that half the gate drive losses of a switch are internally dissipated in the switch while the other half is dissipated externally (i.e., in the gate drive units and gate resistors),

$$P_{S,eq} = P_{S,eq,c} + \frac{P_{S,eq,g}}{2}. \quad (27)$$

$P_{S,eq,c}$ and $P_{S,eq,g}$ are respectively calculated with (15), (24) and (25). T_{Am} is the ambient temperature. At this point all the information required to calculate the equivalent, line-cycle averaged semiconductor losses is available. Due to the interdependency of the quantities, a numerical solver is applied to solve: $P_{S,eq} = f(R_{DS(on)}, \dots)$, $R_{DS(on)} = f(T_J, \dots)$, and $T_J = f(P_{S,eq}, \dots)$.

4.1.4. Heat Sink Optimization

The surface-to-ambient thermal resistances $R_{th,S-Am,AB1}$ ($=R_{th,S-Am,AB2}$) and $R_{th,S-Am,SR}$ of the forced-convection-cooled heat sinks are obtained from optimizations in which the heat sink geometries are determined in a way that, for a given fan and for given outer heat sink dimensions, these thermal resistances are minimized. This involves calculation of the thermal resistance for conductive heat transfer through the heat sink material, the thermal resistance for convective heat transfer, and the temperature increase of the air flowing through the heat sink channels. The applied optimization procedure and thermal models are described in detail in [33,34], and are summarized in the following, only considering stationary heat transfer. The involved variables are given in Table 2 (Pr , ρ_{AIR} , ν_{AIR} , and λ_{AIR} are slightly temperature dependent. In order to simplify the analysis, the values at an average channel air temperature of $T_{CH} = 80^\circ\text{C}$ are used).

Table 2. Variables used for the calculation of the thermal resistance of a finned heat sink with fan, and for the calculation of the air flow rate in, and the pressure drop across the air channels of the heat sink.

Variable	Unit	Description
d	m	base plate thickness
t	m	width of a fin
b	m	total width of all air channels
c	m	total height of the air channel (=height of the fins)
s	m	width of a single air channel
L	m	length of the air channels
n	-	number of channels
k	-	fin spacing ratio according to (54)
A_{BP}	m ²	area of the heat sink base plate ($A_{BP} = L \times b$)
d_h	m	hydraulic diameter of one channel according to (53)
Δp_{CH}	N/m ²	pressure drop across the heat sink channels
\dot{V}_{AF}	m ³ /s	total volume flow of the air in the heat sink channels
Re_{avg}	-	average Reynolds number according to (58)
$Pr \approx 0.71$	-	Prandtl number (air, 80 °C)
Nu_{avg}	-	average Nusselt number according to (59) for laminar airflow or according to (60) for turbulent airflow
h	W/m ² K	convective heat transfer coefficient according to (61)
λ_{HS}	W/mK	thermal conductivity of the heat sink material
$\rho_{AIR} \approx 0.99$	kg/m ³	air density (80 °C)
$\nu_{AIR} \approx 2.1 \times 10^{-5}$	m ² /s	cinematic viscosity of air (80 °C)
$c_{p,AIR} \approx 1010$	J/kgK	specific thermal capacitance of air
$\lambda_{AIR} \approx 0.03$	W/mK	thermal conductivity of air (80 °C)

For the heat sink geometry with dual-sided base plate shown in Figure 8a, the conductive and convective heat transfer are modeled according to Figure 10. The thermal resistance $R_{th,S-Am}$ from the

base plate surface (index 'S') of this heat sink to the ambient (index 'Am'), i.e., the air temperature at the heat sink inlet, is described by:

$$R_{th,S-Am} = \frac{1}{n} (R_{th,d} + 0.5 (R_{th,F/2} + R_{th,A/2})) + \frac{0.5}{\rho_{AIR} c_{p,AIR} 0.5 \dot{V}_{AF}}, \quad (28)$$

with:

$$R_{th,d} = \frac{d}{\frac{1}{n} A_{BP} \lambda_{HS}}, \quad (29)$$

$$R_{th,F/2} = \frac{\frac{1}{4} c}{\frac{1}{2} t L \lambda_{HS}}, \quad (30)$$

$$R_{th,A/2} = \frac{1}{h L \frac{1}{2} c}. \quad (31)$$

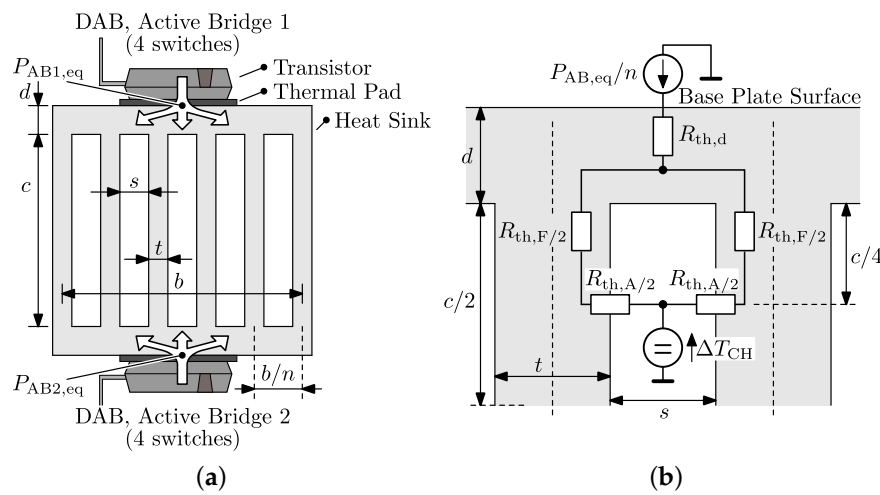


Figure 10. (a) Heat sink geometry with dual-sided base plate, considered to cool the switches of the DAB's active bridges; (b) Thermal network describing stationary heat transfer between the surface of a base plate and the air in the heat sink channel (temperature T_{CH}).

For the heat sink geometry with single-sided base plate shown in Figure 8b, the conductive and convective heat transfer are modeled according to Figure 11. $R_{th,S-Am}$ is now described by:

$$R_{th,S-Am} = \frac{1}{n} (R_{th,d} + 0.5 (R_{th,F} + R_{th,A})) + \frac{0.5}{\rho_{AIR} c_{p,AIR} \dot{V}_{AF}}, \quad (32)$$

with:

$$R_{th,d} = \frac{d}{\frac{1}{n} A_{BP} \lambda_{HS}}, \quad (33)$$

$$R_{th,F} = \frac{\frac{1}{2} c}{\frac{1}{2} t L \lambda_{HS}}, \quad (34)$$

$$R_{th,A} = \frac{1}{h L c}. \quad (35)$$

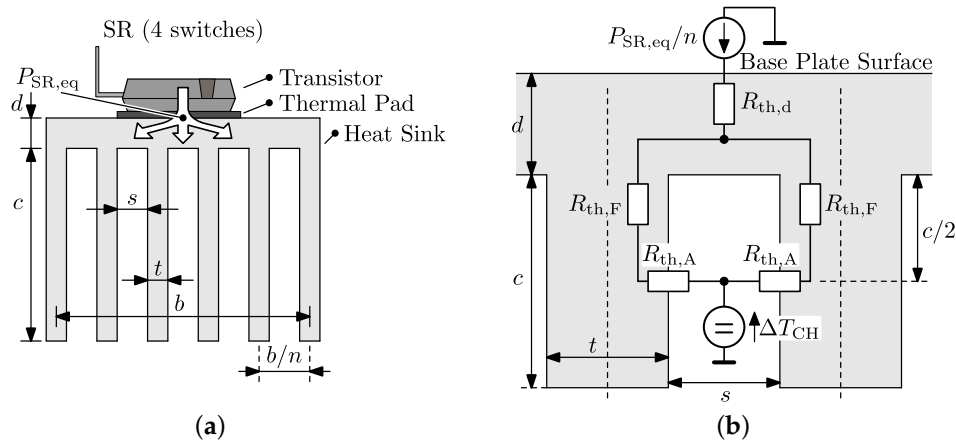


Figure 11. (a) Heat sink geometry with single-sided base plate, considered to cool the switches of the SR; (b) Thermal network describing stationary heat transfer between the surface of the base plate and the air in the heat sink channel (temperature T_{CH}).

The last term of the thermal resistance $R_{th,S-Am}$ in both (28) and (32) considers the average temperature rise of the air from channel inlet to channel outlet. Calculation of the convective heat transfer coefficient h and the total volume flow \dot{V}_{AF} of the air in the heat sink channels, which are both required for the calculation of $R_{th,S-Am}$ in (28) and (32), goes as follows.

Based on (53)–(56) of Appendix A.1, the air flow pressure drop in the heat sink channels for laminar ('lam') and turbulent ('turb') flow can be calculated. Balancing the pressure drop with the pressure of the fan, as defined by the fan characteristic in (57), gives the fan's operating point which defines the air flow and pressure drop in the heat sink channels. Using (58), the Reynolds number is found as well. In case of laminar flow, with $Re < 2300$, Equation (59) is used to calculate the Nusselt number, which describes the convective heat transfer from the channel walls into the air. In case of turbulent flow, with $Re > 2300$, the Nusselt number is calculated with Equation (60). Using (61), the convective heat transfer coefficient h of the configuration is finally found.

By repeating the above procedure for different heat sink geometries, an optimal set of geometrical parameters (d, t, b, c, s, L , and n) can be found which leads to the lowest thermal resistance $R_{th,S-Am}$. This is done for both heat sinks, assuming predefined outer heat sink dimensions (i.e., variables b, c, L , and d). As a result, the geometric parameters that are varied during the optimization are the number of channels n and the fin spacing ratio k , which is equivalent to varying the channel width s ; see Equation (54). The results are discussed below.

Heat sink of the DAB with dual-sided base plate, conform Figure 10: The fan size defines the heat sink front geometry as only the fins that are facing the fan contribute to the convective heat transfer. After thorough iteration of the mechanical design of the final prototype converter, a 40 mm × 40 mm fan turned out to be most feasible, leading to the selection of the SanAce40GA shown in Figure 12 (The SanAce40GA fan type 9GA0412P7G001, see Figure 12a, has been selected due to its high static pressure, high air flow rate, and low sound pressure level, in combination with an ultra low power consumption). Consequently, a heat sink geometry with $b = c = 40$ mm is most appropriate in order to fully utilize the fan. The pressure-flow curve, $\Delta p_{FAN}(\dot{V}_{AF})$, of this fan is depicted in Figure 12b (gray line) and can be described by a 5th order approximation (black line in Figure 12b):

$$\Delta p_{FAN}(\dot{V}_{AF}) = (5.38 \times 10^{13} \times \dot{V}_{AF}^5 - 2.115 \times 10^{12} \times \dot{V}_{AF}^4 + 1.96 \times 10^{10} \times \dot{V}_{AF}^3 - 6.315 \times 10^7 \times \dot{V}_{AF}^2 + 2.828 \times 10^4 \times \dot{V}_{AF} + 185.7). \quad (36)$$

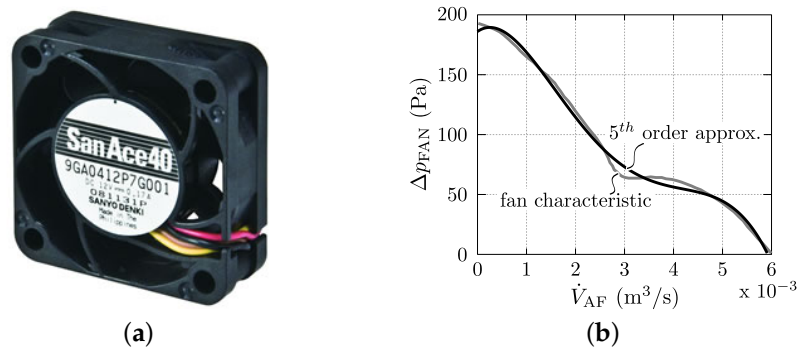


Figure 12. (a) Picture of the selected fan: SanAce40GA, type 9GA0412P7G001, 40 mm \times 40 mm \times 15 mm, 12 V; (b) Datasheet pressure-flow curve (gray line) and 5th order approximation (black line).

The length L of the heat sink channels must be large enough so that sufficient space is provided on the base plates to mount the switches. Assuming a minimum spacing of 5 mm between the packages of adjacent switches, a minimum spacing of 10 mm between the base plate borders and a package, and a package width of approximately 16 mm for the TO-247 package, the minimum base plate length becomes $L_{\min} = 3 \times 5 \text{ mm} + 2 \times 10 \text{ mm} + 4 \times 16 \text{ mm} = 99 \text{ mm}$. Preferably the maximum base plate length should not be much higher than L_{\min} , assuring homogeneous heat distribution across the base plate. The final base plate length is $L = 99.8 \text{ mm}$. The base plate thickness d should be large enough to homogeneously spread the heat and small enough to limit the thermal resistance of the heat sink. The value $d = 6 \text{ mm}$ is selected as a good trade-off between these two considerations.

Figure 13 shows the results of the optimization, applying the assumed outer heat sink dimensions, i.e., the above discussed variables b , c , L , and d , and assuming a minimum achievable fin thickness and channel width of 1 mm, which are enabled by using high-end milling machines. Furthermore, aluminium is considered for the heat sink material, defining the thermal conductivity value $\lambda_{\text{HS}} = 210 \text{ W/mK}$. Figure 13a depicts the relation between $R_{\text{th,S-Am,tot}} (=0.5 \times R_{\text{th,S-Am}})$ and the two geometric parameters n and k that are independently varied (The multiplication of $R_{\text{th,S-Am}}$ with a factor “0.5” is required since $R_{\text{th,S-Am}}$ is experienced from just one base plate of the heat sink and thus has to be divided by two in order to take both base plates (top and bottom) into account). The performance indices and parameter values for the resulting (optimal) heat sink design are given in the top inset of Table A4 of Appendix A.1. There, V_{HS} is the boxed volume of the heat sink, excluding the fan and an additional airflow inlet between the fan and the heat sink. V_{CS} is the volume of the cooling system, including the heat sink, the fan, and an additional airflow inlet between the fan and the heat sink. CSPI is the cooling system performance index [33–35], which is an objective measure that allows to compare different cooling system designs with regard to power density. For the cooling system of the DAB, with dual-sided base plate, CSPI is defined as [34]:

$$\text{CSPI} = \frac{1}{R_{\text{th,S-Am,tot}} \times V_{\text{CS}}} = \frac{1}{0.5 \times R_{\text{th,S-Am}} \times V_{\text{CS}}}. \quad (37)$$

If a heat sink design shows a CSPI that is two times higher than the CSPI of another one, the cooling volume V_{CS} can be made two times smaller for the same thermal resistance. Knowing that typical commercially available heat sink/fan combinations have a CSPI of around 5, the extensive heat sink optimization, achieving $\text{CSPI} \approx 9$, is justified. The (boxed) volume $V_{\text{CS,tot}}$, which besides the heat sink, the fan, and the airflow inlet also includes the semiconductor switching devices, is also listed in Table A4. The bottom inset of Table A4 shows the performance indices and design parameters of the heat sink used in the final (prototype) converter, and considered for further calculations. It in

fact is a near-optimal design, which is due to the fact that the minimum achievable fin thickness and channel width were restricted due to limitations of the in-house manufacturing machines/tools.

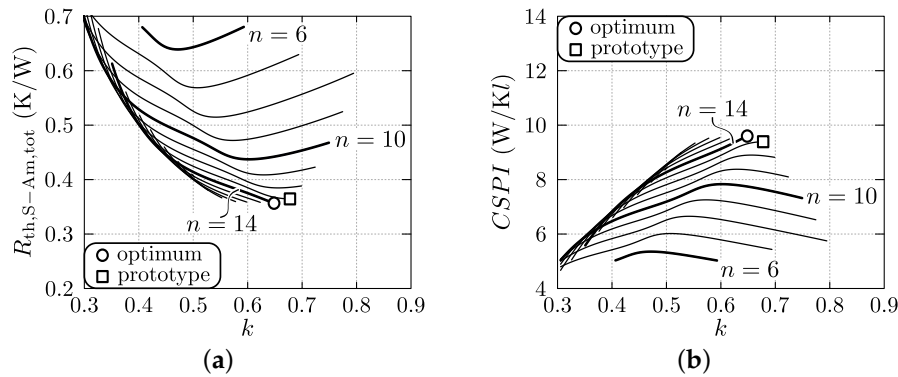


Figure 13. Optimization result for the heat sink of the DAB (geometry with dual-sided base plate, cf. Figure 10), assuming a minimum achievable fin thickness and channel width of 1 mm: (a) Total surface-to-ambient thermal resistance $R_{th,S-Am,tot}$ ($=0.5 \times R_{th,S-Am}$) as function of n and k , which are independently varied; (b) Cooling system performance index $CSPI$ as function of n and k .

Heat sink of the SR with single-sided base plate, conform Figure 11: For the heat sink of the SR, once more the 40×40 mm SanAce40GA fan (see Figure 12) is selected. As the SR requires less cooling effort than the DAB, the heat sink's front geometry values are reduced from $b = c = 40$ mm (most appropriate in order to fully utilize the fan) to $b = 36$ mm and $c = 10$ mm. This allows to use part of the fan's airflow to cool other electronic components. The reduced airflow in the heat sink channels due to the area reduction of the heat sink's front geometry is taken into account by multiplying \dot{V}_{AF} with the heat-sink-front-area to fan-area ratio $(b \times c)/(40 \times 40)$. Furthermore, a slightly increased channel length of $L = 104$ mm is used and a base plate thickness of $d = 5$ mm is applied. Once more, a minimum achievable fin thickness and channel width of 1 mm are assumed.

The performance indices and parameter values for the resulting (optimal) heat sink design are given in the top inset of Table A5 of Appendix A.1. The bottom table inset shows the values for the heat sink design of the final (prototype) converter. For the reason mentioned above this is a near-optimal design and is considered for further calculations. Note that the part of the fan that does not faces fins is not included in the calculation of $V_{CS,tot}$, and that for the heat sink with single-sided base plate $CSPI$ is defined as [34]:

$$CSPI = \frac{1}{R_{th,S-Am} \times V_{CS}}. \quad (38)$$

4.2. Magnetic Elements of the DAB: Inductors and Transformer

As mentioned before, the DAB dc-dc converter consists of three discrete magnetic elements: the HF ac-link transformer, the external series inductor L_{ext} , and the primary-side commutation inductor L_1 . The secondary-side commutation inductance L_2 is implemented by the magnetizing inductance of the transformer ($L_2 = L_M$), avoiding increased volume and costs. Referring to the equivalent DAB model shown in Figure 3, the main energy transfer inductance L is calculated with Equation (4), where $L_{\sigma,1}$ and $L_{\sigma,2}$ are the primary- and secondary-side leakage inductances of the transformer. Consequently, to determine the inductance value L_{ext} , the transformer needs to be designed first (i.e., $L_{\sigma,1}$ and $L_{\sigma,2}$ result from the final transformer design). Remind that the values of L , L_1 , L_2 , and N ($=n_1/n_2$) are derived in Section 3.3 and are given in the right inset of Figure 1.

4.2.1. Design and Optimization Procedure

Two optimization algorithms, i.e., for the transformer and for the inductors, are developed in order to optimize each magnetic element with regard to the losses and their (boxed) volume. Apart from the currents and voltages, losses in inductors and transformers depend on the geometry and the arrangement of the windings, the type of wires, the type of the core, and the geometry and material of the core. The resulting volume is mainly determined by the core geometry and the end turns of the windings. For the different optimizations, planar cores are considered because of their excellent electromagnetic and thermal characteristics and their advantageous properties with respect to the achievable power density [36,37]. All possible EELP and EILP core combinations from FERROXCUBE (ferrite core material: 3F3 and 3F4) and EPCOS (ferrite core material: N49, N87, N92, and N97) in the dimensions range from ELP32 up to ELP64 are considered. The number of stacked cores is limited by setting a maximum of 15 cm to the total core length. Litz wires are chosen to reduce eddy current losses in the windings [38–40], being particularly effective at high switching frequencies. Furthermore, four possible winding arrangements are investigated, including split, concentric, hexagonal and orthogonal type windings. Also the paralleling of several Litz bundles, as well as the interleaving (for the transformer) of the windings, is implemented in the algorithms.

All possible combinations of above mentioned design variables are top level iterated. For each iteration, in a first step, the reluctance model R_m of the considered magnetic element is calculated according to the methods proposed in [41], which inter alia provides a new analytical approach in order to determine the 3D air gap reluctance $R_{m,air}$. The inductance values, i.e., L_{ext} , L_1 , and $L_2 (=L_M)$, are controlled with the air gap length l_g (constrained to $0 \leq l_g \leq l_{g,max} = 1 \text{ mm}$), while guaranteeing that the peak flux density \hat{B} does not exceed a predefined maximum value \hat{B}_{max} . This introduces an upper and a lower limit to the possible number of turns. For the transformer, the minimum and maximum number of turns, i.e., $n_{1,min}$ respectively $n_{1,max}$, for the primary-side winding are determined by:

$$n_{1,min} = \text{ciel} \left(\frac{(V \cdot s)_{p,max}}{2 \hat{B}_{max} A_c} \right), \quad (39)$$

$$n_{1,max} = \text{floor} \left(\sqrt{L'_M (R_{m,core} + R_{m,air})} \Big|_{l_g=l_{g,max}} \right), \quad (40)$$

where $(V \cdot s)_{p,max}$ is the maximum primary-side referred Volt-seconds product, A_c the effective core cross section, $R_{m,core}$ the core reluctance, $R_{m,air}$ the air gap reluctance, and $L'_M (=N^2 \times L_M)$ the primary-side referred magnetizing inductance. The number of turns n_1 for the primary-side winding of the transformer then needs to be in the range $n_{1,min} \leq n \leq n_{1,max}$. Evidently, the number of turns n_2 for the secondary-side winding is directly linked to n_1 via the transformer's turns ratio $N = n_1/n_2$. For the inductors, the minimum and maximum number of turns, i.e., $n_{ind,min}$ respectively $n_{ind,max}$, are determined by:

$$n_{ind,min} = \text{ciel} \left(\frac{L_{ind} i_{ind,max}}{\hat{B}_{max} A_c} \right), \quad (41)$$

$$n_{ind,max} = \text{floor} \left(\sqrt{L_{ind} (R_{m,core} + R_{m,air})} \Big|_{l_g=l_{g,max}} \right), \quad (42)$$

where $i_{ind,max}$ is the peak inductor current and $L_{ind} (=L_{ext} \text{ or } L_1)$ the inductance value of the considered inductor. The number of turns n_{ind} for the inductors then needs to be in the range $n_{ind,min} \leq n_{ind} \leq n_{ind,max}$. The upper boundary of the maximum allowed flux density \hat{B}_{max} is set by the core material saturation flux density B_{sat} at a core temperature of 100°C , applying a 30% safety margin. Subsequently, using an inner iteration loop, the number of turns n_1 (transformer) is varied from $n_{1,min}$ to $n_{1,max}$ while the number of turns n_{ind} (inductors) is varied from $n_{ind,min}$ to $n_{ind,max}$.

In a second step, a predefined objective function, which is determined by the sum of the core losses and the winding losses of the magnetic element at nominal operating conditions of the DAB, is minimized for each of above iterations. The applied loss models are summarized in Section 4.2.2. The optimization algorithm used to minimize the cost function iterates the number of strands in the Litz bundles, as well as the diameter of the individual strands, in order to achieve a window filling that is optimal with regard to the winding losses. Thereby, constraint functions set restrictions on the positioning of the individual Litz bundles by bringing into relation the number of strands, the strand diameter, and wire positioning functions with the given core window area, taking into account creepage distances.

4.2.2. Loss Models

In this section, the models used to calculate the winding and core losses of the magnetic elements are summarized. For the calculation of the core losses, the improved Generalized Steinmetz Equation (iGSE) [40,42] has been evaluated as the most accurate model which only requires the Steinmetz material parameters. This method takes into account the losses due to domain wall motion, which is directly related to the time dependency dB/dt of the core's flux density. Therefore the iGSE is applicable for non-sinusoidal flux waveforms such is the case for the magnetic components of the DAB, which experience piecewise-linear flux-time functions. With the iGSE, the per-unit-volume (index 'V') core losses are calculated using the Steinmetz parameters k , α , and β , according to:

$$P_{\text{core,V}} = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^\alpha (\Delta B)^{\beta-\alpha} dt, \quad (43)$$

with:

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos \theta|^\alpha 2^{\beta-\alpha} d\theta}, \quad (44)$$

where ΔB is the peak-to-peak flux density. The Steinmetz parameters k , α , and β are extracted out of the core's data sheets, providing information about the per-volume-unit core losses as a function of frequency f , peak flux density \hat{B} , and temperature T . This enables extraction of k , α , and β using the empirical Steinmetz Equation $P_{\text{core,V}} = k f^\alpha \hat{B}^\beta$, which is valid for sinusoidal excitation only.

Regarding winding losses, the ohmic losses in the Litz wires (further referred to as Litz bundles) can be separated into skin effect losses P_S from self-induced eddy currents inside the conductors, external proximity effect losses P_{P_e} from eddy currents due to the external magnetic field H_e that originates in the air gap fringing field and in the magnetic field from neighboring Litz bundles, and internal proximity effect losses P_{P_i} from eddy currents due to the internal magnetic field H_i that is produced by the bundle itself. The per-unit-length (index 'L') skin-effect losses (including the dc losses) of a Litz bundle consisting of n_s strands, are calculated with [40]:

$$P_{S,L} = n_s \times R_{\text{dc,s,L}} \times F_R(f) \times \left(\frac{\hat{I}}{n_s} \right)^2, \quad (45)$$

where \hat{I} are the Fourier amplitude coefficients of the total current in the Litz-wire bundle at the different harmonic frequencies f . $R_{\text{dc,s,L}}$ is the per-unit-length dc resistance of a single strand: $R_{\text{dc,s,L}} = 4/(\sigma \pi d_s^2)$, with d_s the diameter of the strand and σ the electric conductivity of the conductor material ($\sigma = 5.26 \times 10^7$ 1/ Ωm for the considered Litz wires). F_R is the skin-effect factor:

$$F_R(f) = \frac{\xi}{4\sqrt{2}} \times \left(\frac{\text{ber}_0(\xi) \text{bei}_1(\xi) - \text{ber}_1(\xi) \text{bei}_0(\xi)}{\text{ber}_1(\xi)^2 + \text{bei}_1(\xi)^2} - \frac{\text{bei}_0(\xi) \text{ber}_1(\xi) + \text{bei}_1(\xi) \text{ber}_0(\xi)}{\text{ber}_1(\xi)^2 + \text{bei}_1(\xi)^2} \right), \quad (46)$$

with $\xi = d_s / (\sqrt{2} \delta)$, where δ is the skin depth according to $\delta = 1 / \sqrt{\pi \mu_0 \sigma f}$. μ_0 is the permeability of the conductor material ($\mu_0 = 4 \pi 10^{-7}$ H/m for air and copper). The per-unit-length proximity losses in a Litz bundle are calculated as [40]:

$$P_{P,L} = P_{P,e,L} + P_{P,i,L} = n_s \times R_{dc,s,L} \times G_R(f) \left(\hat{H}_e^2 + \frac{\hat{I}^2}{2 \pi^2 d_b^2} \right). \quad (47)$$

d_b is the diameter of the Litz bundle while G_R is the proximity-effect factor:

$$G_R(f) = -\frac{\xi \pi^2 d_s^2}{2\sqrt{2}} \times \left(\frac{\text{ber}_2(\xi) \text{ber}_1(\xi) + \text{ber}_2(\xi) \text{bei}_1(\xi)}{\text{ber}_0(\xi)^2 + \text{bei}_0(\xi)^2} + \frac{\text{bei}_2(\xi) \text{bei}_1(\xi) - \text{bei}_2(\xi) \text{ber}_1(\xi)}{\text{ber}_0(\xi)^2 + \text{bei}_0(\xi)^2} \right). \quad (48)$$

H_e is the external magnetic field that originates in the air gap fringing field and in neighboring Litz bundles, and is calculated using the 2D analytical approach proposed in [40]. This approach relies on an imaging and mirroring method in order to inter alia model the impact of a surrounding magnetic conducting material. Thereby the air gap fringing fields are modeled by means of fictitious conductors with eddy currents equal to the magneto-motive force across the air gap. H_i , with $\hat{H}_i^2 = \hat{I}^2 / (2 \pi^2 d_b^2)$; see last term of (47), is the internal magnetic field across one strand, which originates in its neighboring strands. For the calculation of H_i it is assumed that the current is equally distributed over the Litz bundle's cross-sectional area.

4.2.3. Optimization Results

For each magnetic element of the DAB, the outcome of the optimization is a two-dimensional performance space, showing the losses at nominal operating conditions versus the (boxed) volume of the component. Figure 14a–c, respectively depict the resulting performance spaces for the HF transformer and for inductors L_{ext} and L_1 . The designs that are chosen for the hardware realization of the transformer and of inductor L_{ext} are marked with \star . As these designs are located in the corner point of the so called “Pareto Front”, they are an optimal trade-off between efficiency and power density. It should be noted that the hardware realization of L_1 , marked with \star , is a duplicate of the HF transformer with one of the two windings removed and with the air gap length adapted according to the calculated inductance value L_1 . The realization of L_1 is thus non-optimal, and is referred to as the “prototype” (prot.) design. A better solution would be to use the design marked with \star , which is referred to as the “optimal” (opt.) design. The detailed parameter values of the transformer and inductor designs are listed in Tables A6–A8 of Appendix A.2, where Table A8 lists the values for both the “prot.” and the “opt.” design of L_1 . The implication of using the improved design “opt.” for L_1 on the converter performance is further discussed in Section 5.

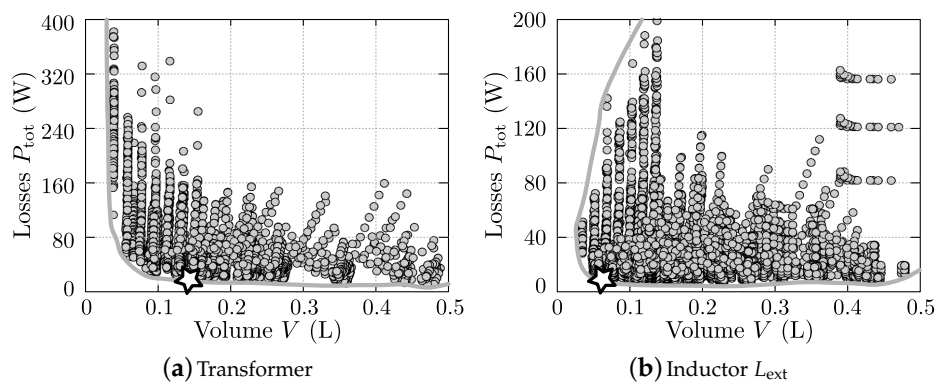


Figure 14. Cont.

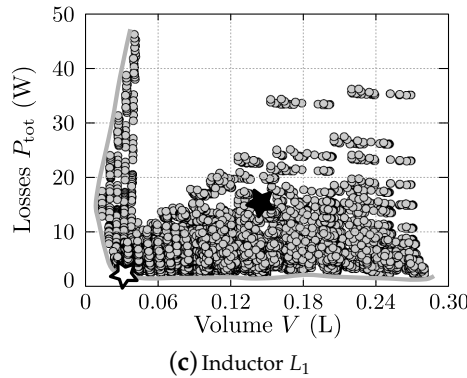


Figure 14. Two-dimensional losses vs. volume performance spaces for (a) the high-frequency (HF) ac-link transformer; (b) inductor L_{ext} ; (c) inductor L_1 , calculated for nominal DAB operating conditions.

4.3. Output Filter Capacitors

4.3.1. Low-Frequency (LF) Output Filter Capacitors

Since the DAB handles the double line frequency component of the converter's ac input power, a LF filter capacitor $C_{2,st}$ is placed at the converter's dc output side (see Figure 1), limiting the output voltage ripple. Assuming unity power factor, where the ac input current $i_{ac}(t)$ and input voltage $v_{ac}(t)$ are in phase, the output voltage ripple $\tilde{V}_{dc,2}(t)$ is calculated as:

$$\tilde{V}_{dc,2}(t) = \frac{-P_{dc,2} \times \sin(2\omega_L t)}{2\omega_L C_{2,st} V_{dc,2}}, \quad (49)$$

where $P_{dc,2} (\approx P_{ac} = V_{ac} \times I_{ac})$ is the constant output power component, $\omega_L = 2\pi f_L$ the angular frequency of the grid, and $V_{dc,2}$ the average dc output voltage of the converter. As a result, the amplitude of the output voltage ripple is equal to $\hat{V}_{dc,2} = P_{dc,2} / (2\omega_L C_{2,st} V_{dc,2})$.

In the final hardware demonstrator, the LF output filter capacitance $C_{2,st}$ is realized using three 390 μF , 500 V dc, electrolytic capacitors (ELCOs), type EETED2W391EA, from Panasonic, Kadoma/Osaka, Japan, which are placed in parallel. This leads to a total LF output filter capacitance value of $C_{2,st} = 1170 \mu\text{F}$. For nominal conditions, i.e., $V_{ac} = 230 \text{ V}_{rms}$, $I_{ac} = 16 \text{ A}_{rms}$, and $V_{dc,2} = 400 \text{ V}$, this results in a very acceptable output voltage ripple amplitude of $\hat{V}_{dc,2} \approx 12 \text{ V}$. The worst case (i.e., at $V_{ac} = V_{ac,max} = 253 \text{ V}_{rms}$, $I_{ac} = I_{ac,nom} = 16 \text{ A}_{rms}$, and $V_{dc,2} = V_{dc,2,min} = 370 \text{ V}$) ripple amplitude is $\hat{V}_{dc,2} \approx 14.2 \text{ V}$, which is still less than 4% of the output voltage.

For the electrolytic LF output filter capacitors, with a diameter of 35 mm and a height of 40 mm (single capacitor), the total boxed volume is 0.147 L. The part of the SR's fan that does not faces heat sink fins is facing the LF filter capacitors, which are thereby cooled. Consequently, an additional volume of 0.024 L is added to the LF capacitor's volume for the system volume calculation in Section 5. Remind that this part of the SR's fan is not taken into account in the volume of the SR's cooling system, see Section 4.1.4.

4.3.2. High-Frequency (HF) Output Filter Capacitors

Besides the electrolytic LF capacitors, small HF filter capacitors C_2 are placed at the output of the DAB in order to bypass the HF components of the DAB output current $i_{dc,2}$. The HF filter capacitance value C_2 is realized using seven 1.5 μF , 630 V dc, metallized polypropylene MKP film capacitors, type B32674D6155, from TDK-EPCOS, Minato, Tokyo, Japan, which are placed in parallel. This leads to a total HF output filter capacitance value of $C_2 = 10.5 \mu\text{F}$ and a maximum HF output voltage ripple amplitude of less than 2 V. With a width of 31.5 mm, a depth of 12.5 mm, and a height of 19 mm (single capacitor), the total boxed volume is 0.052 L.

4.3.3. Capacitor Losses

Losses in the LF filter capacitors are caused by their equivalent series resistance (ESR) and leakage current. The ESR value listed in the datasheet of the employed 390 μF EETED2W391EA ELCOs from Panasonic is 0.34Ω at 120 Hz. According to the datasheet, the leakage current I_{leak} of a single capacitor is calculated as $I_{\text{leak}} = 3 \times 10^{-6} \times \sqrt{C} V$ (A), with C the capacitance value in μF and V the capacitor voltage. Consequently, the total power loss $P_{C_{2,\text{st}}}$ in the LF capacitors is calculated as:

$$P_{C_{2,\text{st}}} = 3 \times (I_{C_{2,\text{st}}}^2 \times \text{ESR} + I_{\text{leak}} \times V_{\text{dc},2}), \quad (50)$$

where $I_{C_{2,\text{st}}}$ is the RMS value of the current in a single capacitor. The factor 3 is applied since three capacitors are placed in parallel. Since the leakage current of polypropylene film capacitors is very low, the losses in the EPCOS HF capacitors are mainly caused by the ESR, producing a total loss of less than 0.5 W, which can be neglected.

4.4. Electromagnetic Compatibility (EMC) Input Filter

In order to comply with the CISPR 22 Class B standard [43] for conducted emission (CE), an electromagnetic compatibility (EMC) filter is designed. Thereby, a differential mode (DM) filter is required to attenuate the HF components of the DAB input current $i_{\text{dc},1}$ (see Figure 1), and a common mode (CM) filter for suppressing the CM noise on the earth wire.

4.4.1. Differential Mode (DM) Filter Design

The DM EMC input filter is designed according to the procedure outlined in [44], and conform the guidelines given in [45] regarding filter damping, in order to comply with the CISPR 22 Class B standard [43] in the frequency range of 150 kHz–30 MHz. The employed procedure includes the correct modeling of the line impedance stabilization network (LISN) and of the EMC test receiver (see Figure 15), i.e., conform the CISPR 16 standard [46]. This enables a prediction of the measurement results and thus gives the basis for the calculation of the required attenuation and for the filter design. The video-filtered quasi-peak (QP) values $V_F(j\omega)$ at the output of the EMC test receiver need to be lower than the CISPR 22 Class B limit $\text{Lim}_B(j\omega)$. For the case where no DM filter is present the most critical QP value is found to be $V_{F,f_{\text{crit}}} = 170.4 \text{ dB}\cdot\mu\text{V}$ at a corresponding frequency of $f_{\text{crit}} = 236.3 \text{ kHz}$, at which the Class B limit value is equal to $\text{Lim}_{B,f_{\text{crit}}} = 62.22 \text{ dB}\cdot\mu\text{V}$. Therefore, the required attenuation $\text{Att}_{\text{req},f_{\text{crit}}}$ of the DM filter, including a margin of 6 dB, is equal to:

$$\text{Att}_{\text{req},f_{\text{crit}}} = V_{F,f_{\text{crit}}} - \text{Lim}_{B,f_{\text{crit}}} + 6 \text{ dB} = 170.4 - 62.22 + 6 = 114.18 \text{ dB}. \quad (51)$$

Note that the simulations are performed under nominal operating conditions, i.e., at the nominal ac input voltage of $V_{\text{ac}} = 230 \text{ V}_{\text{rms}}$, the nominal ac input current of $I_{\text{ac}} = 16 \text{ A}_{\text{rms}}$, and an output voltage of $V_{\text{dc},2} = 400 \text{ V}$. Also note that towards the dc side of the DAB's input bridge, the bridge current i_1 is rectified into $i_{\text{dc},1}$, doubling the frequency. Therefore, and due to operation with variable switching frequency, the value of 236.3 kHz for f_{crit} can be explained.

The DM filter needs to provide the required attenuation $\text{Att}_{\text{req},f_{\text{crit}}}$ so that, in combination with an appropriate CM filter, the converter complies with the standards. Thereby, control-oriented aspects have to be considered as well, ensuring a satisfactory operation of the converter. Using the recursive design procedure outlined in [44], the two-stage DM filter structure shown in Figure 15 turns out to be most appropriate for achieving these goals (The components of the DM filter in Figure 15 are indexed "DM", i.e., "DM1" for the first filter stage and "DM2" for the second filter stage. The capacitive part C_{DM1} of the first filter stage is effectively realized by the HF dc-link capacitor C_1). In order to provide sufficient damping of the filter resonances without decreasing the attenuation in the frequency range that is relevant for compliance with the CISPR 22 Class B standard [43], for each filter stage an (optimized) passive damping network is employed. Thereby, a series inductor damping network with

coupled inductors is selected for the first filter stage while a parallel capacitor damping network is used for the second filter stage. The resulting values and specifications of the employed DM filter components are listed in Table A9 of Appendix A.3. Note that the second filter stage is formed by capacitance C_{DM2} in combination with the LISN ($R_{LISN} = 50 \Omega$, $C_{LISN} = 250 \text{ nF}$, $L_{LISN} = 50 \mu\text{H}$, see Figure 15) and the mains inductance L_{mains} , i.e., no discrete inductor L_{DM2} is present.

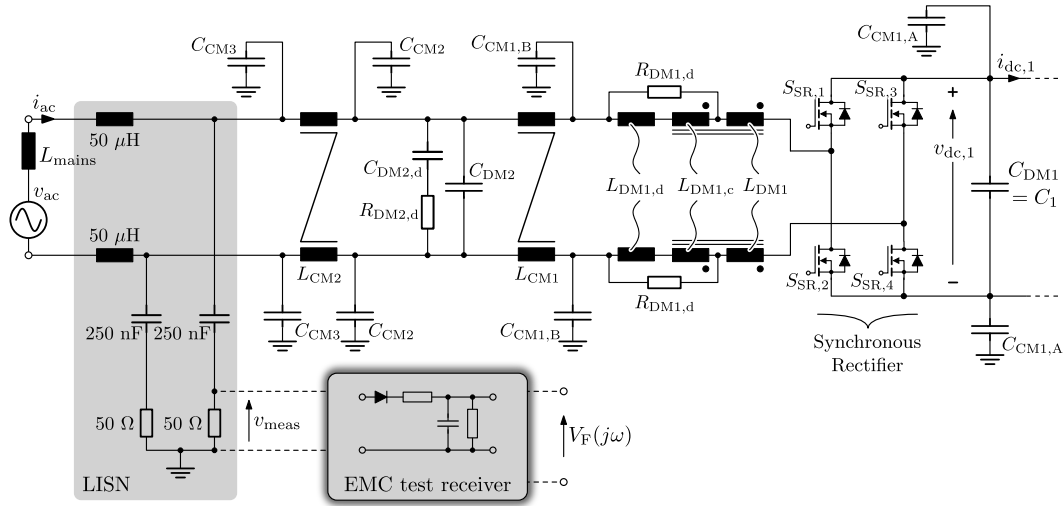


Figure 15. Schematic of the differential mode/common mode (DM/CM) electromagnetic compatibility (EMC) filters, connected to the synchronous rectifier of the ac-dc converter. Also shown are the line impedance stabilization network (LISN) and the EMC test receiver.

Figure 16 shows the simulated (nominal operating conditions) video-filtered quasi-peak (QP) values $V_F(j\omega)$ (indicated by a “☆”), along with the CISPR 22 Classes A and B limits and the lower boundary value $Min_{res}(j\omega)$ after insertion of the designed DM input filter and under the assumption of zero mains impedance (Note that the curve $Min_{res}(j\omega)$ is obtained as the square root of the sum of the squares of the RMS values of all harmonic components $V_{meas}(j\omega)$ located within the resolution bandwidth (RBW) of the EMC test receiver [44]). It can be seen that the critical output value $V_{F,f_{crit}}$ (indicated by a “★”) is 6.67 dB lower than the Class B limit $Lim_{B,f_{crit}}$, meaning that compliance with the CISPR 22 Class B standard is achieved. Furthermore, the simulated low-frequency harmonics of the mains current i_{ac} , which in the case at hand need to be below the limits defined in the IEC 61000-3-2 standard [30] for Class A equipment, are depicted in Figure 17 and are well below the limits.

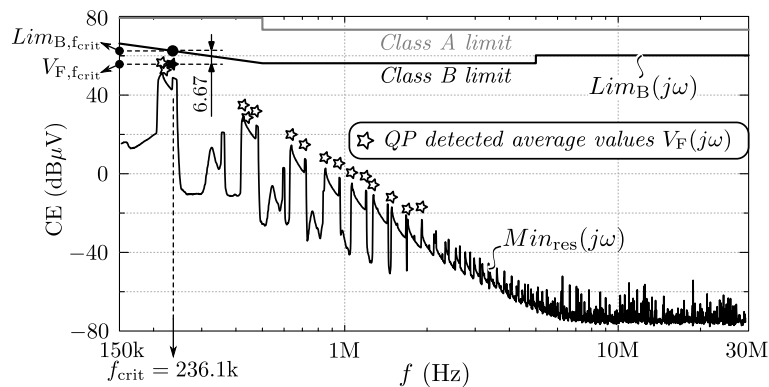


Figure 16. Simulation of the quasi-peak (QP) measurement after insertion of the designed differential mode (DM) input filter and under the assumption of zero mains impedance. Also shown is the absolute lower boundary $Min_{res}(j\omega)$ for the measurement result and the conducted emission (CE) limits according to CISPR 22 Classes A and B.

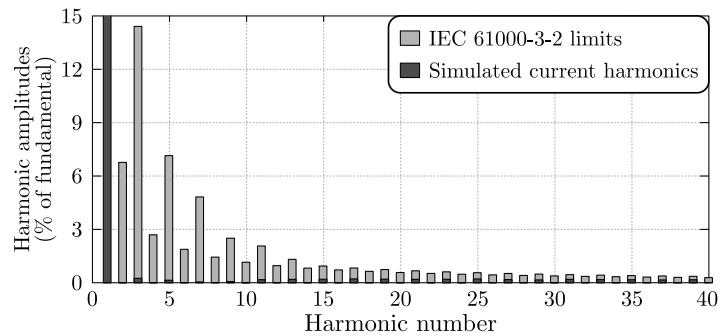


Figure 17. Simulated low-frequency harmonics of the mains current i_{ac} and the IEC61000-3-2 limits.

4.4.2. Common Mode (CM) Filter Design

In order to successfully design a common mode (CM) filter that suppresses the CM noise on the earth wire, an equivalent CM noise-source model is required [47]. Thereby, detailed knowledge of the relevant parasitic impedances, through which the CM currents circulate, is essential. As a result, the design of the CM EMC filter is mostly performed after the realization of a first converter prototype system. The parasitic impedances can then be identified through impedance measurements and a CM noise propagation model can be derived. Consequently, several design iterations of the prototype system and/or the CM filter might be required until compliance with CISPR 22 Class B standard for conducted emission (CE) is obtained. Therefore, and as it is the DM filter and not the CM filter which mainly defines the EMC filter volume, the low-load power factor, and the dynamics of the system, here the detailed modeling of the CM filter is omitted. Nevertheless, a CM filter has been included in the converter hardware but, however, the selection of the filter architecture and the determination of the CM component values are based on intuition rather than on modeling and optimization. As can be seen from Figure 15, in which the components of the CM filter are indexed “CM” (i.e., “CM1” for the first, “CM2” for the second, and “CM3” for the third filter stage), a three-stage CM EMC filter structure is employed. The final values and specifications of the CM filter components used in the converter prototype system are listed in Table A10 of Appendix A.3.

4.4.3. EMC Filter Losses and Volume

The hardware realization of the CM and DM EMC input filter can be seen in the picture of the prototype system presented in Section 5. With a width of 132 mm, a height of 72 mm, and a depth of 25 mm, the total boxed volume of the filter board is 0.238 L. This volume includes the converter’s ac connection terminals and an ac fuse, the converter’s dc connection terminals and a dc fuse, a 2-electrode surge arrester (type EC600-X, EPCOS), and several metal oxide varistors. An additional volume of 0.042 L is occupied by six CM filter capacitors that are placed on another PCB, yielding a total EMC filter volume of 0.279 L. Since the leakage current of polypropylene film capacitors is very low, the losses in the EPCOS HF EMC filter capacitors are mainly caused by the ESR, producing a total loss of less than 0.4 W. Consequently, the losses in the EMC filter capacitors can be neglected. The same goes for the losses (less than 0.1 W) in damping resistors $R_{DM1,d}$ and $R_{DM2,d}$, and for the core losses of the DM inductors. Therefore, the main contributors to the overall losses of the EMC input filter are the losses due to dc resistance of the CM and DM inductor windings.

4.4.4. Implementation of the Controller

The control hardware consists of an on-board FPGA (field-programmable gate array), in particular the ALTERA EP3C25E144C8N CYCLONE III (Altera, San Jose, CA, United States), which is operated with a clock frequency of 62.5 MHz and programmed in the VHDL hardware description language. The FPGA is responsible for generating the PWM gate drive signals, for reading in the current and voltage measurement peripherals (A/D converters), and for ‘fast’ overcurrent and overvoltage protection.

Moreover it communicates over Ethernet with an off-board PC-based Real-Time Target (RTT). The RTT can be programmed and operated through Matlab/Simulink™ (MathWorks, Natick, MA, United States) where the PI current controller, the ‘slow’ protection, the start-stop procedures, and the control parameter generation are implemented. The Real-TimeWorkshop™ (MathWorks, Natick, MA, United States) automatic code generator translates the Matlab/Simulink™ model into C-code which is executed by the RTT.

The cascaded control structure used to control the switching-cycle averaged DAB input current $\langle i_{dc,1} \rangle$ according to Equation (2) is shown in Figure 18 (A more extensive description of the control structure used can be found in [25], also discussing some ‘advanced’ features that are implemented in the hardware, such as switching-delay compensation and variable dead-time generation). The dashed lines indicate which part of the controller hardware performs each particular task. The measured quantities (index ‘m’) that are available in the PFPGA as digital signals are also indicated in Figure 18. For testing of the prototype system a fixed dc voltage was applied to the output of the DAB. Optionally, an outer PI voltage controller can be used to control the output voltage $V_{dc,2}$ required by the dc load.

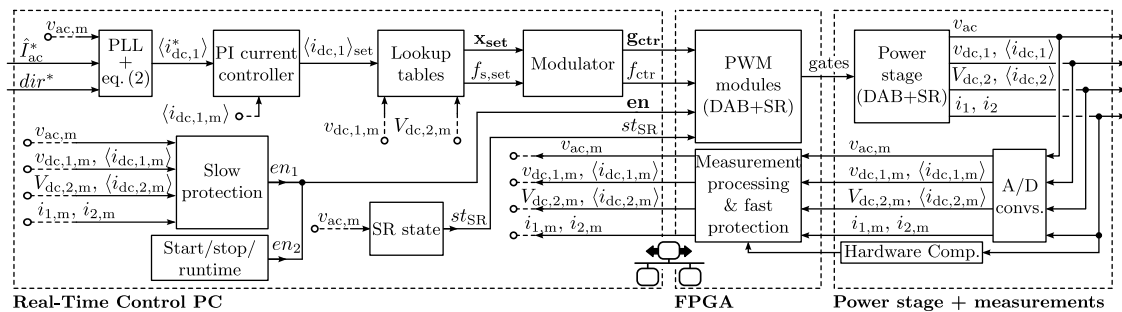


Figure 18. Control structure employed to control the switching-cycle averaged DAB input current $\langle i_{dc,1} \rangle$ according to Equation (2).

The PI current control loop outputs set-current $\langle i_{dc,1} \rangle_{set}$ in order to control $\langle i_{dc,1} \rangle$ based on the measured value $\langle i_{dc,1,m} \rangle$ and a reference value $\langle i_{dc,1}^* \rangle$ which is generated using a Phase Locked Loop (PLL) and calculation of Equation (2) based on the amplitude set-point \hat{I}_{ac}^* of the ac input current and the requested power flow direction dir^* . In the test setup, \hat{I}_{ac}^* and dir^* are directly inputted by the user but they can also origin from an external source such as a battery management system or a vehicle power management system. The control parameters needed by the DAB to effectively generate set-current $\langle i_{dc,1} \rangle_{set}$ are determined using lookup tables which are calculated for the whole converter’s operating range, as explained in Section 3.2. Thereby, modulation parameters $\mathbf{x}_{set} = \{\phi, \tau_1, \tau_2\}_{set}$ and switching frequency $f_{s,set}$ are determined based on $\{\langle i_{dc,1} \rangle_{set}; v_{dc,1,m}; V_{dc,2,m}\}$ and using linear table interpolation. Finally, the modulator function calculates the frequency counter f_{ctr} and the bridge-leg gate counters: $\mathbf{g}_{ctr} = \{g_{ctr,S_{11-12}}; g_{ctr,S_{13-14}}; g_{ctr,S_{21-22}}; g_{ctr,S_{23-24}}\}$. These, as well as the enable signals $\mathbf{en} = \{en_1; en_2\}$ and the SR state st_{SR} , are inputted to the FPGA PWM-generation modules. Enable signals en_1 and en_2 origin from the ‘slow’ protection and start/stop/runtime units while the SR state st_{SR} is defined by:

$$st_{SR} = \begin{cases} 1 & \text{if } v_{ac,m} \geq 0 : S_{SR,1-4} \text{ on}; S_{SR,2-3} \text{ off}, \\ -1 & \text{if } v_{ac,m} < 0 : S_{SR,1-4} \text{ off}; S_{SR,2-3} \text{ on}. \end{cases} \quad (52)$$

5. Hardware Demonstrator and Calculated Performance

Based on the loss and volume models, and on the results of the component optimizations presented in Section 4, in this section the performance of the 1-S DAB ac-dc converter is calculated in terms of losses (and efficiency) and volume (and power density). The results are obtained under the assumption of $T_{Am} = 22^\circ\text{C}$ ambient temperature since this has also been the test condition

(see Section 6). The 3.7 kW hardware demonstrator, being realized in accordance with the design and optimization results of Section 4, is shown in Figure 19. It should be mentioned that the primary-side commutation inductance L_1 was originally not included in the hardware design. During testing L_1 was connected to the converter with the screws that are located on the top power PCB. Nevertheless, the volume of this inductor is included in the results for the system's volume and power density. Below, the calculated performance is presented for two converter designs which only differ from each other by the implementation of the primary-side commutation inductor L_1 :

- Converter design A; prototype converter; uses the design “prot.” (prototype) for L_1 . This is how the hardware demonstrator is implemented;
- Converter design B; further optimized; uses the improved design “opt.” (optimal) for L_1 (see Section 4.2.3). This design yields higher conversion efficiencies and power density compared to converter design A.

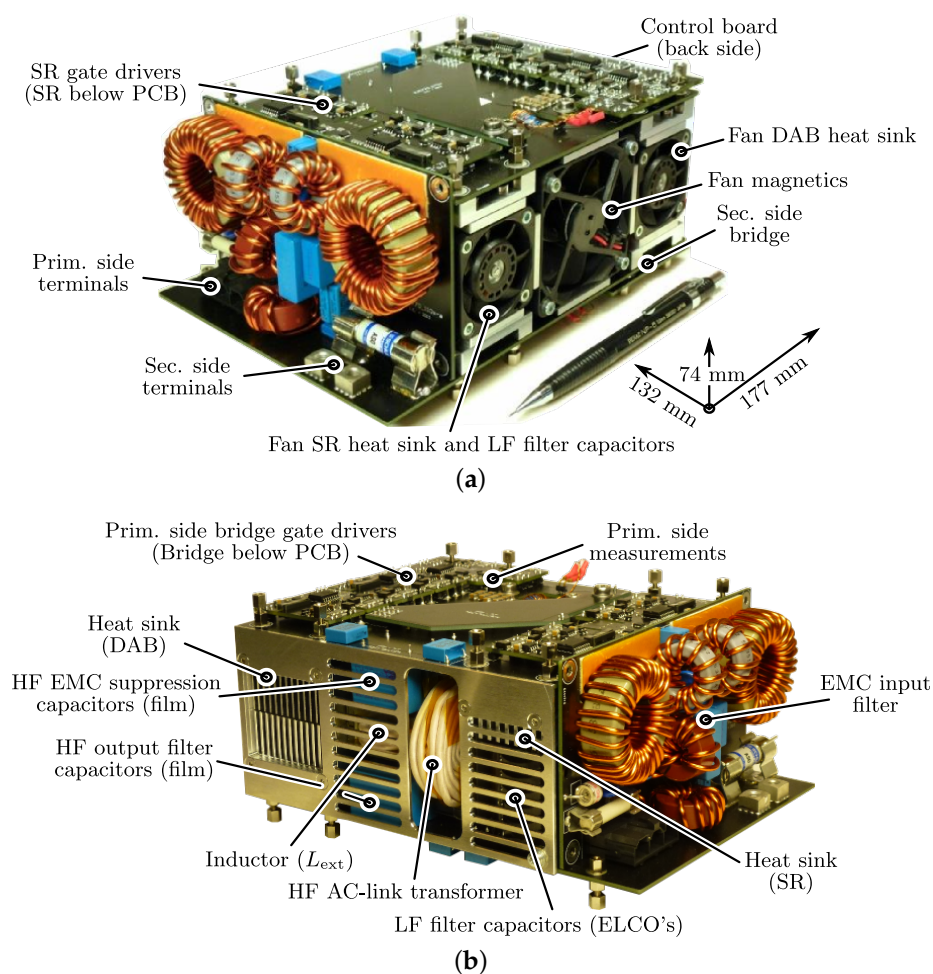


Figure 19. The 3.7 kW, 1-S (single-stage), single-phase, bidirectional, and isolated DAB ac-dc hardware demonstrator: (a) Front-right view; (b) Front-left view.

The losses of the individual functional elements of the converter are presented in Figures B1–B5 of Appendix B. They are shown as function of the ac input current I_{ac} , which is expressed as percentage of its nominal value $I_{ac} = 16 A_{rms}$. Each figure is obtained for the nominal ac input voltage of $V_{ac} = 230 V_{rms}$ and the nominal dc output voltage of $V_{dc,2} = 400 V$. In Figure B3 it can be seen that the improved design “opt.” for L_1 performs significantly better than the design

“prot.” (prototype converter), implying that a substantial performance enhancement of the hardware demonstrator would be possible by replacing L_1 .

By summation of the losses of the individual components, the overall converter losses are calculated which are shown in Figure 20 for both converters designs A (prototype; see Figure 20a) and B (further optimized; see Figure 20b). As expected, the latter design yields a substantial overall loss reduction. Note that the calculated overall converter losses include the auxiliary power losses, which comprise the power consumption of the fans and of the control board. These losses are estimated to be approximately 7 W. Figure 21 shows the resulting overall conversion efficiency, which for design A (prototype; see Figure 21a) is above 95% for input powers higher than 20% of the nominal input power, with a very flat efficiency curve and thus a high partial-load efficiency. The peak efficiency is around 96.1% and the efficiency at nominal input power approximately 95.6%. From Figure 21b it is clear that, at all power levels, an important efficiency enhancement is feasible (up to around 0.8%) when considering converter design B with optimized inductor L_1 .

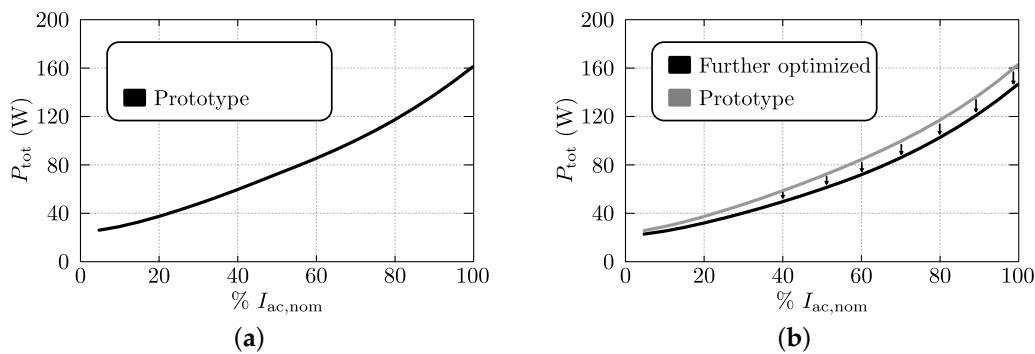


Figure 20. Calculated total losses of the 1-S DAB ac-dc converter implemented according to (a) converter design A (prototype converter) and (b) converter design B (further optimized).

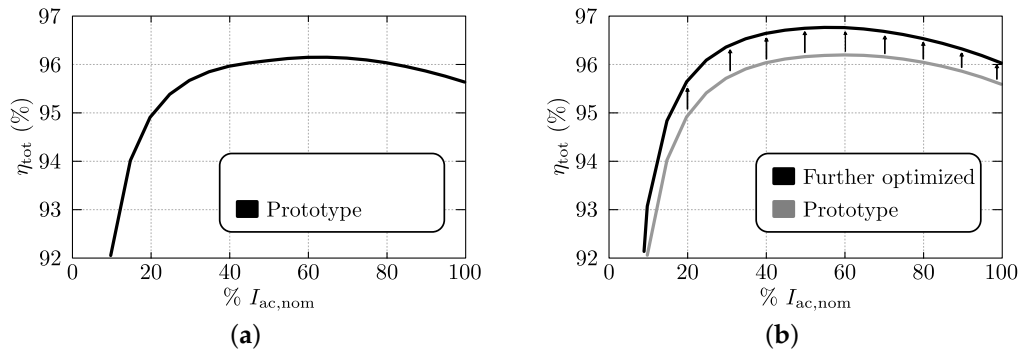


Figure 21. Calculated efficiency of the 1-S DAB ac-dc converter implemented according to (a) converter design A (prototype converter) and (b) converter design B (further optimized).

Figure 22 shows the loss contribution of the different converter components for both converter designs A (prototype; dark gray bars) and B (further optimized; light gray bars). Figure 22a corresponds with the nominal ac input voltage of $V_{ac} = 230 \text{ V}_{rms}$, the nominal ac input current of $I_{ac} = 16 \text{ A}_{rms}$, and the nominal dc output voltage of $V_{dc,2} = 400 \text{ V}$. Figure 22b corresponds with the same voltage conditions but reduced ac input current of $I_{ac} = 0.2 \times I_{ac,nom} = 3.2 \text{ A}_{rms}$.

Figure 23 shows the volume contribution of the different converter components for both converter designs A (prototype; dark gray bars) and B (further optimized; light gray bars), calculated using the boxed component volumes derived in Section 4. The bars “total, excl. other” represent the summation of the component volumes while the bars “total, incl. other” represent the total boxed

volume of the complete converter system, including the “dead space” and the volume of the remaining electronic components such as the measurement circuits, the PCBs, and the gate drive units. The volume reduction of 0.107 L achieved for converter design B results from the smaller size of the optimized primary-side commutation inductor L_1 .

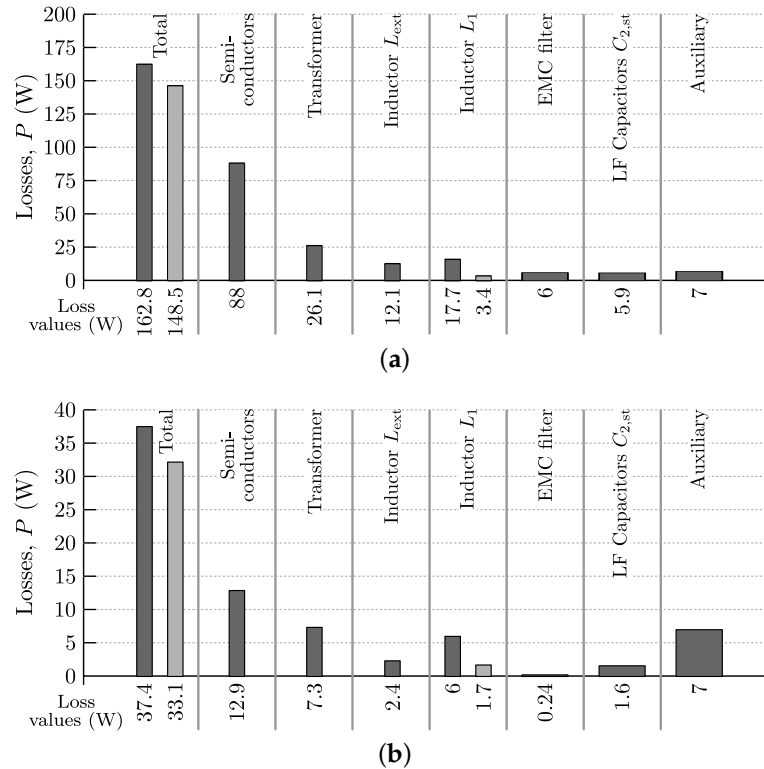


Figure 22. Loss contribution of the different converter components for both converter designs A (prototype; dark gray bars) and B (optimized; light gray bars) at $V_{ac} = 230 \text{ V}_{rms}$, $V_{dc,2} = 400 \text{ V}$ for (a) $I_{ac} = I_{ac,nom} = 16 \text{ A}_{rms}$ (100% power) and (b) $I_{ac} = 0.2 \times I_{ac,nom} = 3.2 \text{ A}_{rms}$ (20% power).

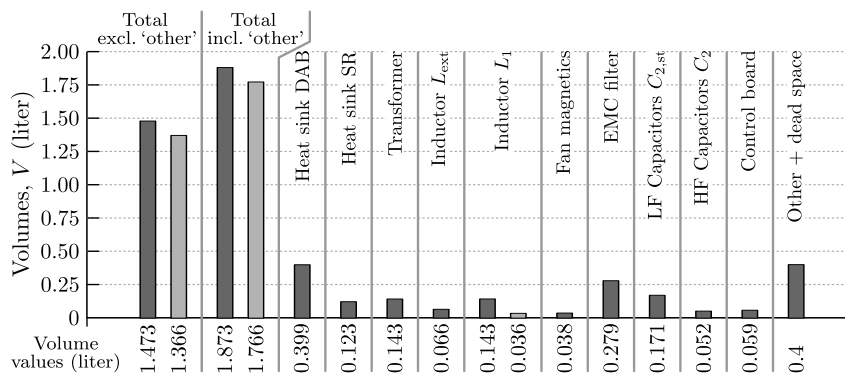


Figure 23. Volume contribution of the different converter components for both converter designs A (prototype; dark gray bars) and B (optimized; light gray bars).

The power density values (ρ) that correspond with the total volumes in Figure 23, calculated for the nominal input power of 3.7 kW, are listed in Table 3. A high power density of approximately 2 kW/L is achieved for the prototype converter (i.e., design A) while the power density of the improved converter design (i.e., design B) is around 2.1 kW/L. When only considering the volume occupied by the main converter components, i.e., neglecting the “dead space” and the volume occupied by the measurement circuits, PCBs, and gate drive units, the power densities are respectively 2.5 and

2.7 kW/L. This means that there is still room for reducing the total volume of the system by a more effective assembly of the components. By dividing the volume value “total, excl. other” by the volume value “total, incl. other”, the packing factor f_{pack} is obtained, being a measure of how “good” the different components are assembled. The packing factors for converter designs A and B are respectively $f_{\text{pack,A}} = 0.786$ and $f_{\text{pack,B}} = 0.774$ (see Table 3).

Table 3. Converter power density values (at 3.7 kW, nominal input power).

Volume Definition	Design A (prot.)		Design B (opt.)	
	V (L)	ρ (kW/L)	V (L)	ρ (kW/L)
Incl. “other + dead space”	1.87	2	1.76	2.1
Excl. “other + dead space”	1.47	2.5	1.36	2.7
Packing factor f_{pack}	$1.47/1.87 = 0.79$		$1.36/1.76 = 0.77$	

6. Measurements

The 3.7 kW hardware demonstrator shown in Figure 19 is successfully tested within the full power range (up until an output power of 3.7 kW), showing ac waveforms with little distortion, and which are in very good agreement with the waveforms obtained from simulations. For illustration, Figure 24 depicts the measured waveforms at the ac and dc side of the converter at nominal ac input voltage of $V_{\text{ac}} = 230 \text{ V}_{\text{rms}}$, nominal ac input current of $I_{\text{ac}} = 16 \text{ A}_{\text{rms}}$ and 450 V dc output voltage. The conversion efficiency and the converter’s ac input power quality are evaluated using the Yokogawa WT3000 precision power analyzer, having a power accuracy reading of $\pm 0.02\%$.

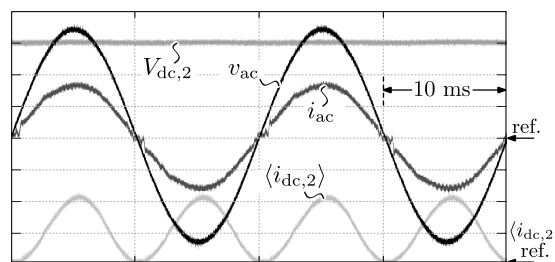


Figure 24. Measured waveforms at the ac and dc side of the converter at nominal ac input voltage of $V_{\text{ac}} = 230 \text{ V}_{\text{rms}}$, nominal ac input current of $I_{\text{ac}} = 16 \text{ A}_{\text{rms}}$ and 450 V dc output voltage. Voltage and current scale: v_{ac} : 100 V/div., i_{ac} : 12.5 A/div., $V_{\text{dc,2}}$: 150 V/div., $\langle i_{\text{dc,2}} \rangle$: 7.5 A/div.

Figure 25 shows the measured performance of the converter with regard to the reached efficiency and with regard to the quality of the ac input power. The measured efficiency (Figure 25a; solid lines) corresponds well with the efficiency calculated in Section 5 (see dashed lines). Although the trends match very well, a slight discrepancy (mostly less than 0.4%) can be noticed between the calculated and the measured efficiencies. This might require further refinement of the loss models developed in Section 4, especially regarding possible non-zero ZVS losses of the MOSFETs. The measured efficiencies are higher than 95% within the major part of the output power range, with a very flat efficiency curve and thus a high partial-load efficiency. The peak efficiency is around 96.1% and the efficiency at nominal output power approximately 95.6% (see curve for the nominal output voltage of $V_{\text{dc,2}} = 400 \text{ V}$). As predicted by the calculations, only a minor difference (around 0.25%–0.3% at maximum) can be noticed between the efficiency curves at different output voltages, i.e., the efficiency is highest for the lowest output voltage and lowest for the highest output voltage. Furthermore, as can be seen in Figure 25b a (true) power factor (PF) close to unity, and a low total harmonic distortion (THD) of the ac input current of around 4%, are obtained within the major part of the output power range and within the whole output voltage range. This makes that, regarding conversions efficiency,

system power density, PF, and THD, the converter requirements specified in Table 1 of the introduction are achieved, confirming the competitiveness of the investigated 1-S DAB ac-dc converter.

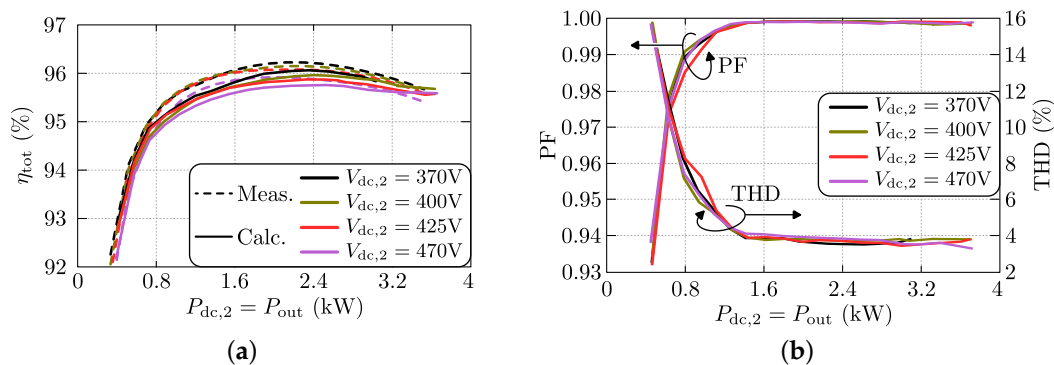


Figure 25. Measurement of (a) the efficiency and (b) the total harmonic distortion (THD) and (true) power factor (PF). The measurements are taken at the nominal ac input voltage of $V_{ac} = 230 V_{rms}$, in the complete power range (up to 3.7 kW output power), and at different dc output voltages.

For completeness, Figure 26 compares the efficiency of the presented 1-S DAB ac-dc converter (black line; converter A) with the efficiency of two state-of-the-art dual-stage converter systems reported in literature. The efficiency obtained is substantially higher than that of the converter presented in [48] (converter B; Si MOSFETs and SiC diodes), while the converter presented in [49] (converter C) has the highest efficiency but, however, is not bidirectional. The power density reached with converter A (2 kW/L, this work) is substantially higher than the 0.66 kW/L power density of converter B while converter C has the highest power density of 2.5 kW/L. A characteristic comparison of the three converter systems is given in Table 4.

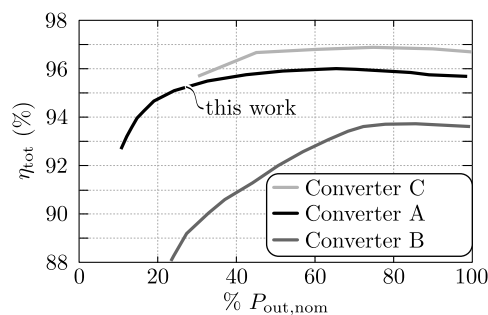


Figure 26. Comparison of the efficiency of the presented 1-S DAB ac-dc converter (black line; converter A) and the efficiency of two state-of-the-art dual-stage converter systems reported in literature: converter B presented in [48] and converter C presented in [49].

Table 4. Characteristic comparison of the presented 1-S DAB ac-dc converter (converter A) and the two state-of-the-art dual-stage converter systems reported in literature: converter B presented in [48] and converter C presented in [49].

Variable	Conv. A (This Work)	Conv. B [48]	Conv. C [49]
$V_{ac,nom}$ (V)	230	240	230
$V_{dc,2,nom}$ (V)	400	400	48
P_{nom} (kW)	3.7	3.33	3.33
η_{nom} (%)	95.6	93.6	96.6
ρ (kW/L)	2	0.66	2.5
Bidirectional	yes	no	no

Lastly, in Figures 27 and 28, measured switching waveforms (see Figures 27b and 28b) of the ac-link currents and voltages are shown, and match very well with the corresponding simulations (see Figures 27a and 28a). The measurements are performed when applying dc voltages at both the input (ac-side) and output (dc-side) terminals of the DAB ac-dc converter, i.e., regarding two different operating points as detailed in the figure captions.

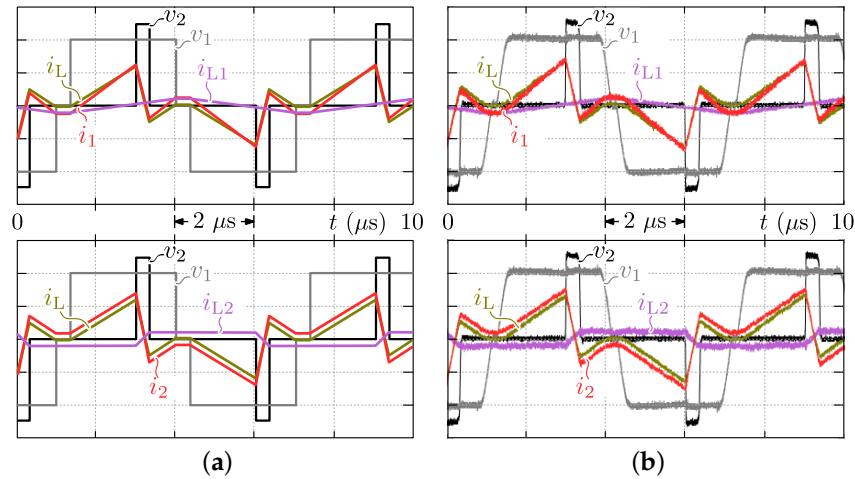


Figure 27. (a) Calculated and (b) measured HF ac-link currents and voltages at $v_{dc,1} = 50$ V, $\langle i_{dc,1} \rangle = 3.05$ A, $V_{dc,2} = 370$ V, where $\tau_1 = 2.77$ rad., $\tau_2 = 0.35$ rad., $\phi = -0.7$ rad., $f_s = 83.1$ kHz (mode 1 operation). Voltage and current scale, v_1 : 25 V/div., v_2 : 150 V/div., i_x : 10 A/div.

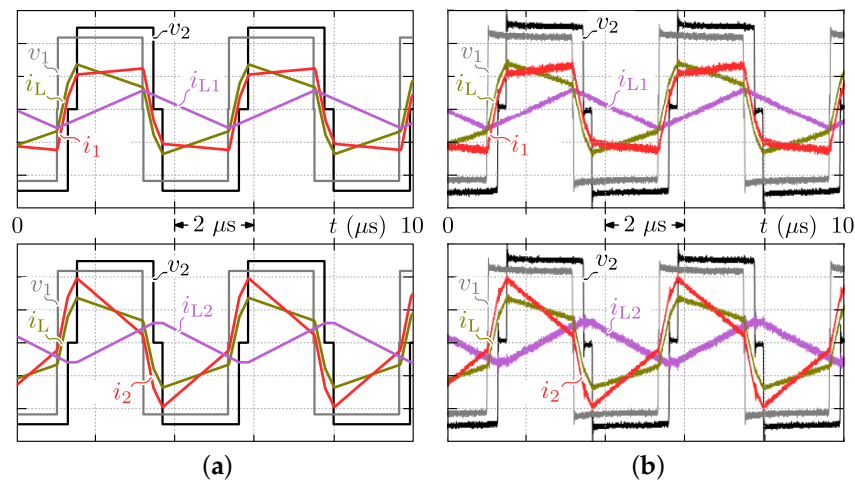


Figure 28. (a) Calculated and (b) measured HF ac-link currents and voltages at $v_{dc,1} = 325.27$ V, $\langle i_{dc,1} \rangle = 18$ A, $V_{dc,2} = 370$ V, where $\tau_1 = 3.11$ rad., $\tau_2 = 2.81$ rad., $\phi = 0.4$ rad., $f_s = 120$ kHz (mode 2 operation). Voltage and current scale, v_1 : 150 V/div., v_2 : 150 V/div., i_x : 20 A/div.

7. Conclusions

In this paper, a single-stage (1-S) converter approach is analyzed to realize a single-phase, bidirectional, isolated ac-dc converter, combining all functionalities into one conversion stage and thus enabling a cost-effective efficiency and power density increase compared to traditional dual-stage (2-S) ac-dc converters. The converter topology consists of a quasi-lossless synchronous rectifier followed by an isolated DAB dc-dc converter, putting a small filter capacitor in between.

In a first step, the operating principle/conditions of the 1-S ac-dc converter are presented, the available modulation parameters and relevant switching modes of the DAB are detailed, and the

method used for calculating an efficient full-operating-range ZVS modulation scheme is summarized. The selection of the high-level circuit variables such as the switching frequency, the inductance values, and the transformer's turns ratio is outlined as well.

To show the performance potential of the investigated 1-S DAB ac-dc converter, a comprehensive design procedure and multi-objective optimization with respect to efficiency and power density is presented, using detailed loss and volume models. The models and procedures are verified by a 3.7 kW hardware demonstrator, interfacing a 400 V dc-bus with the single-phase 230 V, 50 Hz utility grid. A high power density of approximately 2 kW/L is achieved for the prototype converter, which is implemented with all silicon (Si) MOSFETs. Moreover, measured efficiencies are higher than 95% within the major part of the output power range, with a very flat efficiency curve and thus a high partial-load efficiency. The peak efficiency is around 96.1% and the efficiency at nominal output power approximately 95.6%. The measured efficiency corresponds well with the calculated efficiency, showing only a slight discrepancy of mostly less than 0.4%. This might require further refinement of the loss models, especially regarding possible non-zero ZVS losses of the MOSFETs. Furthermore, a (true) power factor (PF) close to unity, and a low total harmonic distortion (THD) of the ac input current of around 4%, are obtained within the major part of the output power range and within the whole output voltage range. This makes that, regarding conversions efficiency, system power density, PF, and THD, the predefined (automotive) converter requirements are met.

Lastly, the performance of the presented 1-S DAB ac-dc converter is compared with the performance of two state-of-the-art dual-stage converter systems reported in literature. Therefrom, it can be concluded that the achieved efficiency and power density are very close to the absolute state-of-the-art, confirming the competitiveness of the investigated 1-S converter architecture, especially since it is shown that a further efficiency increase of up around 0.8% and a further power density increase of 0.1 kW/L is feasible by a simple improvement of one of the inductor designs (i.e., commutation inductor L_1). Evidently, an even higher efficiency and/or power density is enabled by use of gallium nitride (GaN) or silicon carbide (SiC) semiconductor devices.

Acknowledgments: Costs to publish this paper in open access are covered by the Electromechanics and Power Electronics (EPE) group of the Eindhoven University of Technology (TU/e). The major part of this work was carried out in the framework of the doctoral (Ph.D.) studies of Jordi Everts at the division of Electrical Energy and Computer Architectures (ELECTA) of the University of Leuven (KU Leuven; Leuven, Belgium) under supervision of Johan Driesen. The research of Jordi Everts was partly funded by a Ph.D. grant of the Institute for the Promotion of Innovation through Science and Technology in Flanders (IWT Vlaanderen). The author also wants to acknowledge Tiphase N.V. (Leuven, Belgium), and in particular Jeroen Van den Keybus for the support provided.

Author Contributions: Jordi Everts developed the models, performed the analysis, designed and built the prototype, conceived and designed the experiments, performed the experiments, analyzed the data, and wrote the paper.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

1-S	Single-Stage
2-S	Dual-Stage
BEV	Battery Electric Vehicle
CE	Conducted Emission
CM	Common Mode
CSPI	Cooling System Performance Index
DAB	Dual Active Bridge
DM	Differential Mode
ELCO	Electrolytic Capacitor
EMC	Electromagnetic Compatibility
ESR	Equivalent Series Resistance

FPGA	Field-Programmable Gate Array
HF	High-Frequency
iGSE	improved Generalized Steinmetz Equation
LF	Low-Frequency
LISN	Line Impedance Stabilization Network
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
PF	Power Factor
PFC	Power Factor Correction
PHEV	Plug-in Hybrid Electric Vehicle
QP	Quasi-Peak
RBW	Resolution Bandwidth
SR	Synchronous Rectifier
TCM	Triangular Current Mode
THD	Total Harmonic Distortion
V2G	Vehicle-to-Grid
ZVS	Zero Voltage Switching

Appendix A. Supplement to Section 4

Appendix A.1. Semiconductors and Heat Sinks

Table A1. Most relevant parameters of the FCH76N60NF high-voltage super-junction MOSFETs employed in the DAB and the STY112N65M5 MDmesh™ V power MOSFETs employed in the SR.

Quantity	Value (FCH76...)	Value (STY112...)	Condition	Description
V_{DS} (V)	600	650	$T_J = 25^\circ\text{C}$	Drain to source blocking voltage
I_{DS} (A)	72.8	96	$T_J = 25^\circ\text{C}$	Continuous drain current
I_{DS} (A)	46	61	$T_J = 100^\circ\text{C}$	Continuous drain current
$R_{th,j-c}$ (K/W)	0.23	0.2	-	Thermal resistance, junction to case
$R_{DS(on)}$ (m Ω)	28.7 ($I_{DS} = 38\text{ A}$)	19 ($I_{DS} = 48\text{ A}$)	$V_{GS} = 10\text{ V}$, $T_J = 25^\circ\text{C}$	Static drain to source on-resistance (typ.)
I_{SD} (A)	76	96	$T_J = 25^\circ\text{C}$	Maximum continuous drain to source diode forward current
Q_g (nC)	230	350	$\Delta V_{GS} = 10\text{ V}$	Total gate charge (typ.)
Q_{rr} (μC)	1.8 ($I_{SD} = 38\text{ A}$)	17 ($I_{SD} = 96\text{ A}$)	$V_{GS} = 0\text{ V}$	Reverse recovery charge
t_{rr} (ns)	200 ($I_{SD} = 38\text{ A}$)	570 ($I_{SD} = 96\text{ A}$)	$V_{GS} = 0\text{ V}$	Reverse recovery time
-	TO-247	Max247	-	Package

Table A2. Coefficients (a_0 , a_1 , a_2 and b_0 , b_1 , b_2) required to evaluate (20) and (21), i.e., the second order approximations of the dependency of the drain to source on-resistance $R_{DS(on)}$ on the junction temperature T_J and on the switch current I_S for the used MOSFETs.

MOSFET Type	a_0	a_1	a_2	b_0	b_1	b_2
FCH76N60NF	$I_{S,ref} = 38\text{ A}$, $V_{GS(on),ref} = 10\text{ V}$			$T_{J,ref} = 25^\circ\text{C}$, $V_{GS(on),ref} = 10\text{ V}$		
	2.33×10^{-2}	1.8921×10^{-4}	1.007×10^{-6}	2.79×10^{-2}	2.6065×10^{-5}	5.3553×10^{-8}
STY112N65M5	$I_{S,ref} = 48\text{ A}$, $V_{GS(on),ref} = 10\text{ V}$			$T_{J,ref} = 25^\circ\text{C}$, $V_{GS(on),ref} = 10\text{ V}$		
	1.51×10^{-2}	1.606×10^{-4}	1.2649×10^{-7}	1.79×10^{-2}	2.0204×10^{-5}	3.1405×10^{-10}

Table A3. Coefficients (α_1 , α_2 and β_1 , β_2) and values for $T_{j,ref}$ and $I_{S,ref}$, required to evaluate (23) for the used MOSFETs.

MOSFET Type	α_1	α_2	β_1	β_2	$T_{j,ref}$	$I_{S,ref}$
FCH76N60NF	8.3587×10^{-3}	3.5136×10^{-5}	1.0402×10^{-3}	1.8487×10^{-6}	25 °C	38 A
STY112N65M5	8.6966×10^{-3}	6.59×10^{-6}	1.0691×10^{-3}	-1.6643×10^{-8}	25 °C	48 A

$$d_h = \left(\frac{2sc}{s+c} \right), \quad (53)$$

$$k = \left(\frac{s}{b/n} \right), \quad (54)$$

$$\Delta p_{CH,lam} = \frac{48 \rho_{AIR} v_{AIR} L}{n s c d_h^2} \times \dot{V}_{AF}, \quad (55)$$

$$\Delta p_{CH,turb} = \frac{\frac{L}{d_h} \rho_{AIR} 0.5 \left(\frac{\dot{V}_{AF}}{n s c} \right)^2}{(0.79 \ln \left(\frac{2 \dot{V}_{AF}}{n(s+c) v_{AIR}} \right) - 1.64)^2}, \quad (56)$$

$$k \Delta p_{FAN}(\dot{V}_{AF}) = \Delta p_{CH}(\dot{V}_{AF}) \rightarrow \dot{V}_{AF}, \quad (57)$$

$$Re_{avg} = \frac{2 \dot{V}_{AF}}{n(s+c) v_{AIR}}, \quad (58)$$

$$Nu_{avg,lam} = \frac{3.657 (\tanh(2.264 X^{1/3} + 1.7 X^{2/3}))^{-1} + \frac{0.0499}{X} \tanh(X)}{\tanh(2.432 Pr^{1/6} X^{1/6})} \quad \text{with } X = \frac{L}{d_h Re_{avg} Pr}, \quad (59)$$

$$Nu_{avg,turb} = \frac{(8 (0.79 \ln(Re_{avg}) - 1.64)^2)^{-1} (Re_{avg} - 1000) Pr}{1 + 12.7 \sqrt{(8 (0.79 \ln(Re_{avg}) - 1.64)^2)^{-1} (Pr^{2/3} - 1)}} \times \left(1 + \left(\frac{d_h}{L} \right)^{2/3} \right), \quad (60)$$

$$h = \frac{Nu_{avg} \lambda_{AIR}}{d_h}. \quad (61)$$

Table A4. Performance indices and parameter values that result from the optimization of the heat sink of the DAB (geometry with dual-sided base plate, cf. Figure 10). Top inset: result of the optimization, bottom inset: heat sink used in the final prototype converter.

Predef. Values						Calc. Optimal Values		
Optimum	L (mm)	c (mm)	d (mm)	b (mm)	n	s (mm)	t (mm)	k
	99.8	37	6	40.3	14	1.9	1	0.6482
	V_{HS} (L)	V_{CS} (L)	$V_{CS,tot}$ (L)	$R_{th,S-Am}$ (K/W)		$R_{th,S-Am,tot}$ (K/W)		$CSPI$ (W/K·L)
	0.2279	0.2918	0.399	0.7142		0.3571		9.5967
Prototype (used for calc.)	L (mm)	c (mm)	d (mm)	b (mm)	n	s (mm)	t (mm)	k
	99.8	37	6	40.3	13	2.1	1	0.6774
	V_{HS} (L)	V_{CS} (L)	$V_{CS,tot}$ (L)	$R_{th,S-Am}$ (K/W)		$R_{th,S-Am,tot}$ (K/W)		$CSPI$ (W/K·L)
	0.2279	0.2918	0.399	0.7298		0.3649		9.3907

Table A5. Performance indices and parameter values that result from the optimization of the heat sink of the SR (geometry with single-sided base plate, cf. Figure 11). Top inset: result of the optimization, bottom inset: heat sink used in the final prototype converter.

	Predef. Values					Calc. Optimal Values		
	L (mm)	c (mm)	d (mm)	b (mm)	n	s (mm)	t (mm)	k
Optimum	104	10	5	36	14	1.6	1	0.608
	V_{HS} (L)	V_{CS} (L)	$V_{CS,tot}$ (L)		$R_{th,S-Am}$ (K/W)	$R_{th,S-Am,tot}$ (K/W)		$CSPI$ (W/K·L)
	0.0624	0.0767	0.1227		1.4372	1.4372		9.0741
Prototype (used for calc.)	L (mm)	c (mm)	d (mm)	b (mm)	n	s (mm)	t (mm)	k
	104	10	5	36	9	2.5	1.5	0.625
	V_{HS} (L)	V_{CS} (L)	$V_{CS,tot}$ (L)		$R_{th,S-Am}$ (K/W)	$R_{th,S-Am,tot}$ (K/W)		$CSPI$ (W/K·L)
	0.0624	0.0767	0.1227		1.7264	1.7264		7.5542

Appendix A.2. Magnetic Elements of the DAB: Inductors and Transformer

Table A6. Design values for the HF ac-link transformer.

Variable	Value	Description
$N = n_1/n_2$	1	turns ratio
n_1	6	number of turns (primary-side winding)
n_2	6	number of turns (secondary-side winding)
$L_{\sigma,1}$ (μH)	0.76	primary-side leakage inductance
$L_{\sigma,2}$ (μH)	0.76	secondary-side leakage inductance
$L_M = L_2$ (μH)	62.1	magnetizing inductance, which is equal to the secondary-side commutation inductance
l_g (mm)	0.234	air gap length
$n_{s,1}$	700	number of strands in a Litz bundle (primary-side winding)
$n_{s,2}$	700	number of strands in a Litz bundle (secondary-side winding)
$d_{s,1}$ (μm)	80	strand diameter (primary-side winding)
$d_{s,2}$ (μm)	80	strand diameter (secondary-side winding)
$N_{par,1}$	2	number of paralleled Litz bundles (primary-side winding)
$N_{par,2}$	2	number of paralleled Litz bundles (secondary-side winding)
-	no	interleaving of the windings
-	N97	core material
-	EELP58	core type/combination
-	2	number of stacked core combinations
$l_{core,tot}$ (m)	0.076	total core length
V_{trans} (L)	0.143	boxed volume of the transformer

Table A7. Design values for the external series inductor L_{ext} .

Variable	Value	Description
n_{ind}	4	number of turns
L_{ind} (μH)	12.2	inductance value
l_g (mm)	0.603	air gap length
n_s	1458	number of strands in a Litz bundle
d_s (μm)	71	strand diameter
N_{par}	1	number of paralleled Litz bundles
-	N97	core material
-	EELP38	core type/combination
-	3	number of stacked core combinations
$l_{core,tot}$ (m)	0.076	total core length
V_{ind} (L)	0.0661	boxed volume of the inductor

Table A8. Design values for the primary-side commutation inductor L_1 . Both the values for the “prot.” and the “opt.” design of L_1 are listed.

Variable	Value, “opt.”	Value, “prot.”	Description
n_{ind}	13	6	number of turns
L_{ind} (μH)	62.1	62.1	inductance value
l_g (mm)	0.92	0.234	air gap length
n_s	184	700	number of strands in a Litz bundle
d_s (μm)	50	80	strand diameter
N_{par}	2	2	number of paralleled Litz bundles
-	N97	N97	core material
-	EELP32	EELP58	core type/combination
-	3	2	number of stacked core combinations
$l_{\text{core,tot}}$ (m)	0.061	0.076	total core length
V_{ind} (L)	0.0358	0.143	boxed volume of the inductor

Appendix A.3. EMC Input Filter

Table A9. Differential mode (DM) EMC input filter components.

Component	Value	Quantity	Specification
Filter Stage 1			
$L_{\text{DM1}}/L_{\text{DM1,c}}$, coupled inductor	34.6/1.64 μH	2	Magnetics, High Flux 60, CO58083A2, 23:5 turns, 11 AWG wire
$L_{\text{DM1,d}}$, inductor	6.9 μH	2	Magnetics, MPP60, CO55351A2, 13 turns, 11 AWG wire
C_{DM1} , X2 capacitor (MKP)	13.2 μF	6 in par.	EPCOS-B32923E3225, 2.2 μF, 305 V _{ac}
$R_{\text{DM1,d}}$, SMD resistor	0.19 Ω	2 × 2 in par.	0.38 Ω-1 W
Filter Stage 2			
$L_{\text{DM2}}=L_{\text{mains}}$	0 ... 300 μH	-	Mains inductance
C_{DM2} , X2 capacitor (MKP)	1 μF	1	EPCOS-B32923C3105, 1 μF, 305 V _{ac}
$C_{\text{DM2,d}}$, X2 capacitor (MKP)	0.47 μF	1	EPCOS-B32922C3474, 0.47 μF, 305 V _{ac}
$R_{\text{DM2,d}}$, SMD resistor	20 Ω	2 in ser.	10 Ω-0.33 W

Table A10. Common mode (CM) EMC input filter components.

Component	Value	Quantity	Specification
AC-Side: Filter Stage 1			
L_{CM1} , inductor	0.34 mH @ 100 kHz	1	Vacuumschmelze VAC, VITROPERM 500F, L2020-W409, 2 × 5 turns, 11 AWG wire
$C_{\text{CM1,A}}$, Y2 capacitor (MKP)	6.8 nF	2 × 1	EPCOS-B32021A3682, 6.8 nF, 300 V _{ac}
$C_{\text{CM1,B}}$, Y2 capacitor (MKP)	2.2 nF	2 × 1	EPCOS-B32021A3222, 2.2 nF, 300 V _{ac}
AC-Side: Filter Stage 2			
L_{CM2} , inductor	0.34 mH @ 100 kHz	1	Vacuumschmelze VAC, VITROPERM 500F, L2020-W409, 2 × 5 turns, 11 AWG wire
C_{CM2} , Y2 capacitor (MKP)	10 nF	2 × 1	EPCOS-B32022A3103, 10 nF, 300 V _{ac}
AC-Side: Filter Stage 3			
C_{CM3} , Y2 capacitor (MKP)	1 nF	2 × 1	EPCOS-B32021A3102, 1 nF, 300 V _{ac}
DC-Side			
C_{MP} , Y2 capacitor (MKP)	13.6 nF	2 × 2	EPCOS-B32021A3682, 6.8 nF, 300 V _{ac}

Appendix B. Supplement to Section 5

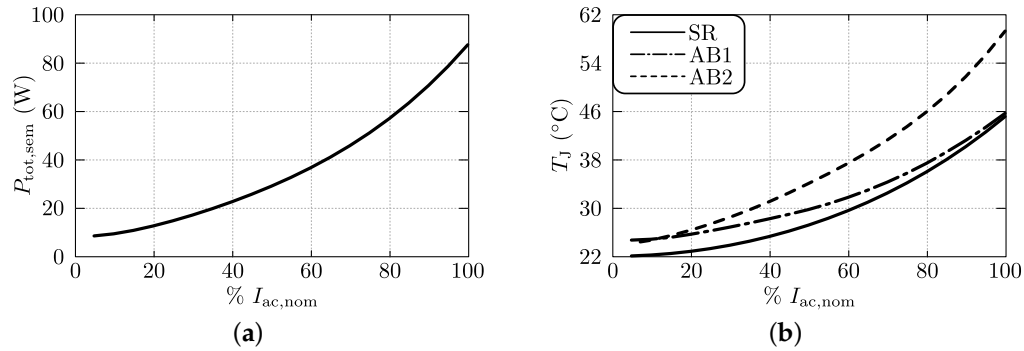


Figure B1. (a) Calculated total losses generated by all semiconductors of the DAB and SR; (b) Junction temperatures of all semiconductors, i.e., the switches of active bridge 1 (DAB), of active bridge 2 (DAB), and of the SR.

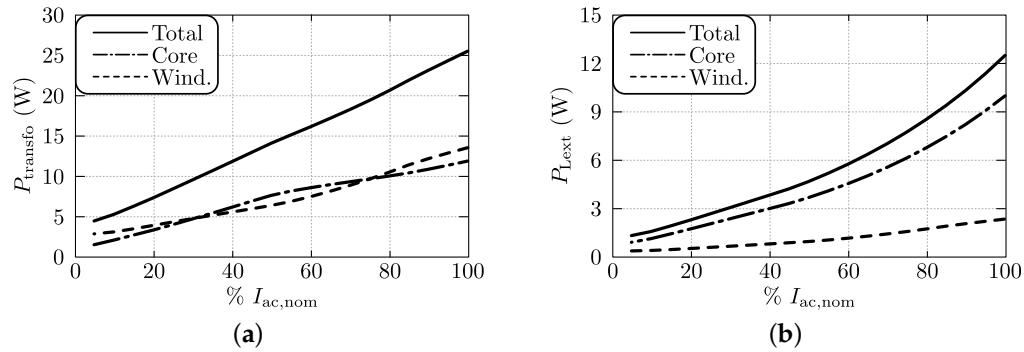


Figure B2. Calculated losses of (a) the HF ac-link transformer and (b) the external series inductor L_{ext} .

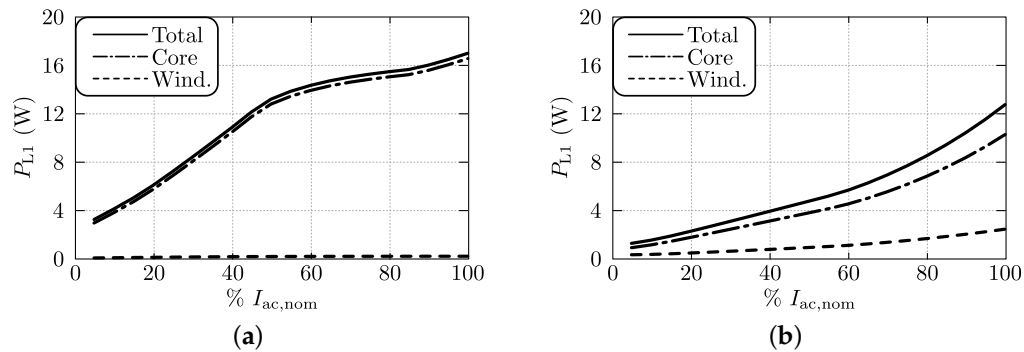


Figure B3. Calculated losses of the commutation inductor L_1 implemented according to (a) design “prot.” (prototype converter) and (b) the improved design “opt.” (further optimized).

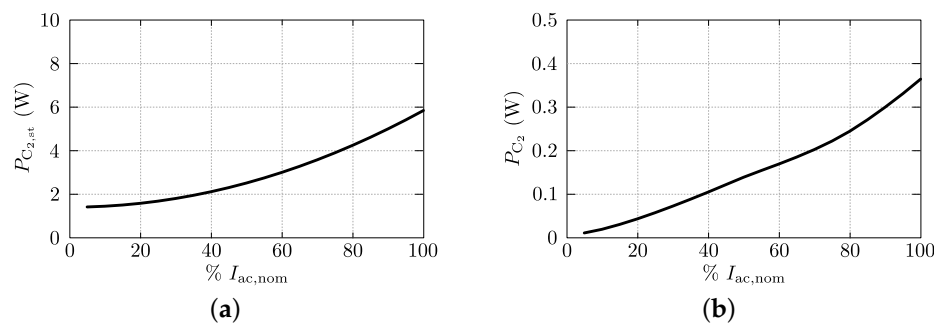


Figure B4. (a) Calculated total losses of the LF output filter capacitors $C_{2,st}$; (b) Calculated total losses of the HF output filter capacitors C_2 .

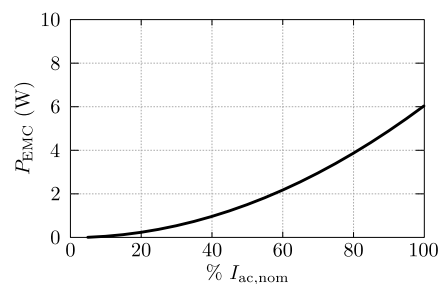


Figure B5. Calculated total losses of the EMC input filter.

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