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A High-Precision Control for a ZVT PWM Soft-Switching Inverter to Eliminate the Dead-Time Effect

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Abstract: Attributing to the advantages of high efficiency, low electromagnetic interference (EMI) noise and closest to the pulse-width-modulation (PWM) converter counterpart, zero-voltage-transition (ZVT) PWM soft-switching inverters are very suitable for high-performance applications. However, the conventional control algorithms intended for high efficiency generally results in voltage distortion. Thus, this paper, for the first time, proposes a high-precision control method to eliminate the dead-time effect through controlling the auxiliary current in the auxiliary resonant snubber inverter (ARSI), which is a typical ZVT PWM inverter. The dead-time effect of ARSI is analyzed, which is distinguished from hard-switching inverters. The proposed high-precision control is introduced based on the investigation of dead-time effect. A prototype was developed to verify the effectiveness of the proposed control. The experimental results shows that the total harmonic distortion (THD) of the output current of the ARSI can be reduced compared with that of the hard-switching inverter, because the blanking delay error is eliminated. The quality of the output current and voltage can be further improved by utilizing the proposed control method.

Keywords: Zero-voltage-transition (ZVT); soft-switching; auxiliary resonant snubber inverter (ARSI); high precision; dead-time effect

1. Introduction

In high-performance applications, the high switching frequency is the least requirement for power inverters to achieve high dynamical response and high precision [1]. However, hard-switching power inverters suffer from large switching loss and severe electromagnetic interference (EMI) as the switching frequency increases [2,3].

In order to solve the problems of large switching loss and severe EMI in a power inverter with high switching frequency, the use of the soft-switching technique is one of the best options. It utilizes auxiliary components to limit the di/dt or dv/dt during the commutation period, and thus reduces the overlap between the voltage and current of semiconductor switches. To date, a variety of soft-switching DC-AC topologies have been proposed [4–22]. Among them, the zero-voltage transition (ZVT) pulse-width-modulation (PWM) inverters is a typical soft-switching inverters. An auxiliary circuit connected in parallel with the main power path is employed in ZVT PWM inverters, which only operate for a short interval before and after the commutation period of the main switches. This makes ZVT inverters the closest to the PWM converter counterpart. In addition, ZVT PWM inverters have the advantages of operating with soft switching within a wide load range and low voltage and current stresses over other types of soft-switching inverters.

Several topologies of the ZVT PWM inverters have been proposed. The auxiliary resonant commutated pole inverter (ARCPI) has been proposed with two auxiliary switches per phase [4,5].

The ARCPI can meet the demand for high efficiency and low voltage and current stresses. However, the major drawback is the existence of the split capacitors, which cause the problems of capacitor charge balance. The auxiliary resonant snubber inverter (ARSI) has been proposed to eliminate the split capacitors, but the three-phase topology cannot utilize the conventional space-vector-pulse-width modulation (SVPWM) [6,7]. Thus, they are more suitable for permanent magnet brushless DC motors instead of all types of motors. The single-phase topology is very attractive with only two auxiliary switches and well fit to the conventional PWM. Meanwhile, the ZVT inverter using coupled magnetics has been proposed to eliminate the split capacitors [8–10]. However, these topologies need coupled inductors and a large number of auxiliary switches, which increase the cost and difficulty of the circuit realization. The ZVT PWM converter has been synthesized and summarized in [11,12].

Although each topology has its drawbacks, the ZVT inverters are widely adopted due to its high efficiency, low EMI noise, available to utilize PWM and low voltage and current stresses. However, the main problem in high-performance applications is the dead-time effect, which brings about distortion and nonlinear voltage error. Extensive studies have been completed on the elimination [13,14] and compensation [15–17] of the dead-time effect, but they are focused on hard-switching inverters. With the additional auxiliary circuit, the auxiliary current is a new controllable variable in the ZVT PWM inverters compared with hard-switching inverters. Just as the DC-link soft-switching inverter, the zero-voltage notches can influence the output and increase the nonlinearity [18]. The auxiliary current can also affect the output voltage and current of ZVT PWM inverters, which makes the dead-time effect quite different from that of hard-switching inverters. Besides, the conventional control of ZVT PWM inverters including the fix-timing control [19,20] and variable-timing control [20–22] aim to improve the efficiency and leads to voltage distortion in turn.

Motivated by the dead-effect elimination of hard-switching inverters and lack of studies about the impact of auxiliary current on linearity of a ZVT PWM soft-switching inverter, this paper analyzes the dead-time effect of a typical example of ZVT PWM soft-switching inverters—ARSI. A high-precision control by controlling the auxiliary current to eliminate the dead-time effect is proposed. A prototype was developed to verify the effectiveness of the proposed control method.

2. Commutation of the Auxiliary Resonant Snubber Inverter

Figure 1 depicts the single-phase ARSI topology analyzed in this paper, which consists of a standard H-bridge inverter, resonant capacitors and an auxiliary circuit. The proper operation of the auxiliary switches S_{r1} and S_{r2} can create zero-voltage-switching (ZVS) condition for the main switches S_1–S_4. Meanwhile, the auxiliary switches can realize zero-current switching (ZCS).

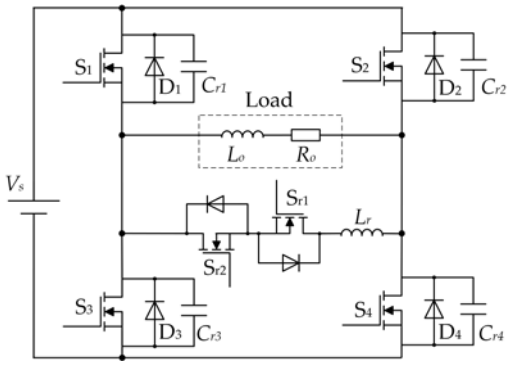

Figure 1. The circuit of auxiliary resonant sunbber inverter.

The detailed circuit operation will be analyzed in the case of positive output current. In the following, we assume that:

1) All components and devices are ideal;
2) The gate signals of the MOSFETs are ideal square-wave;
3) The load L_o is large enough to maintain the load current constant during each switching cycle.

One switching cycle of the operating stages and the operating waveforms are, respectively, shown in Figures 2 and 3, where v_{ds} is the drain-source voltage of a MOSFET, i_d is the drain current of a MOSFET, v_g is the practical gate signal with dead-time, $v_{g,id}$ is the ideal gate signal, i_{Lr} is the resonant inductor current, v_{ab} is the practical pole voltage across the load with dead-time, $v_{ab,id}$ is the ideal pole voltage across the load and v_{err} is the voltage error between v_{ab} and $v_{ab,id}$.

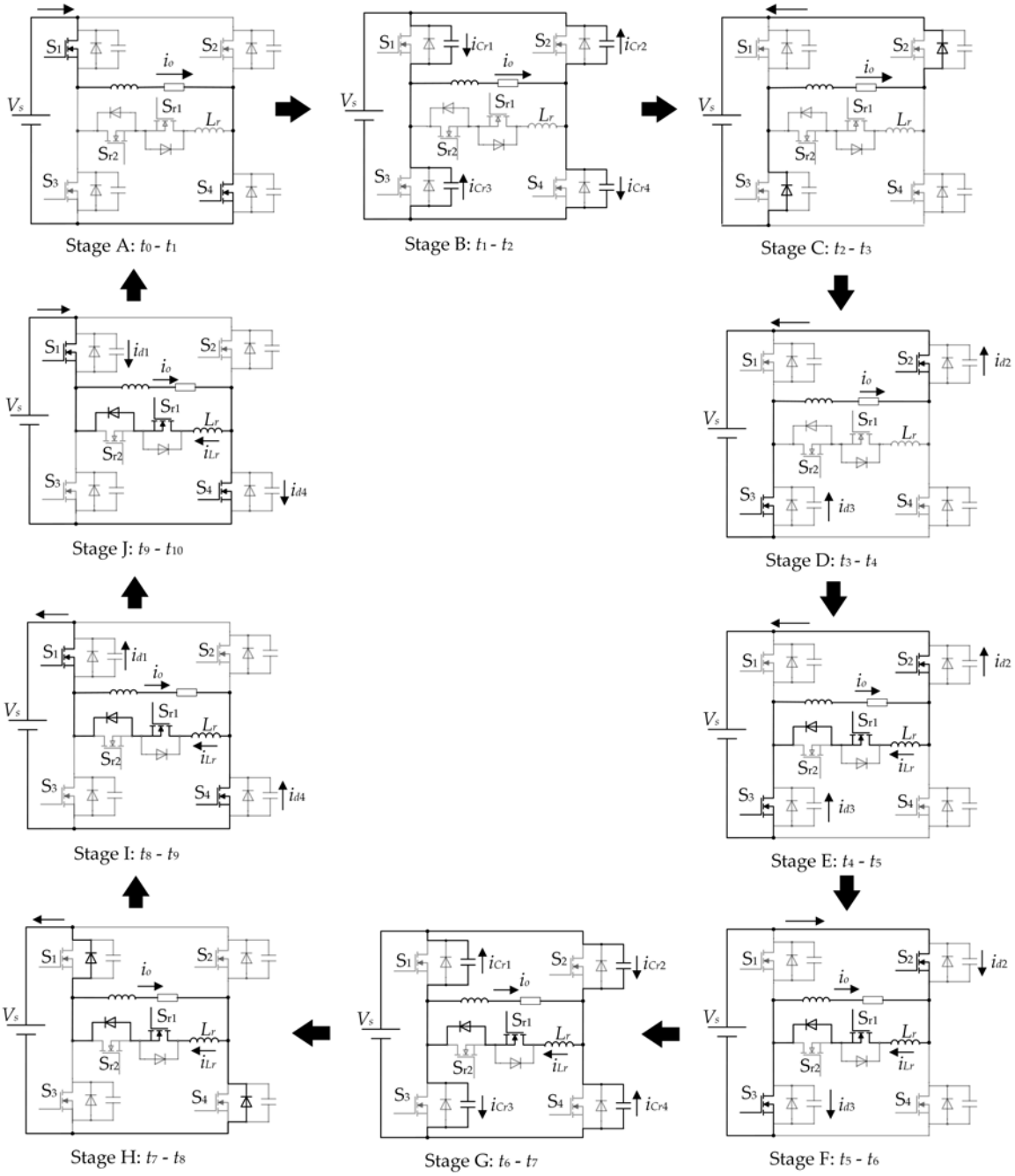

Figure 2. The operating stage when the output current is positive.

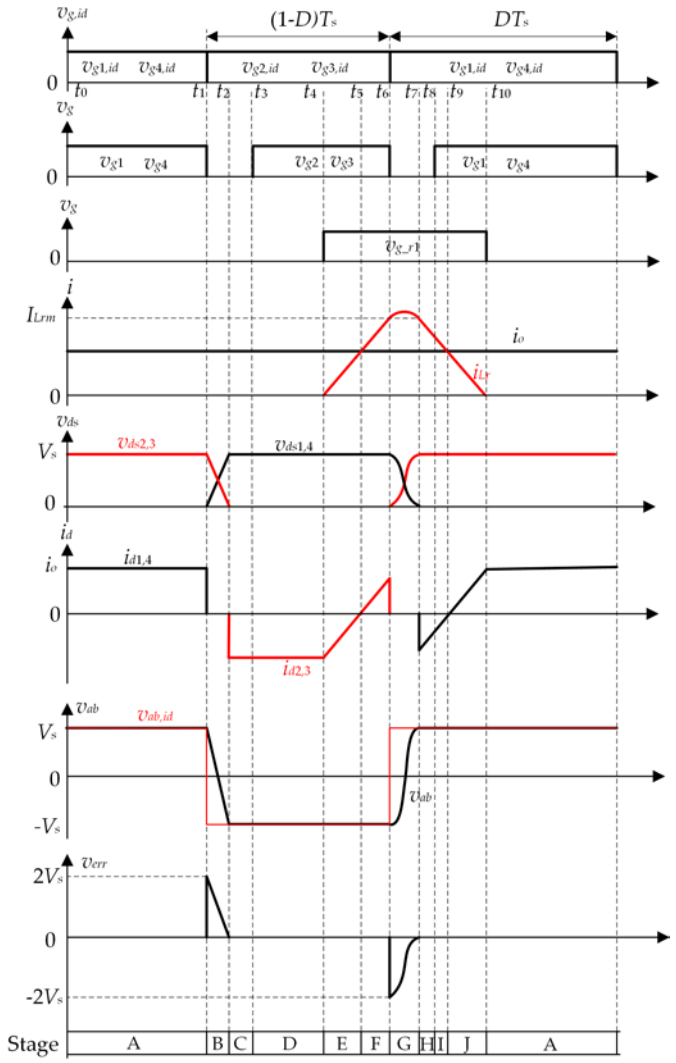

Figure 3. The key waveforms of the ARSI when the output current is positive.

1) Stage A (t_0–t_1): The main switches S_1 and S_4 fully conducts the load current and S_2 and S_3 are in the off state. Therefore, the pole voltage v_{ab} is expressed as follows:

$$v_{ab}(t) = V_s \tag{1}$$

2) Stage B (t_1–t_2): Due to the existence of the resonant capacitors C_{r1} and C_{r4}, v_{ds1} and v_{ds4} increase very slowly. Therefore, S_1 and S_4 are turned off at ZVS at t_1. Then, the load begins resonating with four resonant capacitors. C_{r2} and C_{r3} are discharged and C_{r1} and C_{r4} are charged due to the positive load current. The drain-source voltages of MOSFETs can be calculated as follows:

$$v_{ds1}(t) = v_{ds4}(t) = \frac{i_o}{2C_r}(t - t_1) \tag{2}$$

$$v_{ds2}(t) = v_{ds3}(t) = V_s - \frac{i_o}{2C_r}(t - t_1) \tag{3}$$

The pole voltage can be obtained as follows:

$$v_{ab}(t) = v_{ds3}(t) - v_{ds4}(t) = V_s - \frac{i_o}{C_r}(t - t_1) \tag{4}$$

When v_{ds2} and v_{ds3} decrease to zero at t_2, the resonant period is over. The resonant time is calculated as follows:

$$\Delta t_{12} = t_2 - t_1 = \frac{2C_r V_s}{i_o} \tag{5}$$

3) Stage C and D (t_2–t_4): After the v_{ds2} and v_{ds3} decrease to zero, the current freewheels through the body diodes D_2 and D_3 and v_{ds2} and v_{ds3} are clamped to zero. Therefore, S_2 and S_3 are turned on at ZVS condition at t_3. After t_3, the current is diverted from D_2 and D_3 to the channels of S_2 and S_3. During these stages, the pole voltage v_{ab} can be written as follows:

$$v_{ab}(t) = -V_s \tag{6}$$

4) Stage E and F (t_4–t_6): S_{r1} is turned on at t_4 at ZCS condition, resulting in charging the resonant inductor with voltage V_s. The resonant inductor current can be calculated as follows:

$$i_{Lr}(t) = \frac{V_s}{L_r}(t - t_4) \tag{7}$$

At t_5, the resonant inductor current i_{Lr} equals the load current i_o. After t_5, S_2 and S_3 work from third quadrant to first quadrant because i_{Lr} is larger than i_o. To obtain the resonant inductor current I_{Lrm}, the charging time can be obtained according to Equation (7).

$$\Delta t_{46} = t_6 - t_4 = \frac{I_{Lrm} L_r}{V_s} \tag{8}$$

During this stage, the pole voltage is as follows:

$$v_{ab}(t) = -V_s \tag{9}$$

5) Stage G (t_6–t_7): The resonant inductor is charged to I_{Lrm} at t_6. Meanwhile, S_2 and S_3 are turned off at ZVS condition at t_6. Thus, the resonant inductor begins resonating with four resonant capacitors. C_{r1} and C_{r4} are discharged and C_{r2} and C_{r3} are charged. The equations during this resonant period can be written as follows.

$$v_{ds1}(t) + v_{ds3}(t) = V_s \tag{10}$$

$$i_{cr1}(t) = C_r \frac{dv_{ds1}(t)}{dt} \tag{11}$$

$$i_{cr3}(t) = C_r \frac{dv_{ds3}(t)}{dt} \tag{12}$$

$$i_{cr1}(t) + i_{Lr}(t) = i_o + i_{cr3}(t) \tag{13}$$

$$v_{ds1}(t) - v_{ds3}(t) = L_r \frac{di_{Lr}(t)}{dt} \tag{14}$$

Therefore, the inductor current and drain-source voltages of the main MOSFETs can be obtained as follows according to Equations (10)–(14).

$$i_{Lr}(t) = (I_{Lrm} - i_o)\cos\omega_A (t - t_6) + \frac{V_s}{Z_A}\sin\omega_A (t - t_6) + i_o \tag{15}$$

$$v_{ds1}(t) = v_{ds4}(t) = \frac{1}{2}V_s + \frac{1}{2}V_s\cos\omega_A (t - t_6) - \frac{1}{2}Z_A (I_{Lrm} - i_o)\sin\omega_A (t - t_6) \tag{16}$$

$$v_{ds2}(t) = v_{ds3}(t) = \frac{1}{2}V_s - \frac{1}{2}V_s\cos\omega_A (t - t_6) + \frac{1}{2}Z_A (I_{Lrm} - i_o)\sin\omega_A (t - t_6) \tag{17}$$

where $\omega_A = \frac{1}{\sqrt{L_r C_r}}$, $Z_A = \sqrt{\frac{L_r}{C_r}}$, and I_{Lrm} is the initial resonant inductor current.

The pole voltage can be obtained as follows:

$$v_{ab}(t) = v_{ds3}(t) - v_{ds4}(t) = Z_A(I_{Lrm} - i_o)\sin\omega_A(t - t_6) - V_s\cos\omega_A(t - t_6) \tag{18}$$

For $v_{ds1}(t) = 0$, the resonant time can be calculated as:

$$\Delta t_{67} = t_7 - t_6 = \frac{2}{\omega_A}\arcsin\frac{V_s}{\sqrt{V_s^2 + Z_A^2(I_{Lrm} - i_o)^2}} \tag{19}$$

At the end of the resonant time t_7, i_{Lr} can be obtained from Equations (15) and (19).

$$i_{Lr}(t_7) = I_{Lrm} \tag{20}$$

6) Stage H–J (t_7–t_{10}): After the voltages v_{ds1} and v_{ds4} decrease to zero, the body diodes D_1 and D_4 conduct the current so that v_{ds1} and v_{ds4} are clamped to zero. Therefore, S_1 and S_4 are turned on at the ZVS condition at t_8 and take over the load current. During these stages, the pole voltage can be obtained.

$$v_{ab}(t) = V_s \tag{21}$$

Owing to the positive pole voltage, the resonant inductor is discharged. During the discharging period, i_{Lr} can be calculated as follows:

$$i_{Lr}(t) = I_{Lrm} - \frac{V_s}{L_r}(t - t_7) \tag{22}$$

After the current i_{Lr} decreases to zero, S_{r1} are turned off at ZCS condition. The discharging time can be obtained as follows according to Equation (22).

$$\Delta t_{710} = t_{10} - t_7 = \frac{I_{Lrm}L_r}{V_s} \tag{23}$$

3. Dead-Time Effect and Voltage Error

The duty ratio and output voltage are respectively the direct input and output of the inverters. Thus, the linearity of inverters is related the relationship duty ratio and output voltage.

From the analysis in Section 2, the pole voltage can be obtained in one switching cycle (t_0–t_{10}) as follows according to Equations (1), (4), (6), (9), (18) and (21).

$$v_{ab} = \begin{cases} V_s - \frac{i_o}{C_r}(t - t_1) & t_1 \leqslant t \leqslant t_2 \\ -V_s & t_2 < t < t_6 \\ Z_A(I_{Lrm} - i_o)\sin\omega_A(t - t_6) - V_s\cos\omega_A(t - t_6) & t_6 \leqslant t \leqslant t_7 \\ V_s & t_0 \leqslant t < t_1 \text{ or } t_7 < t < t_{10} \end{cases} \tag{24}$$

The voltage error v_{err} between the practical pole voltage and the ideal pole voltage can be obtained as follows:

$$v_{err} = v_{ab} - v_{ab,id} = \begin{cases} 2V_s - \frac{i_{Lf\_u}}{C_r}(t - t_1) & t_1 \leqslant t \leqslant t_2 \\ -V_s - V_s\cos\omega_A(t - t_6) + Z_A(I_{Lrm} - i_o)\sin\omega_A(t - t_6) & t_6 \leqslant t \leqslant t_7 \\ 0 \qquad t_0 \leqslant t < t_1 \text{ or } t_2 < t < t_6 \text{ or } t_7 < t < t_{10} \end{cases} \tag{25}$$

The average voltage error in a switching cycle can be obtained as follows:

$$V_{err} = \frac{1}{T_s}\int_{t_0}^{t_{10}} v_{err}dt = \frac{\Delta t_{12} - \Delta t_{67}}{T_s}V_s \tag{26}$$

The average output voltage can be calculated as follows:

$$V_o = \frac{1}{T_s}\int_{t_0}^{t_{10}} v_{ab}dt = (2D-1)V_s + \frac{\Delta t_{12} - \Delta t_{67}}{T_s}V_s = V_{ab,id} + V_{err} \tag{27}$$

The output voltage is related to not only the duty ratio but also the commutation times according to Equation (27). The nonlinearity of the ARSI is caused by the dead-time effect.

Figure 4 shows when the output current is positive, the dead-time effect of the hard-switching inverter and the ARSI without considering the turn-on and turn-off delay. Due to the finite rise- and fall-times of voltage caused by the output capacitors of MOSFETs, the rise- and fall-errors occur in the hard-switching inverter. Additionally, the dead-time effect also causes the blanking delay error which is the main error source in the hard-switching inverter [16]. As for the ARSI, only the commutation stages (t_1–t_2) and (t_6–t_7) lead to the voltage errors according to Equation (25). Although the rise- and fall-errors are enlarged in the ARSI due to the additional resonant capacitors compared with the hard-switching inverter, the blanking delay error that caused by the blanking delay times (t_2–t_3) and (t_6–t_7) is eliminated, because the body diodes of the next turn-on MOSFETs conduct the current during the blanking delay time. Therefore, the dead-time effect is reduced in the ARSI.

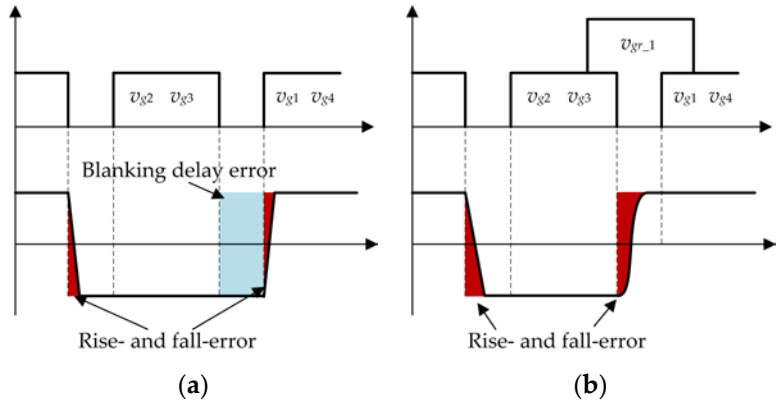

Figure 4. The pole voltage and voltage error of the ARSI and hard-switching inverters in a switching cycle when the output current is positive: (**a**) hard-switching inverters and (**b**) ARSI.

In one switching cycle, there are two commutations among the main switches. The PTN (positive to negative) commutation is the commutation that the current is diverted from positive switches (S_1 and S_4) to negative switches (S_2 and S_3), while the NTP (negative to positive) commutation is the commutation that the current is diverted from negative switches (S_2 and S_3) to positive switches. In Figure 3, (t_1–t_2) is PTN commutation and (t_6–t_7) is NTP commutation.

According to Equation (25), the average voltage error of each commutation in a switching cycle can be obtained as follows:

$$V_{err,PTN} = \frac{1}{T_s}\int_{t_1}^{t_2} v_{err}dt = \frac{\Delta t_{12}}{T_s}V_s = \frac{t_{rf,PTN}}{T_s}V_s \tag{28}$$

$$V_{err,NTP} = \frac{1}{T_s}\int_{t_6}^{t_7} v_{err}dt = -\frac{\Delta t_{67}}{T_s}V_s = -\frac{t_{rf,NTP}}{T_s}V_s \tag{29}$$

where $t_{rf,PTN}$ is the commutation time of PTN commutation and $t_{rf,NTP}$ is the commutation time of NTP commutation.

When the output current is positive, the S_2 and S_3 realize natural ZVS (NZVS) without the operation of auxiliary circuit during the PTN commutation, while S_1 and S_4 realize auxiliary ZVS (NZVS) with the proper operation of auxiliary circuit during the NTP commutation. According

to Equations (28) and (29), the PTN commutation introduce positive voltage error and the NTP commutation create negative voltage error in conclusion. The magnitude of the voltage error is proportional to the commutation time t_{rf} regardless of whether the main switches realize NZVS or AZVS. Table 1 shows the average voltage errors of the PTN and NTP commutations. The analysis above is discussed in the case of positive output current, but the conclusion can also be used in the condition of negative output current.

Table 1. The average voltage errors of PTN and NTP commutations.

Type	PTN Commutation	NTP Commutation
Voltage error V_{err}	$\frac{V_s}{T_s} t_{rf}$	$-\frac{V_s}{T_s} t_{rf}$

The commutation time t_{rf} is related to the realization of the ZVS type. If the main switches achieve NZVS, the commutation time can be obtained according to Equation (5).

$$t_{rf,NZVS} = \left| \frac{2C_r V_s}{i_o} \right| \tag{30}$$

To achieve AZVS with the proper operation of the auxiliary circuit, the commutation time can be obtained according to Equation (19).

$$t_{rf,AZVS} = \left| \frac{2}{\omega_A} \arcsin \frac{V_s}{\sqrt{V_s^2 + Z_A^2 I_{boost}^2}} \right| \tag{31}$$

where I_{boost} is the initial resonant current which is the current to charge and discharge the resonant capacitors $I_{boost} = I_{Lrm} - i_o$ and I_{Lrm} is the auxiliary current at the beginning of the resonant time.

According to Equations (30) and (31), the commutation time can be summarized in Table 2. To achieve NZVS, the commutation time is related to the load current. To achieve AZVS, the commutation time is related to the initial resonant current I_{boost}.

Table 2. The commutation time with different type of ZVS.

Type	NZVS	AZVS
Commutation time t_{rf}	$\left\| \frac{2C_r V_s}{i_o} \right\|$	$\left\| \frac{2}{\omega_A} \arcsin \frac{V_s}{\sqrt{V_s^2 + Z_A^2 I_{boost}^2}} \right\|$

In a switching cycle, one commutation aims to realize NZVS of the main switches, while the other commutation aims to achieve AZVS. When the output current is positive, NZVS of the main switches can be achieved during the PTN commutation. When output current is negative, NZVS can only be achieved during the NTP commutation. The voltage error can be obtained according to Tables 1 and 2.

$$V_{err} = \begin{cases} \frac{V_s}{T_s} \left(\left| \frac{2C_r V_s}{i_o} \right| - \left| \frac{2}{\omega_A} \arcsin \frac{V_s}{\sqrt{V_s^2 + Z_A^2 I_{boost}^2}} \right| \right) & i_o > 0 \\ \frac{V_s}{T_s} \left(\left| \frac{2}{\omega_A} \arcsin \frac{V_s}{\sqrt{V_s^2 + Z_A^2 I_{boost}^2}} \right| - \left| \frac{2C_r V_s}{i_o} \right| \right) & i_o < 0 \end{cases} \tag{32}$$

Figure 5 shows the pole voltage and voltage error in a switching cycle. The PTN commutation introduces positive voltage error, while the NTP commutation creates negative voltage error. The NZVS results in linear changing of v_{ab} and AZVS results in nonlinear changing of v_{ab}.

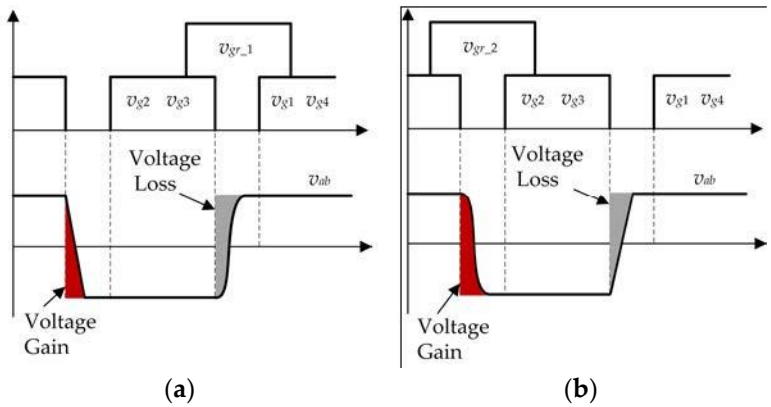

Figure 5. The pole voltage and voltage error in a switching cycle: (**a**) $i_o > 0$ and (**b**) $i_o < 0$.

4. Control Strategy

4.1. Proposed Control Strategy

The dead-time effect causes the nonlinearity of the ARSI, which results in nonlinear relationship between the output voltage and the duty ratio. This leads to voltage error. As in the analysis in Section 2, the voltage error is proportional to the commutation time. To achieve NZVS, the commutation time related to the load current is uncontrollable. However, to achieve AZVS, the commutation time related to the initial resonant current can be controlled by the auxiliary current. Therefore, the voltage error of AZVS can be controlled. Under the realization of "AZVS + NZVS" in a switching cycle, the voltage error is shown in Equation (32). For $V_{err}(t) = 0$ in Equation (32), the initial resonant current I_{boost} can be obtained as follows.

$$I_{boost} = \frac{V_s}{Z_A \tan \frac{\omega_A C_r V_s}{|i_o|}} \tag{33}$$

If the initial resonant current can be controlled to meet the requirement of Equation (33), the voltage error caused by the dead time can be eliminated. The output voltage can be obtained as follows.

$$V_o = (2D - 1)V_s \tag{34}$$

The output voltage is proportional to the duty ratio when the current I_{boost} meet Equation (33). However, when the load current is small enough, the commutation time of NZVS may be longer than the dead time t_{dead} according to Equation (30). The NZVS of the main switches fails, which is shown in Figure 6. This leads to incorrectness of Equation (32). Thus, the initial resonant current meeting Equation (33) cannot eliminate the voltage error when the output current is small enough.

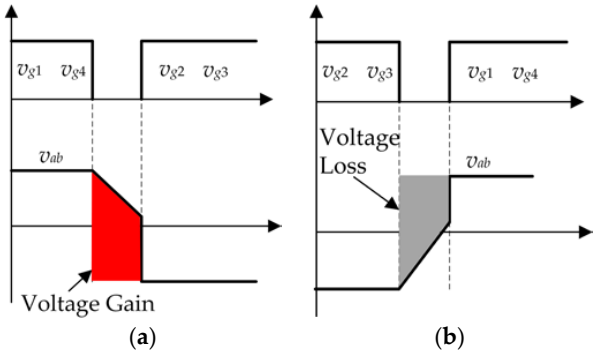

Figure 6. NZVS fails when the load current is small enough: (**a**) $i_o > 0$ and (**b**) $i_o < 0$.

To achieve ZVS from zero load to full load and eliminate the dead-time effect, the realization of "AZVS + AZVS", which means all the main switches realize AZVS in a switching cycle, is adopted. According to Tables 1 and 2, the voltage error can be obtained as follows:

$$V_{err} = \frac{V_s}{T_s}\left(\left|\frac{2}{\omega_A}\arcsin\frac{V_s}{\sqrt{V_s^2 + Z_A^2 I_{boost,PTN}^2}}\right| - \left|\frac{2}{\omega_A}\arcsin\frac{V_s}{\sqrt{V_s^2 + Z_A^2 I_{boost,NTP}^2}}\right|\right) \tag{35}$$

For $V_{err} = 0$ in Equation (35), the initial resonant current can be obtained as follows:

$$I_{boost,PTN} = I_{boost,NTP} \tag{36}$$

If the initial resonant current meets Equation (36), the voltage error caused by the dead time can also be eliminated with the realization of "AZVS + AZVS".

Table 3 shows the realization type of ZVS from zero load to full load. When $|i_o| > I_{th}$, "AZVS + NZVS" is adopted. The initial resonant current is controlled to meet Equation (33). When $|i_o| \leqslant I_{th}$, "AZVS + AZVS" is adopted. The initial resonant current must meet the Equation (36). In this case, the voltage error caused by the dead-time effect can be eliminated from zero load to full load, resulting in a linear relationship between the output voltage and the duty ratio according to Equation (34).

Table 3. The realization type of ZVS from zero load to full load.

Type	PTN Commutation	NTP Commutation
$i_o > I_{th}$	NZVS	AZVS (S_{r1})
$-I_{th} \leqslant i_o \leqslant I_{th}$	AZVS (S_{r2})	AZVS (S_{r1})
$i_o < -I_{th}$	AZVS (S_{r2})	NZVS

Meanwhile, to ensure the success of NZVS, threshold current I_{th} should meet the requirement as follows so that the ZVS can succeed from zero load to full load.

$$I_{th} > \frac{2C_r V_s}{t_{dead}} \tag{37}$$

4.2. Conventional Control Strategy

The conventional control involves two methods, fix-timing control and variable-timing control. Although fix-timing control is simple to be implemented, it has the difficulties of achieving ZVS at every load current and it also leads large conduction loss [19,20]. These disadvantages limit the application of fixed-timing control in ZVT inverters. The variable-timing control utilizes the instantaneous load current to generate the gate signal of the auxiliary switches, which can achieve soft-switching for a wide load range and reduce the conduction loss [20–22]. These advantages make variable-timing control be widely used. Therefore, only the variable-timing control is discussed below.

The initial resonant current I_{boost} is selected to be as low as possible over the entire load range and I_{boost} is kept constant in variable-timing control. Therefore, the voltage error of the variable-timing control can be obtained as follows.

$$V_{err,VTC} = \begin{cases} \frac{V_s}{T_s}\left(\left|\frac{2C_r V_s}{i_o}\right| - \left|\frac{2}{\omega_A}\arcsin\frac{V_s}{\sqrt{V_s^2+Z_A^2 I_{boost}^2}}\right|\right) & i_o > I_{th} \\ 0 & -I_{th} \leqslant i_o \leqslant I_{th} \\ \frac{V_s}{T_s}\left(\left|\frac{2}{\omega_A}\arcsin\frac{V_s}{\sqrt{V_s^2+Z_A^2 I_{boost}^2}}\right| - \left|\frac{2C_r V_s}{i_o}\right|\right) & i_o < -I_{th} \end{cases} \tag{38}$$

Due to constant I_{boost}, the error occurs in the output voltage. Figure 7 shows the voltage error according to Equation (38) with the parameters in Table 4. The voltage error only occurs when "AZVS + NZVS" is adopted. A large voltage error about 1.2 V occurs at the threshold current 3 A. As the output current increases, the voltage error decreases first and then increases.

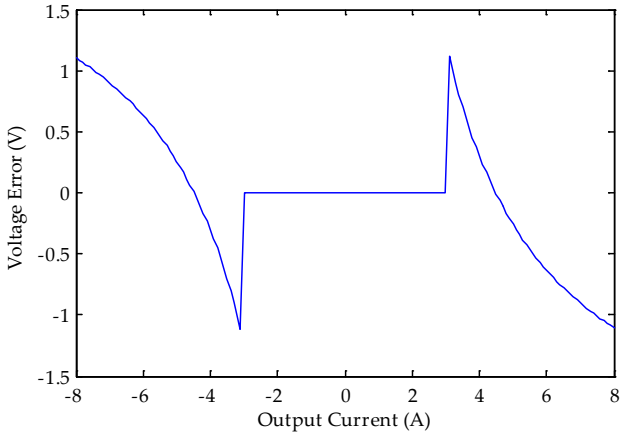

Figure 7. The average voltage error vs. output current with conventional variable-timing control.

Table 4. The parameters of the circuit.

Parameter	Value
DC voltage V_s	80 V
Switching frequency f_s	200 kHz
Dead time t_{dead}	0.5 µs
Load	3.7 Ω, 4.87 mH
Resonant inductor L_r	4.4 µH
Resonant capacitor C_r	4.7 nF
Threshold current I_{th}	3 A
I_{boost}	4 A

4.3. Realization of the Proposed Control Strategy

In the proposed control strategy of Section IV, the initial resonant current I_{boost} can be controlled to eliminate the voltage error caused by the dead-time effect. With the proper conduction of the auxiliary switches S_{r1} and S_{r2}, the initial resonant inductor current I_{Lrm} can be controlled to obtain the required I_{boost}. During the conduction period of S_2 and S_3, S_{r1} is turned on to obtain a positive I_{boost} to achieve AZVS of S_1 and S_4. Furthermore, during the conduction period of S_1 and S_4, S_{r2} is turned on to obtain a negative I_{boost} to realize AZVS of S_2 and S_3. Thus, to obtain the required I_{boost}, the resonant inductor must be charged to I_{Lrm} at the beginning of the resonant time as follows.

$$I_{Lrm} = \begin{cases} I_{boost} + i_o & for \ \ S_{r1} \\ I_{boost} - i_o & for \ \ S_{r2} \end{cases} \tag{39}$$

where I_{boost} and I_{Lrm} is always positive without including the direction.

Figure 8 shows the auxiliary current during the charging time t_{ch}, commutation time t_{rf} and discharging time t_{dch}. The charging time determines the initial resonant inductor current I_{Lrm}. During the charging period, as in stages E and F in Figure 3, the inductor current is charged with the DC voltage V_s. According to Equation (8), the charging time can be obtained as follows.

$$t_{ch} = \frac{L_r I_{Lrm}}{V_s} \tag{40}$$

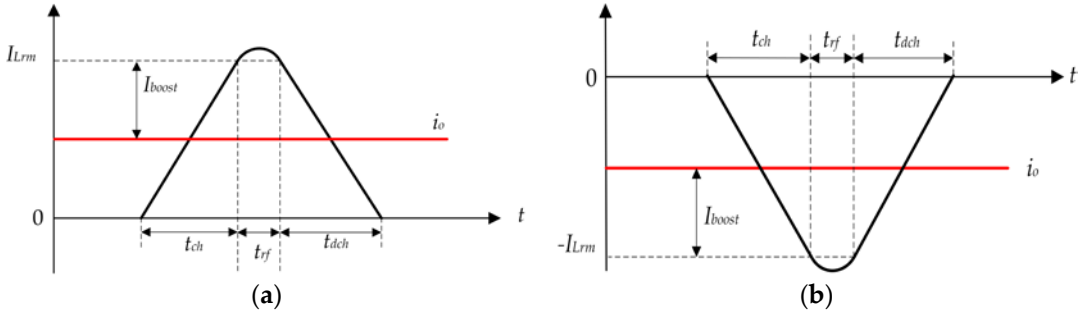

Figure 8. The waveforms of the auxiliary current: (**a**) $i_o > 0$ and (**b**) $i_o < 0$.

The charging time t_{ch} determines the turn-on moment of the auxiliary switches. According to Equations (8) and (23), the discharging time t_{dch} equals t_{ch}. Therefore, the on-time of the auxiliary switches can be obtained as follows:

$$t_A = t_{ch} + t_{dead} + t_{dch} = 2t_{ch} + t_{dead} \tag{41}$$

Due to $t_{dead} > t_{rf}$, the on-time t_A in Equation (39) is larger than the required t_A with some margin to ensure that the auxiliary switches is turned off after the auxiliary current drops to zero.

Figure 9 shows the open-loop realization diagram of the proposed control. The proposed control method is implemented in the FPGA of a digitally controlled ARSI prototype. FPGA samples the load current every switching cycle. Then the mode judgment is done according to Table 3. If the "AZVS + NZVS" is adopted when $|i_o| \geqslant I_{th}$, the initial resonant current is calculated from Equation (33). If the "AZVS + AZVS" is adopted when $|i_o| < I_{th}$, I_{boost} is fixed at I_B. Then, I_{Lrm}, t_{ch} and t_A are calculated from Equations (39)–(41). The gate signal of the auxiliary switches can be generated by t_{ch} and t_A.

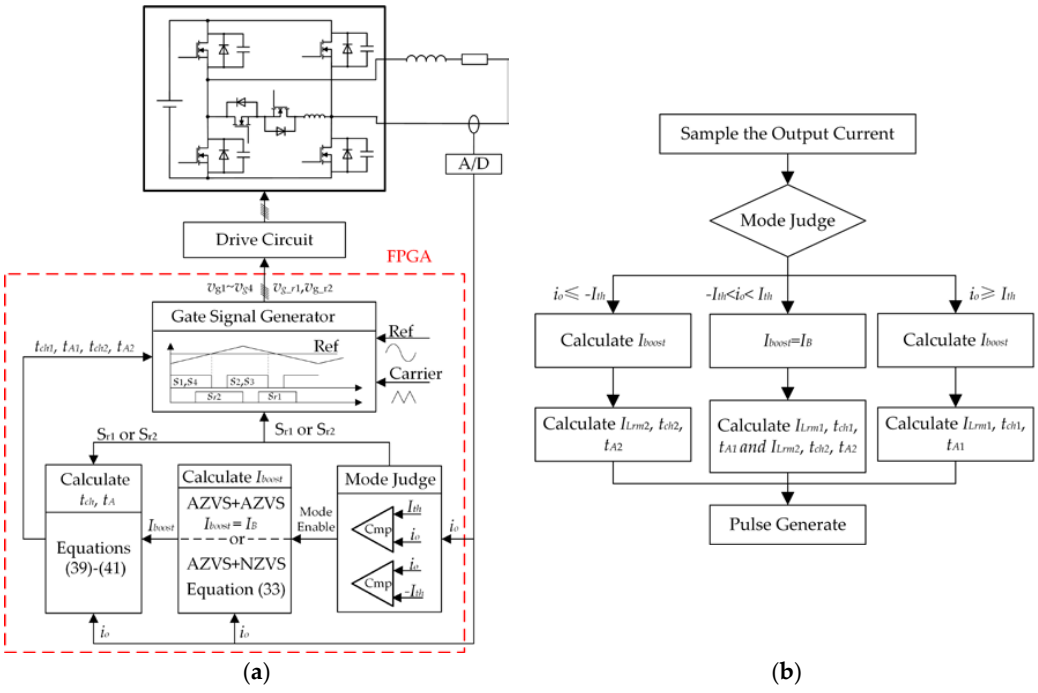

Figure 9. The open-loop realization diagram of the proposed control: (**a**) the control diagram and (**b**) the flowchart of the proposed control.

5. Experiment

The proposed method was implemented in the Altera Cyclone IV FPGA with parameters in Table 4. Figure 10 shows the photograph of the prototype. It consists of FPGA (Altera Corporation EP4CE22E22C7N, the USA) control board, switching power supply, MOSFET driver and the power circuit.

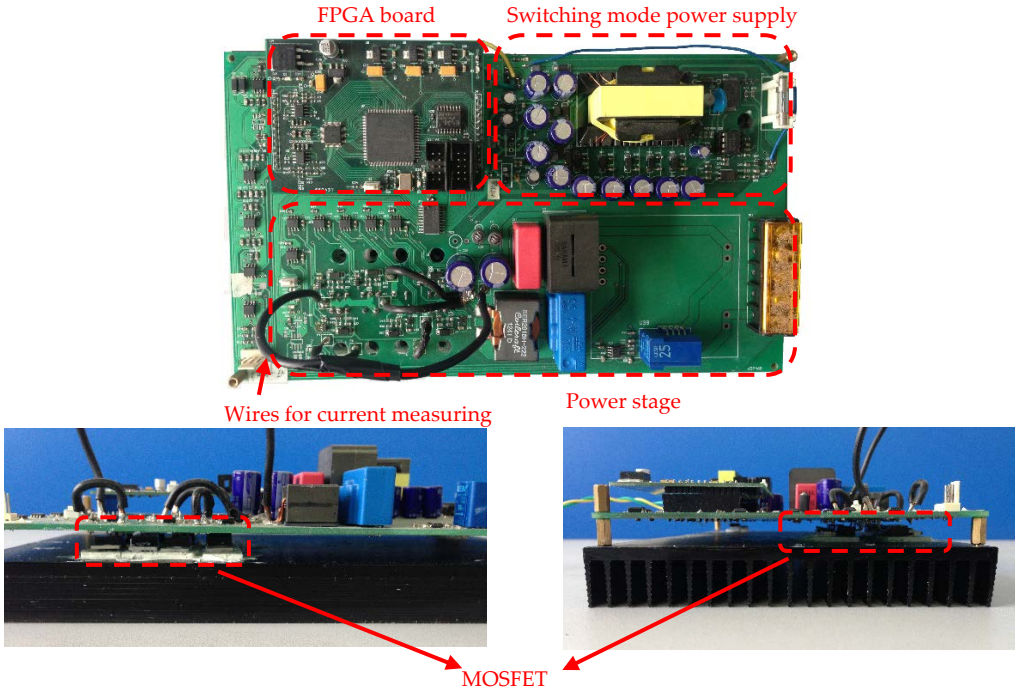

Figure 10. The photograph of the prototype.

The dead-time effect leads to the nonlinearity of inverter, which introduces the baseband harmonics in the output voltage and current. In the experiment, the total harmonic distortion (THD) of output current and output voltage with different methods are compared to verify the effectiveness of the proposed control method. The oscilloscope MSO4034B with the probes TCP0030, TPP0500 and P5025 is used to measure the voltages and currents. The power analysis module DPO4PWR is used to analyze the THD of the current and voltage.

Figure 11 shows the voltage and current waveforms of ARSI with conventional variable-timing control and proposed control when the modulation index is 0.4 in an open-loop configuration. The auxiliary circuit is operated twice with bidirectional current in a switching cycle to realize the "AZVS + AZVS". However, a single direction current occurs in the auxiliary circuit with realization of "NZVS + AZVS". To measure the output voltage v_o, a filter is added to attenuate the carrier harmonics of the pole voltage v_{ab}. Figure 11a shows that a large voltage error occurs in the output voltage with conventional control due to the unequal commutation times. The distortion is obvious especially at the mode switching point between the "AZVS + AZVS" and "NZVS + AZVS". The quality of the output voltage is improved with the proposed control in Figure 11b. The voltage error with proposed control should be zero in theory. However, the voltage error exists in the experimental results due to the limited PWM resolution of 8 bit and current detecting error.

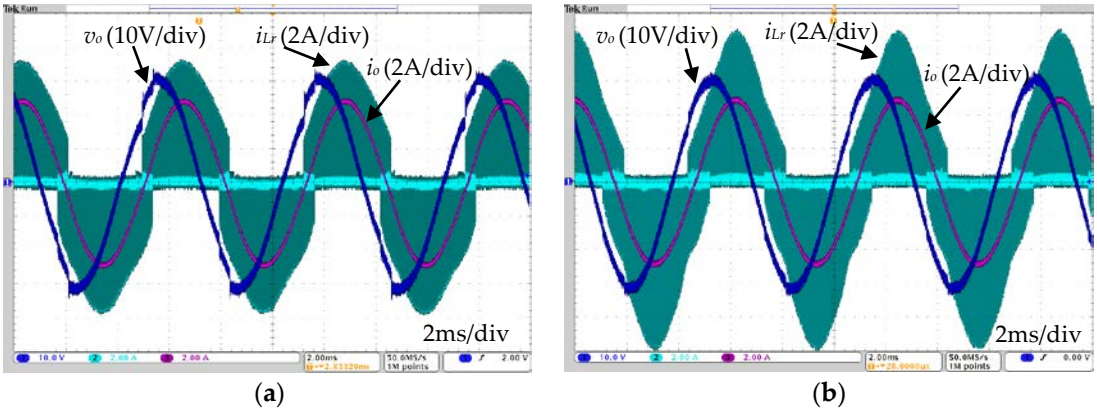

Figure 11. The current and voltage waveforms of ARSI with conventional control and proposed control: (**a**) conventional control and (**b**) proposed control.

Figure 12 shows the voltage waveforms and their harmonic analysis results when the modulation index is 0.4 in an open-loop configuration. THD-F is the ratio of the RMS value of harmonic components to the RMS value of the fundamental component, while THD-R is the ratio of the RMS value of harmonic components to the RMS value of the source waveform. THD-F is used in the experiment to compare the quality of the voltage and current. The THD-F and magnitude of the harmonic voltages respect to the fundamental voltage are indicated by the red boxes in Figure 12. THD-F of the output voltage with proposed control is 3.21%, which is less than 6.29% with conventional control. The magnitudes of the baseband harmonics are reduced by using the proposed control.

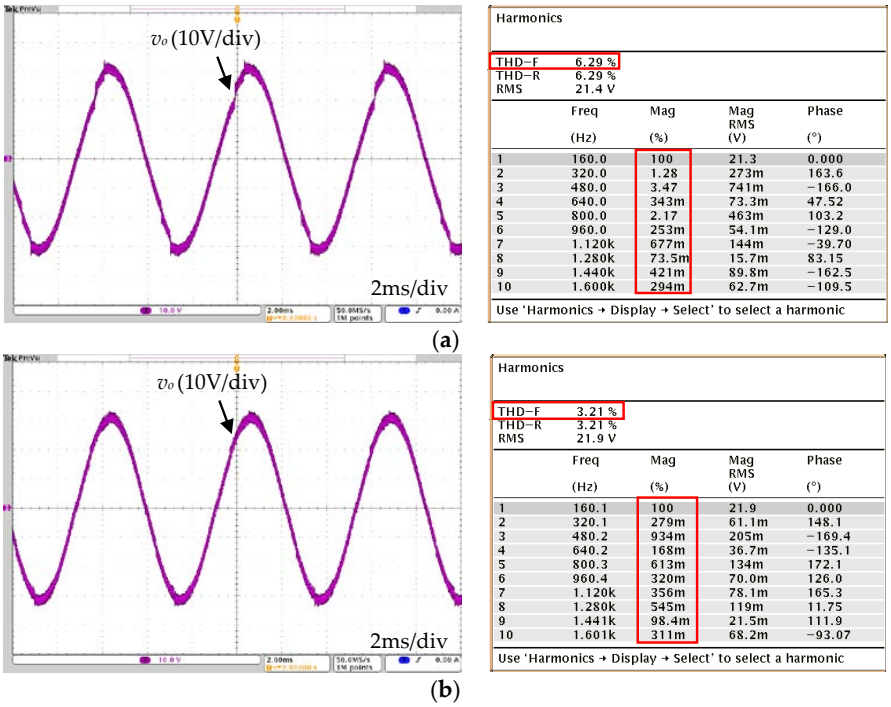

Figure 12. The current waveforms and their harmonic analysis results: (**a**) conventional control and (**b**) proposed control.

Figure 13 shows the magnitudes of the 2nd–10th harmonic voltages with respect to the fundamental voltage. The magnitudes of the harmonic voltages are reduced obviously with the proposed control, except the 6th, 8th and 10th harmonic currents.

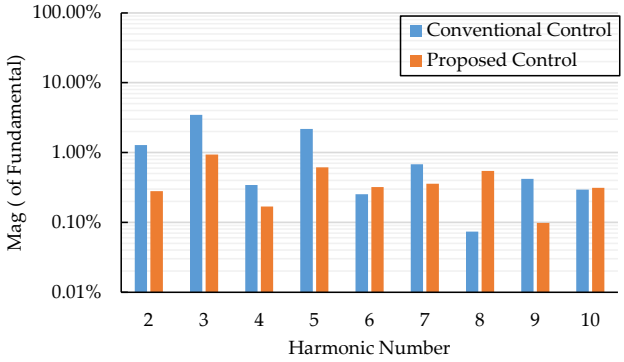

Figure 13. The magnitudes of the 2nd–10th harmonic voltages respect to the fundamental voltage.

Figure 14 shows the current waveforms and their harmonic analysis results when the modulation index is 0.4 in an open-loop configuration. The THD-F, RMS and magnitude of the harmonic voltages with respect to the fundamental voltage are indicated by the red boxes. Due to a large dead time, severe distortion occurs in the output current of the hard-switching inverter, as shown in Figure 14a. The RMS of the current is only 2A, which is much lower than the RMS of the soft-switching inverters with the modulation index 0.4. The THD-F of the hard-switching inverter is 4.36%. As for the ARSI, the THD-F is reduced to 1.57% and the RSM of the current is improved with conventional control, because the blanking delay error is eliminated which is the main error source in the hard-switching inverter. The THD-F of the output current is further improved to 0.607% by using the proposed control.

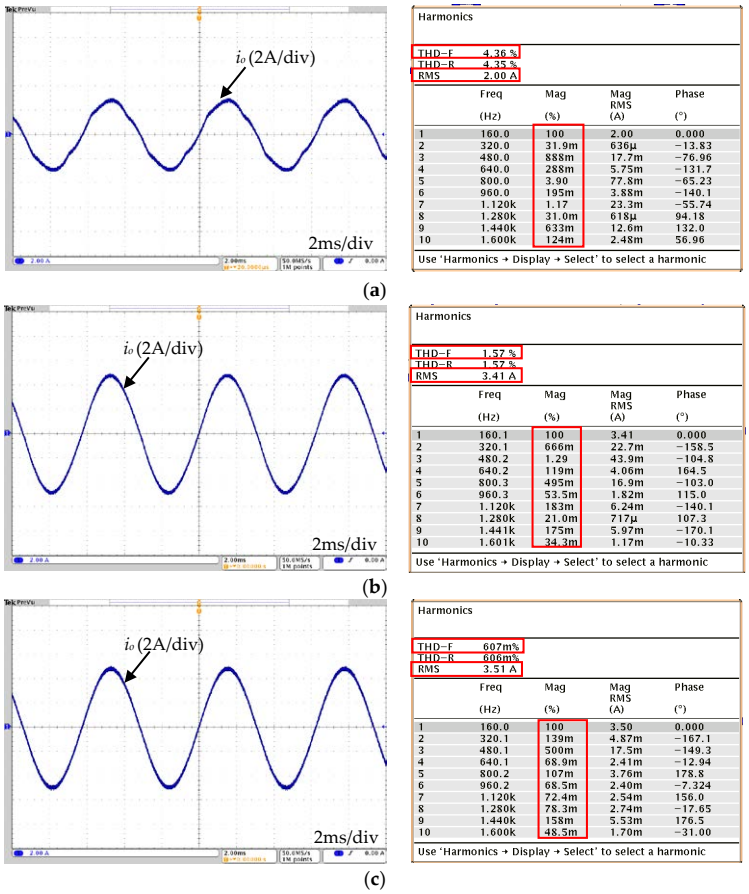

Figure 14. The current waveforms and their harmonic analysis results: (**a**) hard-switching inverter; (**b**) the ARSI with conventional control; and (**c**) the ARSI with proposed control

Figure 15 shows the magnitudes of the 2nd–10th harmonic currents of the ARSI respect to the fundamental current. The magnitudes of the harmonic currents are reduced obviously with the proposed control, except the 6th, 8th and 10th harmonic currents. The current results are in good agreement with the voltage results in Figure 13.

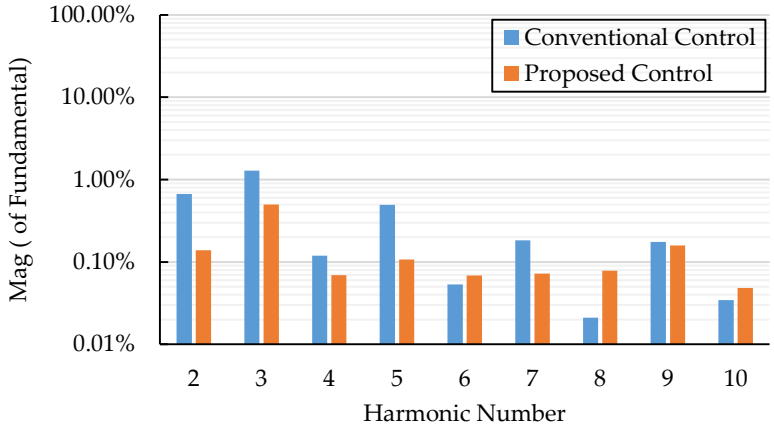

Figure 15. The magnitudes of the 2nd–10th harmonic currents of the ARSI respect to the fundamental current.

6. Conclusions

This paper analyzed the dead-time effect of ARSI, which is a typical example of ZVT PWM inverters. The blanking delay error that is the main error source of the hard-switching inverter is eliminated in the ARSI. Only the error caused by the rise- and fall-times exist in the ARSI. For the dead-time effect, the PTN and NTP commutations, respectively, cause the positive and negative voltage errors that are proportional to the commutation time, regardless whether NZVS or AZVS of the main switches is realized. NZVS and AZVS determine the commutation time of the ARSI. Based on the analysis, a high-precision control has been proposed to eliminate the voltage error. In the experiment, the THD of the output current and voltage are greatly reduced from 1.57% and 6.29% to 0.607% and 3.21%, respectively, by using the proposed control. In conclusion, the output quality can be improved with the high-precision control method.

However, objectively speaking, there are still some disadvantages in the proposed control. This novel method improves the precision at the expense of efficiency, because of relatively higher auxiliary current compared with that of the traditional control. Besides, the current I_{boost} should be calculated online, resulting higher calculation effort.

Anyway, the proposed control is very attractive in the high-precision applications to improve the output quality. Despite the fact that the analysis and proposed control is based on the ARSI, they can be used similarly to other types of the ZVT PWM inverters to eliminate the dead-time effect.

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