

Article

# Electric Characteristic Enhancement of an AZO/Si Schottky Barrier Diode with Hydrogen Plasma Surface Treatment and $\text{Al}_x\text{O}_x$ Guard Ring Structure

Chien-Yu Li <sup>1</sup>, Min-Yu Cheng <sup>1</sup>, Mau-Phon Houg <sup>1,\*</sup>, Cheng-Fu Yang <sup>2</sup> and Jing Liu <sup>3,\*</sup>

<sup>1</sup> Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University, No. 1, University Road, Tainan 701, Taiwan; q18021014@mail.ncku.edu.tw (C.-Y.L.); q16044082@mail.ncku.edu.tw (M.-Y.C.)

<sup>2</sup> Department of Chemical and Materials Engineering, National University of Kaohsiung, No. 700, Kaohsiung University Road, Nan-Tzu District, Kaohsiung 811, Taiwan; cfyang@nuk.edu.tw

<sup>3</sup> School of Information Engineering, Jimei University, Xiamen 361021, China

\* Correspondence: mphoung@eembox.ncku.edu.tw (M.-P.H.); jingliu@jmu.edu.cn (J.L.)

Received: 2 December 2017; Accepted: 4 January 2018; Published: 8 January 2018

**Abstract:** In this study, the design and fabrication of AZO/n-Si Schottky barrier diodes (SBDs) with hydrogen plasma treatment on silicon surface and  $\text{Al}_x\text{O}_x$  guard ring were presented. The Si surface exhibited less interface defects after the cleaning process following with 30 w of  $\text{H}_2$  plasma treatment that improved the switching properties of the following formed SBDs. The rapid thermal annealing experiment also held at 400 °C to enhance the breakdown voltage of SBDs. The edge effect of the SBDs was also suppressed with the  $\text{Al}_x\text{O}_x$  guard ring structure deposited by the atomic layer deposition (ALD) at the side of the SBDs. Experimental results show that the reverse leakage current was reduced and the breakdown voltage increased with an addition of the  $\text{Al}_x\text{O}_x$  guard ring. The diode and fabrication technology developed in the study were applicable to the realization of SBDs with a high breakdown voltage (>200 V), a low reverse leakage current density ( $\leq 72 \mu\text{A}/\text{mm}^2$  @100 V), and a Schottky barrier height of 1.074 eV.

**Keywords:** Schottky barrier diodes; hydrogen plasma; guard ring; atomic layer deposition; rapid thermal annealing

## 1. Introduction

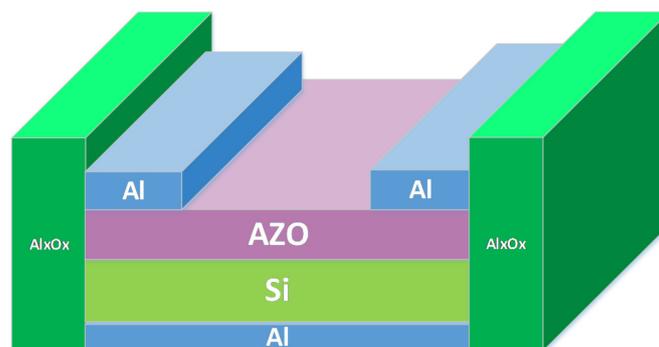
A Schottky barrier diode (SBD) can be simply formed by a semiconductor substrate coming in contact with a metal electrode. It is a majority-carrier device that is mainly used in high-frequency applications, and it provides the advantage of fast reverse recovery without the minority-carrier stored charge that is observed in p–n rectifiers. In most of these devices, using a power rectifier with high-speed switching capability is indispensable. However, due to their low breakdown voltage characteristic, SBDs have rarely been applied to high-power devices. Several studies have investigated the causes of the low breakdown voltage issue. Most of these studies have indicated that the edge effect and the interface trap cause the low breakdown voltage and leakage current [1–4]. In SBDs, voltage drop under forward bias ( $V_F$ ) and leakage current density under reverse bias ( $J_R$ ) are the main concerns related to power applications, which strongly depend on the Schottky barrier height (SBH). Therefore, developing an SBD with a high breakdown voltage ( $V_{BD}$ ), low reverse leakage current density ( $J_R$ ), and low forward voltage drop ( $V_F$ ) is essential in the electronic market. Generally, a large SBH leads to a low  $J_R$  but a high  $V_F$ . Moreover,  $V_{BD}$  is strongly influenced by the distribution of the surface electric field of the devices under reverse bias. There have been several studies discussed the edge effect that caused the leakage current [5]. The guard ring structure of  $p^+$  poly Si and metal

oxide were studied to suppress the leakage current of the SBDs [6–8]. The interface between the substrate with existed multiple defects can also be removed by a treating plasma cleaning process and an annealing process [9–11]. Low-temperature processes are also important for the semiconductor industry because they help avoid unintentional diffusion effects and unwanted chemical reactions. An AZO/n-Si SBD fabricated using a simple process and low-cost material has the potential to succeed in the electronic commerce market [12,13]. In this paper, the design and fabrication of AZO/n-Si SBDs through the H<sub>2</sub> plasma treatment of the Si surface and the introduction of an Al<sub>x</sub>O<sub>x</sub> guard ring are presented.

## 2. Fabrication of AZO/Si Diode

To fabricate the AZO/Si SBDs, a single-crystalline Si wafer of (100) direction was first phosphorus doped with a resistivity of 1–10 cm. The thickness of the Si wafer was 525 μm. The resultant Si substrates were then wet-process treated. Specifically, the Si substrates were dipped in a buffered oxide etch (BOE) solution for 1 min to remove the native oxide. Thereafter, they were dipped in a sulfuric and hydrogen peroxide mixture (SPM) solution that consisted of 80% H<sub>2</sub>SO<sub>4</sub> and 20% H<sub>2</sub>O<sub>2</sub> for 5 min at 120 °C. The SPM process was performed to remove organic contamination on the surface of the Si substrates. Subsequently, the treated substrates were dipped in an ammonia and hydrogen peroxide mixture (APM) solution that consisted of 4% of NH<sub>4</sub>OH and 4.2% of H<sub>2</sub>O<sub>2</sub> for 5 min at 70 °C in a constant temperature environment. The APM process has been demonstrated to effectively remove particles. The Si substrates were then dipped in a hydrochloric acid and peroxide mixture (HPM) solution that consisted of 4.5% of HCl and 3.75% of H<sub>2</sub>O<sub>2</sub> for 5 min at 60 °C. The HPM process was performed to remove metal impurities. Finally, the Si substrates were again dipped in the BOE solution for 1 min. At the end of each process, the substrates were rinsed with DI water and dried with N<sub>2</sub> gas.

After all of the Si substrates were thoroughly cleaned using the wet etching process, they were treated with H<sub>2</sub> plasma through microwave plasma chemical vapor deposition for 10, 30, and 60 s at room temperature. The H<sub>2</sub> plasma power was 30 W at 1.4 torr. Subsequently, an n-type AZO thin film was deposited on the Si substrates to obtain a strong Schottky contact through radio frequency (RF) magnetron sputtering. The deposition of the AZO thin film was performed in an Ar (purity: 99.99%) atmosphere, with the deposition pressure maintained at  $5 \times 10^{-3}$  torr and the RF power controlled at 100 W. During deposition, the temperature of the substrates was maintained at 200 °C. After deposition, the Al layer served as the front and back electrodes to provide strong ohmic contact. Finally, an Al<sub>x</sub>O<sub>x</sub> guard ring was added to the AZO/n-Si SBDs by using atomic layer deposition (ALD), followed by annealing in a N<sub>2</sub> atmosphere at 400 °C for 30 min. A high-purity N<sub>2</sub> (purity: 99.999%) atmosphere was utilized to carry the precursors and purge the by-products. The deposition pressure was kept constant at 1.4 torr. The structure of the AZO/Si diode was shown in the Figure 1. The size of the Si substrate was  $1 \times 1$  cm<sup>2</sup>, with approximately 39 nm AZO deposited on the Si substrate. The Al electrodes were defined in  $1 \times 0.3$  cm<sup>2</sup> with the utilization of metal mask. The guard ring structure was deposited with metal mask in  $1 \times 0.2$  cm<sup>2</sup>.



**Figure 1.** The structure of the AZO/Si diode with Al<sub>x</sub>O<sub>x</sub> guard ring.

In this study, the contact angle of the Si substrates was determined through water contact angle measurement. Additionally, energy dispersive X-ray spectrometry and grazing-incidence X-ray diffraction (XRD, Rigaku, Tokyo, Japan) were performed to determine the crystalline properties of the AZO thin film by using Cu K $\alpha$  radiation and a scanning angle ( $2\theta$ ) range of 20°–80°. Ultraviolet-visible spectroscopy was also conducted to determine the transmittance of the AZO thin film, and transmission electron microscopy (TEM, JEOL, Tokyo, Japan) was used to examine the grain sizes and structure of the poly-Si films. Conductive atomic force microscopy (Bruker, Billerica, MA, USA) was used to detect the surface height and current distribution, which could then be applied to detect the leakage current of the AZO/Si SBDs. Finally, Agilent B1500 (Agilent, Santa Clara, CA, USA) was used to measure the current density–voltage (J–V) characteristic of the fabricated SBDs.

### 3. Results and Discussion

In this section, we discuss the electrical properties of the fabricated AZO/Si SBDs. First, the deposition results of the AZO thin film, which affects the electrical properties of the diodes, are discussed. The switching characteristics of the diodes were observed using TEM images, C–V images, and J–V images; the H<sub>2</sub> plasma treatment of the Si substrate surfaces was also observed using J–V images. Notably, a weak leakage current of the reverse bias and an exponential increment of the forward bias current were the characteristics of the rectifying contacts. Thermionic emission theory indicates that the current density in an SBD is given by the Equation (1) [14]:

$$J = J_s \left( e^{-\frac{qV}{nkT}} - 1 \right) \quad (1)$$

Additionally, the saturation current density is given by

$$J_0 = A^* T^2 e^{-\frac{q\phi_B}{kT}} \quad (2)$$

where  $A^*$  is the effective Richardson constant,  $T$  is the temperature,  $q$  is the electronic charge,  $k$  is the Boltzman constant,  $V$  is the forward bias,  $n$  is the ideality factor,  $J_0$  is the saturation current density, and  $\phi_B$  is the effective barrier height. Notably,  $J_0$  is derived from the straight line intercept of  $\ln(J)$  at zero bias, and  $\phi_B$  is calculated by Equation (2). The utility of the Al<sub>x</sub>O<sub>y</sub> guard ring on the side of the SBDs was also examined. The cleanliness of the Si substrates and the crystallization of the AZO substantially affect the electrical properties of SBDs. Hence, in this study, we performed AZO deposition at three temperatures: room temperature, 200, and 300 °C. According to the X-ray diffraction measurement results in Figure 2a, a higher zinc oxide peak of (002) and a relatively lower peak of (103) were detected when AZO thin film deposition was performed at 200 °C. The full width at half maximum (FWHM) of the AZO (002) peak reduced with the raised of the deposition temperature, indicating the improved quality of crystallization. The calculated grain size of the AZO under 200 °C showed approximately size with 300 °C of 21 and 22 nm in the following figure.

The improvement of the AZO crystallization quality also in concert with the Hall measurement result. The carrier concentration was up to 10<sup>20</sup> order at 200 °C deposition which providing more conductivity. The resistivity, mobility, and carrier concentration of the AZO thin film, calculated using the Hall measurement, are presented in Figure 3. Notably, the carrier concentration of the AZO thin film deposited at 300 °C was higher than that of the film deposited at 200 °C. However, the higher ratio of Al to Z in the AZO thin film led to greater ionized impurity scattering and lower mobility, and the conductivity of the AZO thin film deposited at room temperature was too low for the film to be applied on the diode.

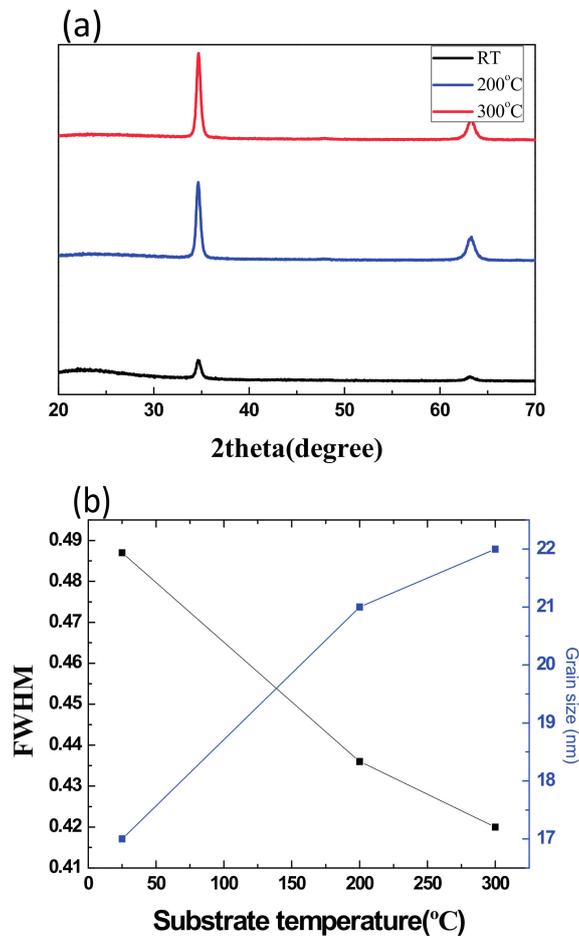


Figure 2. (a) The X-ray diffraction (XRD) measurement; (b) FWHM and grain size of AZO thin film deposited in room temperature, 200, and 300 °C.

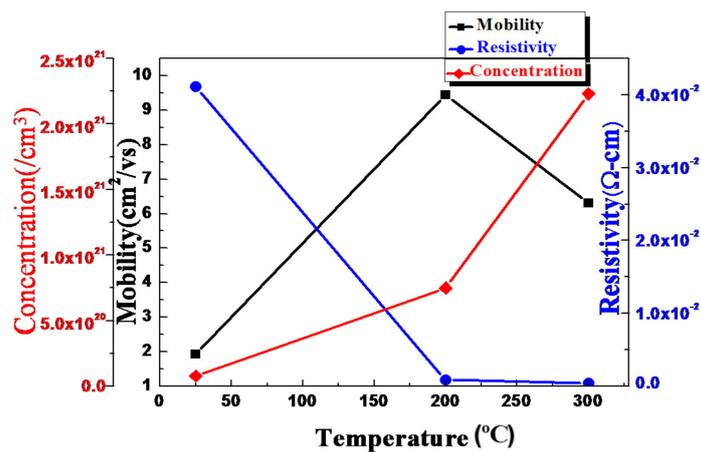
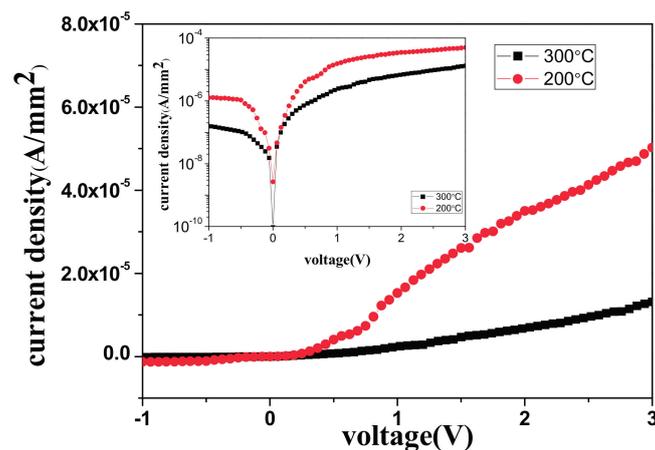


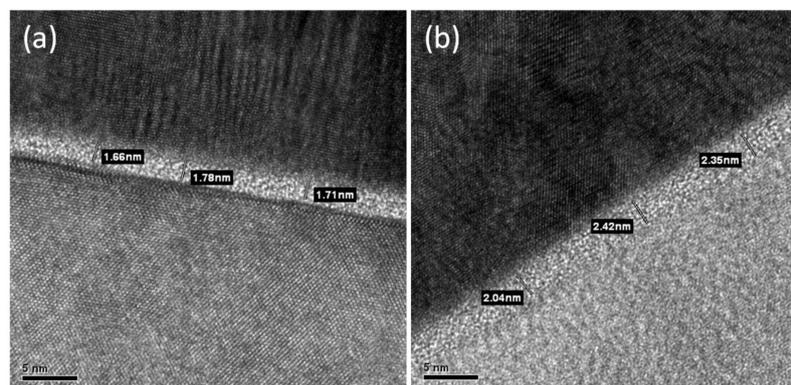
Figure 3. The Hall measurement of AZO thin film deposited in room temperature, 200, and 300 °C, showing the mobility, resistivity, and carrier concentration.

Figure 4 reveals the experimental semi-log J–V characteristics of the AZO/n-Si SBDs at room temperature. The reverse saturation current density of the AZO/Si SBDs deposited at 300 °C was  $1.18 \times 10^{-8}$  A/mm<sup>2</sup>, which is lower than that of the AZO/Si SBDs deposited at 200 °C ( $5.78 \times 10^{-8}$  A/mm<sup>2</sup>). However, the AZO/Si SBDs deposited at 200 °C had a lower turn on voltage than the AZO/Si SBDs deposited at 300 °C.



**Figure 4.** The J–V figure of 200 °C/300 °C AZO thin film deposited on Si substrate demonstrated a lower turn on voltage on 200 °C AZO/Si Schottky barrier diodes (SBDs).

Differences between the AZO/Si SBDs deposited at 200 °C and those deposited at 300 °C are also evident in the TEM images shown in Figure 5. In particular, the SiO<sub>x</sub> layer in the AZO/Si intermediate region was approximately 1.7 nm in the AZO/Si SBDs deposited at 200 °C (Figure 5a) and 2.3 nm in the AZO/Si SBDs deposited at 300 °C (Figure 5b). A thicker SiO<sub>x</sub> layer decreased the reverse tunneling saturation current due to the addition of the effective barrier height, as shown in Figure 4.

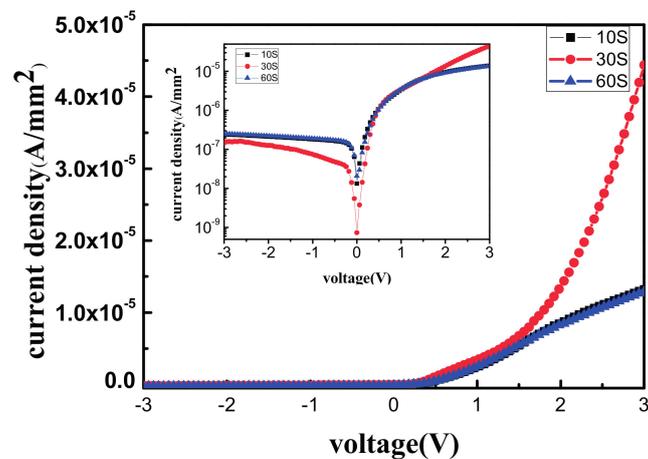


**Figure 5.** Transmission electron microscopy (TEM) figures of (a) 200 °C and (b) 300 °C AZO thin film deposited on Si substrate showed 1.7 and 2.3 nm SiO<sub>x</sub> at the interface of AZO and Si substrate.

A native oxide layer and metal particles on the surface of the Si substrates affect the SBD breakdown voltage. Although the Si substrates were thoroughly cleaned using the wet etching process, the ultrathin oxide layer formed during the subsequent process of AZO deposition on the substrate surface. The ultrathin oxide layer between Si and AZO causes tunneling of carrier and leakage current [15]. The interface trap between Si and SiO<sub>2</sub>, which was caused by the dangling bonds from the oxide layer, metal impurities, and the hot carrier, consumed the electronic charge and affected the I–V properties.

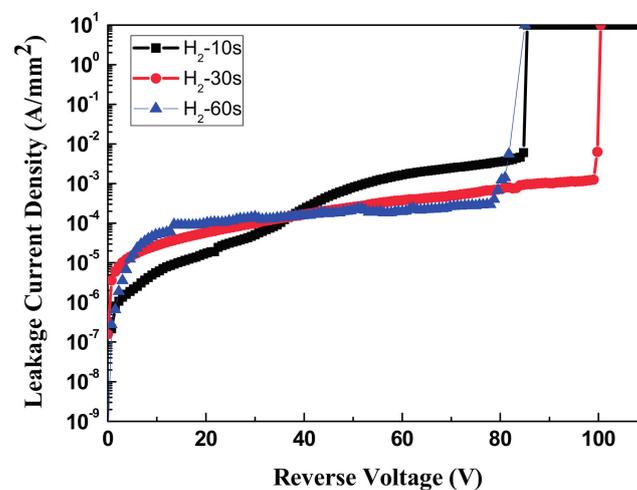
To overcome the aforementioned issues, we treated the Si substrate surfaces with H<sub>2</sub> plasma to remove the native oxide layer and eliminate the dangling bonds [10,11]. The H<sub>2</sub> plasma power was set to 30 W for 10, 30, and 60 s at room temperature. As depicted in Figure 6, this figure indicates that the saturation current density  $J_0$ , which was analyzed by extrapolation to the forward bias of 0 V, was  $4.43 \times 10^{-9}$ ,  $2.27 \times 10^{-9}$ , and  $4.85 \times 10^{-9}$  A/mm<sup>2</sup>, respectively. By substituting  $J_0$  in Equation (2), the SBH was determined to be 0.92, 0.93, and 0.85 eV, respectively. Our results demonstrated that the

SBD with a Si substrate treated with H<sub>2</sub> plasma for 30 s had the lowest reverse current density and the highest forward current.



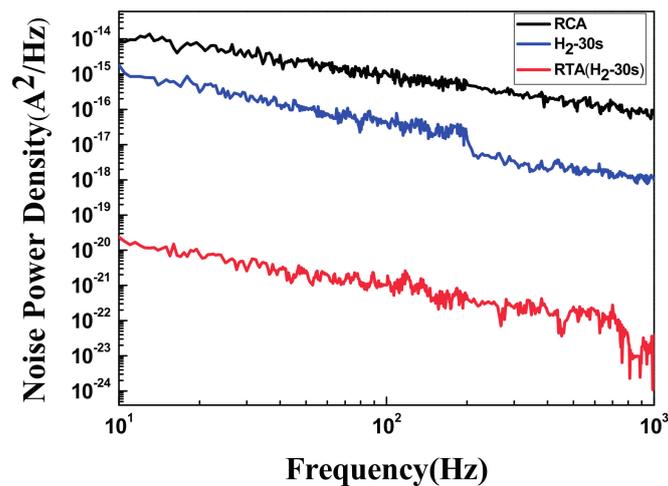
**Figure 6.** The J–V figure of 10 s/30 s/60 s H<sub>2</sub> plasma treated on Si substrate demonstrated  $4.43 \times 10^{-9}$ ,  $2.27 \times 10^{-9}$ , and  $4.85 \times 10^{-9}$  A/mm<sup>2</sup> reverse saturation current density of the SBDs.

With an appropriate amount of power, the H<sub>2</sub> plasma treatment effectively removed the oxide layer; however, if the H<sub>2</sub> plasma treatment used too much power or too much time, the Si surface was damaged and defects were formed in the surface. After H<sub>2</sub> plasma treated on the Si surface for 10, 30, 60 s, the breakdown voltages of the following formed AZO/n-Si SBDs increased to 85, 100, and 81 V, as revealed in Figure 7.



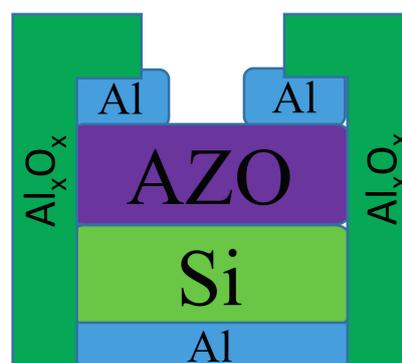
**Figure 7.** The J–V figure of 10 s/30 s/60 s H<sub>2</sub> plasma treated on Si substrate presented the SBDs breakdown voltage of 85 v/100 v/81 v.

Notably, the defects between the interface of the Si and the oxide layer trapped and detrapped the carriers and produced flicker noise. A subsequent annealing process would rearrange the atoms and decrease the number of defects on the Si surface. The flicker noise measurement was held under the constant current of 400  $\mu$ A. The results of our flicker noise analysis are presented in Figure 8, and they show that the number of defects at the interface between the oxide layer and the Si surface considerably decreased following the H<sub>2</sub> plasma treatment and annealing process. This result confirmed that the H<sub>2</sub> plasma treatment and annealing decrease the number of defects at the interface.



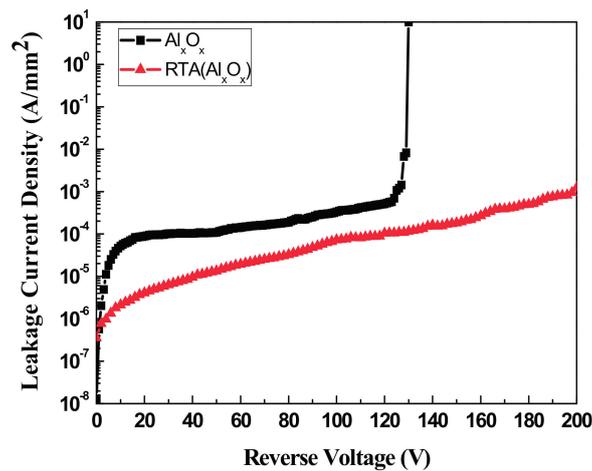
**Figure 8.** The flicker noise measurement of the H<sub>2</sub> plasma treated sample demonstrated a lower noise power density than the sample that only treated with Radio Corporation of America (RCA) standard cleaning process. The Rapid Thermal Annealing (RTA) treated sample can further suppress the flicker noise and improved the interface of Si substrate.

The reverse current is the most critical characteristic influencing the switching behavior of SBDs. Notably, the leakage current at the edge of SBDs, which is caused by the deep edge of the metal electrode, comprises most of the reverse current. To eliminate the adverse effect of the leakage current, some researchers have included a guard ring when fabricating SBDs. In most previous studies, the guard rings used consisted of a deep doped P-type diffusion area. However, in the present study, Al<sub>x</sub>O<sub>x</sub> was utilized as the guard ring and was deposited around the AZO/Si SBDs by using ALD. The structure of the AZO/Si SBDs with the guard ring is shown in Figure 9. The green vertical part of Figure 9 is the Al<sub>x</sub>O<sub>x</sub> layer. The deposition was processed through the metal mask covering on the middle of the diode. The exposed part at the side of diode was then deposited on the Al<sub>x</sub>O<sub>x</sub> layer.



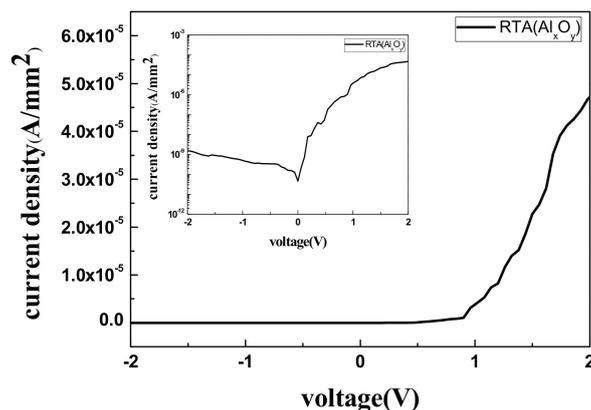
**Figure 9.** The structure of the AZO/Si SBD with Al<sub>x</sub>O<sub>x</sub> guard ring.

The Al<sub>x</sub>O<sub>x</sub> guard ring isolated the leakage current around the electrode and enabled the SBDs to have the switching properties of a high breakdown voltage and low reverse current. As illustrated in Figure 10, the breakdown voltage of the unannealed SBDs increased to 130 V when the Al<sub>x</sub>O<sub>x</sub> guard ring was added; these SBDs also had a lower reverse current. However, following the rapid thermal annealing process, the breakdown voltage of these SBDs were further improved to over 200 V.



**Figure 10.** The breakdown voltage of the SBDs with guard ring structure raised to 130 V before the RTA annealing process and further increased to over 200 V after the RTA annealing.

The J–V results of the SBDs with  $\text{Al}_x\text{O}_x$  guard ring presented in Figure 11 illustrate a reverse saturation current density ( $J_s$ ) of  $4.62 \times 10^{-11}$  A/mm<sup>2</sup> and a barrier height of 1.074 eV. Therefore, adding a guard ring to SBDs reduces the reverse current and improves the forward bias.



**Figure 11.** The J–V figure of the SBDs with  $\text{Al}_x\text{O}_x$  guard ring showed a  $4.62 \times 10^{-11}$  A/mm<sup>2</sup> saturation current density ( $J_s$ ).

#### 4. Conclusions

In this study, we successfully fabricated AZO/Si SBDs with a high breakdown voltage. By modifying the AZO deposition parameters, we were able to improve the crystallization of the AZO and the saturation current density ( $J_s$ ) of the SBDs. Additionally, we demonstrated that the  $\text{H}_2$  plasma treatment substantially reduced the number of defects at the interface between the oxide layer and the Si surface, as well as reduced the current noise power spectral density by 10 times. Prior to annealing, the AZO/Si SBDs had the following switching properties: a breakdown voltage of 100 V, leakage current density of  $2.27 \times 10^{-9}$  A/mm<sup>2</sup>, and SBH of 0.923 eV. The current noise power spectral density of the annealed AZO/Si SBDs was also  $10^6$  times less than that of the unannealed SBDs. Finally, adding a guard ring and proceeding the Rapid Thermal Annealing (RTA) at 400°C was found to further increase the breakdown voltage to over 200 V and reduce the leakage current density to less than  $72 \mu\text{A}/\text{mm}^2$  at the 100 V bias. The reverse saturation current density was also reduced to  $4.62 \times 10^{-11}$  A/mm<sup>2</sup>, and the SBH was increased to 1.074 eV.

**Acknowledgments:** The authors would like to thank the laboratory of Yon-Hua Tzeng at the Institute of Microelectronics, Department of Electrical Engineering, National Cheng-Kung University, for providing the instrument. This work was also supported by the National Science Council of Taiwan under Contract Number MOST 106-2221-E-006-228 and by NSFC projects under Grant Nos. 61505068 and 11505079.

**Author Contributions:** Chien-Yu Li organized the experimental procedure and results and paper writing. Min-Yu Cheng helped the experimental procedure and analyzed the measured results. Mau-Phon Houng, Cheng-Fu Yang, and Jing Liu analyzed the measured results helped in the paper writing.

**Conflicts of Interest:** The authors declare no conflict of interest.

## References

1. Rhoderick, E.H. Metal-semiconductor contacts. *IEEE Proc. I-Solid-State Electron Devices* **1982**, *129*, 1. [[CrossRef](#)]
2. Chang, C.Y.; Fang, Y.K.; Sze, S.M. Specific contact resistance of metal-semiconductor barriers. *Solid-State Electron.* **1971**, *14*, 541–550. [[CrossRef](#)]
3. Cheung, S.K.; Cheung, N.W. Extraction of Schottky diode parameters from forward current-voltage characteristics. *Appl. Phys. Lett.* **1986**, *49*, 85–87. [[CrossRef](#)]
4. Fujihira, T.; Miyasaka, Y. Simulated superior performances of semiconductor superjunction devices. In Proceedings of the 10th International Symposium on Power Semiconductor Devices and ICs, Kyoto, Japan, 3–6 June 1998.
5. Lepselter, M.P.; Sze, S.M. Silicon Schottky Barrier Diode with Near-Ideal I–V Characteristics. *Bell Syst. Tech. J.* **1968**, *47*, 195–208. [[CrossRef](#)]
6. Liou, B.W.; Lee, C.L.; Lei, T.F. High breakdown voltage Schottky barrier diode using p<sup>+</sup>-polycrystalline silicon diffused guard ring. *Electron. Lett.* **1995**, *31*, 1950–1951. [[CrossRef](#)]
7. Liou, B.W.; Lee, C.L. Characteristics of high breakdown voltage Schottky barrier diodes using p<sup>+</sup>-polycrystalline-silicon diffused-guard-ring. *Solid-State Electron.* **2000**, *44*, 631–638. [[CrossRef](#)]
8. Liou, B.W. Fabrication of high breakdown voltage silicon Schottky barrier diodes using various edge termination structures. *Thin Solid Films* **2009**, *517*, 6558–6564. [[CrossRef](#)]
9. Card, H.C.; Rhoderick, E.H. Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes. *J. Phys. D Appl. Phys.* **1971**, *4*, 1589. [[CrossRef](#)]
10. Altmannshofer, S.; Boudaden, J.; Wieland, R.; Kutter, C. Microwave plasma assisted process for cleaning and deposition in future semiconductor technology. *IOP Conf. Ser. Mater. Sci. Eng.* **2017**, *213*. [[CrossRef](#)]
11. Altmannshofer, S.; Eisele, I.; Gschwandtner, A. Hydrogen microwave plasma treatment of Si and SiO<sub>2</sub>. *Surf. Coat. Technol.* **2016**, *304*, 359–363. [[CrossRef](#)]
12. Sheu, J.K.; Lee, M.L.; Tun, C.J.; Lin, S.W. Ultraviolet band-pass Schottky barrier photodetectors formed by Al-doped ZnO contacts to n-Ga N. *Appl. Phys. Lett.* **2006**, *88*, 043506. [[CrossRef](#)]
13. Li, B.; Adachi, Y.; Li, J.; Okushi, H.; Sakaguchi, I.; Ueda, S.; Yoshikawa, H.; Yamashita, Y.; Senju, S.; Kobayashi, K.; et al. Defects in ZnO transparent conductors studied by capacitance transients at ZnO/Si interface. *Appl. Phys. Lett.* **2011**, *98*, 082101. [[CrossRef](#)]
14. Di Bartolomeo, A. Graphene Schottky diodes: An experimental review of the rectifying graphene/semiconductor heterojunction. *Phys. Rep.* **2016**, *606*, 1–58.
15. Bartolomeo, A.D.; Luongo, G.; Giubileo, F.; Funicello, N.; Niu, G.; Schroeder, T.; Lisker, M.; Lupina, G. Hybrid graphene/silicon Schottky photodiode with intrinsic gating effect. *2D Mater.* **2017**, *4*, 025075. [[CrossRef](#)]

