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Developing a Generalized Multi-Level Inverter with Reduced Number of Power Electronics Components

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Abstract: Reducing the number of components of power electronic converters has been an important research topic over the past few decades. This paper introduces a new structure for a multi-level inverter based on reduced switch basic modules. The proposed basic module requires fewer switches and auxiliary devices. In addition, a lesser number of on-state switches for the synthesis of each voltage level results in less conduction losses, which enhances the converter efficiency. The proposed structure is capable of being implemented in both symmetrical and asymmetrical topologies. This is a merit feature for the proposed topology, which produces high voltage levels with a limited number of elements. The proposed structure is controlled using the fundamental frequency control scheme. The proposed basic module consists of six unidirectional switches and five DC voltage sources, generating five positive voltage levels. The performance of the recommended topology is analyzed from the various circuitry parameters, and a comprehensive comparison carried out with similar recent structures. The presented comparison reveals the advantage of the recommended inverter from different aspects of the circuitry parameters. The suggested structure is simulated using Matlab/Simulink software, and its performance is validated using a laboratory prototype. The results are reported for various steady-state and dynamic conditions.

Keywords: multi-level inverter; reduced switch basic modules; efficiency

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1. Introduction

Multi-level inverters are widely used in various applications due to their various features, such as low dv/dt stress, modularity, and high-power quality. In high voltage applications, equipment with low and medium voltage levels is often used [1]. Multi-level inverters are usually utilized in high power quality [2], FACTS devices [3], electric vehicles [4], variable speed drives [5], smart grids [6], high voltage applications [7], etc. The traditional multi-level inverters are segmented into three primary categories, which include Diode Clamped Multi-Level Inverter (DC-MLI) or Neutral Point Clamped Multi-Level Inverters (NPC-MLI), Flying Capacitor Multi-Level Inverter (FC-MLI), and Cascade H-Bridge Multi-Level Inverters (CHB-MLI) [8,9]. From the number of circuitry components view, the DC-MLI structure requires multiple diodes if the number of levels increases, making circuit control complex and tedious [1]. In the FC-MLI structure, the voltage balance problem of the capacitors can be solved by using additional switching modes. However, the number of passive components will increase which will be a threat to the

reliability of the converter [10]. The CHB-MLI structure is modular and relatively simple compared to the other two topologies. Besides, it does not need additional circuits to match the voltage, but instead uses several isolated DC sources [11]. Despite the simplicity and modularity of CHB-MLIs, adding one module increases four switches and related devices. The need for more circuit devices in the classic topologies of multi-level inverters is a research motivation for new topologies by reducing the number of devices [12].

An advanced configuration was represented in [13] for a symmetrical voltage source multi-level inverter that the high voltage levels are synthesized by extending basic cells. This structure has fewer switches compared to the cascaded H-bridge inverter. However, the number of switches in this topology is still high. In [14], a sub-multi-level structure is introduced, and its cascaded structure was investigated, which requires many switches and drivers. In [14,15], a six-switch H-bridge configuration was utilized for an incremental combination of DC voltage sources. To generalize the voltage levels of this structure, bidirectional switches are considered on both sides of the basic structure. These structures also require a large number of switches. In [16], an extended cascaded structure is introduced, which was based on a basic module and level booster circuit. The number of power electronic devices is high in this structure. An improved symmetric generalized topology was introduced in [17]. This topology consists of two parts, the Level Generation Unit (LGU) and the Polarity Generation Unit (PGU), which uses bidirectional switches. This structure requires a high number of switches, and also the total blocking voltage is significant. In [18], a multi-level cascaded inverter structure was introduced with a new design in symmetrical and asymmetrical topologies, where the number of switches is relatively high. In [19], a bidirectional cascaded multi-level inverter topology was reported, where can operate in symmetrical and asymmetrical modes. This structure was designed by improving the other two structures, which have fewer switches. However, in this inverter, the number of switches and the blocking voltage are also high. In [20], a multi-level inverter for dynamic loads was suggested, which provides two separate structures for symmetrical and asymmetrical topologies. Its symmetrical structure consists of an advanced cascaded H-bridge with many semiconductors. The reference [21] introduces a symmetrical modular multi-level topology with a relatively low number of switches. However, the voltage sources number in this structure is a high value. The reference [22] introduced a switch-ladder structure for a new multi-level converter. This structure was implemented symmetrically and asymmetrically using unidirectional and bidirectional switches. A diode-containing bidirectional structure for a multi-level inverter was reported in [23], which solves the voltage spike problem in such diode-based structures. However, this structure uses a current sensor to realize the current polarity, complicating the control scheme. Also, a generalized diode-containing bidirectional structure for multi-level inverters was represented in [24]. This structure solved the current sensor problem in [23] yet has many switches and considerable blocking voltage. In [25], a modified K-type multi-level inverter structure was reported, utilizing the cascading method to generalize to higher voltage levels. This structure requires eight unidirectional switches to produce seven levels, while the number of switches is not small. A Cross-Switched T-Type (CT-Type) was presented in [26], which used a T-type inverter embedded on either side of the structure to yield more voltage levels. This inverter can operate symmetrically or asymmetrically, while the number of switches was not reduced.

This paper develops a novel configuration for multi-level inverters with symmetrical and asymmetrical topologies. Fewer power electronic devices and fewer switches in the current path of different voltage levels are the main design goals of the recommended topology. These goals make the suggested inverter useful for different applications. The main features of the proposed structure are as follows.

1. The proposed basic module has a lesser number of switches, which by generalizing the basic module, the proposed extended structure is realized.

2. As the number of switches decreases, the axillary circuit number of devices, including the number of gate drivers, snubber circuits, heat sinks, etc., decreases as well, which reduces the cost and volume of the suggested inverter.
3. The voltage stress of the recommended basic module switches is low.
4. The maximum number of conducting switches in the current path of each voltage level is low for the proposed structure. Thus, the switches total conduction losses are reduced and the efficiency increased.

The rest of this paper is organized as follows. Section 2 presents the configuration of the suggested MLI converter and its functionality. Section 3 compares the recommended structure with other topologies in terms of circuitry parameters, including switches and gate driver's number, and total standing voltage (TSV) for different voltage levels. Section 4 presents the mathematical equations and simulations related to losses and efficiency. The analysis of the simulation and laboratory results is reported in Section 5, and finally, the conclusions are presented in Section 6.

2. Suggested Structure

2.1. The Reduced Switch Basic Module

The proposed reduced switch basic module (RSBM) is depicted in Figure 1. It consists of five DC sources and six semiconductor switches along with their anti-parallel diodes. The proposed reduced switch basic module is responsible for producing positive levels. The switches (S_1, $\overline{S_1}$), (S_2, $\overline{S_2}$), (S_3, $\overline{S_3}$) of the proposed RSBM operate complementarily. In other words, the conducting switches in the current path of any voltage level are always half of the total switches of the suggested RSBM. The recommended RSBM can produce five positive voltage levels.

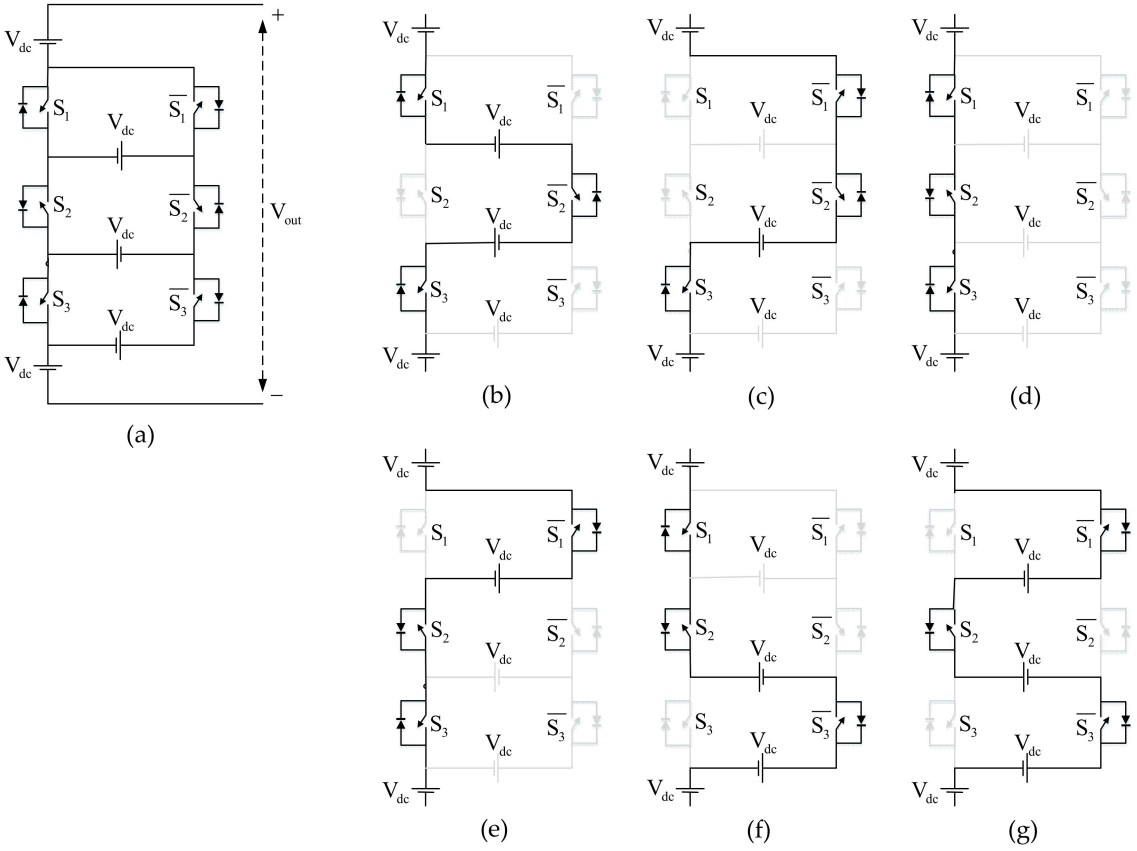


Figure 1. (**a**) The suggested RSBM, (**b**) $V_{out} = 0$, (**c**) $V_{out} = V_{dc}$, (**d**) $V_{out} = 2V_{dc}$, (**e**) $V_{out} = 3V_{dc}$, (**f**) $V_{out} = 4V_{dc}$, (**g**) $V_{out} = 5V_{dc}$.

The reduced switch basic module consists of three switches S_1, S_2, S_3, and their complementary pairs. According to Figure 1, if the switches S_1, S_3 are turned on, the output voltage 0 is generated, and if the switch S_3 is turned on, the first voltage level is produced. To generate the second voltage level, the switches S_1, S_2, S_3 are turned on, and switches S_2, S_3 are turned on to generate the third voltage level. The RSBM also generates the fourth voltage level when the switches S_1, S_2 are turned on, and the fifth voltage level is generated when the switch S_2 is turned on. Table 1 demonstrates the switching pattern of the suggested basic module to produce voltage levels. In this table, 1 means on-state, and 0 means off-state for switches. Naturally, complementary switches behave inversely with the main switches.

Table 1. The switching logic of the RSBM.

S_1	S2	S_3	V_{out}
1	0	1	0
0	0	1	V_{dc}
1	1	1	$2V_{dc}$
0	1	1	$3V_{dc}$
1	1	0	$4V_{dc}$
0	1	0	$5V_{dc}$

2.2. Blocking Voltage of the Proposed Reduced Switch Basic Module

Maximum blocking voltage (MBV) indicates the peak voltage across the off-state switch. Considering the MBV of all switches of the converter, the total blocking voltage (TBV) for the converter is obtained, which can be expressed as follows:

$$\mathrm{TBV} = \sum_{\text{Switches}} \mathrm{MBV} \tag{1}$$

The MBV and TBV parameters are an important challenge for multi-level inverters. The parameter MBV is the most important in selecting the voltage rating of switches. The price of the switches is proportional to their allowable voltage rating. Therefore, the lower the MBV value of the converter switches, the lower the total cost. The MBV value for each switch of the proposed basic module is given in the following relations.

$$S_1 = \overline{S_1} = V_{dc} \tag{2}$$

$$S_2 = \overline{S_2} = S_3 = \overline{S_3} = 2\,V_{dc} \tag{3}$$

The MBV relations of the proposed RSBM reveal that this basic unit can generate five voltage levels using low-voltage rating switches.

2.3. The Proposed Generalized Inverter Structure

The proposed reduced switch basic module can generate only positive voltage levels. So, a structure must generate positive and negative voltage polarity. The H-bridge module can be used for this purpose. Figure 2 displays the proposed multi-level inverter structure. According to this figure, the proposed structure consists of two parts. The first part is related to the level generator, and the second part is related to the polarity generator. In the proposed multi-level inverter, the reduced switch basic modules are connected in series and form the level generator. All switches of the proposed structure operate complementarily. This means that only half of the switches are in on-state at any output voltage level. In other words, the low number of on-state switches reduces the conduction losses of the switches. The size of voltage sources in the RSBMs can be designed and adjusted both symmetrically and asymmetrically.

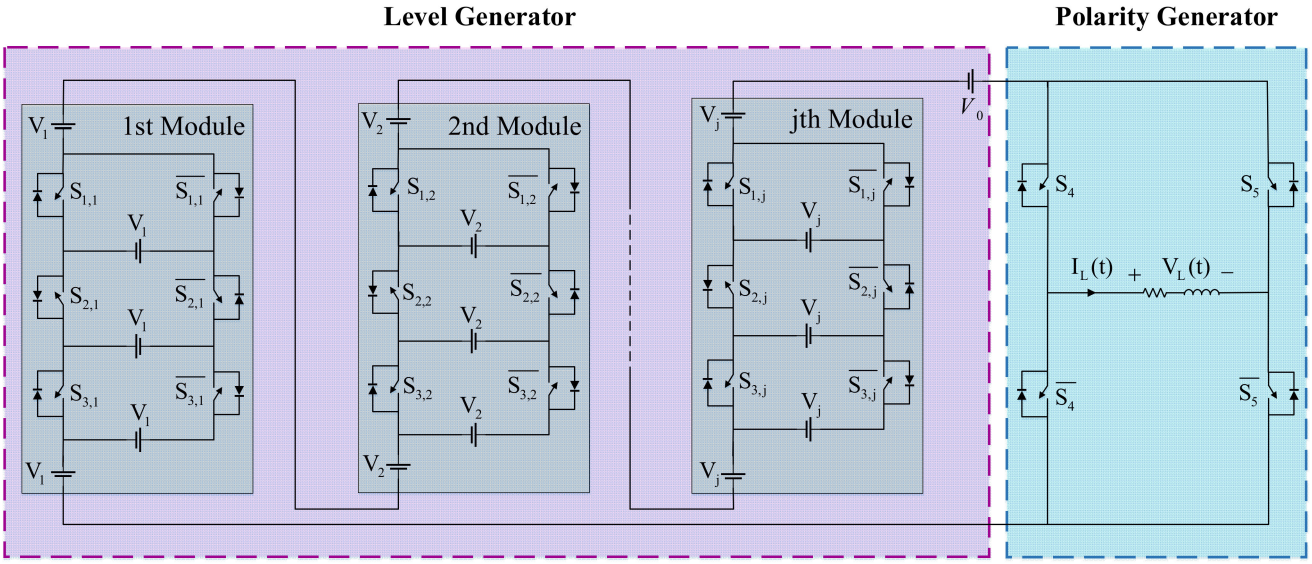


Figure 2. The proposed generalized inverter structure.

In a symmetric topology, the size of voltage sources of the RSBMs is equal. If the voltage source size of the RSBMs is assumed to be V_{dc}, the following relations provide the various parameters of the proposed multi-level inverter in the symmetric topology.

$$V_0 = V_1 = V_2 = \ldots = V_j = V_{dc} \quad (4)$$

$$N_L = 11j + 1 \quad (5)$$

$$N_{IGBT} = N_S = 6j + 4 \quad (6)$$

$$N_{GD} = 6j + 4 \quad (7)$$

$$TBV = 30j \times V_{dc} \quad (8)$$

In the above relations, j shows number of RSBMs, V_j shows the size of the voltage sources of the jth basic module, N_L shows the number of output voltage levels that can be synthesized by the topology, N_{IGBT}, and N_S show the number of IGBT and switches, respectively. Since the bidirectional switch is not utilized in the structure, the number of switches and IGBTs are equal. N_{GD} shows the number of gate drivers, and the TBV shows the total blocking voltage by the switches of the structure.

In an asymmetric topology, voltage source sizes can have different values using various algorithms. Table 2 presents the allowable algorithms for the size of voltage sources in asymmetric topology, where j represents the jth RSBM.

Table 2. Proposed algorithms for asymmetric topology voltage source size.

Proposed Algorithm	Magnitude of dc Voltage Sources	N_{IGBT}	N_L	N_D
1st proposed algorithm	$V_0 = V_1 = V$, $V_2 = \ldots = V_j = 2V_{dc}$	$6j + 4$	$20j + 11$	$6j + 4$
2nd proposed algorithm	$V_0 = V_1 = V_{dc}$, $V_2 = 2V_{dc}$, $V_j = 2V_{j-1}$	$6j + 4$	$10V_j + 10V_{j-1} + \ldots + 11V_1 + 1$	$6j + 4$
3rd proposed algorithm	$V_0 = V_1 = V_{dc}$, $V_2 = 3V_{dc}$, $V_j = 3V_{j-1}$	$6j + 4$	$10V_j + 10V_{j-1} + \ldots + 11V_1 + 1$	$6j + 4$
4th proposed algorithm	$V_0 = V_1 = V_{dc}$, $V_2 = 6V_{dc}$, $V_j = 6V_{j-1}$	$6j + 4$	$10V_j + 10V_{j-1} + \ldots + 11V_1 + 1$	$6j + 4$

2.4. The Proposed Multi-Level Inverter Structure

The structure shown in Figure 2 with a reduced switch basic module is assumed to be the basic cell. By connecting these cells in series, the cascaded structure of the proposed topology is realized. Figure 3 shows the proposed cascaded topology with n basic cells. The

cascading method is also a method for generalizing the proposed structure to achieve high voltage levels by using a small number of sources. In addition, in the cascaded topology, the voltage range of H-bridge switches is limited, and it is possible to achieve medium and even high voltage and power levels using limited Maximum Voltage Blocking (MBV) switches.

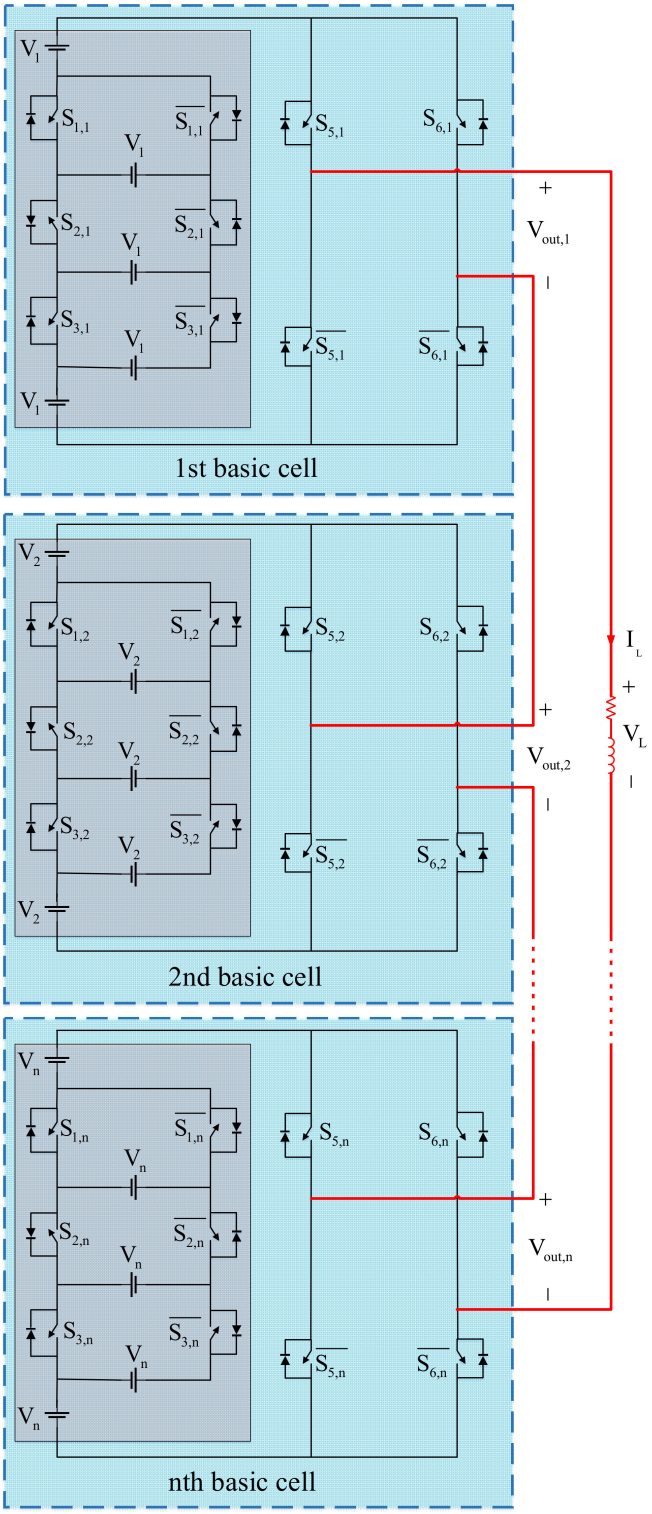


Figure 3. The proposed cascaded topology.

In the cascaded topology, the output voltage (V_L) is obtained from the output voltage of the multiple basic cells:

$$V_L = V_{out,1} + V_{out,2} + \ldots + V_{out,n} \quad (9)$$

In the cascaded topology, different algorithms can be used to generate voltage levels. The cascaded topology can be implemented with the following algorithm.

In this algorithm, the voltage value of independent voltage sources is determined as follows:

$$V_1 = V_{dc},\ V_2 = 11V_{dc}\ ,\quad V_n = 5V_{n-1} + 5V_{n-2} + \ldots + 5V_1 + V_{dc} \quad (10)$$

In the main structure shown in Figure 2, the voltage sources simply have an incremental combination. However, the voltage sources in the cascaded topology, in addition to incremental combination, can also have a decreasing combination, which leads to a significant increase in the number of output voltage levels. The number of voltage levels, the number of IGBTs, and the number of drivers for the cascaded topology are presented in the following equations.

$$N_L = 2(5V_1 + 5V_2 + \ldots + 5V_n) + 1 \quad (11)$$

$$N_{IGBT} = N_S = 10n \quad (12)$$

$$N_D = 10n \quad (13)$$

where n represents the number of basic cells.

One of the advantages of cascaded topology is the replacing capability for the basic cells. If one of the basic cells is damaged, it can be taken out of the circuit, and the structure will continue to work with fewer voltage levels.

3. Efficiency Calculation

In this section, the calculation and simulation of the conduction losses and switching losses are presented to estimate the efficiency of an 11-level basic cell. The conduction losses are divided into two parts: switch conductance losses and anti-parallel diode conduction losses. A detailed analysis of the power losses of a power electronic converter is investigated in the following.

3.1. Conduction Losses

Power electronic switches have conduction losses when conducting the current in ON-state. The conduction losses of the switch and its anti-parallel diode is calculated by the following equations:

$$P_{c,S}(t) = [V_{S,ON} + R_S i^{\alpha}(t)]i(t) \quad (14)$$

$$P_{c,D}(t) = [V_{D,ON} + R_D i(t)]i(t) \quad (15)$$

where S indicates the switch and D indicates the diode. The voltages vs. and V_D are the voltage drop across the switch and the anti-parallel diode in their conduction interval. The resistors R_S and R_D represent the equivalent resistance of the switch and its anti-parallel diode, i(t) is the current flowing through the switch and the anti-parallel diode at the conduction moments. The parameter α is a switch constant that depends on the switch specifications, which is introduced by the manufacturer in the switch datasheet. The conduction losses are calculated from the sum of the conduction losses presented in Equations (14) and (15). The amount of conduction losses of a multi-level inverter depends on the number of switches conducted at different voltage levels. Considering N_S as the conducting number of switches and N_D as the conducting anti-parallel diodes in a time

interval, the average conduction losses of the converter in an output voltage period can be represented by (16):

$$P_c = \frac{1}{2\pi}\int_0^{2\pi}\left[N_S(t)P_{c,S}(t) + N_D(t)P_{c,D}(t)\right]d(t) \tag{16}$$

3.2. Switching Losses

The switching losses are based on the energy losses due to the non-ideal switch performance. The energy losses include switch ON and OFF losses calculated by Equations (17) and (18):

$$\begin{aligned} E_{ON,j} &= \int_0^{t_{ON}} [v(t)\ i(t)]\, d(t) \\ &= \int_0^{t_{ON}} \left[\left(\frac{V_{S,j}}{t_{ON}}\right)\left(-\frac{I'}{t_{ON}}(t - t_{ON})\right)\right] d(t) \ = \frac{1}{6} V_{S,j}\, I'\, t_{ON} \end{aligned} \tag{17}$$

$$\begin{aligned} E_{OFF,j} &= \int_0^{t_{OFF}} [v(t)\ i(t)]\, d(t) \\ &= \int_0^{t_{OFF}} \left[\left(\frac{V_{S,j}}{t_{OFF}}\right)\left(-\frac{I}{t_{OFF}}(t - t_{OFF})\right)\right] d(t) = \frac{1}{6} V_{S,j} I t_{OFF} \end{aligned} \tag{18}$$

which $E_{ON,j}$ and $E_{OFF,j}$ are the energy dissipation of the switch j at the moments of turning on and off, t_{ON} and t_{OFF} are the time intervals required to turn a switch on and off, respectively. The parameters I and I' are the current that passes through the switch before turning it off, and after turning it on. $V_{S,j}$ is the reverse voltage across the switch after it is turned off. The switching power losses of switches in an output voltage period can be written as follows:

$$P_s = \sum_{j=1}^{N_S}\left[\sum_{i=0}^{N_{ON,j}} E_{ON,ji} + \sum_{i=0}^{N_{OFF,j}} E_{OFF,ji}\right] f \tag{19}$$

which $N_{ON,j}$ and $N_{OEE,j}$ are the number of times that switch turns on and off in a cycle, and f is the output voltage frequency. Finally, the total losses are calculated by Equation (20):

$$P_{Total} = P_c + P_s \tag{20}$$

To investigate the efficiency of the proposed 11-level basic cell, power losses on proposed MLI at the output loads Z_1 = 50 Ω, Z_2 = 50 + j12.56 Ω, and Z_3 = 50 + j25.12 Ω are simulated with output voltage steps of 50 V. Figure 4a, b show the conduction and switching power losses for all three types of the loads, respectively. Besides, the efficiency and total losses are also displayed in Figure 4c. To compare the efficiency of the proposed 11-level structure, the efficiency curve for different output power is shown in Figure 5.

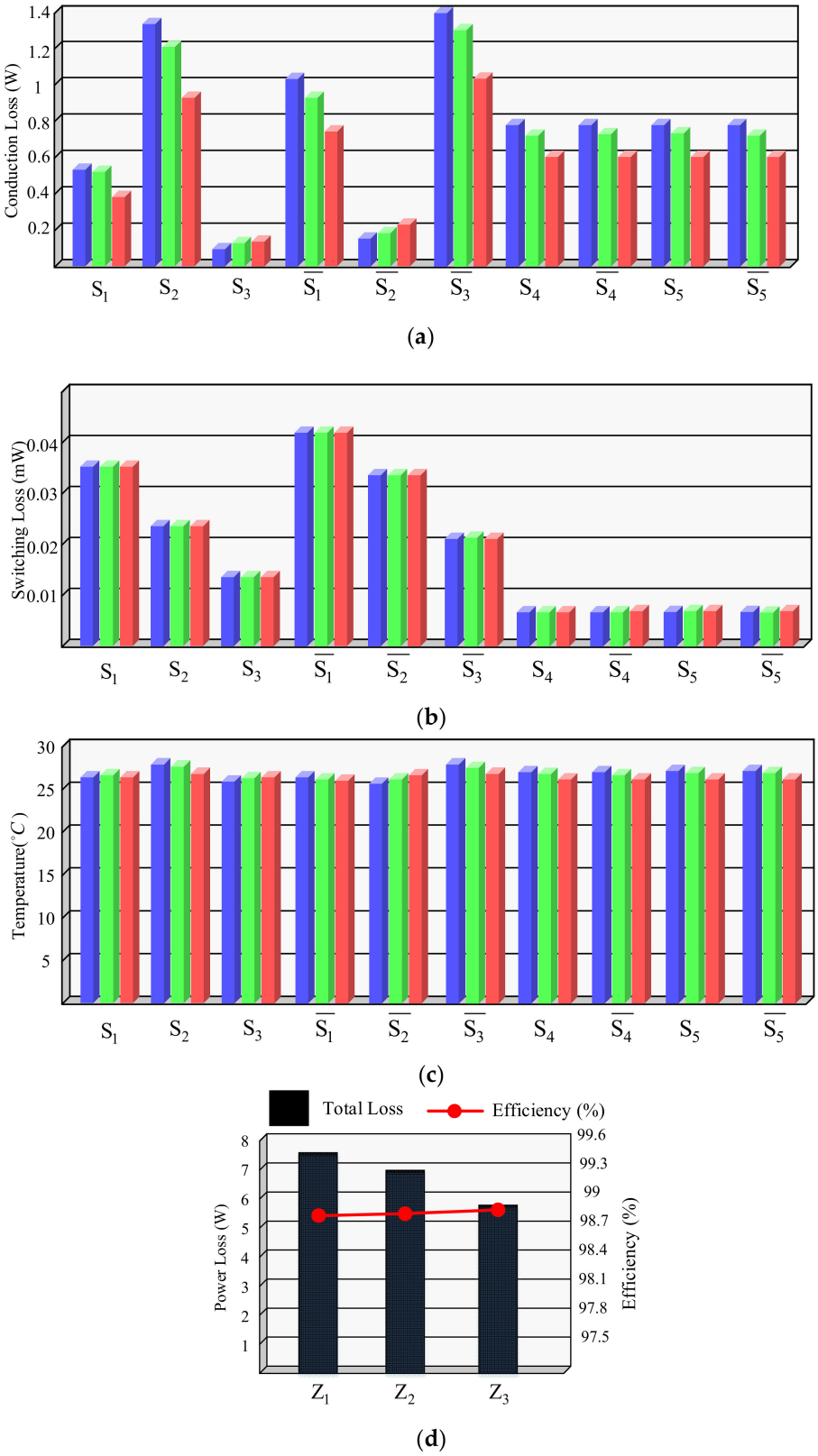


Figure 4. (**a**) Power losses and efficiency curves for the proposed 11-level basic cell topology at three types of loads, (**a**) Conduction losses, (**b**) Switching losses, (**c**) Temperature of switches, (**d**) Efficiency and total losses.

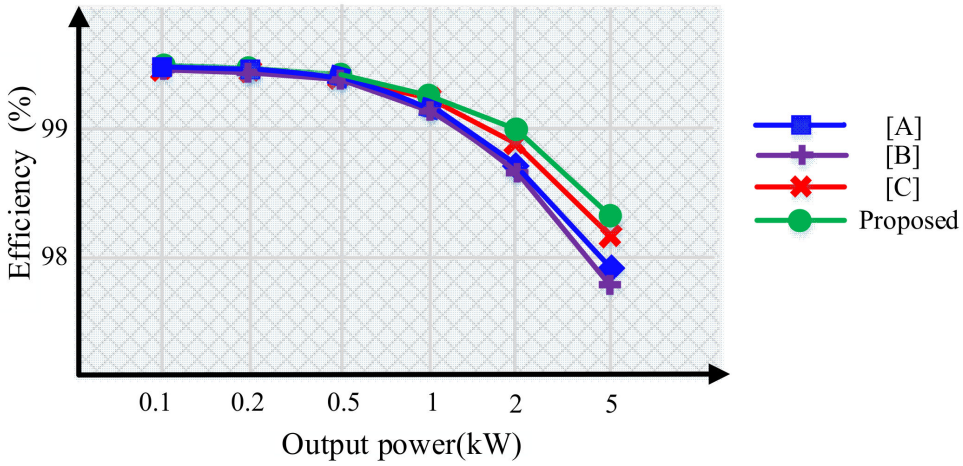


Figure 5. Efficiency comparison of the proposed 11-level basic cell with other topologies. [A] Alishah et al., 2021, [B] Jayabalan et al., 2017, [C] Ponraj et al., 2021.

4. Comparative Study

In this section, the proposed topology is compared with other recent topologies presented in [13–31] to evaluate the validity and capability of the proposed MLI. For a fair comparison of the structures, a graph of the number of switches to different voltage levels is presented, and in addition, the N_{IGBT}/N_L ratio is calculated and presented in Table 3 for the proposed basic module and the comparative structures. Moreover, Table 3 lists other comparative parameters, including N_{IGBT} (number of IGBTs), N_{GD} (number of drivers), N_L (number of voltage levels synthesized by structure), N_{DC} (number of DC voltage source), TBV (total blocking voltage), N_D (number of Diodes) and $N_{IGBT,\,ON}$ (number of conducting IGBTs in each voltage level) for the proposed topology and other symmetric topologies. According to this Table, the presented basic module utilizes fewer switches for various voltage levels.

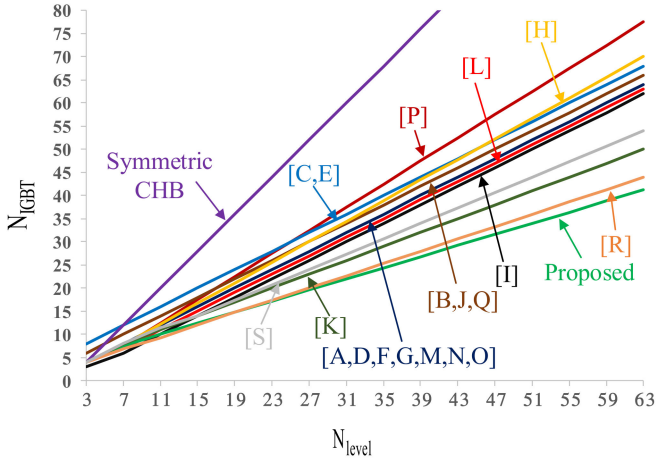
To fairly compare the number of IGBTs in the proposed structure with other structures, a graph of the number of IGBTs relative to the number of voltage levels (N_{IGBT}/N_L) is evaluated. This ratio also provides cost-effectiveness of structures. The larger this ratio, the steeper the slope of the comparison curve, and the more IGBTs are used to achieve higher output voltage levels. Furthermore, the smaller this ratio, the lower the slope of the comparison curve, and the fewer IGBTs are required.

As shown in Figure 6a, using the proposed structure, a large number of voltage levels can be achieved with a smaller number of IGBTs, which produces high-quality output voltage with a smaller number of switches. Some structures use bidirectional common-emitter switches, which makes the number of gate drivers different from the number of IGBTs. For a fair comparison of the number of gate drivers of the proposed structure with other structures, the ratio of the number of gate drivers to the number of voltage levels (N_{GD}/N_L) is presented. Figure 6 demonstrates the (N_{IGBT}/N_L) and (N_{GD}/N_L) diagrams for the proposed and other structures. As shown in Figure 6a, the proposed topology has the lowest slope for (N_{IGBT}/N_L) diagram, which means the proposed structure utilizes the lowest number of switches to generate different voltage levels. Figure 6b also shows a comparison of the number of gate drivers, in which the proposed structure does not have the lowest curve slope regarding the number of gate drivers since it has not utilized a bidirectional switch. Nevertheless, the proposed structure still has a relatively good condition regarding the number of gate drivers compared to most comparative structures.

Table 3. Comparing the parameters of the proposed topology with other basic topologies.

	N_{IGBT}	N_{GD}	N_L	N_{DC}	TBV(* V_{dc})	N_D	$N_{IGBT,ON}$	N_{IGBT}/N_L
[13]	10	10	9	4	22	0	5	1.11
[14]	12	10	9	4	24	0	7	1.33
[15]	12	9	7	3	18	0	7	1.71
[16]	10	10	7	3	20	0	5	1.42
[17]	10	7	7	3	21	1	4	1.42
[18]	8	7	7	3	14	0	4	1.14
[19]	8	7	7	3	18	0	4	1.14
[20]	5	5	3	2	9	4	2	1.66
[21]	6	6	7	4	12	0	3	0.85
[22]	12	10	9	4	24	0	7	1.33
[23]	11	10	11	5	31	1	5	1
[24]	11	10	11	5	31	2	4	1
[25]	8	8	7	3	12	0	3	1.14
[26]	10	8	9	4	20	0	4	1.11
[27]	10	10	9	4	20	0	5	1.11
[28]	10	7	7	3	20	0	3	1.42
[29]	10	9	7	3	14	0	4	1.42
[30]	10	9	9	4	18	0	4	1.11
[31]	9	9	9	4	22	1	5	1
Proposed	10	10	13	5	30	0	5	0.77

* Indicates product symbol.



(**a**)

Figure 6. *Cont.*

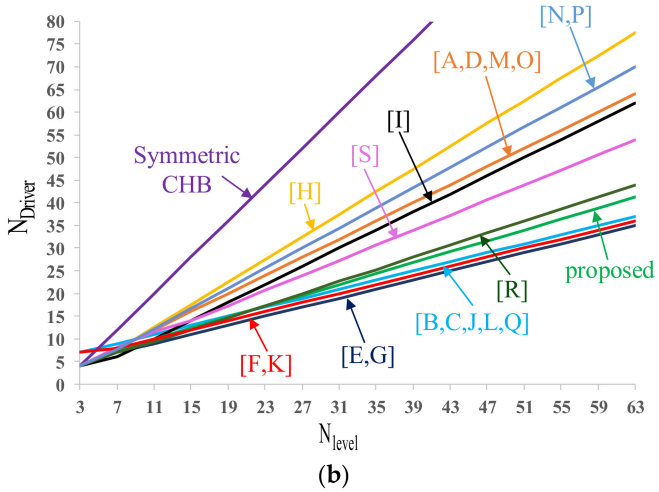


Figure 6. Comparative diagrams including: (**a**) N_{IGBT}/N_L, (**b**) N_{GD}/N_L. [A] Oskuee et al., 2015, [B] Alishah et al., 2021, [C] Jayabalan et al., 2017, [D] Ponraj et al., 2021, [E] Peddapati 2020, [F] Siddique et al., 2019, [G] Samsami et al., 2017, [H] Dhanamjayulu et al., 2017, [I] Gohari et al., 2019, [J] Alishah et al., 2016, [K] Hosseinpour et al., 2020, [L] Hosseini Montazer et al., 2021, [M] Selvaraj et al., 2020, [N] Meraj et al., 2019, [O] Ponraj et al., 2021, [P] Lee et al., 2017, [Q] Siddique et al., 2019, [R] Ali 2018, [S] Seifi et al 2020.

The total blocking voltage (TBV), the sum of the maximum blocking voltage (MBV) of the converter switches, is an essential parameter in comparing and evaluating structures because the voltage rating of required IGBTs for the structure is determined based on the MBV parameter, and the TBV parameter is directly related to the cost of the structure switches. Here, for a fair comparison of the TBV value, a graph of the ratio of this parameter to the number of output voltage levels (TBV/N_L) is used, and this graph is plotted for different topologies, as shown in Figure 7. As Figure 7 displays, the proposed structure provides a relatively good TBV compared to other structures.

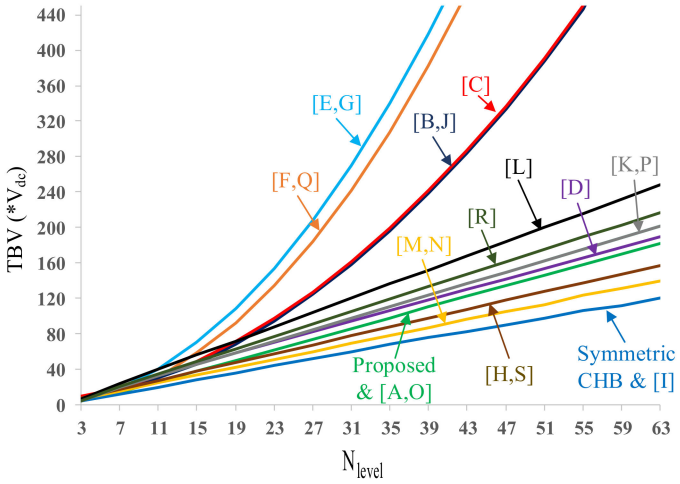


Figure 7. TBV/N_L diagram for the proposed structure and other structures.* Indicates product symbol. [A] Oskuee et al., 2015, [B] Alishah et al., 2021, [C] Jayabalan et al., 2017, [D] Ponraj et al., 2021, [E] Peddapati 2020, [F] Siddique et al., 2019, [G] Samsami et al., 2017, [H] Dhanamjayulu et al., 2017, [I] Gohari et al., 2019, [J] Alishah et al., 2016, [K] Hosseinpour et al., 2020, [L] Hosseini Montazer et al., 2021, [M] Selvaraj et al., 2020, [N] Meraj et al., 2019, [O] Ponraj et al., 2021, [P] Lee et al., 2017, [Q] Siddique et al., 2019, [R] Ali 2018, [S] Seifi et al., 2020.

5. Simulation and Laboratory Results of the Proposed Structure

To investigate the performance of the proposed structure, a prototype containing two RSBM is simulated, and a laboratory prototype is implemented. The proposed structure containing two RSBM is investigated for the symmetric and asymmetric topologies. The laboratory sample hardware includes MOSFET IRFP460 power switches. The ARDUINO MEGA2560 microcontroller is used to generate gate pulses, which are isolated and amplified to drive the switches using the TLP250 optocoupler. The laboratory prototype and related instruments are shown in Figure 8.

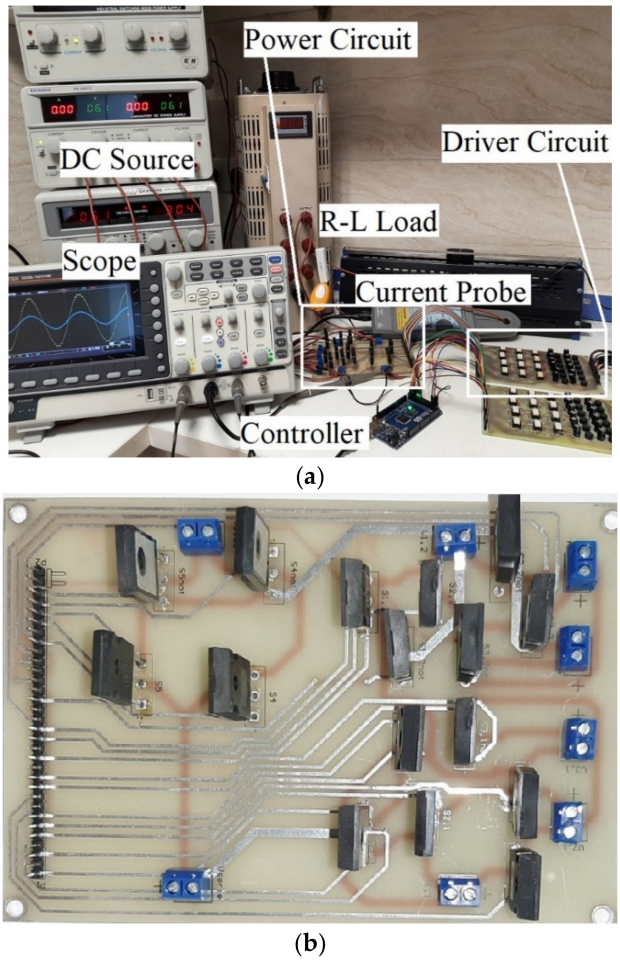


Figure 8. (**a**) A laboratory prototype of the proposed structure, (**b**) The power circuit of proposed structure.

As it is known, multi-level inverter switching methods are classified into two categories according to the switching frequency, which can be low frequency or high frequency, respectively. From the first class it can be mentioned the staircase switching, fundamental frequency switching, active harmonic elimination, nearest level modulation (NLM) and selective harmonic elimination (SHE) technique. The second class includes sinusoidal PWM and space vector modulation (SVM) techniques. The modulation methods in both classes can be easily adapted and implemented to the topology proposed in this paper. The NLM method has been used to generate the switching pulses (see Figure 9a), using an integer that is close to the nearest voltage level as the reference signal. For example, if the voltage is in the range of 1.5 to 2.5, then the reference of 2Vdc will be generated. Figure 9b presents the NLM operation. The switching frequency is not well-known in NLM method. But it is low and is relatively near to output voltage frequency. The output voltage frequency is considered 50 Hz.

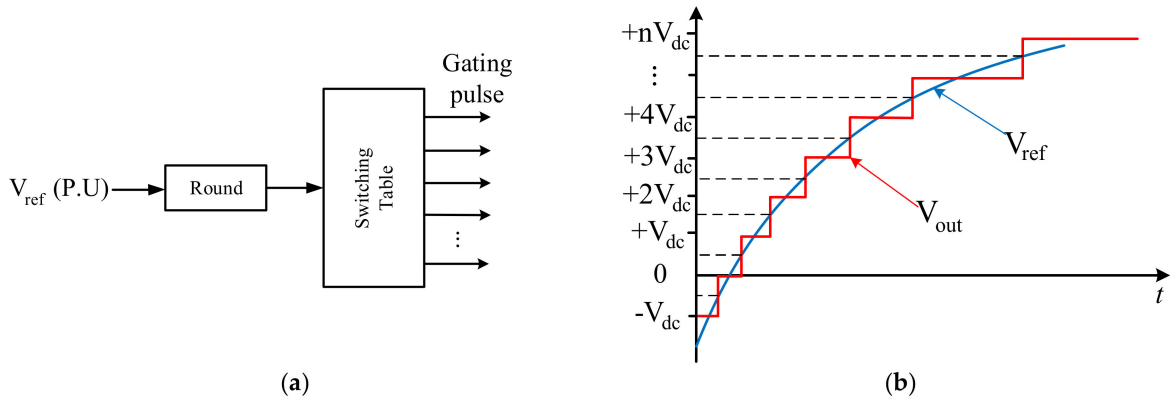


Figure 9. (**a**) NLM method, (**b**) The NLM operation.

In symmetric topology, the value of DC voltage sources is $V_0 = V_1 = V_2 = 6$ V. First, the inverter results for a purely resistive load $Z_{load1} = 6.6\ \Omega$ are presented in Figure 10. The peak output voltage of the inverter with 11 levels of 6 V steps results in 66 volts. The peak load current, in this case, is 10A. The harmonic spectrum of the proposed topology is presented in Figure 10c, highlighting that the total harmonic distortion (THD) is 3.25%, with advantage in size and cost of the output filter.

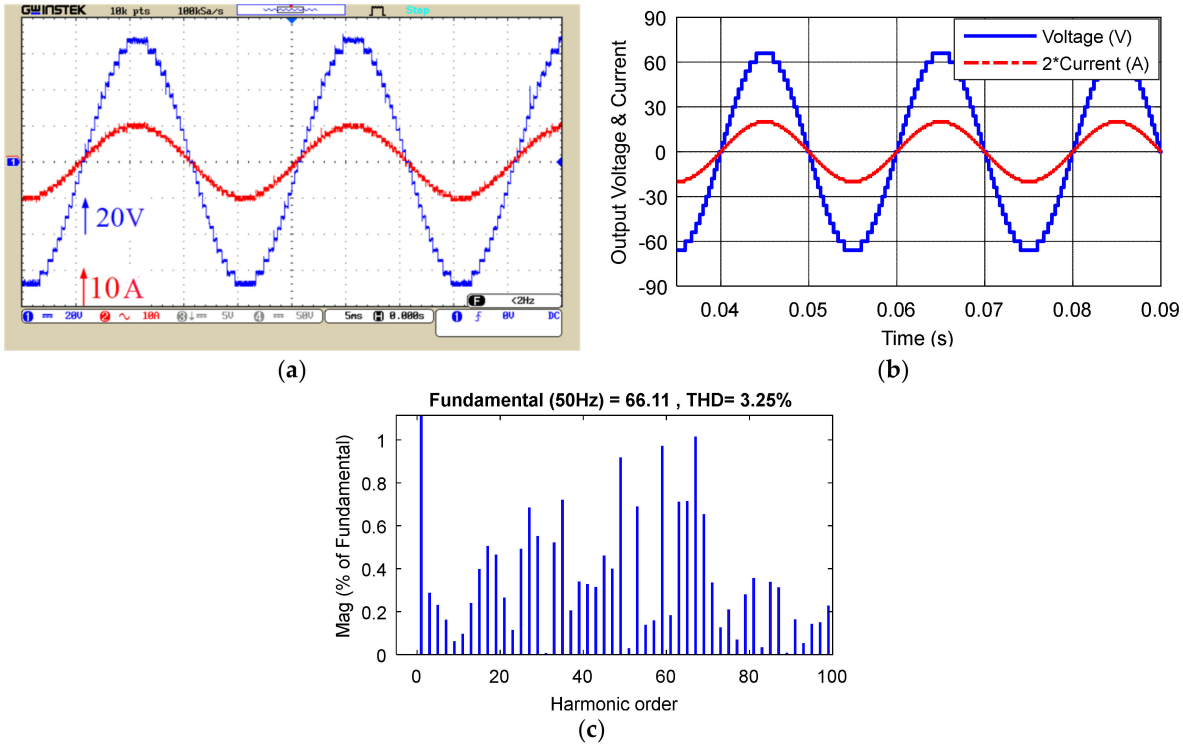


Figure 10. The waveforms for resistive output load in symmetric topology, (**a**) laboratory sample voltage and current, (**b**) simulation voltage and current, (**c**) output voltage THD. * Indicates product symbol.

Additionally, Figure 11 displays the results of the proposed structure in the case of symmetric sources for a resistive-inductive load $Z_{load2} = 6.6 + j4.71\ \Omega$. The peak load current in the case of R-L output load is 8.1 A, in which the inductance of the load filters, the current, and the load current is obtained similar to a sine wave.

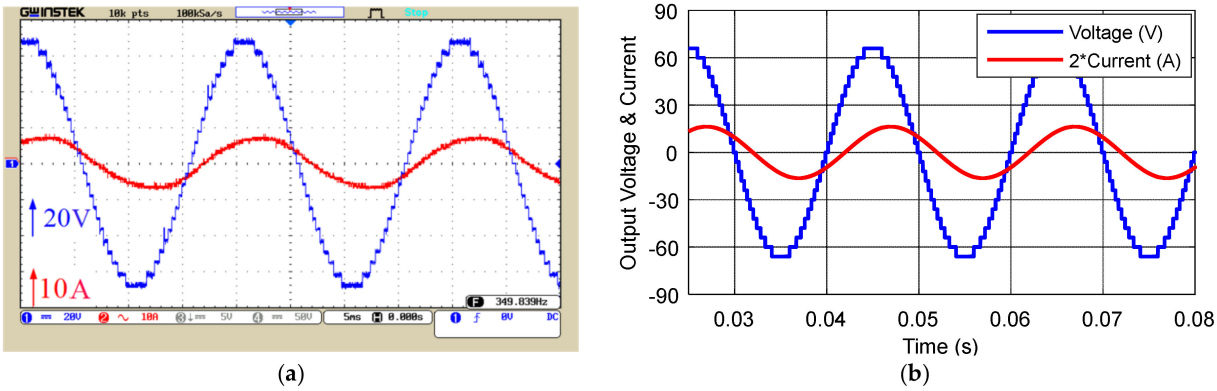


Figure 11. Resistive-inductive load waveforms in symmetric topology, (**a**) laboratory sample voltage and current, (**b**) simulation voltage and current. * Indicates product symbol.

To analyze and introduce the response of the proposed MLI in a dynamic situation, the modulation index changes abruptly, and the system response is evaluated. It should be noted that, this test is only open loop dynamic responses. As shown in Figure 12, for this purpose, the modulation index is once changed from 1 to 0.65 according to Figure 12a, and again according to Figure 12b, the modulation index is changed from 0.65 to 0.3. The proper performance of the proposed multi-level inverter in dynamic conditions is visible for changing the modulation index in Figure 12.

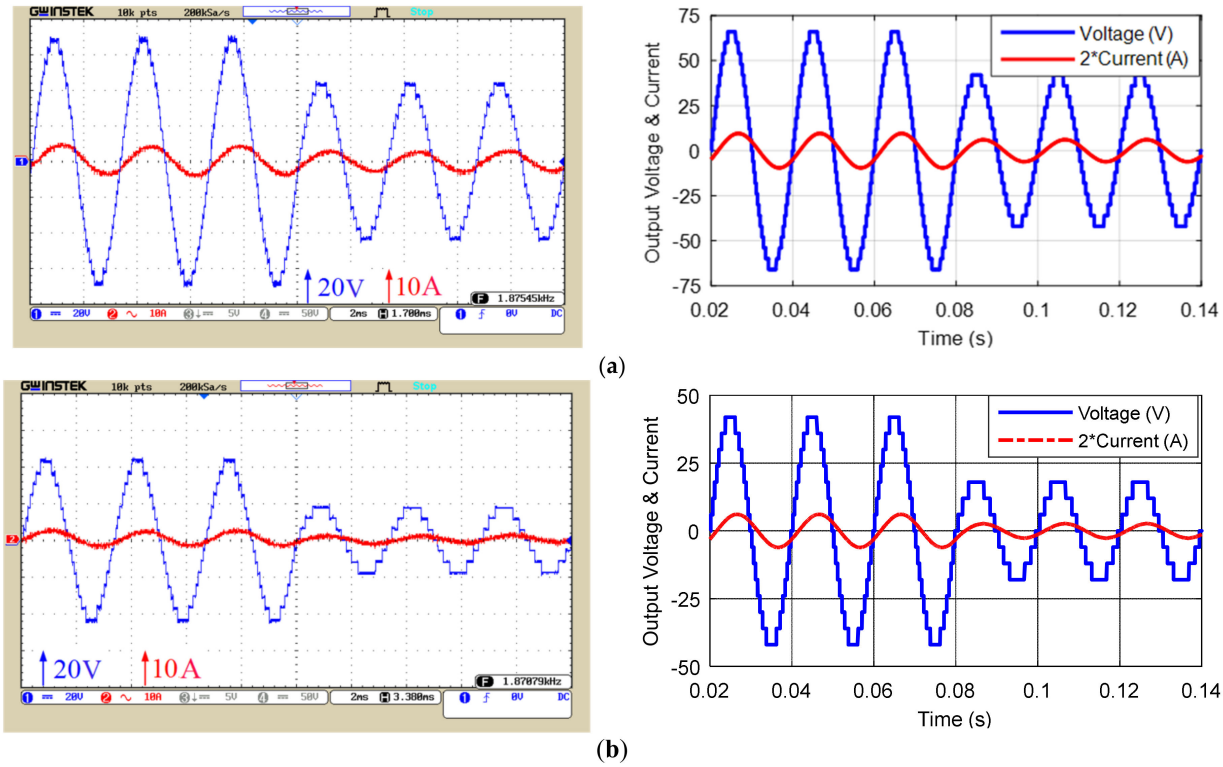
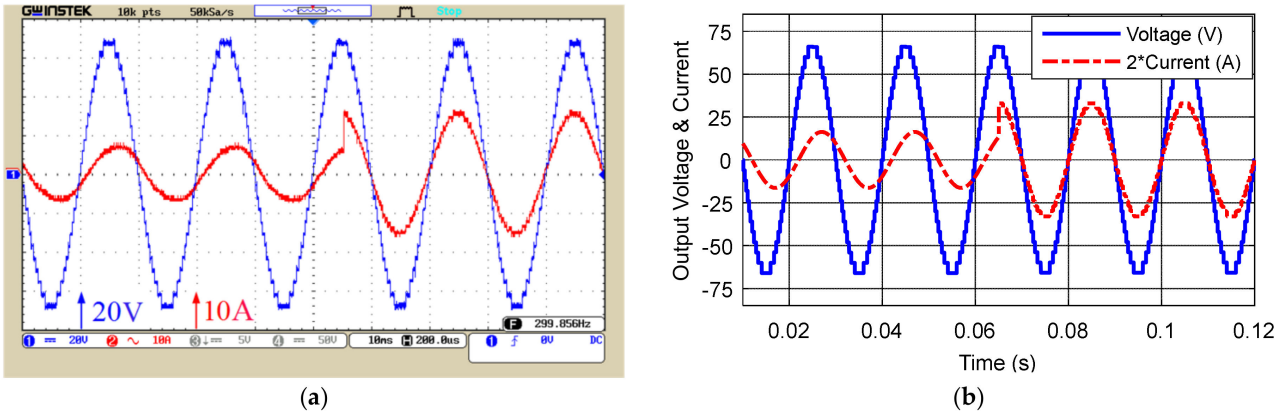


Figure 12. Voltage and current waveforms for changes of the modulation index: (**a**) from 1 to 0.65 and (**b**) from 0.65 to 0.3. * Indicates product symbol.

The behavior of the proposed structure for a sudden change in load is evaluated as well. For this purpose, the load changes abruptly from resistive-inductive to pure resistive. Figure 13 illustrates inverter output voltage and current for a sudden change of the resistive-inductive load Z_{load2} = 6.6 + j4.71 Ω to a purely resistive load Z_{load3} = 4 Ω. The proposed structure performs well under dynamic load change conditions as well.



(**a**) (**b**)

Figure 13. Voltage and current waveforms related to load's dynamic change, (**a**) laboratory result, (**b**) simulation result. * Indicates product symbol.

Figure 14 displays the blocking voltage for switches of the proposed structure in the symmetric topology. Based on these curves, the maximum voltage across each switch is determined. These diagrams confirm the correct operation of the proposed structure.

To evaluate the performance of multi-level inverter in asymmetric topology, the value of DC voltage sources is selected based on the proposed fourth algorithm according to Table 2 and assumed as $V_0 = V_1 = 2$ V, $V_2 = 12$ V. The performance results of the proposed multi-level inverter with asymmetric topology for a resistive-inductive load are presented in Figure 15. The number of voltage steps increases from 11 levels in the symmetric topology to 36 levels of 2 V steps in the asymmetric topology. In this case, the peak output voltage results in 72 V. The peak load current equals 11.4 A in this condition. Figure 15b displays the zoomed staircase waveform of the output voltage. The proper performance of the proposed structure is clearly shown in this figure in the production of voltage steps. In addition, the THD value is decreased from 3.26% in the symmetric topology to 1.01% in the asymmetric topology. This THD value demonstrates that the asymmetric topology of the suggested MLI can operate properly without any output filter, which results in more reduction in overall size and cost.

Dynamic load testing is necessary to evaluate the capability of the proposed structure in the application of electric motor drives. Based on the simulation results and laboratory results of the prototype, it can be concluded that the performance of the proposed structure is satisfactory, and the proposed topology provides a desirable performance.

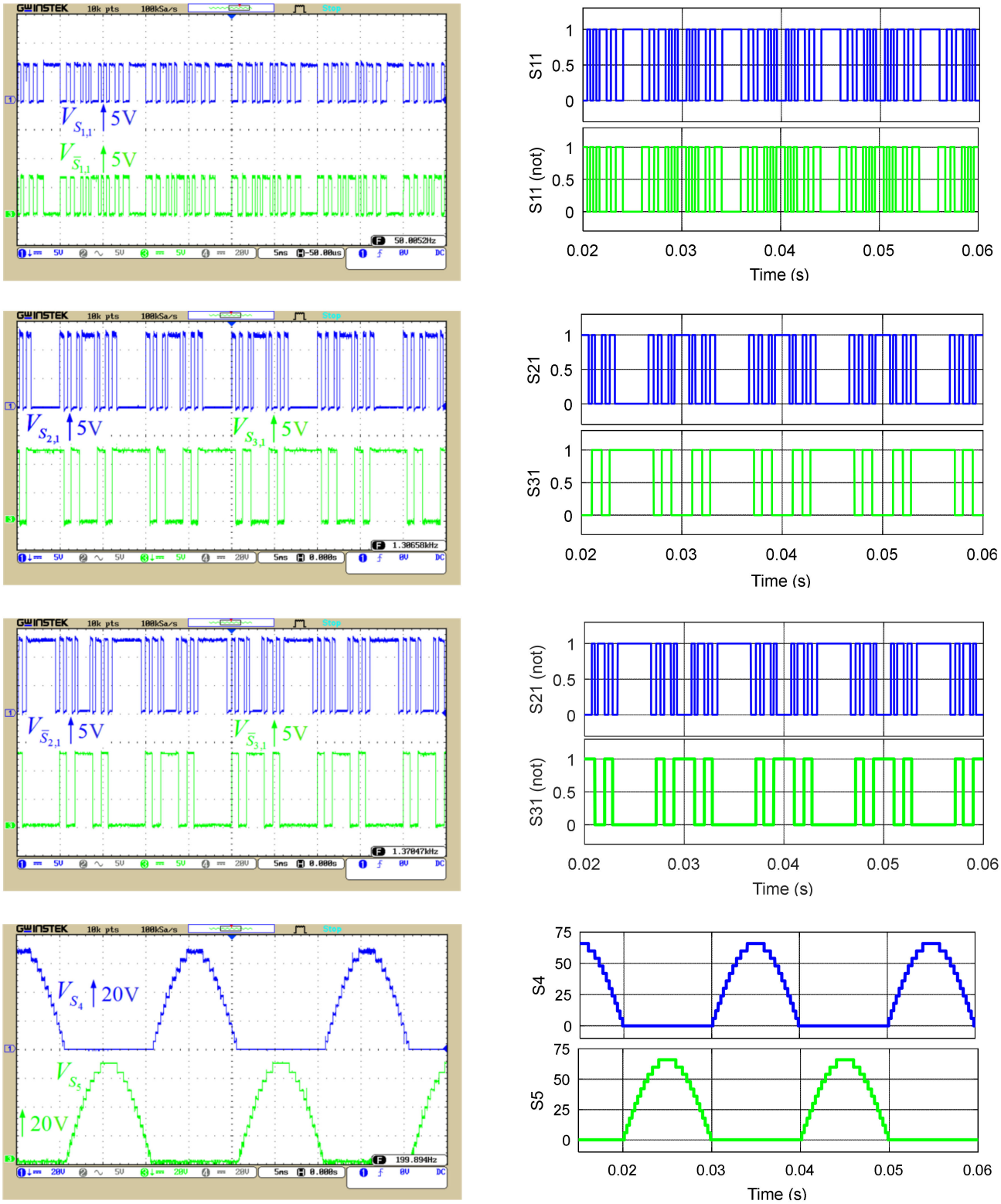


Figure 14. Blocking voltage of the proposed structure switches for symmetric topology.

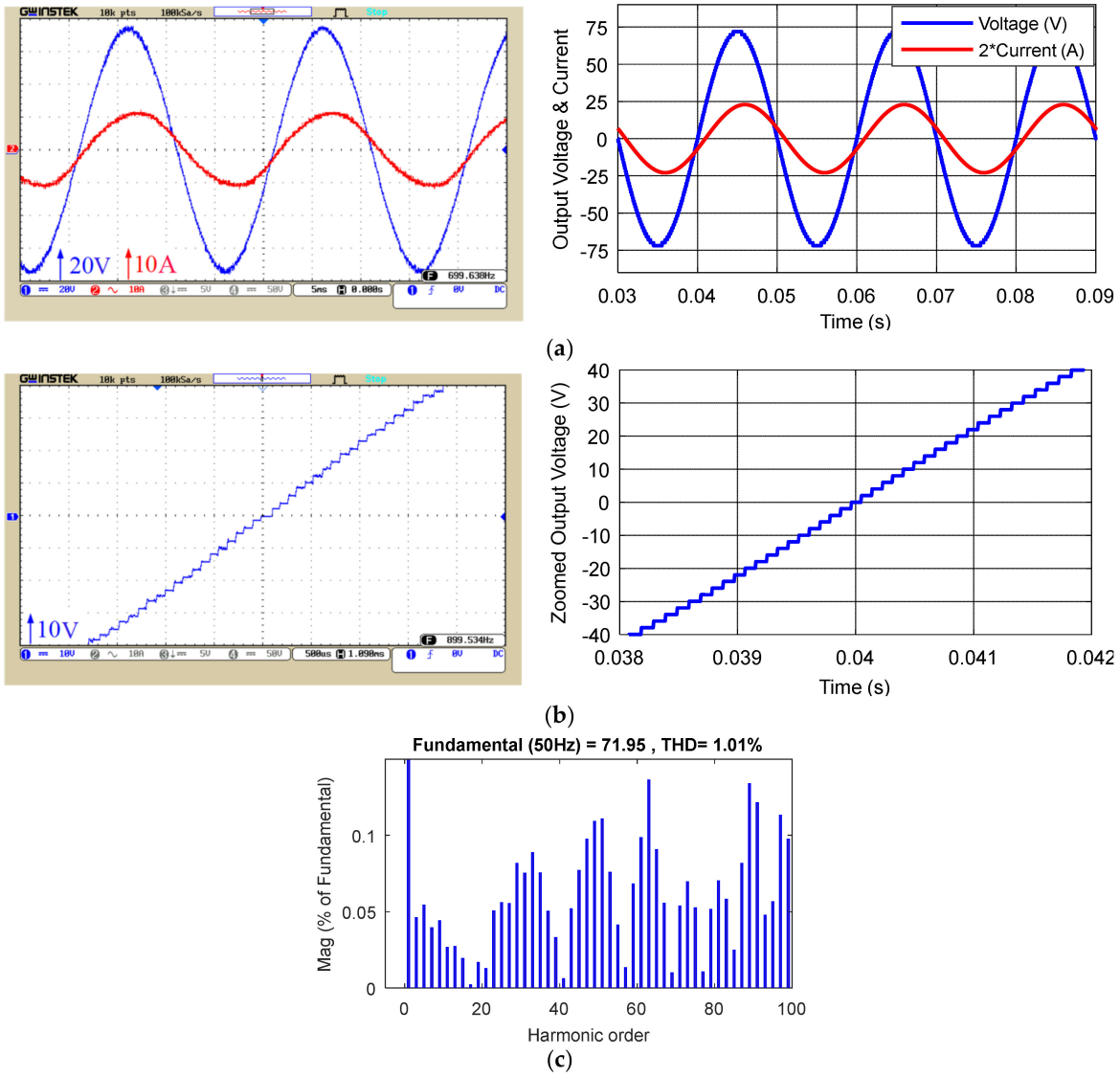


Figure 15. The waveforms of Proposed MLI in asymmetric topology (**a**) voltage and current, (**b**) zoomed voltage, (**c**) output voltage THD. * Indicates product symbol.

6. Conclusions

In this paper, a novel configuration is proposed for multi-level voltage source inverters to reduce the number of switches. The proposed structure uses a reduced switch basic module to generate more output voltage levels. This structure is investigated for symmetric and asymmetric topologies. The efficiency of the structure is presented for different loads and compared with several other structures. The result is shown that the suggested inverter has higher efficiency. Besides, the comparison in terms of circuit devices reveals that the number of switches of the proposed structure is less than other reported structures. This difference in the number of switches is clearly evident at higher levels, and the graph slope of the number of switches to the number of levels is 0.6, which is less than other structures. Also, the number of gate driver, as well as the TBV parameter are in good situation and superior in comparison with most of similar structures. These results make that the proposed structure has a low cost and size. The performance of the proposed structure is confirmed by simulation and laboratory results. In the laboratory prototype, different loading conditions, including resistive load, resistive-inductive load as well as dynamic load, have been used to validate the proposed structure. Modulation index change is also performed for the proposed structure. Results evaluation of simulations

and laboratory samples, as well as the results of comparisons, indicate the appropriate performance of the proposed structure.

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