

Article

# A Smart Floating Gate Transistor with Two Control Gates for Active Noise Control

Cheng Mao, Cheng Yang, Haowen Ma, Feng Yan and Limin Zhang \* 

School of Electronic Science and Engineering, Nanjing University, Nanjing 210023, China; 13771683113@163.com (C.M.); njuyangcheng@163.com (C.Y.); mahaowen2012@163.com (H.M.); fyan@nju.edu.cn (F.Y.)

\* Correspondence: lmzhang@nju.edu.cn

Received: 16 September 2019; Accepted: 24 October 2019; Published: 25 October 2019

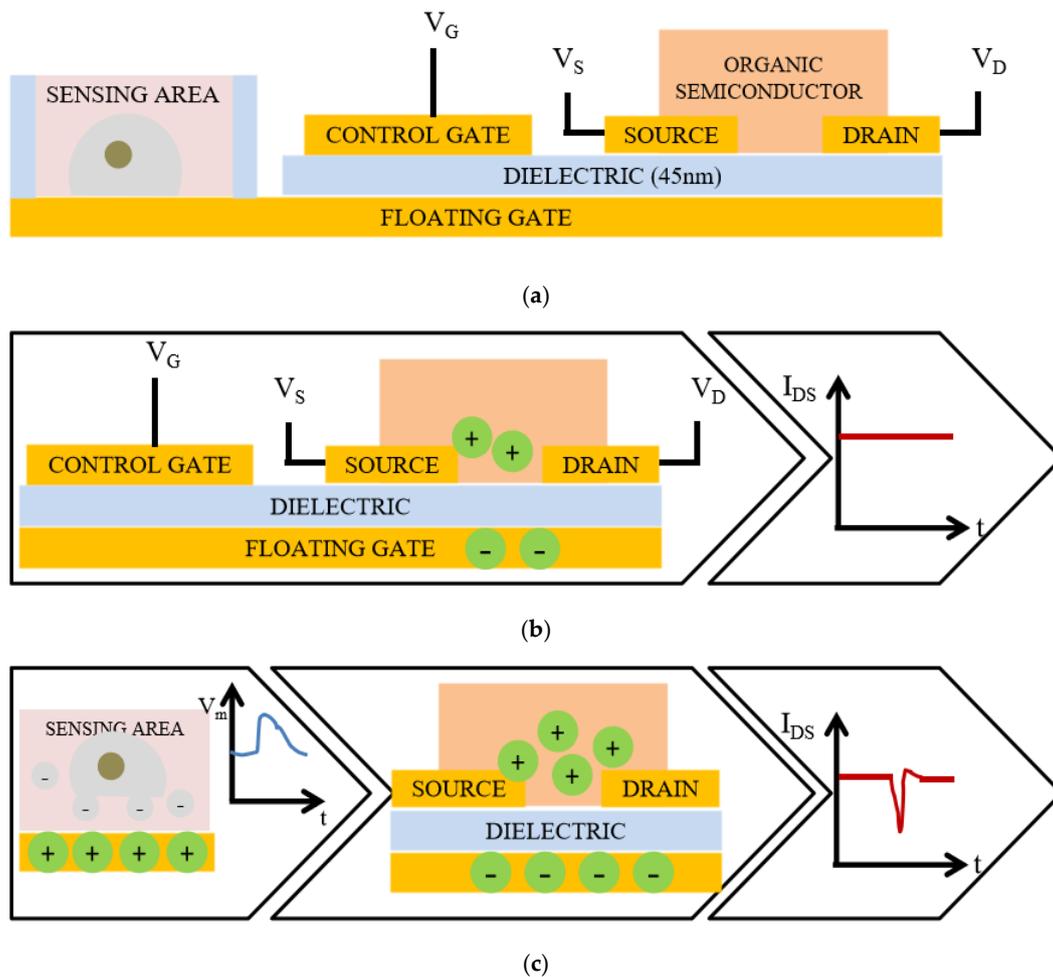


**Abstract:** A smart floating gate transistor with two control gates was proposed for active noise control in bioelectrical signal measurement. The device, which is low cost and capable of large-scale integration, was implemented in a standard single-poly complementary metal–oxide–semiconductor (CMOS) process. A model of the device was developed to demonstrate the working principle. Theoretical analysis and simulation results proved the superposition of the two control gates. A series of test experiments were carried out and the results showed that the device was in accordance with the basic electrical characteristics of a floating gate transistor, including the current–voltage ( $I$ – $V$ ) characteristics and the threshold characteristics observed on the two control gates. Based on the source follower circuit, the experimental results proved that the device can reduce interference by more than 29 dB, which demonstrates the feasibility of the proposed device for active noise control.

**Keywords:** floating gate transistor; control gate; CMOS device; active noise control

## 1. Introduction

There is growing interest in detecting chemical or bioelectrical signals with solid-state sensors in a complementary metal–oxide–semiconductor (CMOS) process [1,2]. One of the major classes of solid-state sensors is based on the field-effect transistor (FET) [3–5]. The multiparametric nature and intrinsic signal amplification ability of FETs make them capable of achieving well beyond what is possible with two terminal devices. The ion-sensitive field-effect transistor (ISFET) [6,7] is an important branch of FET and has attracted great research interest regarding chemical signal detection due to its small size, capability of mass fabrication, and fast response time. The organic thin-film transistor (OTFT) [8–10] is another meaningful branch and has been extensively studied for bioelectrical signal detection. For example, a sensing platform based on floating gate OTFTs is used for bioelectrical signal sensing [11–14]. The working principle of a floating gate organic charge-modulated field-effect transistor (OCMFET) is shown in Figure 1a, where the sensing area is part of the floating gate exposed to the surrounding bioelectrochemical environment to detect signals, and the control gate is used to set the working point with the control capacitor, as shown in Figure 1b. Ionic or cell charge variations occurring in close proximity to the sensing area cause a charge separation in the floating gate, which leads to a modulation of the charge carrier density inside the channel of the transistor, as shown in Figure 1c [15]. The OCMFET device can detect signals in the frequency range of cell electrical activity (10–1000 Hz) and can work without any external reference electrode. However, the floating gate and sensing area are integrated as a whole and can only detect charge signals, which is not suitable for detecting voltage signals because the voltage signal on the floating gate fixes the working point of the device. In addition, it is difficult for the device to suppress interference, which is important for small signal detection.



**Figure 1.** Working principle of a floating gate organic charge-modulated field-effect transistor (OCMFET). (a) Cross section of the device, where the floating gate is exposed to the surrounding bioelectrochemical environment as the sensing area. (b) The setting of the working point by applying the appropriate  $V_G$ . (c) The charge sensing and modulation principle of the device, where the charge variations occurring in close proximity to the sensing area cause a charge separation in the floating gate, which leads to modulation of the charge carrier density inside the channel of the transistor and variation of the output current.

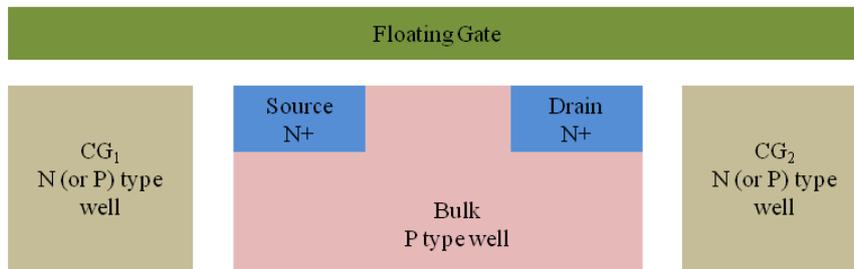
In order to detect voltage signals, some modifications must be made, such as separating the sensing area and the floating gate. Moreover, the detected signal is accompanied by some interference and the interference can also modulate the channel charge. To suppress the interference actively, the active noise control (ANC) concept has been introduced, which cancels the unwanted primary interference by using a secondary source for signal superposition [16–18]. Generally, two input ports are required to achieve active noise control, where one input port is used for primary source detection and another for secondary source input [19]. Therefore, we have proposed a smart floating gate transistor with two control gates (called an ANC device), which is characterized by active noise control and a low-cost standard CMOS process.

Firstly, the physical model of the proposed device was developed to demonstrate the working principle, and the layout of the device was implemented in a standard single-poly CMOS process. Secondly, simulation results are illustrated to show the ANC performance based on the proposed device. Finally, the experimental electrical characterizations of the fabricated device are provided, which demonstrate the feasibility of the device for active noise control applications.

## 2. ANC Device

### 2.1. Device Structure

The proposed ANC device is based on an evolution of a single-poly metal–oxide–semiconductor field-effect transistor (MOSFET) and the cross section of the proposed ANC device is shown in Figure 2, including a source region (S), a drain region (D), a bulk region (B), a floating gate (FG), and two control gates (CG<sub>1</sub> and CG<sub>2</sub>). Two heavily doped N<sup>+</sup> regions are generated on a P-type bulk to serve as the source and the drain, and two N- or P-type physically isolated wells are generated beside the bulk to serve as the two control gates CG<sub>1</sub> and CG<sub>2</sub>, respectively. The floating gate is generated by a single-poly layer, which is isolated from the bulk and the two control gates by a dielectric layer. The floating gate overlaps the bulk and the two control gates, which leads to the coupling capacitors. The channel current of the proposed device is controlled with two control gates by the coupling capacitors with the floating gate. In application, control gates CG<sub>1</sub> and CG<sub>2</sub> are connected to two standard PADs to receive voltage signals. The source, drain, and bulk are connected to three standard PADs for the normal working condition setting.



**Figure 2.** Cross section of the proposed active noise control (ANC) device based on an evolution of a single-poly metal–oxide–semiconductor field-effect transistor (MOSFET), including a source region (S), a drain region (D), a bulk region (B), a floating gate (FG), and two control gates (CG<sub>1</sub> and CG<sub>2</sub>).

### 2.2. Device Model

The equivalent schematic diagram of the proposed ANC device is shown in Figure 3a, where  $C_{FC1}$ ,  $C_{FC2}$ ,  $C_S$ ,  $C_D$ , and  $C_B$  are the capacitors between the floating gate and the control gate CG<sub>1</sub>, the control gate CG<sub>2</sub>, the source, the drain, and the bulk region, respectively. Considering that the charge  $Q$  of the floating gate should be equal to 0, the simple model of the proposed device is expressed in Equation (1) [20]:

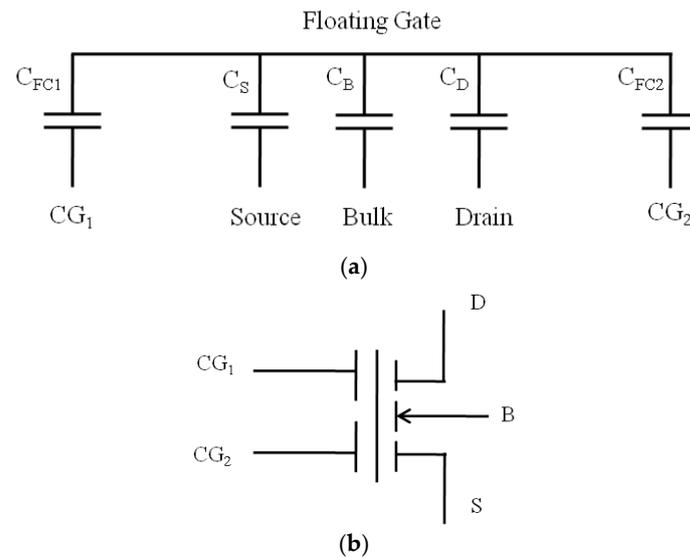
$$Q = 0 = C_{FC1}(V_{FG} - V_{CG1}) + C_{FC2}(V_{FG} - V_{CG2}) + C_S(V_{FG} - V_S) + C_D(V_{FG} - V_D) + C_B(V_{FG} - V_B) \quad (1)$$

where  $V_{FG}$  is the potential on the floating gate;  $V_{CG1}$  is the potential on the control gate CG<sub>1</sub>;  $V_{CG2}$  is the potential on the control gate CG<sub>2</sub>; and  $V_S$ ,  $V_D$ , and  $V_B$  are the potentials on the source, the drain, and the bulk, respectively. Defining the total capacitors  $C_T$  as the sum of the capacitors of  $C_{FC1}$ ,  $C_{FC2}$ ,  $C_S$ ,  $C_D$ , and  $C_B$ , the potential on the floating gate due to capacitive coupling can be expressed as

$$V_{FG} = \frac{C_{FC1}}{C_T} V_{CG1} + \frac{C_{FC2}}{C_T} V_{CG2} + \frac{C_S}{C_T} V_S + \frac{C_D}{C_T} V_D + \frac{C_B}{C_T} V_B. \quad (2)$$

For  $C_S$  and  $C_D$  being far less than  $C_T$ , and the bulk being grounded, Equation (2) can be simplified as

$$V_{FG} = \frac{C_{FC1}}{C_T} V_{CG1} + \frac{C_{FC2}}{C_T} V_{CG2}. \quad (3)$$



**Figure 3.** (a) The simple model of the equivalent schematic diagram of the proposed ANC device, where  $C_{FC1}$ ,  $C_{FC2}$ ,  $C_S$ ,  $C_D$ , and  $C_B$  are the capacitors between the floating gate and the control gate  $CG_1$ , the control gate  $CG_2$ , the source, the drain, and the bulk region, respectively. (b) Symbols for the ANC device with five terminals.

Generally,  $CG_1$  and  $CG_2$  are equivalent in terms of electrical characteristics and one of them is always set to zero for measurement of the threshold voltage, so the threshold voltages and conductivity factors of the floating gate and control gates  $CG_1$  and  $CG_2$  satisfy the following relationships:

$$V_T^{FG} = \frac{C_{FC1}}{C_T} V_T^{CG1} = \frac{C_{FC2}}{C_T} V_T^{CG2} \tag{4}$$

$$\beta^{FG} = \frac{C_T}{C_{FC1}} \beta^{CG1} = \frac{C_T}{C_{FC2}} \beta^{CG2} \tag{5}$$

where  $V_T^{FG}$  is the threshold for the floating gate,  $V_T^{CG1}$  is the threshold for control gate  $CG_1$ ,  $V_T^{CG2}$  is the threshold for control gate  $CG_2$ ,  $\beta^{FG}$  is the conductivity factor for the floating gate,  $\beta^{CG1}$  is the conductivity factor for control gate  $CG_1$ , and  $\beta^{CG2}$  is the conductivity factor for control gate  $CG_2$ .

Accordingly, the transformed current–voltage (I–V) equations of the proposed ANC device in the triode region (TR) and the saturation region (SR) can be expressed by

$$I_D = \beta^{CG1} \left[ \left( V_{CG1} + \frac{C_{FC2}}{C_{FC1}} V_{CG2} - \frac{C_T}{C_{FC1}} V_S - V_T^{CG1} \right) V_{DS} - \frac{1}{2} \frac{C_T}{C_{FC1}} V_{DS}^2 \right] \tag{6}$$

$$I_D = \frac{\beta^{CG1}}{2} \left( \frac{C_{FC1}}{C_T} \right) \left( V_{CG1} + \frac{C_{FC2}}{C_{FC1}} V_{CG2} - \frac{C_T}{C_{FC1}} V_S - V_T^{CG1} \right)^2 \tag{7}$$

which show the relationship between  $I_D$  and  $V_{CG1}$ ,  $V_{CG2}$ ,  $V_S$ , and  $V_D$ . In Equation (7),  $I_D$  in the saturation region is not affected by  $V_{DS}$ , which is greatly convenient for reading the output signal of the ANC device. Assuming  $I_D$  to be a constant value and the source voltage  $V_S$  to be the output signal, the signal of the control gate is easily obtained by measuring the output voltage  $V_S$ . This readout method is called the source follower method, where the voltage of source  $V_S$  can be expressed by the voltage of two control gates as

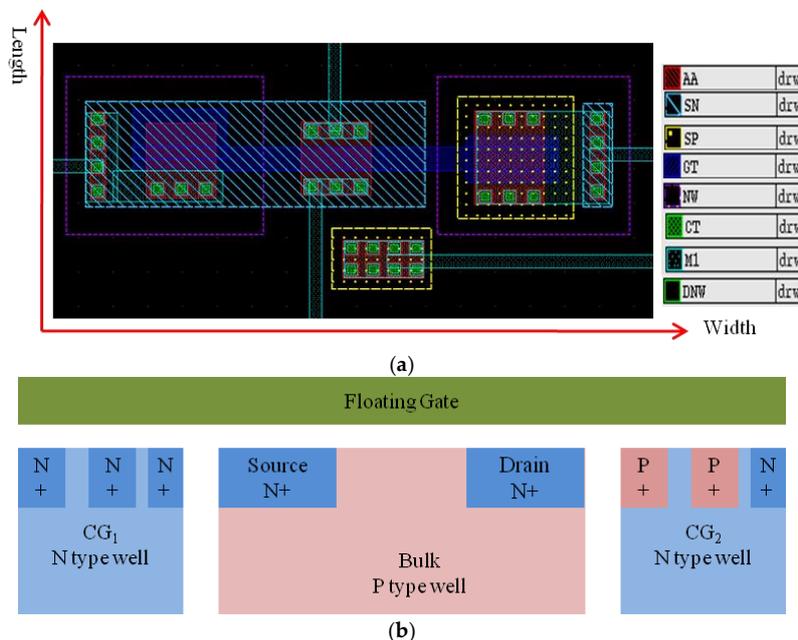
$$V_S = \frac{C_{FC1}}{C_T} V_{CG1} + \frac{C_{FC2}}{C_T} V_{CG2} - \sqrt{\frac{2I_D}{\beta^{CG1}} \left( \frac{C_{FC1}}{C_T} \right) - \frac{C_{FC1}}{C_T} V_T^{CG1}} \quad (8)$$

Normally, one control gate is used to set the DC operation point of the device and works as the secondary source input, and the other control gate is used to detect the effective signal with background interference. The subsequent circuits extract the interference from the output signal  $V_S$  and actively generate an inverse interference for secondary input. Thus, the secondary interference on one control gate and the primary interference on the other control gate work together to cancel each other and, finally, output the effective signal in  $V_S$ , with the interference being as small as possible.

According to the equivalent schematic diagram of the proposed ANC device shown in Figure 3a and the standard symbols for MOS transistors, the symbols for the proposed ANC device are shown in Figure 3b, which has five terminals of drain (D), source (S), bulk (B), control gate ( $CG_1$ ), and control gate ( $CG_2$ ).

### 2.3. Device Layout

The proposed ANC device was implemented in a standard 0.18  $\mu\text{m}$  single-poly CMOS process. Figure 4 shows the layout and cross section of the proposed ANC device, where AA is the active area, SN is the N+ implantation for source and drain, SP is the P+ implantation, GT is the polysilicon gate, NW is the N-type well, DNW is the deep N-type well, CT is the contact area, and M1 is the metal one. As shown in Figure 4, two control gates were formed in two N-type wells without special isolation from the P-type bulk.  $CG_1$  is an N-MOSC, while  $CG_2$  is a P-MOSFET with a common source, drain, and substrate. The two different structures both modulated the charges in the floating gate by the coupling capacitors. The coupling capacitor was determined by the overlap area between the floating gate and the control gate. The design parameters of the ANC device are listed in Table 1, where L is the abbreviation for the length and W is the abbreviation for the width of the areas shown in Figure 4a.



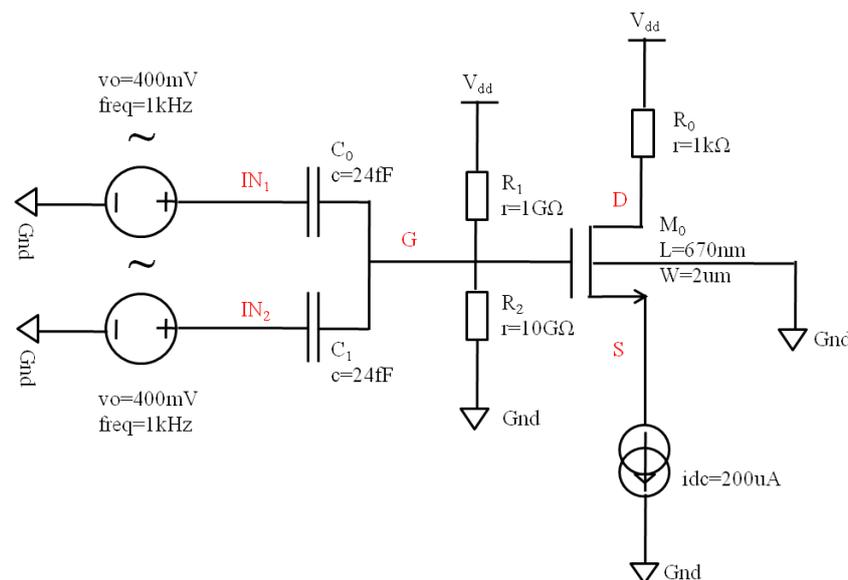
**Figure 4.** (a) Layout of the proposed ANC device, where AA is the active area, SN is the N+ implantation for the source and drain, SP is the P+ implantation, GT is the polysilicon gate, NW is the N-type well, DNW is the deep N-type well, CT is the contact area, and M1 is the metal one. (b) Cross section of the layout, where  $CG_1$  is a N-MOSC and  $CG_2$  is a P-MOSFET with a common source, drain, and substrate.

**Table 1.** The design parameters of the device.

Device	Length ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )
CG <sub>1</sub>	1.375	2.01
MOS	0.67	2.03
CG <sub>2</sub>	1.35	2.00

### 3. Simulation Results

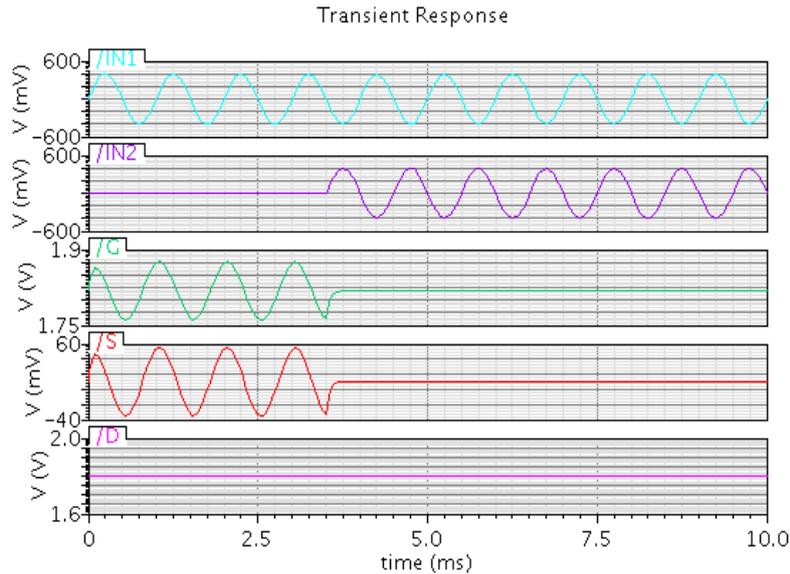
A simulation schematic based on the proposed ANC device is shown in Figure 5. The device is equivalent to a standard MOSFET  $M_0$  and two capacitors  $C_0$  and  $C_1$ , where capacitors  $C_0$  and  $C_1$  can be seen as the coupling capacitors  $C_{FC1}$  and  $C_{FC2}$ , and MOSFET  $M_0$  is equivalent to the combination of the floating gate, the source, the drain, and the p-bulk. Inputs  $IN_1$  and  $IN_2$  are equivalent to the control gates  $CG_1$  and  $CG_2$ . Two resistors  $R_1$  and  $R_2$  were used to provide the bias potential for the gate. The device was operated in the source follower mode under the saturation state. The values of two capacitors  $C_0$  and  $C_1$  were set to 24 fF according to the parameters of  $CG_1$  and  $CG_2$ , as shown in Table 1, calculated as Equation (9). The saturation current based on the standard MOSFET  $M_0$  was calculated as Equation (10), where  $V_{GS}$  is the potential difference between the gate and the source, and  $V_T$  is the threshold for the MOSFET device. Signals  $IN_1$  and  $IN_2$  are two sinusoidal wave signals with inverse phase and the same frequency and amplitude. The voltages of nodes G, D, and S were measured and the results are shown in Figure 6. From 0 to 3.5 ms, signal  $IN_2$  was a DC signal, only signal  $IN_1$  modulated the gate voltage with a certain attenuation, and the source voltage followed the gate voltage. After 3.5 ms, signals  $IN_1$  and  $IN_2$  both modulated the gate voltage. When the primary interference was detected by input end  $IN_1$ , the source follower structure output the similar primary interference, and subsequent circuits actively generated an inverse secondary interference for input end  $IN_2$ , which led to an effective signal without the primary interference at the source output by the superposition of two input signals. As a result, the source voltage was a DC voltage without the input sinusoidal signal, which showed the good performance of active noise control.



**Figure 5.** A simulation schematic based on the proposed ANC device with a standard MOSFET  $M_0$  and two capacitors  $C_0$  and  $C_1$ , where capacitors  $C_0$  and  $C_1$  can be seen as the coupling capacitors  $C_{FC1}$  and  $C_{FC2}$ ; MOSFET  $M_0$  represents the combination of the floating gate, the source, the drain, and the p-bulk; inputs  $IN_1$  and  $IN_2$  are equivalent to the control gates  $CG_1$  and  $CG_2$ ; and two resistors  $R_1$  and  $R_2$  are used to provide the bias potential for the gate.

$$C = WLC'_{ox} = WL \frac{\epsilon_r(\text{ox})\epsilon_0}{t_{ox}} = 1.35 \times 10^{-4} \text{cm} \times 2 \times 10^{-4} \text{cm} \times \frac{3.9 \times (8.85 \times 10^{-14} \text{F/cm})}{4 \times 10^{-7} \text{cm}} = 23.3 \text{fF} \quad (9)$$

$$\begin{aligned} I_D &= \frac{W\mu C'_{ox}}{2L} (V_{GS} - V_T)^2 \\ &= \frac{2 \times 10^{-4} \text{cm} \times 500 \text{cm}^2/\text{V}\cdot\text{s}}{2 \times 0.67 \times 10^{-4} \text{cm}} \times \frac{3.9 \times (8.85 \times 10^{-14} \text{F/cm})}{4 \times 10^{-7} \text{cm}} \times (1.8 \text{V} - 0.5 \text{V} - 0.7 \text{V})^2 \\ &= 232 \mu\text{A} \end{aligned} \quad (10)$$



**Figure 6.** Simulation result of the proposed ANC device, where signals  $IN_1$ ,  $IN_2$ ,  $G$ ,  $S$ , and  $D$  are the measured voltages from the red node  $IN_1$ ,  $IN_2$ ,  $G$ ,  $S$ , and  $D$  shown in Figure 5, and signals  $IN_1$  and  $IN_2$  are simulated as the primary interference and secondary interference, respectively. From 0 to 3.5 ms, only signal  $IN_1$  modulates the gate voltage with a certain attenuation and the source voltage follows the gate voltage. After 3.5 ms, signals  $IN_1$  and  $IN_2$  both modulate the gate voltage and the source voltage becomes a DC voltage without noise.

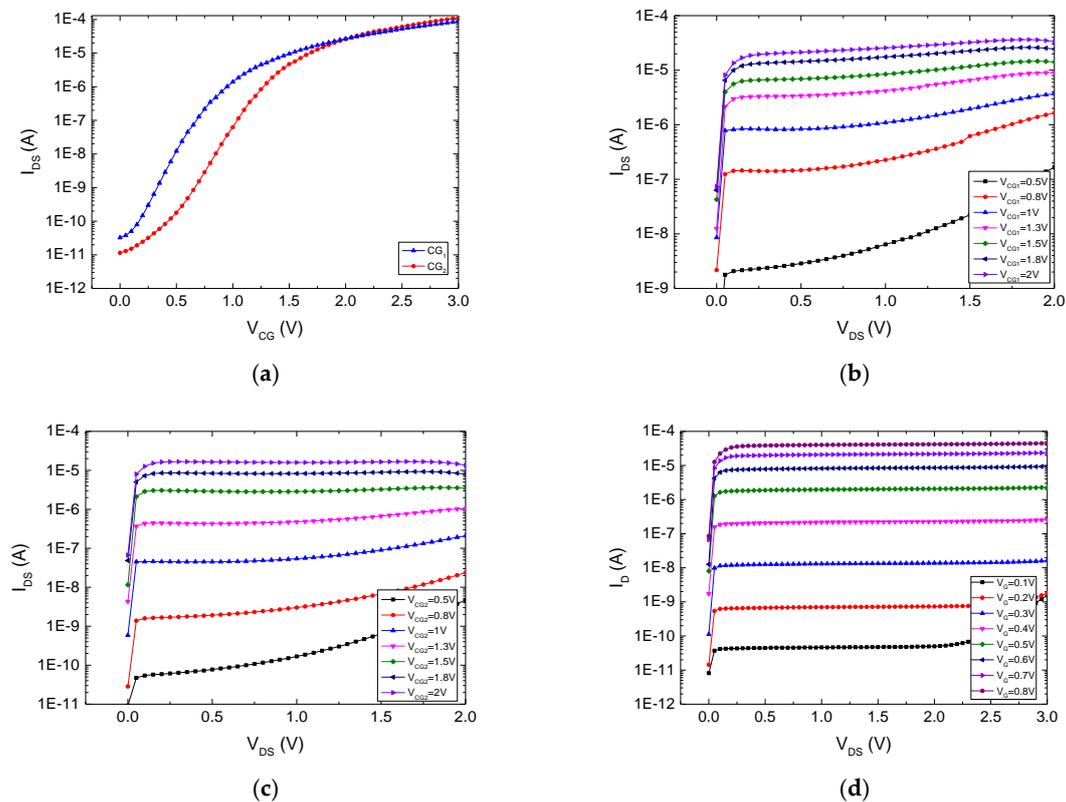
## 4. Experimental Results

### 4.1. $I$ - $V$ Characteristics

The proposed ANC device was fabricated in a 0.18  $\mu\text{m}$  single-poly CMOS process and the performance was measured with the Keithley 4200 Semiconductor Characterization System. To test the capability of each control gate to modulate the charge carrier density of the device channel, one of the two control gates was set to zero voltage and the other was input with a scanning voltage, while the source and the bulk were grounded and the drain was set to 0.5 V. Figure 7a shows the  $I_D$ - $V_G$  characteristics of the device, where the blue line is for control gate  $CG_1$  and the red line is for control gate  $CG_2$ , which shows that each control gate was able to modulate the device and the threshold voltages were within a reasonable range.

Figure 7b and c show the  $I_D$ - $V_D$  curves for control gates  $CG_1$  and  $CG_2$ , respectively. When the control gate voltage was not large enough, a high drain voltage caused a secondary increase of the drain current. For comparison, the  $I_D$ - $V_D$  curve for a standard MOSFET with the same gate size as that of the ANC device is shown in Figure 7d. It can be seen that when the gate voltage of the standard MOSFET is less than 0.2 V, the current  $I_D$  increases again after saturation, which is a characteristic similar to that of the proposed device. This may be caused by reverse breakdown of the pn junction

between the drain and the substrate because most of the increasing current comes from the substrate end, which can easily happen when the gate voltage is far below the threshold voltage. When the gate voltage becomes higher, a deeper depletion region is generated below the channel, which connects to the depletion region below the drain region and protects the pn junction from breakdown. Fortunately, in active noise control detection applications, the device is always turned on in the saturation state, which will not cause serious secondary increase.

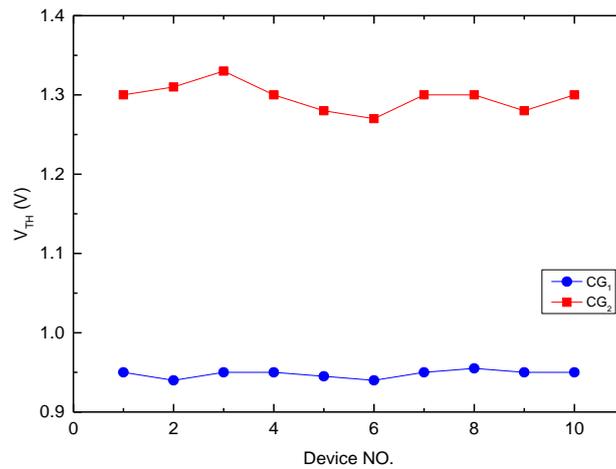


**Figure 7.** Current–voltage ( $I$ – $V$ ) characteristics of an ANC device and a standard MOSFET. (a) The  $I_D$ – $V_G$  characteristics of an ANC device show that each control gate can modulate the device and the threshold voltages are within a reasonable range. (b)  $I_D$ – $V_D$  characteristics for control gate  $CG_1$ . (c)  $I_D$ – $V_D$  characteristics for control gate  $CG_2$ . (d)  $I_D$ – $V_D$  characteristics of a standard MOSFET.

#### 4.2. Device Threshold Characteristic

The basic structure of the proposed ANC device was a 1.8 V MOSFET with a channel length of  $0.67 \mu\text{m}$  and a channel width of  $2.03 \mu\text{m}$ . The designed overlap area between control gate  $CG_1$  and the floating gate was slightly bigger than that between control gate  $CG_2$  and the floating gate. In the measurement, one of the control gates was grounded and the other was for threshold scanning. The threshold voltage for each control gate is illustrated clearly in Figure 8. The average threshold voltage for  $CG_1$  was 0.95 V and that for  $CG_2$  was 1.3 V.

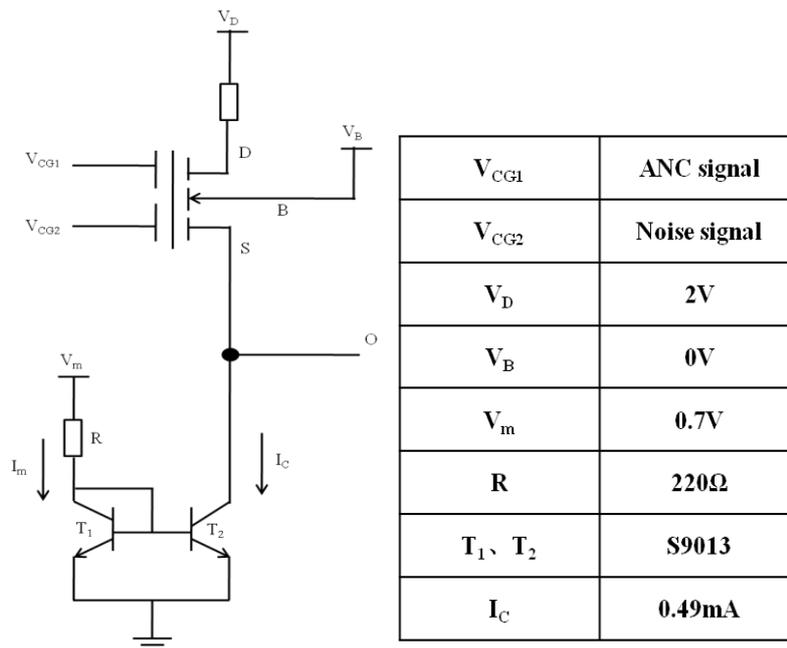
As discussed in the section on the device model, the threshold relationships satisfy Equation (4). According to the parameters in Table 1, the estimated threshold voltages of the two control gates should almost be the same value, but the measurement result was inconsistent. However, it can be seen from the layout that the real capacitor of  $CG_1$  was larger than that of  $CG_2$ , which explains why the threshold voltage of control gate  $CG_1$  was smaller than that of control gate  $CG_2$ .



**Figure 8.** The threshold voltages for two control gates of 10 devices, where the average threshold voltage for CG<sub>1</sub> is 0.95 V and that for CG<sub>2</sub> is 1.3 V.

4.3. ANC Experimental Verification

The circuit with source follower mode is shown in Figure 9, where a current mirror, composed of two transistors  $T_1$  and  $T_2$  and a resistor  $R$ , was used to provide a constant saturation current  $I_C$ , and  $V_D$  was set to 2 V to ensure that the device was in the saturation state.

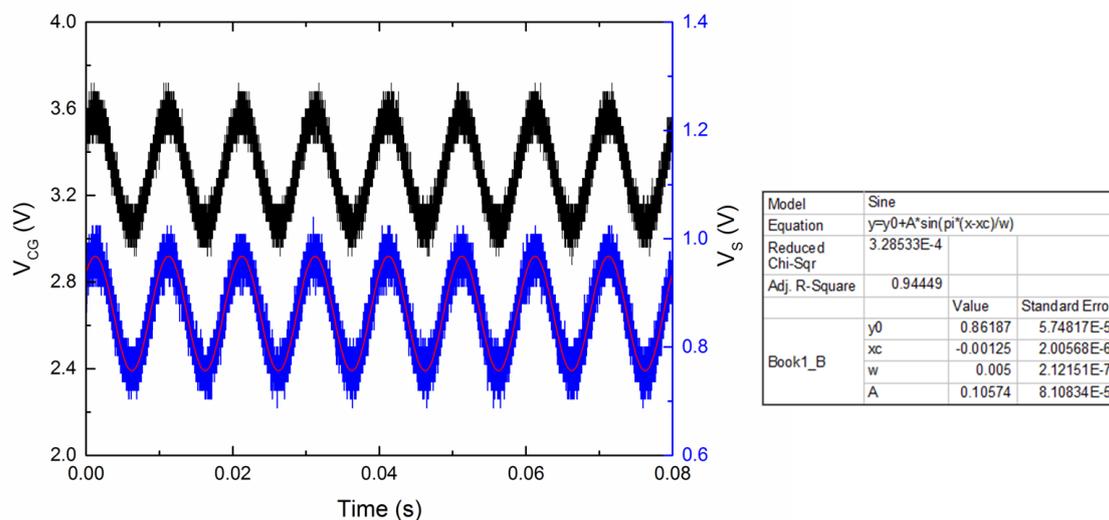


**Figure 9.** The circuit with source follower mode, where a current mirror, composed of two transistors  $T_1$  and  $T_2$  and a resistor  $R$ , is used to provide a constant saturation current  $I_C$ , and  $V_D$  is set to 2 V to ensure the device is in the saturation state.

To characterize the background noise of the proposed ANC device in the circuit system, control gate  $CG_2$  was grounded and control gate  $CG_1$  was applied with a standard sinusoidal signal (with a 3.3 V DC bias), shown as the black line in Figure 10. The output signal  $V_S$  was sampled and analyzed as the blue line, shown in Figure 10. The output signal curve was fitted by a sinusoidal function. The mean square of the residual expressed in Equation (11) represents the background noise of the device in the circuit system, where  $V_{bn}$  is the background noise,  $N$  is the number of sampled points,  $y_{real}$  is

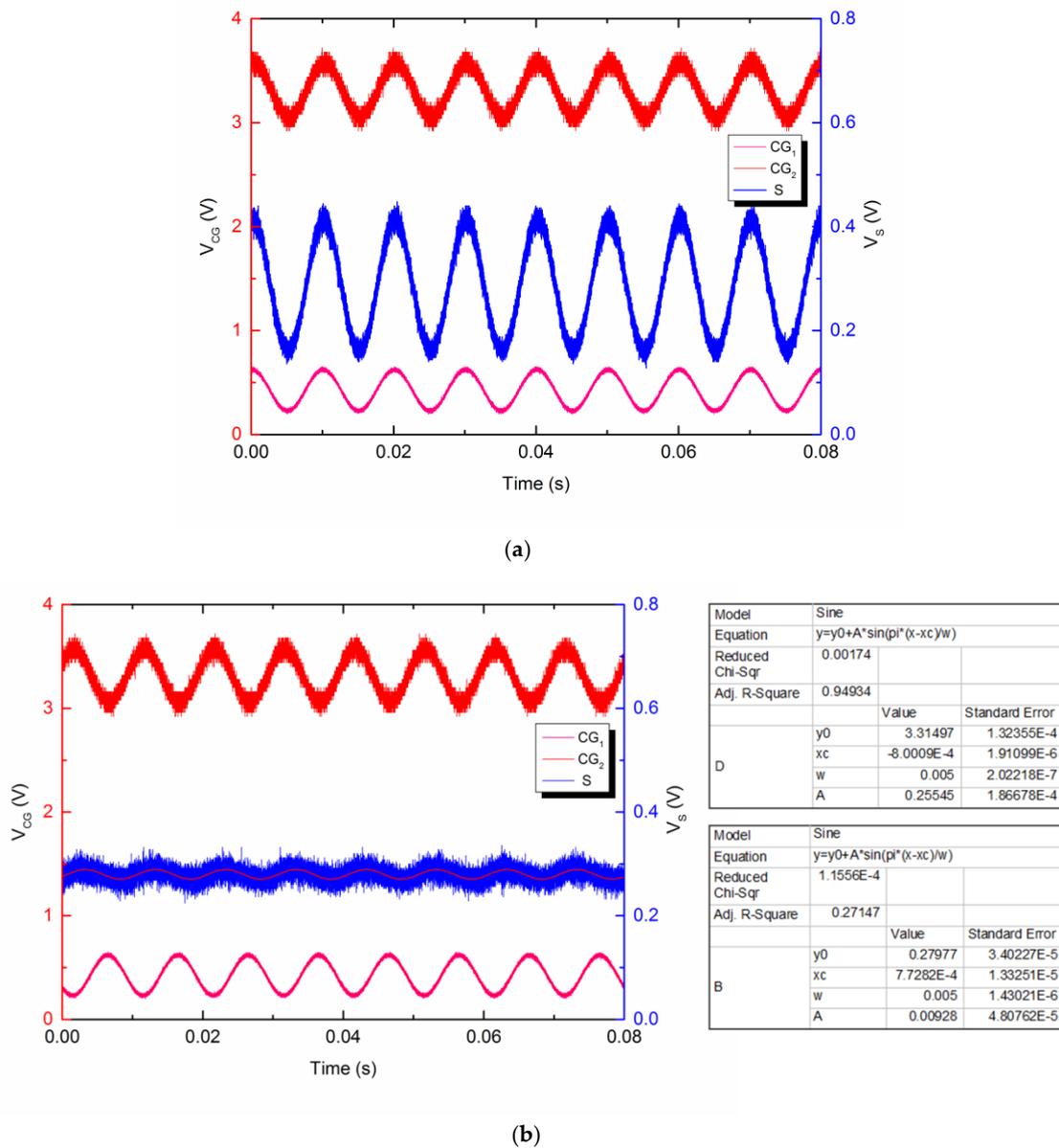
the sampled output signal, and  $y_{fit}$  is the fitted signal as mentioned above. The absolute value of the background noise was less than 0.33 mV for N being 1000, which shows the feasibility of the device in detecting small biosignals. It should be noted that the background noise can be reduced further by integrating all circuits in the same CMOS process.

$$V_{bn} = \sqrt{\frac{\sum_{i=1}^N (y_{real,i} - y_{fit,i})^2}{N}} \tag{11}$$



**Figure 10.** Characterization of device background noise in the circuit, where control gate  $CG_1$  is applied with a standard sinusoidal signal (with a 3.3 V DC bias) as shown with the black line, and the output signal  $V_S$  is shown with the blue line and fitted by a sinusoidal function as the red line with the fitting parameters given in the insets. The absolute value of the background noise is less than 0.33 mV.

In Figure 11, the pink line is the signal on control gate  $CG_1$ , the red line is the signal on control gate  $CG_2$  (both corresponding to the left axis), and the blue line is the output signal  $V_S$ , corresponding to the right axis.  $V_{CG_2}$  is an input sinusoidal wave signal, considered as the primary interference.  $V_{CG_1}$  is the secondary interference relevant to the primary interference from  $V_{CG_2}$ . The measured signal  $V_S$  as function of time is shown in Figure 11, which was in good agreement with expectations. As shown in Figure 11a, the output signal  $V_S$  followed the superposition of signals  $V_{CG_2}$  and  $V_{CG_1}$ , as calculated in Equation (8). When the active noise control system was turned on, the ANC signal on  $CG_1$  was adjusted by the subsequent feedback circuits to a signal with an inverse phase from the primary interference on  $CG_2$ . The amplitude of the ANC signal was modified by adjusting the gain of the subsequent circuits manually until the output signal  $V_S$  became as small as possible. Feedback system design is a large subject area and there are many kinds of specific circuit forms for feedback system implementation. One kind of feedback circuit for an ANC system consists of a bandpass filter and an inverting amplifier. The bandpass filter extracts the interference from the output signal and the inverting amplifier generates an inverse interference for secondary input. Figure 11b shows the result of the ANC system, where the input interference amplitude was 0.255 V and the output interference amplitude after ANC was 0.009 V. Therefore, the circuits can attenuate the interference by greater than 29 dB. The device has proved to be feasible and reliable for active noise control application. Moreover, the device works at ultra-low voltages and without any external reference electrode, and it also provides the capability of large-scale integration at a low cost for fabrication in a standard single-poly CMOS process.



**Figure 11.** The measured voltage as a function of time, where the pink line is the signal on control gate  $CG_1$ , the red line is the signal on control gate  $CG_2$ , the blue line is the output signal  $V_S$ , and the input interference on control gate  $CG_2$  and the output signal are fitted by a sinusoidal function respectively with the parameters given in the insets. (a) Without active noise control, the output signal  $V_S$  follows the superposition of signals  $V_{CG_2}$  and  $V_{CG_1}$  as calculated. (b) With active noise control, the output signal  $V_S$  is 9 mV and has a 29 dB attenuation for the input interference of 255 mV.

### 5. Conclusions

A smart floating gate transistor with two control gates was proposed for active noise control in bioelectrical signal measurement. A model of the device was developed and analyzed to demonstrate the working principle of the electrical behavior. Theoretical analysis and simulation results proved that the superposition of the two control gates can be reflected at the source end. To verify the feasibility of the proposed ANC device, a device with a novel structure was designed and fabricated in a standard 0.18  $\mu\text{m}$  single-poly CMOS process. A series of test experiments were carried out and the results showed that the devices were in accordance with the basic electrical characteristics of floating gate transistors, including the I–V characteristics and the threshold characteristics observed on two control

gates. Based on the source follower circuit, the experimental results proved that the device can reduce interference by more than 29 dB, and that it possesses the outstanding characteristic of low-cost, large-scale integration for fabrication in a standard single-poly CMOS process.

Future work will be directed toward fabricating the readout circuit of the proposed device and the subsequent circuit for secondary input in a standard single-poly CMOS process to enhance the large-scale integration ability and reduce the background noise further.

**Author Contributions:** All authors conceived of and designed the device and experiments; C.M. and C.Y. performed the experiments; H.M. analyzed the data; L.Z. and F.Y. contributed materials and analysis tools; C.M. wrote the paper; L.Z. revised the paper.

**Funding:** This research was funded by the National Key R & D Program of China, grant number 2016YFA0202100 and 2016YFA0202102, and the National Nature Science Foundation Program of China, grant number 11304152 and 61571376. The APC was funded by 2016YFA0202100.

**Conflicts of Interest:** The authors declare no conflict of interest

## References

1. Barbaro, M.; Bonfiglio, A.; Raffo, L. A charge-modulated FET for detection of biomolecular processes: conception, modeling, and simulation. *IEEE Trans. Electron Devices* **2006**, *53*, 158–166. [[CrossRef](#)]
2. Meyburg, S.; Stockmann, R.; Moers, J.; Offenhäusser, A.; Ingebrandt, S. Advanced CMOS process for floating gate field-effect transistors in bioelectronic applications. *Sens. Actuator B-Chem.* **2007**, *128*, 208–217. [[CrossRef](#)]
3. Zhang, Q.; Subramanian, V. DNA hybridization detection with organic thin film transistors: Toward fast and disposable DNA microarray chips. *Biosens. Bioelectron.* **2007**, *22*, 3182–3187. [[CrossRef](#)]
4. Zhang, X.H.; Lee, S.M.; Domercq, B.; Kippelen, B. Transparent organic field-effect transistors with polymeric source and drain electrodes fabricated by inkjet printing. *Appl. Phys. Lett.* **2008**, *92*, 243307. [[CrossRef](#)]
5. Kergoat, L.; Piro, B.; Berggren, M.; Pham, M.C.; Yassar, A.; Horowitz, G. DNA detection with a water-gated organic field-effect transistor. *Org. Electron.* **2012**, *13*, 1–6. [[CrossRef](#)]
6. Jimenez-Jorquera, C.; Orozco, J.; Baldi, A. ISFET Based Microsensors for Environmental Monitoring. *Sensors* **2009**, *10*, 61–83. [[CrossRef](#)] [[PubMed](#)]
7. Moser, N.; Rodriguez-Manzano, J.; Lande, T.S.; Georgiou, P. A Scalable ISFET Sensing and Memory Array with Sensor Auto-Calibration for On-Chip Real-Time DNA Detection. *IEEE Trans. Biomed. Circuits Syst.* **2018**, *12*, 390–401. [[CrossRef](#)] [[PubMed](#)]
8. Ogier, S.D.; Matsui, H.; Feng, L.; Simms, M.; Mashayekhi, M.; Carrabina, J.; Terés, L.; Tokito, S. Uniform, high performance, solution processed organic thin-film transistors integrated in 1 MHz frequency ring oscillators. *Org. Electron.* **2018**, *54*, 40–47. [[CrossRef](#)]
9. Krammer, M.; Borchert, J.W.; Petritz, A.; Karner-Petritz, E.; Schider, G.; Stadlober, B.; Klauk, H.; Zojer, K. Critical Evaluation of Organic Thin-Film Transistor Models. *Crystals* **2019**, *9*, 85. [[CrossRef](#)]
10. Liao, C.; Yan, F. Organic Semiconductors in Organic Thin-Film Transistor-Based Chemical and Biological Sensors. *Polym. Rev.* **2013**, *53*, 352–406. [[CrossRef](#)]
11. Lai, S.; Viola, F.; Cosseddu, P.; Bonfiglio, A. Floating Gate, Organic Field-Effect Transistor-Based Sensors towards Biomedical Applications Fabricated with Large-Area Processes over Flexible Substrates. *Sensors* **2018**, *18*, 688.
12. Spanu, A.; Viola, F.; Lai, S.; Cosseddu, P.; Ricci, P.C.; Bonfiglio, A. A reference-less pH sensor based on an organic field effect transistor with tunable sensitivity. *Org. Electron.* **2017**, *48*, 188–193. [[CrossRef](#)]
13. Demelas, M.; Lai, S.; Casula, G.; Scavetta, E.; Barbaro, M.; Bonfiglio, A. An organic, charge-modulated field effect transistor for DNA detection. *Sens. Actuator B-Chem.* **2012**, *171–172*, 198–203. [[CrossRef](#)]
14. Lai, S.; Barbaro, M.; Bonfiglio, A. Tailoring the sensing performances of an OFET-based biosensor. *Sens. Actuator B-Chem* **2016**, *233*, 314–319. [[CrossRef](#)]
15. Spanu, A.; Lai, S.; Cosseddu, P.; Tedesco, M.; Martinoia, S.; Bonfiglio, A. An organic transistor-based system for reference-less electrophysiological monitoring of excitable cells. *Sci. Rep.* **2015**, *5*, 8807. [[CrossRef](#)] [[PubMed](#)]

16. Zhang, L.; Tao, J.; Qiu, X. Active control of transformer noise with an internally synthesized reference signal. *J. Sound Vib.* **2012**, *331*, 3466–3475. [[CrossRef](#)]
17. Zhang, L.; Wu, L.; Qiu, X. An intuitive approach for feedback active noise controller design. *Appl. Acoust.* **2013**, *74*, 160–168. [[CrossRef](#)]
18. Gan, W.S.; Mitra, S.; Kuo, S.M. Adaptive feedback active noise control headset: implementation, evaluation and its extensions. *IEEE Trans. Consum. Electron.* **2005**, *51*, 975–982. [[CrossRef](#)]
19. Tseng, W.K.; Rafaely, B.; Elliott, S.J. Combined feedback–feedforward active control of sound in a room. *J. Acoust. Soc. AM.* **1998**, *104*, 3417–3425. [[CrossRef](#)]
20. Pavan, P.; Bez, R.; Olivo, P.; Zanoni, E. Flash memory cells-an overview. *Proc. IEEE* **1997**, *85*, 1248–1271. [[CrossRef](#)]



© 2019 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).