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T-Channel Field Effect Transistor with Three Input Terminals (Ti-TcFET)

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Abstract: In this paper, a novel T-channel field effect transistor with three input terminals (Ti-TcFET) is proposed. The channel of a Ti-TcFET consists of horizontal and vertical sections. The top gate is above the horizontal channel, while the front gate and back gate are on either side of the vertical channel. The T-shaped channel structure increases the coupling area between the top gate and the front and back gates, which improves the ability of the gate electrodes to control the channel. What's more, it makes the top gate have almost the same control ability for the channel as the front gate and the back gate. This unique structure design brings a unique function in that the device is turned on only when two or three inputs are activated. Silvaco technology computer-aided design (TCAD) simulations are used to verify the current characteristics of the proposed Ti-TcFET. The current characteristics of the device are theoretically analyzed, and the results show that the theoretical analysis agrees with the TCAD simulation results. The proposed Ti-TcFET devices with three input terminals can be used to simplify the complex circuits in a compact style with reduced counts of transistors compared with the traditional complementary metal–oxide–semiconductor/ fin field-effect transistors (CMOS/FinFETs) with a single input terminal and thus provides a new idea for future circuit designs.

Keywords: new device; three-input transistor; T-channel; compact circuit style

1. Introduction

Because of short-channel effects, the size of metal-oxide-semiconductor (MOS) devices is seriously restricted. In order to continue Moore's law, many new device structures have been proposed, such as silicon-on-insulator metal-oxide-semiconductor field-effect-transistors (SOI MOSFETs) with a single-gate structure, fin field-effect transistor (FinFETs) with a double-gate structure [1], and tri-gate field effect transistors (FETs) [2], Ω -gate FETs [3], and Gate-All-Around (GAA)FETs with a multi-gate structure. Among these devices, FinFET has been widely used in chip fabrication since it can considerably improve the ability of the gate electrode to control the channel and thus suppress the short-channel effects.

Most of the multi-gate devices mentioned above have only one input terminal. However, previous studies have shown that designing a circuit with devices with multiple input terminals is more flexible and efficient than using single-input ones [4,5]. The two-input low-threshold FinFET device proposed in the literature [6–10] is equivalent to two parallel transistors, while the two-input high-threshold FinFET device is equivalent to two series transistors. Therefore, the circuit can be simplified to reduce the transistor count by using two-input low-threshold and high-threshold FinFETs, thus reducing power consumption and the chip area. If a device has more input terminals, it is possible to achieve more flexible and efficient circuit designs.

This paper proposes a novel T-channel field effect transistor with three input terminals (Ti-TcFET). The invented T-type channel structure allows the device to have three independent input gates: the top

gate, front gate, and back gate. Because of the device structure with a T-type channel, the coupling areas among the top gate and the front and back gates are increased, which increases the control capability of the gates to the channel. This unique structure design brings a unique function in that the device is turned on only when two or three inputs are activated. Compared with traditional FinFETs with a single input terminal, the proposed Ti-TcFET devices with three input terminals can provide more flexible circuit realizations in a compact style. The proposed Ti-TcFET devices can be fabricated by adding only a small number of process steps on the basis of the current mainstream FinFET process.

This paper is organized as follows. In Section 2, the structure of the proposed device is introduced, and its device parameters are presented. The key processing steps of Ti-TcFET devices are also included in Section 2. In Section 3, the current characteristics of the device are theoretically analyzed, and Silvaco technology computer-aided design (TCAD) simulations are used to verify the accuracy of theoretical analysis. In Section 3, we illustrate how to carry out performance optimization for the proposed Ti-TcFET devices, and device performances are analyzed and evaluated in terms of turn-on and turn-off currents and switching current ratio. The compact circuits based on Ti-TcFET devices are also included in Section 3. We show that Ti-TcFET devices can be used to simplify complex circuits in a compact style with reduced transistor counts compared with the traditional complementary metal–oxide–semiconductor/ fin field-effect transistors (CMOS/FinFETs) with a single input terminal. Finally, the work of this paper is summarized in the last section.

2. Device Structure and Description

This section takes an N-type Ti-TcFET as an example to present the structure and parameters of the proposed device. We also give the fabrication process of Ti-TcFET devices in this section.

2.1. The Structure of the Ti-TcFET

Figure 1a shows a 3D diagram of the N-type Ti-TcFET, while Figure 1b is a cross-sectional diagram of the N-type Ti-TcFET. As seen in Figure 1a, the device has three independent input gates, termed the top gate, front gate, and back gate. From Figure 1b, we can see that the T-type channel of the Ti-TcFET is divided into horizontal and vertical sections. H_{Fin1} and T_{Si1} are the fin height and thickness of the vertical channel, respectively, while H_{Fin2} and T_{Si2} are the fin height and thickness of the horizontal channel, respectively. By adjusting the fin height H_{Fin2} of the horizontal channel, the contact area between the top gate and the horizontal channel can be changed, thus changing the coupling strength between the top gate and the front and back gates. The gate-to-channel control capability can be varied by adjusting the gate work function and the thickness T_{ox} of the high-K dielectric hafnium(IV) oxide (HfO_2).

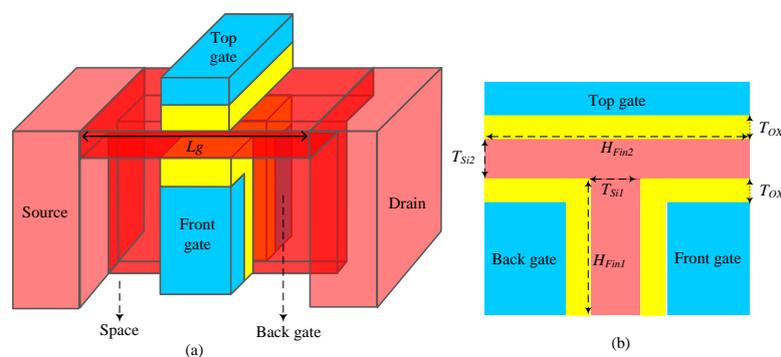


Figure 1. Structure of the N-type T-channel field effect transistor with three input terminals (Ti-TcFET) device: (a) 3D diagram, and (b) cross-sectional view.

In this work, SiO_2 is used as the substrate material for the device. The channel material is silicon, and the gate oxide material employs high-K dielectric HfO_2 . The device parameters of the Ti-TcFET are

shown in Table 1. The optimum values of H_{Fin1} , T_{Si1} , H_{Fin2} , T_{Si2} , T_{OX} (HfO₂ thickness), and L_g (channel length) are listed in Table 1. The doping concentrations N_{drain} and N_{source} of the source and drain regions are $2 \times 10^{20} \text{ cm}^{-3}$, and the channel doping concentration $N_{channel}$ is $1 \times 10^{16} \text{ cm}^{-3}$. The gate work function Φ_m of the N-type Ti-TcFET is set to 4.95 eV, while the gate work function of the P-type Ti-TcFET is selected to be 4.55 eV.

Table 1. Parameters of the T-channel field effect transistor with three input terminals (Ti-TcFET) device.

Parameter	Optimized Value	Parameter	Optimized Value
Gate dielectric thickness (T_{ox})	3 nm	Drain doping (N_{drain})	$2 \times 10^{20} \text{ cm}^{-3}$
Channel thickness 1 (T_{Si1})	4 nm	Source doping (N_{source})	$2 \times 10^{20} \text{ cm}^{-3}$
Channel thickness 2 (T_{Si2})	4 nm	Channel doping ($N_{channel}$)	$1 \times 10^{16} \text{ cm}^{-3}$
Fin height 1 (H_{Fin1})	40 nm	Gate work function (Φ_m)	4.52 eV (P-type)
Fin height 2 (H_{Fin2})	84 nm		4.95 eV (N-type)
Gate length (L_g)	24 nm	-	-

2.2. Key Processing Steps for the Ti-TcFET Device

On the basis of a traditional SOI-independent FinFET process [11], Ti-TcFET devices can be fabricated by adding a few processing steps. A key fabrication process is shown in Figure 2.

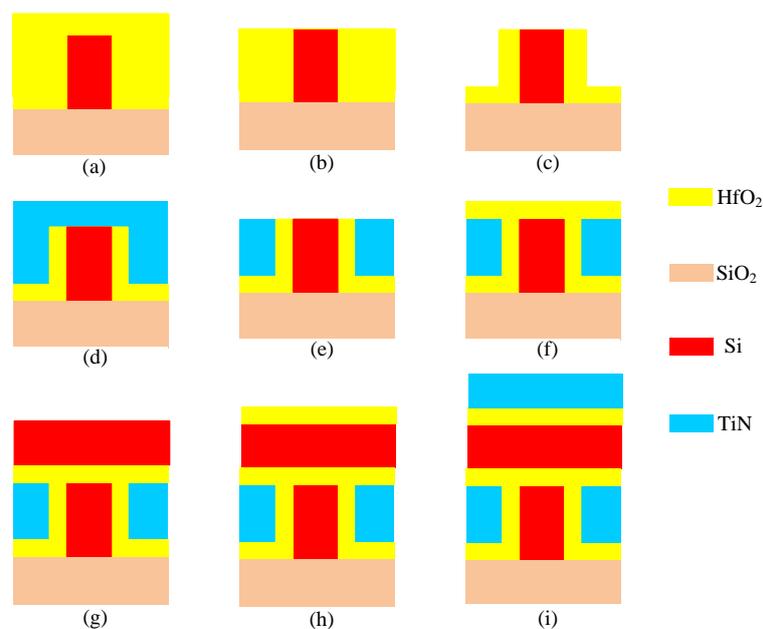


Figure 2. Key process steps of the Ti-TcFET device. (a) Silicon-on-insulator (SOI) layers were etched down to the buried oxide layer to produce the bodies of the devices; (b) chemical mechanical polishing (CMP) processing was used to remove the extra part of gate oxide above the top of the fin; (c) the extra part of gate oxide was etched back; (d) a Si₃N₄ gate electrode mask was deposited and patterned; (e) the gate pattern was etched into the Si₃N₄ and through the TiN to form the gate electrodes; (f) the high-K dielectric was deposited by using atomic layer deposition (ALD) processing; (g) a suitable horizontal channel structure was established by using smart-cut processing; (h) the high-K dielectric layer was deposited by using ALD processing; (i) the gate pattern was etched into the silicon and through the TiN to form the top gate electrodes.

A SiO₂ film was firstly grown as a mask for the silicon fin etching, and then the hard-mask and SOI layers were etched down to the buried oxide layer to produce the bodies of the devices, as shown in Figure 2a [11]. A high-K dielectric layer was deposited by using atomic layer deposition (ALD) processing. Next, chemical mechanical polishing (CMP) processing was used to remove the extra

part of gate oxide above the top of the fin, as shown in Figure 2b. The extra part of gate oxide was etched back, and only the required part on the two sides of the fin remained, as shown in Figure 2c [11]. Thereafter, a Si_3N_4 gate electrode mask was deposited and patterned, as shown in Figure 2d. The gate pattern was etched into the Si_3N_4 and through the TiN to form the gate electrodes, as shown in Figure 2e. The high-K dielectric was deposited by using ALD processing, as shown in Figure 2f. In order to reduce the difficulty of the process, the horizontal channel and vertical channel were separated by HfO_2 , as shown in Figure 2g. Figure 2g shows how a suitable horizontal channel structure was established by using smart-cut processing. In order to establish the gate oxide layer of the top gate, the high-K dielectric layer was deposited by using ALD processing, as shown in Figure 2h. A Si_3N_4 gate electrode mask was deposited and patterned, and finally, the gate pattern was etched into the silicon and through the TiN to form the top gate electrodes, as shown in Figure 2i.

3. Results and Discussion

In this section, the current characteristics of the device are theoretically analyzed by modeling the threshold voltage of Ti-TcFETs, and then Silvaco TCAD simulations are used to verify the accuracy of the theoretical analysis. The Lombardi constant voltage and temperature (CVT), Fermi–Dirac carrier statistics (FERMIDIRAC), Shockley–Read–Hall (SRH) models, and the Bohm quantum potential (BQP) models were considered in these TCAD simulations [12]. The performance optimizations for the proposed Ti-TcFET devices were carried out by selecting the channel thickness, gate oxide thickness, and gate work function, and device performances were evaluated in terms of turn-on and turn-off currents and switching current ratio. The several basic logic cells such as the “majority-not” [13,14], NOT-AND (NAND), and NOT-OR (NOR) logic cells, and the full adder realized by using the proposed Ti-TcFET devices are illustrated, showing that Ti-TcFET devices can be used to simplify complex circuits in a compact style with reduced transistor counts.

3.1. The Threshold Voltage of Ti-TcFET Devices

The Ti-TcFET device has three inputs. The threshold voltage of any gate is affected by the bias voltage of the other two gates because of the coupling effect among the three gates. In other words, the threshold voltage of a gate is a function of the voltages of the other two gates. Taking the threshold voltage of the top gate of the N-type Ti-TcFET as an example, the relationship between the threshold voltage and other gate voltages (front gate and back gates) is analyzed.

The relationship between the threshold voltage of the top gate and the bias voltages of the front gate and back gate can be measured by introducing the coupling coefficients $\gamma_{top\text{-}gate}$ and $\gamma_{top\text{-}back}$ [15,16], as shown in Equations (1) and (2).

$$r_{top\text{-}front} = \frac{\Delta V_{THt}}{\Delta V_{front\text{-}gate}} = \frac{C_{si} \cdot C_{oxf}}{C_{oxt} \cdot (3C_{oxf} + 2C_{si})} \cong \frac{T_{oxf}}{2T_{oxf} + 6.3T_{si}}, \quad (1)$$

$$r_{top\text{-}back} = \frac{\Delta V_{THt}}{\Delta V_{back\text{-}gate}} = \frac{C_{si} \cdot C_{oxb}}{C_{oxt} \cdot (3C_{oxb} + 2C_{si})} \cong \frac{T_{oxb}}{2T_{oxb} + 6.3T_{si}}, \quad (2)$$

where V_{THt} is the threshold voltage of the top gate, $V_{front\text{-}gate}$ and $V_{back\text{-}gate}$ are the voltages of the front gate and back gate, respectively, C_{oxf} , C_{oxb} , and C_{oxt} are the oxide capacitance of the front gate, back gate, and top gate, respectively, C_{si} and T_{si} are the body capacitance and thickness of the channel, respectively, and T_{oxf} and T_{oxb} are e thickness of the front and back gates, respectively.

TCAD simulation show that the threshold voltage V_{THt} of the top gate is not completely linear to the bias voltages of the front and back gates. After considering the secondary effect, the threshold voltage V_{THt} of the top gate can be written as Equation (3).

$$V_{THt} = V_{TH0} - r_{top-front} \cdot V_{front-gate} - r_{top-back} \cdot V_{back-gate} - \alpha \cdot (V_{front-gate}^2 + V_{back-gate}^2) - \beta \cdot V_{front-gate} \cdot V_{back-gate} \quad (3)$$

where V_{TH0} is the threshold voltage of the top gate when both $V_{front-gate}$ and $V_{back-gate}$ are at 0 V, and α and β are the fitting parameters.

The threshold voltage of the top gate versus the voltages of the front gate and the back gate is shown in Figure 3. In Figure 3, the points are the threshold voltages of the Ti-TcFET device obtained by the TCAD simulations, while the lines are the theoretical calculation results obtained by Equation (3) in different voltages of the front and back gates. The results show that the theoretical formula of the threshold voltage agrees with the TCAD simulation results.

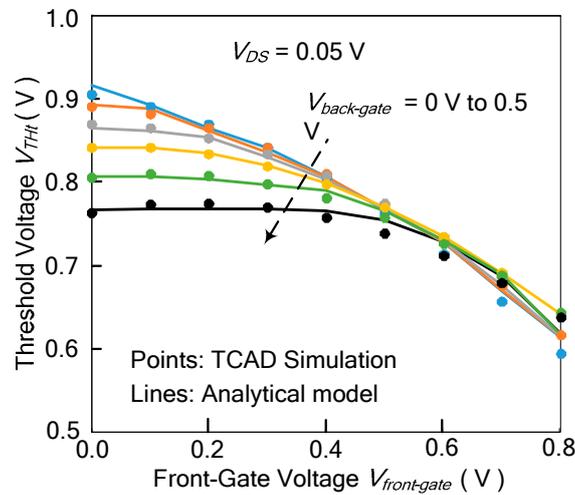


Figure 3. Comparison between calculated and simulated threshold voltages of the top gate versus the front gate in different back gate voltages at $V_{DS} = 50$ mV.

As the size of nanoscale devices decreases, quantum mechanical effects will begin to affect device performance. The threshold voltage drift ΔV_{TH} caused by the quantum mechanical effect can be written as follows [17]:

$$\Delta V_{TH} = \frac{S}{v_T \ln 10} \Delta \Psi, \quad (4)$$

where $v_T = kT/q$ is the thermal voltage—where k is Boltz constant, T is the thermodynamic temperature, and q is the electronic charge quantity—and S is the subthreshold swing of the device. $\Delta \Psi$ is

$$\Delta \Psi = \Psi_S^{QM} - \Psi_S^{CL}, \quad (5)$$

where Ψ_S^{QM} and Ψ_S^{CL} are the potential at the silicon–oxide interface when considering the quantum models and semi-classical models, respectively.

The Ti-TcFETs have been simulated considering both the Bohm quantum potential (BQP) models and semi-classical models. The threshold voltage of the device is reduced by 0.018 V when considering the BQP quantum compared with semi-classical models. Studies have shown that the amount of threshold voltage drift caused by quantum effects will become obvious when the channel silicon thickness is very thin (<2 nm) [18]. For undoped devices with a bulk silicon thickness (>4 nm), the threshold voltage drift caused by quantum effects is small [18].

3.2. Drain Current of the Ti-TcFET

The drain current I_D of the Ti-TcFET device can be expressed by Equation (6).

$$I_D = I_S \cdot \frac{H_{Fin2} T_{Si2}}{L_g} \cdot (V_{top-gate} - V_{THt})^\lambda, \quad (6)$$

where I_S and λ are fitting parameters. For short-channel devices, the range of λ is about 1.3 to 1.5 [19].

The drain current of the Ti-TcFET device versus the voltages of the top gate is shown in Figure 4, where V_{DS} is 0.8 V, $V_{front-gate}$ is 0 V, and $V_{back-gate}$ changes from 0.2 V to 0.8 V. In Figure 4, the points are obtained by the TCAD simulations, while the lines are the theoretical calculation results of the drain current for different voltages of the top gate. The results show that the theoretical formula of the drain current agrees with the TCAD simulation results.

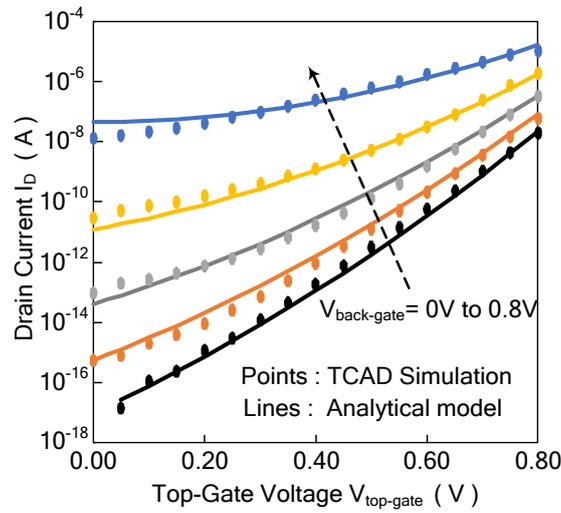


Figure 4. Comparison between the calculated and simulated drain current versus the voltages of the top gate in different back-gate voltages at $V_{DS} = 0.8$ V and $V_{front-gate} = 0$ V.

3.3. Subthreshold Current of the Ti-TcFET

Referring to the literature [20,21], the subthreshold leakage current I_{sub} of the Ti-TcFET device can be calculated by Equation (7):

$$I_{sub} = I_w \cdot \frac{H_{Fin2} T_{Si2}}{L_g} \cdot e^{\frac{(V_{top-gate} - V_{THt}) + m \cdot (V_{top-gate} - V_{THt})^2}{n \cdot v_T}} \cdot \left(1 - e^{-\frac{q \cdot V_{DS}}{v_T}}\right) \cdot e^{b1 \cdot V_{top-gate} + b2 \cdot V_{top-gate}^2 + b3 \cdot V_{top-gate} \cdot V_{THt}}, \quad (7)$$

where I_w , m , $b1$, $b2$, and $b3$ are fitting parameters and n is subthreshold slope parameter.

The drain current of the Ti-TcFET device versus the voltages of the top gate is shown in Figure 5, where V_{DS} is 0.8 V, $V_{front-gate}$ is 0 V, and $V_{back-gate}$ changes from 0 V to 0.5 V. In Figure 5, the points are obtained by TCAD simulations, while the lines are the theoretical calculation results of the drain current for different voltages of the top gate. The calculated subthreshold drains agree well with the simulated subthreshold current for $V_{top-gate} > 0.1$ V.

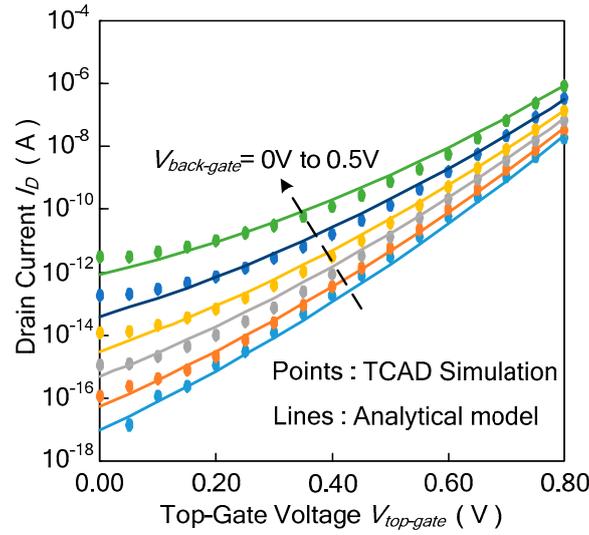


Figure 5. Comparison between the calculated and simulated subthreshold drain current versus the voltages of the top gate in different back-gate voltages at $V_{DS} = 0.8$ V and $V_{front-gate} = 0$ V.

3.4. Performance Optimization of the Ti-TcFET Devices

In order to obtain high-performance Ti-TcFET devices, the following two goals should be achieved. If only one gate is activated, the current should be as small as possible. If any two of the three gates are activated, the current should be as large as possible. In other words, the maximum turn-off current I_{off} should be small and the minimum turn-on current I_{on} should be large. In this subsection, we study the influence of device size and parameters on device performance by changing the channel thickness, gate oxide thickness, and gate work function, and then select the optimized device size and parameters.

In order to achieve the first goal, Ti-TcFET devices should have a high-threshold voltage when only one gate is activated. The threshold voltage of a Ti-TcFET is approximated by Equation (8):

$$V_{Tht} = V_{inv} + \Phi_m + \frac{Q_D}{C_{ox}} + V^{QM} - V^{SCE}, \quad (8)$$

where V_{inv} is a constant, Φ_m is the work function difference of the electrode and the silicon, Q_D is the channel depletion charge, C_{ox} is the oxide capacitance of the front gate, back gate, and top gate, and V^{QM} and V^{SCE} are the threshold voltage increase caused by quantum-mechanical effect models and short-channel effects, respectively. From Equation (8), the threshold voltage of the device can be adjusted by selecting a suitable Φ_m and C_{ox} .

In order to achieve the second goal, Ti-TcFET devices should have a low subthreshold slope, so that the device achieves a large turn-on current with a small turn-off current. The subthreshold slope S is given by Equation (9) [22]:

$$S = \frac{\partial V_{top-gate}}{\partial \log I_D} = \ln 10 \cdot \frac{kT}{q} \cdot \frac{\Delta V_{top-gate}}{\Delta \psi_{Si}} = 60 \cdot \frac{\Delta V_{top-gate}}{\Delta \psi_{Si}}, \quad (9)$$

where ψ_{Si} is the surface potential at the gate electrode. The subthreshold slope can be approximated by Equation (10) [23]:

$$S = 60 \cdot \frac{T_{oxb} + 2.1T_{Si} + T_{oxb}}{T_{oxb}} = 60 \cdot \left(\frac{2.1T_{Si}}{T_{OX}} + 2 \right), \quad (10)$$

From Equation (10), we can get the relationship between the subthreshold slope S , channel thickness T_{Si} , and gate oxide thickness T_{ox} , which can be used to optimize the performances of Ti-TcFET devices.

3.4.1. Effect of Channel Thickness on Current Characteristics

Figure 6 shows the effect of channel thickness T_{Si} on current characteristics at $V_{front-gate} = 0$ V and $V_{back-gate} = 0.8$ V. When the voltage $V_{top-gate}$ of the top gate is set as 0.8 V, the two inputs of the N-type Ti-TcFET are at 0.8 V, and thus the device should be turned on. Its drain current is named as I_{on} (turn-on current). When the voltage of the top gate $V_{top-gate}$ is 0 V, only one input of the Ti-TcFET is at 0.8 V, and thus the device should be turned off. Its drain current is named as I_{off} (turn-off current).

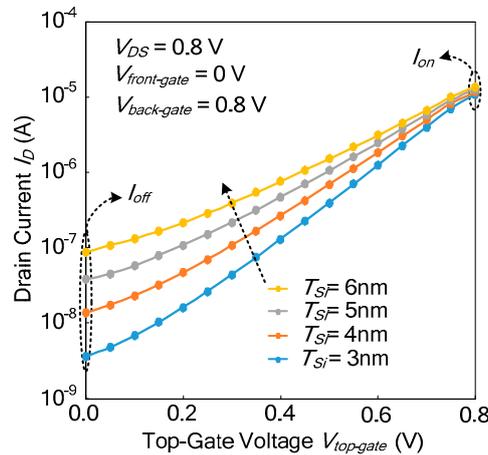


Figure 6. The turn-on current I_{on} and turn-off current I_{off} at different channel thicknesses T_{Si} .

From Figure 6, it can be seen that as the channel thickness reduces from 6 nm down to 3 nm, I_{on}/I_{off} (the switching current ratio) increases. From Equation (10), the subthreshold slope S of the devices reduces when the channel thickness T_{Si} reduces. The results show that the TCAD simulations agree with the theoretical formula. In order to have enough I_{on} and an acceptable I_{on}/I_{off} , the optimized T_{Si} is set to 4 nm.

3.4.2. Effect of Gate Oxide Thickness on Current Characteristics

Figure 7 shows the effect of gate oxide thickness T_{OX} on current characteristics at $V_{front-gate} = 0$ V and $V_{back-gate} = 0.8$ V according to the TCAD simulations. As the gate oxide thickness T_{OX} increases from 2.0 nm to 3.5 nm, I_{on}/I_{off} increases. As shown in Equation (10), when the gate oxide thickness T_{OX} increases, the subthreshold slope S of the Ti-TcFET devices decreases, so that I_{on}/I_{off} increases. The results show that the theoretical formula agrees with the TCAD simulations. In order to have enough I_{on} and an acceptable I_{on}/I_{off} , the optimized gate oxide thickness T_{OX} is set to 3 nm.

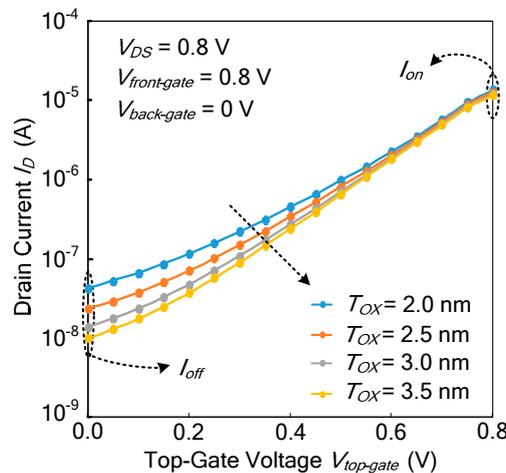


Figure 7. The turn-on current I_{on} and turn-off current I_{off} at different thickness T_{OX} of the dielectric HfO_2 .

3.4.3. Effect of Gate Work Function on Current Characteristics

Figure 8 shows the effect of the gate work function on current characteristics at $V_{front-gate} = 0$ V and $V_{back-gate} = 0.8$ V according to the TCAD simulations. From Figure 8, it can be seen that as the gate work function Φ_m increases from 4.85 eV to 5.00 eV, I_{off} decreases. As shown in Equation (8), a high-threshold voltage can be achieved by increasing the gate work function Φ_m , so that I_{off} decreases. The results show that the theoretical formula agrees with the TCAD simulations. In order to reduce I_{off} , the optimized gate work function is set to 4.95 eV.

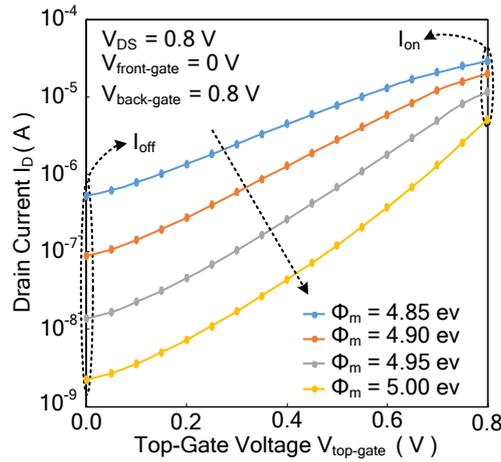


Figure 8. The turn-on current I_{on} and turn-off current I_{off} with different gate work functions Φ_m .

3.5. Drain-Induced Barrier Lowering (DIBL) and S of the Optimized Ti-TcFET Devices

The drain-induced barrier lowering (DIBL) can be calculated by using Equation (11):

$$DIBL(mV/V) = \frac{\Delta V_{Tht}}{\Delta V_{DS}}, \tag{11}$$

As shown in Equation (11), the DIBL is defined as the difference in threshold voltage when the drain voltage is increased. The drain current of the Ti-TcFET is shown in Figure 9 when $V_{front-gate} = 0$ V and $V_{back-gate} = 0.8$ V. From Figure 9, the DIBL of the Ti-TcFET device is about 41.48 mV/V when $V_{front-gate} = 0$ V and $V_{back-gate} = 0.8$ V. Our TCAD simulations show that the DIBL of the Ti-TcFET device is almost the same as the standard FinFET device when using the same device parameters.

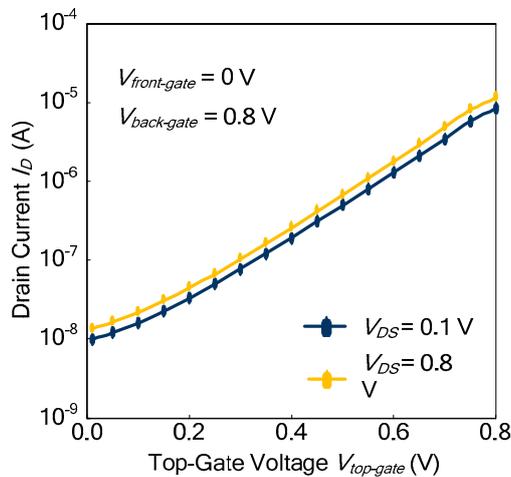


Figure 9. Drain current of the Ti-TcFET when $V_{front-gate} = 0$ V and $V_{back-gate} = 0.8$ V.

The drain current of the Ti-TcFET is shown in Figure 10 when $V_{top-gate} = V_{front-gate} = V_{back-gate}$. From Figure 10, it can be seen that the subthreshold slope S of the Ti-TcFET devices is about 62.6 mV/dec. The TCAD simulations show that the subthreshold slope S of the Ti-TcFET device is also almost the same as the standard FinFET device when using the same device parameters.

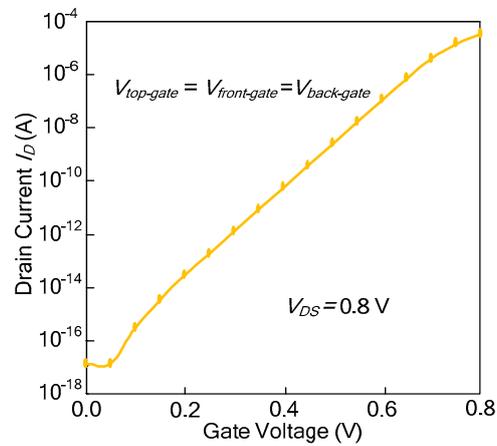


Figure 10. Drain current of the Ti-TcFET when $V_{top-gate} = V_{front-gate} = V_{back-gate}$.

3.6. Scaling Factors of the Ti-TcFET Devices

The minimum turn-on current and maximum turn-off current are shown in Figure 11 as channel length L_g and fin height H_{Fin} scale down, where the scaling factor (SF) is set as 0.707. From Figure 11a, as the channel length L_g and fin height H_{Fin} scale down, the minimum turn-on current reduces slowly. From Figure 11b, as the channel length L_g and fin height H_{Fin} scale down, the maximum turn-off drain is almost a constant.

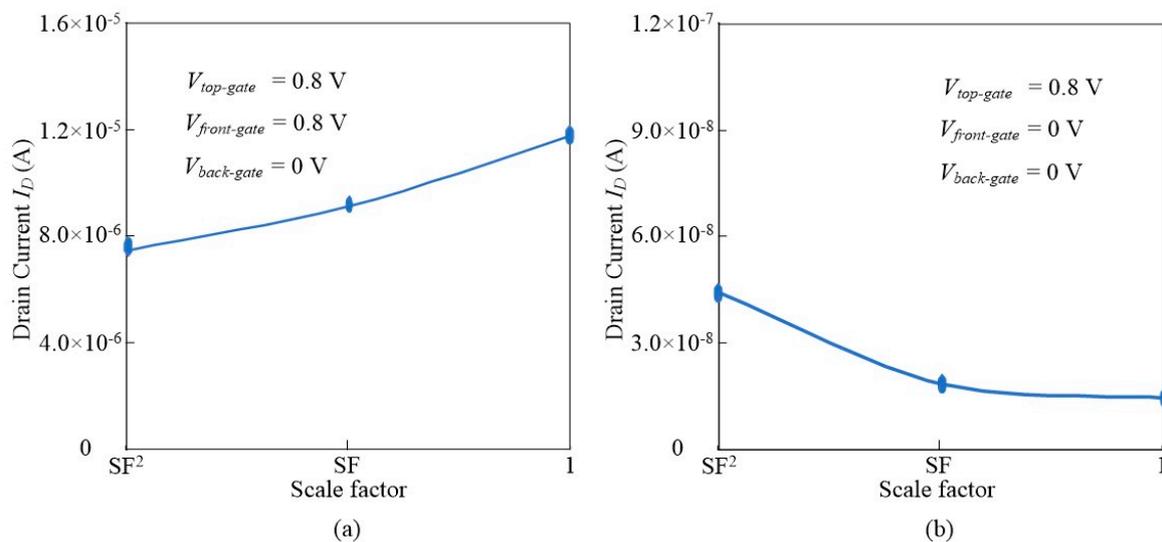


Figure 11. (a) The minimum turn-on current as channel length L_g and fin height H_{Fin} scale down, and (b) the maximum turn-off current as channel length L_g and fin height H_{Fin} scale down. The scaling factor (SF) is set as 0.707.

3.7. Performance Analysis of the Ti-TcFET Devices

The Ti-TcFET device has three input terminals, and each input terminal has two logic values with logic “1” (0.8 V) and logic “0” (0 V), so that the device has eight switching modes. Taking the N-type Ti-TcFET as an example, eight working modes are illustrated in Figure 12. When only one or fewer inputs are “1”, the device is turned off, as shown in Figure 12a. In Figure 12a, there are four switching

modes in the turn-off state. When two or three inputs are “1”, the device is turned on, as shown in Figure 12b. In Figure 12b, there are also four switching modes in the turn-on state.

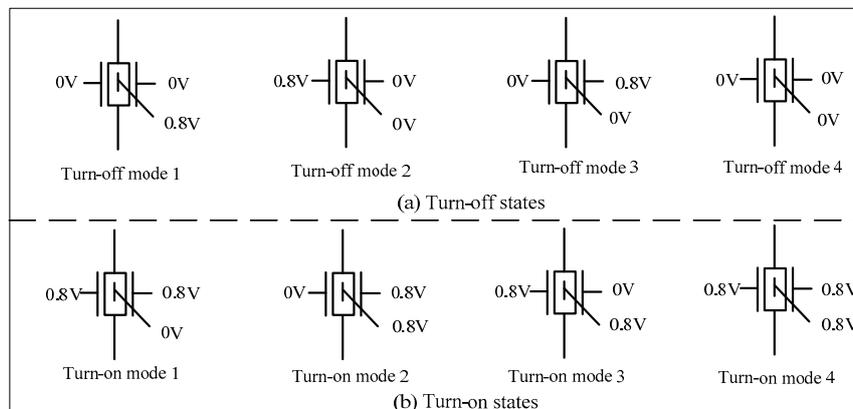


Figure 12. Eight switching modes of the Ti-TcFET device.

Using the optimized parameters and device sizes listed in Table 1, the turn-on and turn-off currents of N-type and P-type Ti-TcFETs working in eight switching modes are listed in Tables 2 and 3, respectively.

Table 2. The turn-on current and turn-off currents of the N-type Ti-TcFET.

State	$V_{top-gate}, V_{front-gate}, V_{back-gate}$	I_D (A)	Normalized
Turn-off mode 1	0.8 V, 0 V, 0 V	2.06×10^{-8}	0.0005
Turn-off mode 2	0 V, 0.8 V, 0 V	1.40×10^{-8}	0.0004
Turn-off mode 3	0 V, 0 V, 0.8 V	1.40×10^{-8}	0.0004
Turn-off mode 4	0 V, 0 V, 0 V	1.47×10^{-17}	3.81×10^{-13}
Turn-on mode 1	0 V, 0.8 V, 0.8 V	1.17×10^{-5}	0.3031
Turn-on mode 2	0.8 V, 0 V, 0.8 V	1.17×10^{-5}	0.3031
Turn-on mode 3	0.8 V, 0.8 V, 0 V	1.14×10^{-5}	0.2953
Turn-on mode 4	0.8 V, 0.8 V, 0.8 V	3.86×10^{-5}	1.0000

Table 3. The turn-on current and turn-off currents of the P-type Ti-TcFET.

State	$V_{top-gate}, V_{front-gate}, V_{back-gate}$	I_D (A)	Normalized
Turn-off mode 1	0 V, 0.8 V, 0.8 V	1.57×10^{-8}	0.0007
Turn-off mode 2	0.8 V, 0 V, 0.8 V	1.06×10^{-8}	0.0004
Turn-off mode 3	0.8 V, 0.8 V, 0 V	1.06×10^{-8}	0.0004
Turn-off mode 4	0.8 V, 0.8 V, 0.8 V	2.75×10^{-17}	1.15×10^{-12}
Turn-on mode 1	0.8 V, 0 V, 0 V	7.48×10^{-6}	0.3116
Turn-on mode 2	0 V, 0.8 V, 0 V	7.09×10^{-6}	0.2954
Turn-on mode 3	0 V, 0 V, 0.8 V	7.09×10^{-6}	0.2954
Turn-on mode 4	0 V, 0 V, 0 V	2.40×10^{-6}	1.0000

Table 2 lists the turn-on current I_{on} and turn-off current I_{off} of the N-type Ti-TcFET in the four turn-on modes and four turn-off modes, respectively. The normalized currents are listed in the rightmost column in Table 2. From Table 2, it can be seen that the maximum turn-off current among the four turn-off modes is 2.06×10^{-8} A, while the minimum turn-on current among the four turn-on modes is 1.14×10^{-5} A. In the worst case, I_{on}/I_{off} (switching current ratio) is 553. In order to increase I_{on}/I_{off} , some new materials such as ferroelectric materials and two-dimensional materials can be used.

Ferroelectric materials can enhance the internal gate voltage through the negative capacitance effect, so that I_{on}/I_{off} (switching current ratio) increases greatly and the subthreshold swing decreases below 60 mV/dec [24]. Two-dimensional (2D) semiconductors, such as transition metal dichalcogenides (TMDs), have the potential for ultra-scaled transistor technology beyond 10 nm node technology because of their atomically thin layered channel and low dielectric constant, which offer strong electrostatic control [25].

Table 3 shows the turn-on current I_{on} and turn-off current I_{off} of the P-type Ti-TcFET in the four turn-on modes and four turn-off modes, respectively. The normalized currents are also listed in the rightmost column in Table 3. From Table 3, it can be seen that the maximum turn-off current among the four turn-off modes is 1.57×10^{-8} A, while the minimum turn-on current among the four turn-on modes is 7.09×10^{-6} A. In the worst case, the switching current ratio is 452.

3.8. Logic Cells Based on Ti-TcFET Devices

A single Ti-TcFET transistor can implement three input “majority-not” switch functions [26,27], and thus only one N-type Ti-TcFET and one P-type Ti-TcFET are needed to realize a “majority-not” logic cell, as shown in Figure 13a. From Figure 13a, the “majority-not” logic cell using traditional CMOS/FinFET devices needs 10 transistors. The transistor counts of the “majority-not” cell using the proposed Ti-TcFET devices is only one-fifth of that of the “majority-not” cell using traditional CMOS/FinFET devices, which shows that the proposed Ti-TcFET devices with three input terminals have a higher information processing capacity than traditional CMOS/FinFETs with a single input terminal.

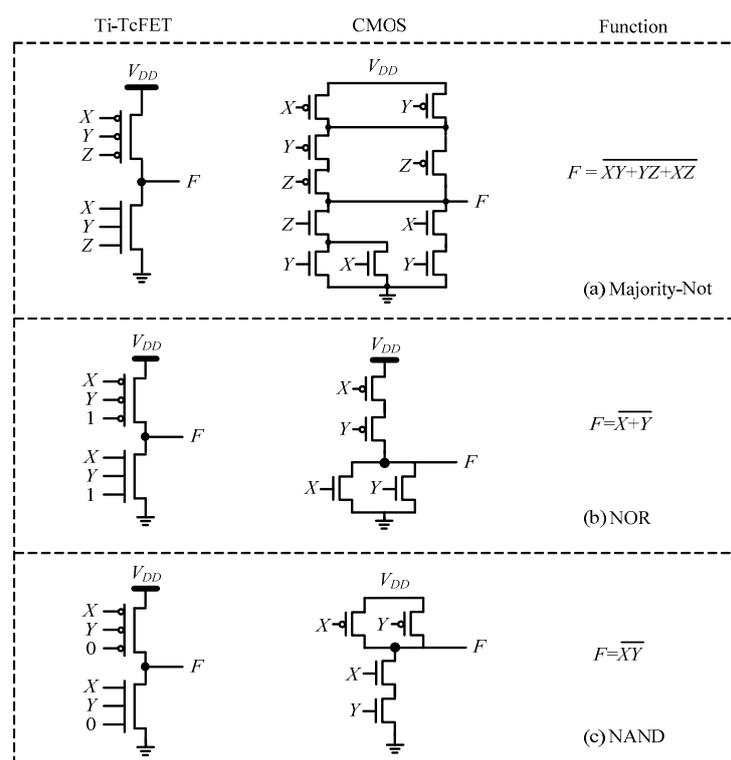


Figure 13. The logic cells based on Ti-TcFET devices: (a) majority-not, (b) NOT-OR (NOR), and (c) NOT-AND (NAND).

The Ti-TcFET devices can also be used to implement other logic gates in a compact style, such as NOR and NAND, as shown in Figure 13b,c, respectively. For more complex logic circuits, such as a full adder, the circuit structure can also be simplified by using Ti-TcFET devices, as shown in Figure 14a. For comparison, Figure 14b shows the full adder using traditional CMOS/FinFETs.

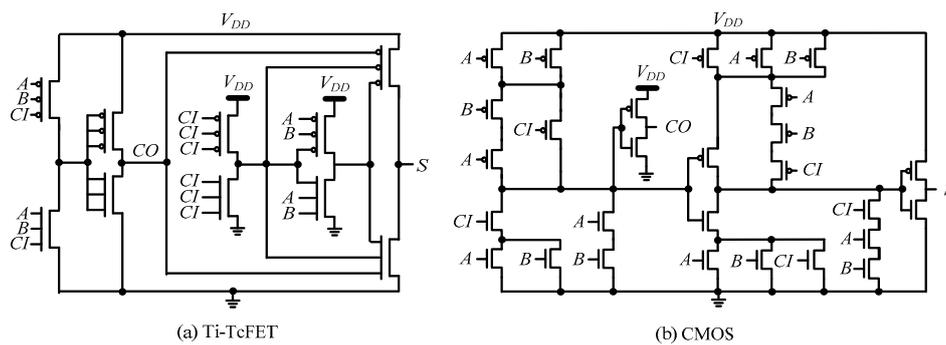


Figure 14. Full adders based on Ti-TcFET devices (a) and complementary metal-oxide-semiconductor (CMOS) devices (b).

The power consumption, delay, and power delay product of the one-bit full adder using Ti-TcFET devices and standard FinFET devices are compared in Table 4. From Table 4, the power consumption and power delay product of the one-bit full adder based on Ti-TcFET devices are smaller than standard FinFET devices, with an acceptable delay penalty.

Table 4. The power consumption, delay, and power delay product of the one-bit full adder using Ti-TcFET devices and standard FinFET devices.

Full Adder	Power Consumption (nW)	Delay (pS)	Power Delay Product (zJ)
FinFET	19.29	44.38	856
Ti-TcFET	9.26	59.59	554

4. Conclusions

In this paper, a novel T-channel field effect transistor with three input terminals (Ti-TcFET) is proposed. The T-channel structure increases the coupling area between the top gate and the front and back gates so that the device can realize the “majority-not” function well. By adjusting the gate work function, channel thickness, and the thickness of the gate oxide layer, the performance of the Ti-TcFET device is optimized. The results show that when the gate work function Φ of the N-type Ti-TcFET is 4.95 eV, $T_{Si} = 4$ nm, and $T_{OX} = 3$ nm, the minimum turn-on current I_{on} is 1.14×10^{-5} A and the maximum turn-off I_{off} is 2.06×10^{-8} A, with the switching current ratio I_{on}/I_{off} of 553. When the gate work function Φ of the P-type Ti-TcFET is 4.52 eV, $T_{Si} = 4$ nm, and $T_{OX} = 3$ nm, the minimum turn-on current I_{on} is 7.09×10^{-6} A and the maximum turn-off current I_{off} is 1.57×10^{-8} A, with the switching current ratio I_{on}/I_{off} of 452. The purpose of this paper was to propose a three input device to simplify the circuit structure and thus to provide a new idea for future circuit designs.

In the future, we will optimize the N-type and P-type Ti-TcFETs by applying new materials such as ferroelectric materials and two-dimensional materials, which should be helpful to increase the switching current ratio of the device and to decrease the leakage current.

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References

1. Colinge, J.P.; Gao, M.H.; Romano-Rodriguez, A.; Maes, H.; Claeys, C. Silicon-on-insulator 'gate-all-around device'. In Proceedings of the 1990 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 9–12 December 1990; pp. 595–598.
2. Kavalieros, J.; Doyle, B.; Datta, S.; Dewey, G.; Doczy, M.; Jin, B.; Lionberger, D.; Metz, M.; Rachmady, W.; Radosavljevic, M.; et al. Tri-gate transistor architecture with high-k gate dielectrics, metal gates and strain engineering. In Proceedings of the 2006 Symposium on VLSI Technology, 2006. Digest of Technical Papers, Honolulu, HI, USA, 13–15 June 2006; pp. 50–51.
3. Yang, F.L.; Chen, H.Y.; Chen, F.C.; Huang, C.C.; Chang, C.Y.; Chiu, H.K.; Lee, C.C.; Chen, C.C.; Huang, H.T.; Chen, C.J.; et al. 25 nm CMOS omega FETs. In Proceedings of the 2002 International Electron Devices Meeting, San Francisco, CA, USA, 8–11 December 2002; pp. 255–258.
4. Liu, C.; Zheng, F.; Sun, Y.; Li, X.; Shi, Y. Highly flexible SRAM cells based on novel tri-independent-gate FinFET. *Superlattices Microstruct.* **2017**, *110*, 330–338. [[CrossRef](#)]
5. Liu, C.; Zheng, F.; Sun, Y.; Li, X.; Shi, Y. Novel tri-independent-gate FinFET for multi-current modes control. *Superlattices Microstruct.* **2017**, *109*, 374–381. [[CrossRef](#)]
6. Datta, A.; Goel, A.; Cakici, R.T.; Mahmoodi, H.; Lekshmanan, D.; Roy, K. Modeling and circuit synthesis for independently controlled double gate FinFET devices. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2007**, *26*, 1957–1966. [[CrossRef](#)]
7. Tawfik, S.A.; Kursun, V. Low-power and compact sequential circuits with independent-gate FinFETs. *IEEE Trans. Electron Devices* **2007**, *55*, 60–70. [[CrossRef](#)]
8. Gupta, S.K.; Kulkarni, J.P.; Roy, K. Tri-mode independent gate FinFET-based SRAM with pass-gate feedback: Technology–circuit co-design for enhanced cell stability. *IEEE Trans. Electron Devices* **2013**, *60*, 3696–3704. [[CrossRef](#)]
9. Zhang, X.; Hu, J.; Luo, X. Optimization of dual-threshold independent-gate FinFETs for compact low power logic circuits. In Proceedings of the 2016 IEEE 16th International Conference on Nanotechnology (IEEE-NANO), Sendai, Japan, 22–25 August 2016; pp. 529–532.
10. Ni, H.; Hu, J.; Yang, H.; Zhu, H. Comprehensive Optimization of Dual Threshold Independent-Gate FinFET and SRAM Cells. *Act. Passive Electron. Compon.* **2018**, *2018*, 1–10. [[CrossRef](#)]
11. Fried, D.M.; Duster, J.S.; Kornegay, K.T. Improved independent gate N-type FinFET fabrication and characterization. *IEEE Electron Device Lett.* **2003**, *24*, 592–594. [[CrossRef](#)]
12. *ATLAS User's Manual Volume I*. Silvaco International. Available online: <https://dynamic.silvaco.com/dynamicweb/jsp/downloads/DownloadManualsAction.do?req=silen-manuals&nm=atlas> (accessed on 30 August 2016).
13. Amaru, L.; Gaillardon, P.E.; De Micheli, G. Majority-inverter graph: A new paradigm for logic optimization. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2015**, *35*, 806–819. [[CrossRef](#)]
14. Amaru, L.; Gaillardon, P.E.; De Micheli, G. Majority-inverter graph: A novel data-structure and algorithms for efficient logic optimization. In Proceedings of the 51st Annual Design Automation Conference, San Francisco, CA, USA, 1 June 2014; pp. 1–6.
15. Han, J.W.; Kim, C.J.; Choi, Y.K. Universal potential model in tied and separated double-gate MOSFETs with consideration of symmetric and asymmetric structure. *IEEE Trans. Electron Devices* **2008**, *55*, 1472–1479. [[CrossRef](#)]
16. Ghai, D.; Mohanty, S.P.; Thakral, G. Comparative analysis of double gate FinFET configurations for analog circuit design. In Proceedings of the 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS), Columbus, OH, USA, 4 August 2013; pp. 809–812.
17. Granzner, R.; Schwierz, F.; Polyakov, V.M. An analytical model for the threshold voltage shift caused by two-dimensional quantum confinement in undoped multiple-gate MOSFETs. *IEEE Trans. Electron Devices* **2007**, *54*, 2562–2565. [[CrossRef](#)]
18. Fossum, J.G. Physical insights on nanoscale multi-gate CMOS design. *Solid-State Electron.* **2007**, *51*, 188–194. [[CrossRef](#)]
19. Hu, C. Low-voltage CMOS device scaling. In Proceedings of the IEEE International Solid-State Circuits Conference-ISSCC'94, San Francisco, CA, USA, 16 February 1994; pp. 86–87.

20. Lin, X.; Wang, Y.; Pedram, M. Stack sizing analysis and optimization for FinFET logic cells and circuits operating in the sub/near-threshold regime. In Proceedings of the Fifteenth International Symposium on Quality Electronic Design, Santa Clara, CA, USA, 3 March 2014; pp. 341–348.
21. Harris, D.M.; Keller, B.; Karl, J.; Keller, S. A transregional model for near-threshold circuits with application to minimum-energy operation. In Proceedings of the 2010 International Conference on Microelectronics, Cairo, Egypt, 19 December 2010; pp. 64–67.
22. Rostami, M.; Mohanram, K. Dual- V_{th} independent-gate FinFETs for low power logic circuits. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2011**, *30*, 337–349. [[CrossRef](#)]
23. Masahara, M.; Surdeanu, R.; Witters, L.; Doornbos, G.; Nguyen, V.H.; Vrancken, C.; Jurczak, M.; Biesemans, S. Experimental investigation of optimum gate workfunction for CMOS four-terminal multigate MOSFETs (MUGFETs). *IEEE Trans. Electron Devices* **2007**, *54*, 1431–1437. [[CrossRef](#)]
24. McGuire, F.A.; Lin, Y.C.; Price, K.; Rayner, G.B.; Khandelwal, S.; Salahuddin, S.; Franklin, A.D. Sustained sub-60 mV/decade switching via the negative capacitance effect in MoS₂ transistors. *Nano Lett.* **2017**, *17*, 4801–4806. [[CrossRef](#)]
25. Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-layer MoS₂ transistors. *Nat. Nanotechnol.* **2011**, *6*, 147–150. [[CrossRef](#)] [[PubMed](#)]
26. Chu, Z.; Tang, X.; Soeken, M.; Petkovska, A.; Zgheib, G.; Amarù, L.; Xia, Y.; Ienne, P.; De Micheli, G.; Gaillardon, P.E. Improving circuit mapping performance through mig-based synthesis for carry chains. In Proceedings of the on Great Lakes Symposium on VLSI 2017, New York, NY, USA, 10 May 2017; pp. 131–136.
27. Navi, K.; Moaiyeri, M.H.; Mirzaee, R.F.; Hashemipour, O.; Nezhad, B.M. Two new low-power full adders based on majority-not gates. *Microelectron. J.* **2009**, *40*, 126–130. [[CrossRef](#)]



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