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Design of the Threshold-Controllable Memristor Emulator Based on NDR Characteristics

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Abstract: Due to the high manufacturing cost of memristors, an equivalent emulator has been employed as one of the mainstream approaches of memristor research. A threshold-type memristor emulator based on negative differential resistance (NDR) characteristics is proposed, with the core part being the R-HBT network composed of transistors. The advantage of the NDR-based memristor emulator is the controllable threshold, where the state of the memristor can be changed by setting the control voltage, which makes the memristor circuit design more flexible. The operation frequency of the memristor emulator is about 250 kHz. The experimental results prove the feasibility and correctness of the threshold-controllable memristor emulator circuit.

Keywords: memristor emulator; controllable threshold; NDR

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1. Introduction

Memristors have received widespread attention in the world since HP Labs successfully manufactured TiO_2 memristors in 2008 [1,2]. A memristor is a non-linear resistor with memory characteristics, and its *i-v* characteristic curve is related to the frequency. Its proven good performance implies significant potential in the fields of chaotic circuits [3–5], non-volatile memory [6,7], digital logic [8,9], artificial neural networks [10–12], and non-linear circuits. In general, the research of memristors includes physical implementation [2,13,14], applications in electronic circuits [15,16], and memristor emulators [17–26].

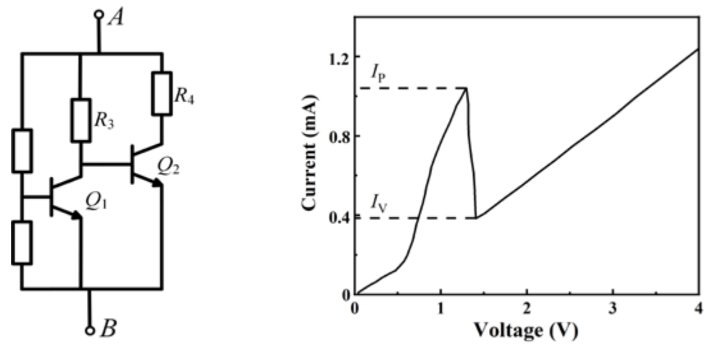
The studies on memristor emulators have achieved many results, and a variety of different memristor emulator circuit structures have been proposed, which can be divided into two categories: grounded memristor emulator circuits [18,19] and floating memristor emulator circuits [20–26]. To design a grounded memristor emulator is easier than a floating memristor emulator. However, due to the fact that one terminal is grounded, the grounded memristor emulator has limited features in circuit designs and applications, and is not suitable for use as a two-terminal device in more complicated circuits [20]. Compared with grounded memristor emulators, the application of floating memristor emulators is more flexible, which can be realized by various active elements, such as second-generation current conveyor (CCII) [21], operational transconductance amplifier (OTA) [22], multi outputs OTA [23], current voltage differencing transconductance amplifier (VDTA) [24], and voltage differencing current conveyor (VDCC) [25] with accompanying passive elements and possibly analog multipliers (AD633) [26]. Although some commercial memristor chips are already available on the market, e.g., Knowm.com (accessed on 9 May 2019) [27], memristor emulators have yet to be widely studied and adopted due to their lower cost.

This article proposes a novel floating threshold-type memristor emulator devised based on the negative differential resistance (NDR) characteristic. Not only does the proposed memristor emulator have a high operating frequency, but it also possesses the controllable threshold voltage, an attribute that makes it more suited for digital logic circuit applications.

The rest of this paper is organized as follows: in Section 2, the NDR hysteresis unit is introduced and improved on the basis of the R-HBT-NDR unit, and its simulation and hardware experiments are carried out. Section 3 presents the circuit diagram of the threshold-controllable memristor based on NDR characteristics. Section 4 provides the specific circuit implementation and the detailed analysis of its operating principle. In Section 5, the simulation experimental results are presented. Section 6 summarizes the paper.

2. Improvement and Design of NDR Hysteresis Unit

Kwang-Jow Gan proposed an R-HBT-NDR unit [28–30] with negative resistance characteristics, as shown in Figure 1.



(**a**) (**b**)

Figure 1. R-HBT-NDR unit and its *i-v* characteristic curve: (**a**) R-HBT-NDR unit, (**b**) the *i-v* characteristic curve of R-HBT-NDR unit.

When a sinusoidal signal V_{AB} is applied to the R-HBT-NDR unit, its *i-v* characteristic curve has a certain hysteresis, as shown in Figure 2 [31].

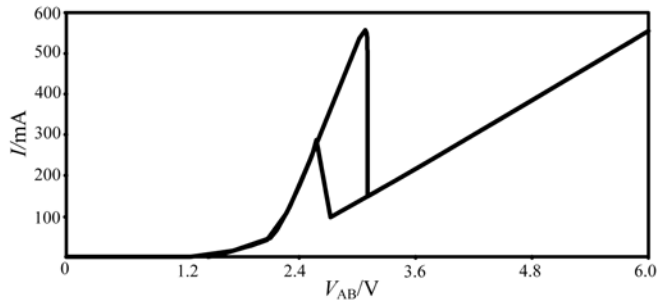


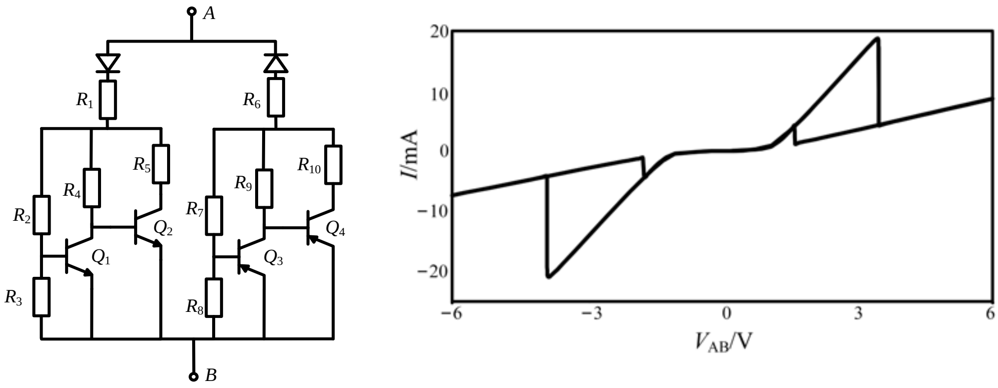
Figure 2. Hysteresis characteristic of the R-HBT-NDR unit.

With the increase in V_{AB}, transistor Q_2 turns on first, and then transistor Q_1; the current flowing through the R-HBT-NDR unit increases. When V_{AB} continues to increase, Q_1 reaches the saturated state, which triggers Q_2 to turn off. The current flowing through the R-HBT-NDR unit then decreases considerably from I_P to I_V, where negative resistance appears. With the further increase of V_{AB}, Q_2 remains off, while Q_1 enters into the deep saturation state, and the current flowing through the R-HBT-NDR unit increases slowly with the change of the input signal V_{AB}.

When V_{AB} starts to decrease, Q_1 enters the cut-off state; Q_2 turns on, and then the current flowing through the R-HBT-NDR unit will increase. As the input signal continues to decrease, Q_2 turns off to end.

Therefore, the movement path of the operation points differs with the increase and decrease of V_{AB}, resulting in a hysteresis loop.

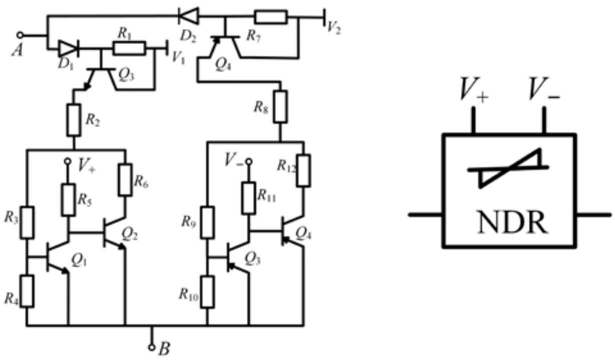
Figure 2 only presents the forward part of the curve because of the feature of the NPN transistor. If an extra R-HBT-NDR unit is implemented in the circuit, which consists of PNP bipolar transistors, shown as Figure 3a, under the excitation of the sinusoidal signal, the bidirectional hysteresis curve can be obtained, as shown in Figure 3b.



(**a**) (**b**)

Figure 3. Bidirectional NDR hysteresis unit and its *i-v* characteristic curve: (**a**) bidirectional NDR hysteresis unit, (**b**) the *i-v* characteristic curve of bidirectional NDR hysteresis unit.

It can be seen from Figure 3b that the characteristic curve of the bidirectional NDR hysteresis unit shows two hysteresis loops. Meanwhile, the curve has a slope of 0 near the origin, indicating that the change of V_{AB} will not affect the resistance, which can be attributed to the influence of the transistor turn-on voltage. Therefore, an improved NDR hysteresis unit is realized, as shown in Figure 4a, and its simplified symbol can be expressed as Figure 4b.

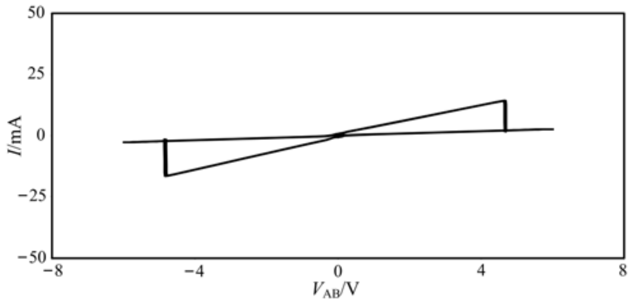


(**a**) (**b**)

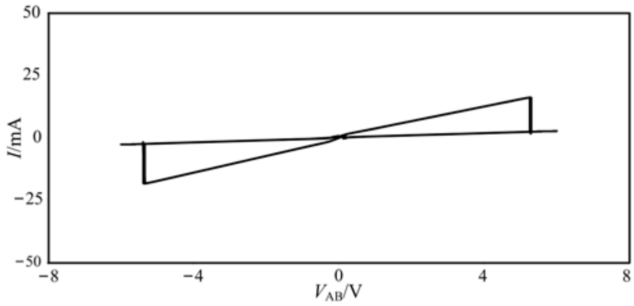
Figure 4. Improved NDR hysteresis circuit and its simplified symbol: (**a**) improved NDR hysteresis circuit, (**b**) the simplified symbol of improved NDR hysteresis circuit.

The improved NDR hysteresis unit differentiates its structure from Figure 3a in its two terminals of V_+ and V_-, which have the same voltage magnitude and opposite signs. With the change of V_+ and V_-, the bias voltage of each device in the NDR hysteresis unit will change accordingly, resulting in the different shape of the output curve, as shown in Figure 5.

In Figure 5a, $V_+ = -V_- = 2$ V, it can be seen that when $V_{AB} = -4.8$ V or 4.6 V, the state of the hysteresis curve is changed. In Figure 5b, $V_+ = -V_- = 6$ V, when $V_{AB} = -5.4$ V or 5.3 V, the state of the hysteresis curve is changed.



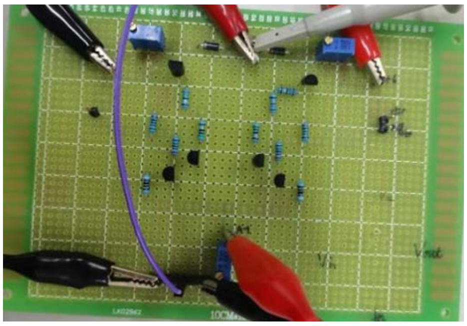
(**a**)



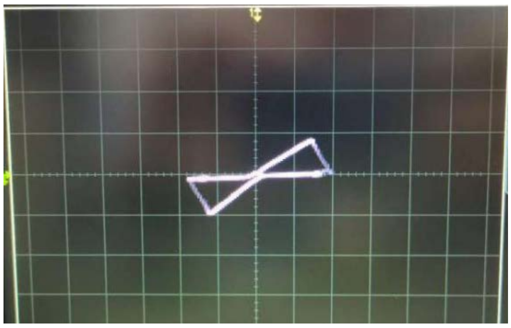
(**b**)

Figure 5. The *i-v* characteristic curve of the improved hysteresis circuit: (**a**) when $V_+ = -V_- = 2$ V, (**b**) when $V_+ = -V_- = 6$ V.

A hardware circuit of the improved NDR hysteresis unit is completed, as shown in Figure 6a. A resistor is connected in series as a load, and the current can be observed by measuring the voltage on the load resistor. Under the excitation of a sinusoidal signal with an amplitude of 6 V and a frequency of 5 kHz, $V_+ = V_1 = 6$ V, $V_- = V_2 = -6$ V, $R_1 = R_7 = 10\ \Omega$, $R_2 = 240\ \Omega$, $R_3 = R_5 = R_9 = R_{11} = 2$ kΩ, $R_4 = R_{10} = 8.8$ kΩ, $R_6 = R_{12} = 50\ \Omega$, $R_8 = 280\ \Omega$. The experimental results are coincident with the simulation results.



(**a**)



(**b**)

Figure 6. Improved NDR hysteresis unit hardware circuit and its experimental result: (**a**) improved NDR hysteresis unit hardware circuit, (**b**) experimental result.

By analyzing the curve in Figure 6, it can be found that it is very similar to the *i-v* curve of the TEAM threshold memristor proposed in 2013 [32], shown in Figure 7.

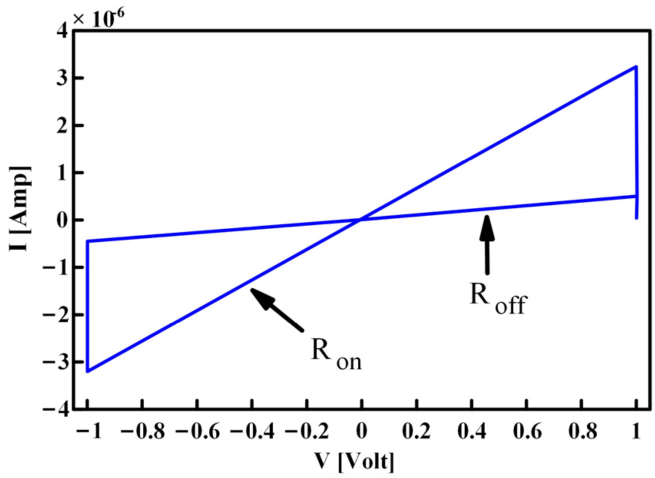


Figure 7. The *i-v* characteristic curve of the TEAM threshold type memristor.

The definition of the threshold type memristor can be expressed as follows [25]:

$$G = \begin{cases} G_H & V_{th1} < V_X \\ \text{hold} & V_{th2} \le V_X \le V_{th1} \\ G_L & V_X < V_{th1} \end{cases} \tag{1}$$

G is the memductance of the threshold memristor, with G_H and G_L corresponding to the two resistance states of the memristor: low resistance (L_{RS}) and high resistance (H_{RS}), respectively. V_{th1} and V_{th2} represent the threshold voltages of the memristor. When the voltage V_X applied to the memristor is greater than V_{th1}, the memristor switches to G_H; when the voltage V_X is less than V_{th2}, the memristor is switched to G_L; if the voltage applied to the memristor is between V_{th1} and V_{th2}, the state of the memristor remains unchanged.

The hysteresis characteristic curve of the improved NDR hysteresis unit is so similar to the threshold-type memristor that we can utilize this unit to design a novel NDR memristor emulator. This is where the inspiration of this paper originates.

3. Circuit Structure Analysis of Threshold-Controllable Memristor Based on NDR Unit

A diagram of the threshold-controllable memristor based on the NDR unit is shown in Figure 8, with an improved bidirectional NDR hysteresis module as the core. It also includes the memductance conversion module, multiplier module, and current transmission module.

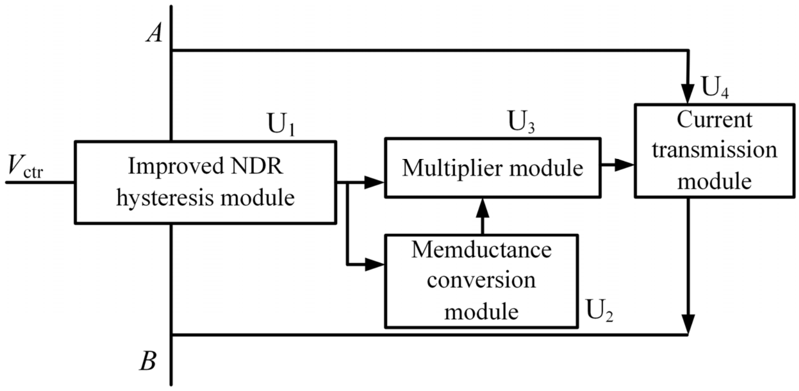


Figure 8. Diagram of threshold-controllable memristor emulator based on NDR units.

The improved NDR hysteresis module U_1 realizes the hysteresis characteristics; the memductance conversion module U_2 realizes the non-volatile and high and low resistance conversion characteristics of the memristor; the multiplier module U_3 converts the current of the memristor into a proportional voltage; the current transmission module U_4 ensures the equal flow of the current at either end of the memristor.

V_{ctr}, represented by V_+ and V_- in Figure 4, is the control voltage. According to the above analysis, by changing the voltage of V_{ctr}, the threshold of the memristor will also be changed to realize the change of the memristor resistance state. The symbol of the threshold-controllable memristor emulator can be expressed in a simplified form, as shown in Figure 9.

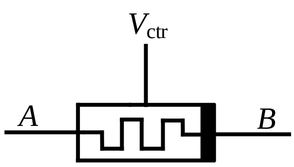


Figure 9. Simplified symbol of threshold-controllable memristor.

4. Circuit Design of Threshold-Controllable Memristor

The threshold-controllable memristor emulator circuit based on the improved NDR hysteresis unit is shown in Figure 10. The specific analysis of each module is as follows.

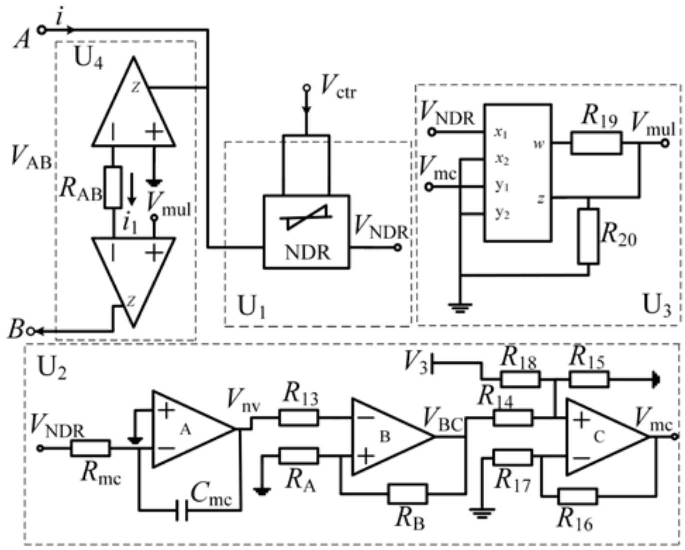


Figure 10. Threshold-controllable memristor emulator circuit based on the improved NDR hysteresis unit.

4.1. Improved NDR Hysteresis Module U_1

U_1 is the improved NDR hysteresis module. V_{ctr} is a threshold control terminal. When V_{ctr} changes, the change trajectories of output V_{NDR} are shown in Figure 11. The input voltage is a sinusoidal signal with an amplitude of 6 V and a frequency of 5 kHz.

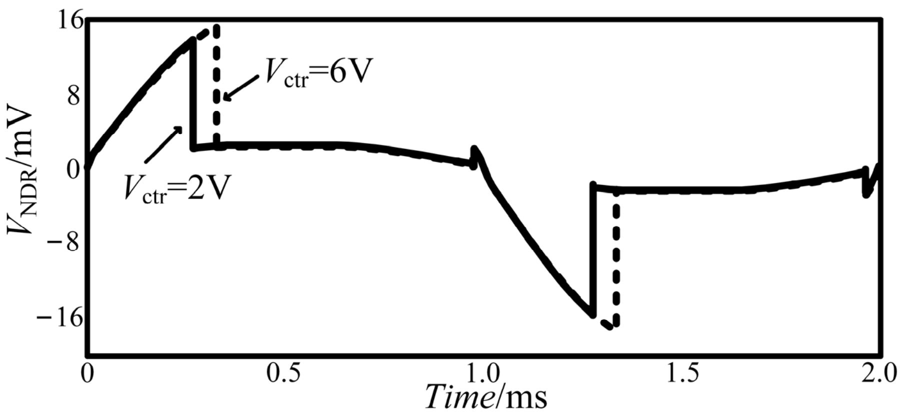


Figure 11. Output curves of V_{NDR}.

A relationship is found between V_{ctr} and V_{NDR}: when V_{ctr} increases, V_{NDR} will increase accordingly, which can be expressed as:

$$V_{NDR} = f(V_{ctr}) \tag{2}$$

4.2. Memductance Conversion Module U_2

U_2 is the memductance conversion module, composed of a four-channel operational amplifier TL084, a capacitor, and several resistors, which is used to achieve the non-volatile and high/low resistance characteristics of memristors. The output V_{NDR} of U_1 is the input signal of U_2.

Since the memristor has the non-volatile characteristic, its resistance must be related to the previous state. R_{mc} and C_{mc} form the integrator with the output V_{nv} of:

$$V_{nv} = -\frac{1}{R_{mc}C_{mc}}\int V_{NDR}dt = -\frac{1}{R_{mc}C_{mc}}\int f(V_{ctr})dt \quad (3)$$

Figure 12 presents the characteristics of the bistable circuit that is composed of part B of TL084.

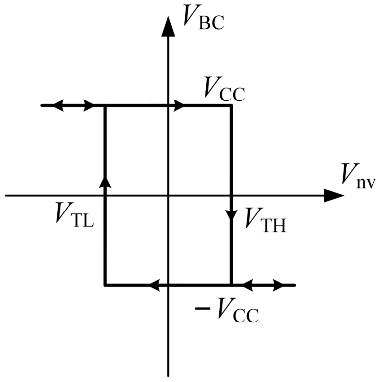


Figure 12. Characteristics of the bistable circuit composed of part B of TL084.

In Figure 12, when V_{nv} is greater than V_{TH}, the output is $-V_{CC}$; when V_{nv} is less than V_{TL}, the output is V_{CC}; when V_{nv} is between V_{TL} and V_{TH}, the state will not change. $-V_{CC}$ and V_{CC} represent the power supply voltages of TL084. Therefore, the output voltage V_{BC} of the bistable circuit is expressed as follows:

$$V_{BC} = \begin{cases} -V_{CC} & V_{TH} < V_{nv} \\ \text{hold} & V_{TL} \le V_{nv} \le V_{TH} \\ V_{CC} & V_{nv} < V_{TL} \end{cases} \quad (4)$$

and the threshold voltages of V_{TH} and V_{TL} are expressed as follows:

$$V_{TH} = -V_{TL} = \frac{R_A}{R_B + R_A}V_{CC} \quad (5)$$

In addition, in order to achieve the single polarity for the output voltage of V_{mc}, a summing circuit is constructed, which consists of part C of TL084, V_3, R_{14}, R_{15}, R_{16}, R_{17}, and R_{18}. The corresponding output V_{mc} is expressed as follows:

$$\begin{aligned} V_{mc} &= \begin{cases} -(bV_3 - aV_{CC}) & V_{TH} < V_{nv} \\ \text{hold} & V_{TL} \le V_{nv} \le V_{TH} \\ -(aV_{CC} + bV_3) & V_{nv} < V_{TL} \end{cases} \\ &= \begin{cases} -(bV_3 - aV_{CC}) & V_{TH} < -\frac{1}{R_{mc}C_{mc}}\int f(V_{ctr})dt \\ \text{hold} & V_{TL} \le -\frac{1}{R_{mc}C_{mc}}\int f(V_{ctr})dt \le V_{TH} \\ -(aV_{CC} + bV_3) & -\frac{1}{R_{mc}C_{mc}}\int f(V_{ctr})dt < V_{TL} \end{cases} \end{aligned} \quad (6)$$

where $a = R_{16}/R_{14}$, $b = R_{16}/R_{15}$; compared to the definition of the threshold-type memristor in (1), $(aV_{CC} + bV_3)$ can be seen as a voltage representation of the high-memductance state of memristor; $(bV_3 - aV_{CC})$ can be seen as a voltage representation of the low-memductance state of the memristor.

4.3. Multiplier Module U_3

U_3 is the multiplier module and it is composed of a multiplier AD633, which converts the current of the memristor into a proportional voltage. The output of U_3 can be expressed as follows:

$$V_{mul} = \frac{R_{19}+R_{20}}{10R_{19}} V_{NDR} V_{mc} = \frac{R_{19}+R_{20}}{10R_{19}} f(V_{ctr}) V_{mc} \quad (7)$$

where V_{NDR} is the output of U_1 and V_{mc} is the output of U_2. R_{19} and R_{20} adjust the multiplication coefficient.

4.4. Current Transmission Module U_4

U_4 is the current transmission module and composed of two AD844 operational amplifiers. This module converts the voltage V_{mul} into the corresponding current and ensures equal currents flowing through A and B terminals. The current through the memristor is expressed as follows:

$$i = \frac{V_{mul}}{R_{AB}} \quad (8)$$

and the current flowing through R_{AB} is $i_1 = V_{AB}/R_{AB}$; therefore, the memductance G can be represented by the voltage V_{mc}, as follows:

$$G = \frac{i}{V_{AB}} = \frac{(R_{19}+R_{20})}{10R_{19} i_1 R_{AB}^2} V_{NDR} V_{mc} = \frac{(R_{19}+R_{20})}{10R_{19} i_1 R_{AB}^2} f(V_{ctr}) V_{mc} \quad (9)$$

Assuming $k_G = (R_{19} + R_{20})/(10R_{19} i_1 R_{AB}^2) = (R_{19} + R_{20})/(10R_{19} i_1 R_{AB}^2)$, G can also be expressed as:

$$G = \frac{i}{V_{AB}} = k_G V_{NDR} V_{mc} = k_G f(V_{ctr}) V_{mc} \quad (10)$$

Therefore, the mathematical emulator of the memristor emulator circuit can be expressed as follows:

$$\begin{aligned} G &= \begin{cases} -k_G\, f(V_{ctr})(aV_{CC} + bV_3) & -R_{mc}C_{mc}V_{TL} < V_{nv} \\ \text{hold} & -R_{mc}C_{mc}V_{TH} \le V_{nv} \le -R_{mc}C_{mc}V_{TL} \\ -k_G\, f(V_{ctr})(bV_3 - aV_{CC}) & V_{nv} < -R_{mc}C_{mc}V_{TH} \end{cases} \\ &= \begin{cases} -k_G\, f(V_{ctr})(aV_{CC} + bV_3) & -R_{mc}C_{mc}V_{TL} < -\frac{1}{R_{mc}C_{mc}}\int f(V_{ctr})dt \\ \text{hold} & -R_{mc}C_{mc}V_{TH} \le -\frac{1}{R_{mc}C_{mc}}\int f(V_{ctr})dt \le -R_{mc}C_{mc}V_{TL} \\ -k_G\, f(V_{ctr})(bV_3 - aV_{CC}) & -\frac{1}{R_{mc}C_{mc}}\int f(V_{ctr})dt < -R_{mc}C_{mc}V_{TH} \end{cases} \end{aligned} \quad (11)$$

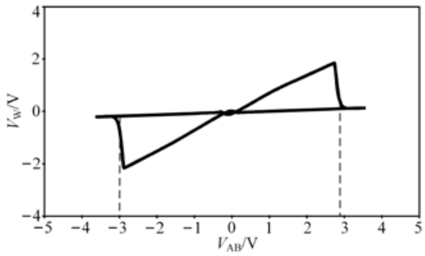
Compared with Equation (1), G in Equation (11) satisfies the definition of threshold memristors. In addition, when the value of V_{ctr} changes, G changes, with the threshold-controllable function thereby being achieved.

5. Verification of Threshold-Controllable Memristor

5.1. Simulation Results

The simulation results of the threshold-controllable memristor are shown in Figure 13: $R_1 = R_7 = 19\ \Omega$, $R_2 = 7.5\ \Omega$, $R_3 = R_5 = R_9 = R_{11} = 2$ kΩ, $R_4 = R_{10} = 8$ kΩ, $R_6 = R_{12} = 51\ \Omega$, $R_8 = 29\ \Omega$, $R_{13} = 1\ \Omega$, $R_{14} = 9.1$ kΩ, $R_{15} = 1$ kΩ, $R_{16} = 10$ kΩ, $R_{17} = R_{18} = 1$ kΩ, $R_{19} = 10$ kΩ, $R_{20} = 5.6$ kΩ, $R_{mc} = 10$ kΩ, $C_{mc} = 1$ nF, $R_A = 0.5$ kΩ, $R_B = 2.5$ kΩ, $R_{AB} = 100$ kΩ. The excitation signal is a sinusoidal signal with a 5 V amplitude 30 kHz frequency.

When $V_{ctr} = 6$ V, the threshold voltage of the memristor is about ± 2.9 V; when $V_{ctr} = 2$ V, the threshold voltage is -2.6 V and 2.7 V. Therefore, when V_{ctr} changes, the memristor threshold voltage changes accordingly. This feature can be applied to digital logic circuits design where the state of the memristor can switch to high or low in order for varied logic states by only changing V_{ctr}, and different functions will be achieved without modifying the circuit structure and input signals.



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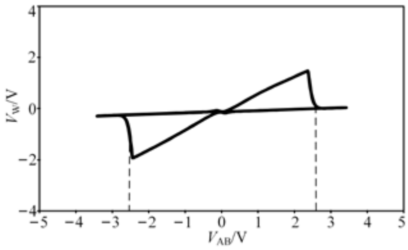
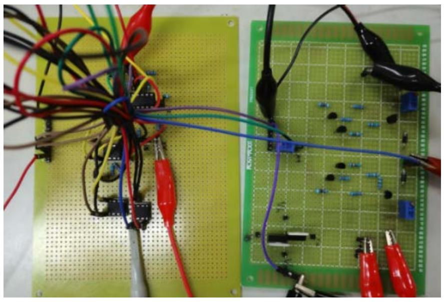


(**b**)

Figure 13. Simulation curves: (**a**) V_{ctr} = 6 V, (**b**) V_{ctr} = 2 V.

5.2. Experimental Results

The hardware circuit of the threshold-controllable memristor emulator based on NDR characteristics and its experimental results is shown in Figure 14.



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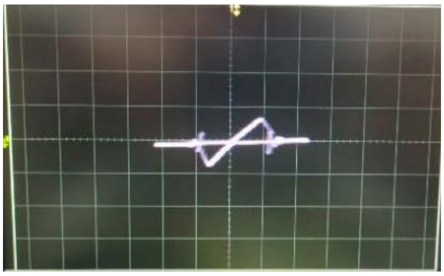

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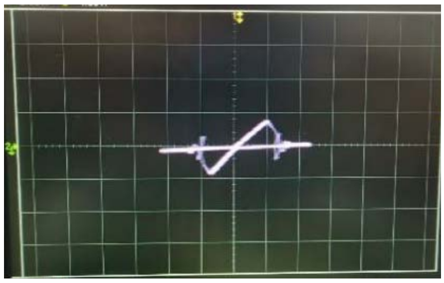

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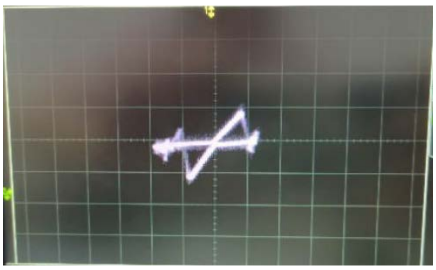

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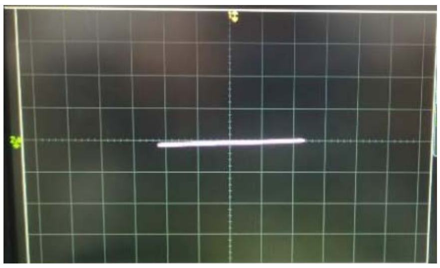

(**e**)

Figure 14. Hardware circuit and experimental results: (**a**) the circuit of the threshold-controllable memristor emulator, (**b**) V_{ctr} = 2 V, f = 72 kHz, (**c**) V_{ctr} = 6 V, f = 72 kHz, (**d**) V_{ctr} = 6 V, f = 250 kHz, (**e**) V_{ctr} = 6 V, f = 345 kHz.

Under the excitation of a sinusoidal signal with an amplitude of 6 V and a frequency of 72 kHz, when V_{ctr} = 2 V, its threshold voltages are −2 V and 2.1 V, as shown in Figure 14b. When V_{ctr} = 6 V, its threshold is about −2.2 V and 2.8 V, as in Figure 14c. If the frequency keeps increasing until 345 kHz, the hysteresis loop will be missing and the non-volatile characteristic disappears, as in Figure 14e.

6. Conclusions

A threshold-controllable memristor emulator based on NDR characteristics is proposed, which is composed of an improved NDR hysteresis unit, multipliers, and operational amplifiers. In addition to the basic characteristics of memristors such as being non-volatile and non-linear, this emulator circuit also has the advantage of threshold controllability and high operating frequency. Compared to the two-terminal structure of the traditional memristor, the threshold-controllable memristor emulator is more suitable for digital circuit design thanks to its additional control terminal structure, where the memristor threshold switches under different control voltages, indicating more flexible and convenient memristor-based circuit designs. Our follow-up effort will be committed to continuously optimizing the performance of the emulator, and the attempt to apply it to the design of memristive digital logic circuits.

Author Contributions: Conceptualization, writing, review, visualization: M.L.; simulation, experiment: W.L. (Wenyao Luo); methodology, data curation: L.L.; formal analysis: Q.H.; investigation, supervision: W.L. (Weifeng Lyu). All authors have read and agreed to the published version of the manuscript.

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