

Article

Ultra-Wideband Transformer Feedback Monolithic Microwave Integrated Circuit Power Amplifier Design on 0.25 μm GaN Process

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Abstract: This paper presents an ultra-wideband transformer feedback (TFB) monolithic microwave integrated circuit (MMIC) power amplifier (PA) developed using a 0.25 μm gallium nitride (GaN) process. To broaden the bandwidth, a drain-to-gate TFB technique is employed in this PA design, achieving a 117% relative -3 dB bandwidth, extending from 5.4 GHz to 20.3 GHz. At a 28 V supply, the designed PA circuit achieves an output power of 25.5 dBm and a 14 dB small-signal gain in the frequency range of 6 to 19 GHz. Within the 6 to 19 GHz frequency range, the small-signal gain exhibits a flatness of less than 0.78 dB. The PA chip occupies an area of 1.571 mm². This work is the first to design a power amplifier with on-chip transformer feedback in a compound semiconductor MMIC process, and it enables the use of the widest bandwidth power amplifier on-chip transformer matching network.

Keywords: MMIC; TFB; wideband matching; transmission line theory



Citation: Luo, J.; Fan, Y.; Wan, J.; Sun, X.; Liang, X. Ultra-Wideband Transformer Feedback Monolithic Microwave Integrated Circuit Power Amplifier Design on 0.25 μm GaN Process. *Micromachines* **2024**, *15*, 546. <https://doi.org/10.3390/mi15040546>

Academic Editor: Parsian K. Mohseni

Received: 1 April 2024

Revised: 14 April 2024

Accepted: 17 April 2024

Published: 18 April 2024



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1. Introduction

To cope with the growing volume of data transmission and the requirement for transmission rate in the 5G era, broadband systems are receiving increasing attention and have become a trend in the development of communication systems. In fields such as national defense, frequency hopping systems required for electronic countermeasures or high-resolution radar surveillance systems also require a wide bandwidth operating space, which puts high demands on the actual RF microwave systems. According to Shannon's theorem, the expansion of channel capacity can be achieved by increasing the bandwidth with a certain signal-to-noise ratio, which is highly instructive for modern communication systems.

As a key component of RF systems, power amplifiers in the form of monolithic microwave integrated circuits (MMICs) are highly valued by designers because of their small size, light weight, and high reliability, and their high level of integration plays an important role in a variety of electronic system fields. There exist numerous design approaches for wideband PAs, encompassing strategies such as reactive matching, transformer matching [1], and distributed topology, among others. For wideband systems, particularly when the relative bandwidth exceeds 40%, feedback networks are typically utilized in the design of amplifier models. As the bandwidth widens, the optimal impedance of the transistor varies sharply, and the gain roll-off characteristic becomes more pronounced. These factors make broadband matching more difficult. The reason for this phenomenon is partly due to the larger volume and more complex parasitic coupling effects of GaN HEMT transistors, especially the parasitic capacitance (C_{gd}) at the gate and drain terminals of transistors that cannot be ignored. To address these challenges, traditional wideband PA designs often resort to methods such as low-Q reactive impedance matching, balanced structures [2,3],

or resistive shunt feedback [4,5]. However, these solutions tend to be less efficient and consume larger chip areas. As a better alternative, some research has begun to use on-chip transformer feedback in broadband amplifier designs to build feedback matching networks [6–8].

Transformer feedback (TFB) has found extensive applications in high-frequency circuits [1,9–16]. Within a single-stage amplifier, the drain-to-source and drain-to-gate TFB configurations serve to counterbalance the device gate–drain capacitance [9,10]. This method has been integrated into broadband amplifiers to boost bandwidth [15,16] and diminish noise levels [17,18]. Thus, the use of TFB technology has great application prospects for achieving good broadband performance.

In this paper, the design procedure for a 6–19 GHz transformer feedback (TFB) GaN power amplifier with a gain flatness of 0.78 dB is described. The TFB method in detail based on the distributed transformer modeling theory is proposed in this PA to achieve an ultra-wideband performance. The remainder of this paper is organized as follows: Section 2 will discuss different transformer design process parameters and the influence on the transformer performance. Section 3 will focus on the analysis of the TFB technique. Section 4 will cover the circuit design and the related measurement results, respectively. The conclusion of this work will be discussed in the final section, Section 5.

2. Transformer Design Process Comparison

For over half a century, under the guiding principle of Moore’s law, the silicon-based CMOS integrated circuit has stood as the cornerstone of the information society. At present, silicon semiconductor scaling has progressed to the nanometer level, encountering technical and performance limitations stemming from the inherent constraints of silicon’s performance characteristics. In pursuit of high-performance and ultra-wideband transceivers operating in the microwave spectrum, research has delved into III-V compound semiconductor technologies such as gallium arsenide (GaAs), indium phosphide (InP), aluminum nitride (AlN), and gallium nitride (GaN). These materials offer promising solutions for solid-state power amplifiers that are high-powered, cost-effective, and reliable. III-V compound semiconductor technology boasts superior transistor characteristics in high-frequency applications, while the semi-insulating substrate facilitates the integration of high-quality passive components with minimal parasitic elements. Table 1 presents a comparative overview of the properties of various semiconductor materials.

Table 1. Properties comparison of various semiconductor materials.

Property	Si	SiC	GaAs	InP	AlN	GaN
Energy bandgap (eV)	1.12	3.2	1.43	1.34	6.2	3.4
Breakdown field (10^6 V/cm)	0.3	3.2	0.4	0.6	11.7	3.3
Electron mobility ($\text{cm}^2/\text{V}\cdot\text{s}$)	1500	700	8500	4600	300	2000
Saturation velocity (10^5 m/s)	1.0	2.0	1.2	1.0	2.0	2.5
Thermal conductivity ($\text{W}/\text{cm}\cdot\text{K}$)	1.31	4.9	0.46	0.77	3.4	1.5

Compared with other materials, GaN materials have various characteristics such as a high breakdown voltage, high electron saturation rate, and high thermal conductivity, making devices made from these materials very suitable for RF applications. As shown in Figure 1, the creation of two-dimensional electron gas (2-DEG) channels in GaN HEMTs is achieved through AlGaIn/GaN heterojunctions, where a wide bandgap semiconductor (AlGaIn) interfaces with a narrow bandgap semiconductor (GaN). By establishing a 2-DEG channel within an undoped pure GaN layer, the impact of scattering by dopants is minimized, enabling the attainment of high electron mobility. The drain and source electrodes are both Ohmic contacts connected to the two-dimensional electron gas, with gate voltage controlling the two-dimensional electron gas beneath the gate Schottky junction to modulate the channel current. The reason for the gate electrode being closer to the source electrode in the structure is that in AlGaIn/GaN HEMTs, if breakdown occurs

during operation, the breakdown typically happens on the side of the gate closer to the drain electrode. This asymmetric structure can enhance the breakdown voltage, allowing the device to operate at higher drain-source voltages. GaN power devices operating at high current densities and voltages generate significant heat, leading to self-heating effects that can diminish the drain current, limit output power, and shorten device lifespan. Efficient heat dissipation is crucial, and one effective method involves releasing heat to the substrate. Silicon carbide (SiC) is a commonly used substrate for epitaxial growth in GaN HEMT technology due to its high thermal conductivity and low thermal resistance. The GaN MMIC process is mainly divided into two parts: front-side process and back-side process. The front-side process mainly produces GaN HEMT active devices and passive components such as resistors, MIM capacitors, microstrip lines, etc.; the back-side process includes wafer thinning, back-side via holes, and back-side metal deposition, which is used to form the ground plane of microstrip lines.

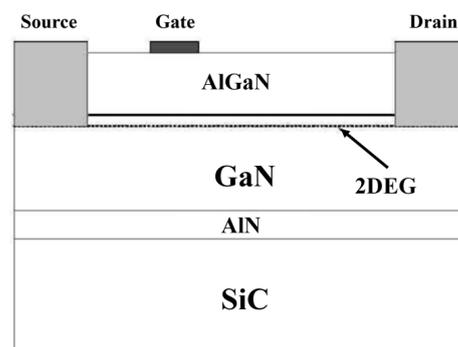


Figure 1. Typical AlGaN/GaN HEMT structure.

The performance of a fabricated inductor or transformer is determined by the IC technology process. This process involves several parameters related to the transformer, including the thickness of the top metal layer, metal conductance, minimum metal space, the distance of the metal layers from the substrate, the dielectric constant of the substrate, and so on. Due to parasitic and various loss mechanisms, the impedance transformation ratio is highly dependent on frequency and size and can deviate from its ideal value of 1, even in the case of a 1:1 transformer [19]. While some of these parameters are predefined in the technology process, they can still serve as a reference for transformer design.

Table 2 provides a comparison of major RF technology process parameters. The advanced CMOS process with a smaller feature size has more metal layers and a thicker top metal layer. For instance, the top metal conductance significantly improves to 5.816×10^7 S/m in the TSMC 0.13 μm CMOS process. The number of metal layers increases from 5 to 8 when transitioning from the TSMC 0.25 μm to the 0.13 μm CMOS process. In contrast, III-V compound processes like GaAs and GaN, also listed in this table, have only two metal layers, but they exhibit larger metal conductance and layer spacing. In the 0.25 μm GaN process, the top metal thickness reaches 4 μm , which is the thickest among the processes listed. Designing an on-chip transformer using a thicker metal layer can effectively increase the coupling coefficient and reduce loss. Additionally, it helps to increase the transformer's self-resonant frequency (f_{srf}), which is highly beneficial in practical design.

Therefore, in comparison to CMOS technology, the GaN process features a thicker top metal layer and larger metal conductance. However, its metal layers are closer to the substrate, leading to a higher degree of substrate loss. The GaN process also has a comparatively larger minimum metal layer space, with 6 μm for the MET2 layer. This characteristic may limit the coupling coefficient of a designed coplanar transformer to some extent.

Table 2. Technology process parameter comparison for transformer design.

Technology Process	TSMC 0.13 μm RF CMOS	TSMC 0.18 μm RF CMOS	TSMC 0.25 μm RF CMOS	WIN 0.15 μm InGaAs pHEMT	WIN 0.25 μm GaN on SiC
Number of metal layers	8	6	5	2	2
Min. metal layer space (μm)	/	1.5	/	4	6
Top layer metal thickness (μm)	3.3	2.34	0.99	2	4
Top metal to substrate distance (μm)	7.47	8.15	7.47	5.2	1.62
Top metal conductance (S/m)	5.816×10^7	2.464×10^7	2.464×10^7	4.1×10^7	4.1×10^7
Substrate dielectric constant	11.9	11.9	11.9	12.9	9.7

3. Analysis of Transformer Feedback Technique

In GaN transistors, the parasitic capacitance (C_{gd}) and its associated Miller effect pose significant challenges for wideband matching. Moreover, the parasitic negative feedback caused by C_{gd} between the gate and drain limits the power gain and reverse isolation, potentially leading to instability [20,21]. To counteract these issues, the gate–drain feedback mechanism is used to neutralize C_{gd} , broaden the maximum available gain/power gain frequency response, and ensure stability. Instead of the conventional RLC reactive feedback network (as seen in Figure 2a), TFB offers an alternative approach for wideband PA design. Figure 2b illustrates the schematic design of a gate–drain TFB amplifier. Here, L_1 and L_2 represent the inductance at the gate and drain biasing circuits, respectively, while k denotes the coupling coefficient between the primary and secondary windings. The TFB technique operates on the principle that the secondary inductance (L_2) senses the output current, and a proportion of this is fed back to the PA input through the primary inductance (L_1) [22]. This technique does sacrifice a portion of the transistor’s power gain, but it results in a flattened frequency response and expanded bandwidth. Furthermore, the use of a transformer feedback network can adjust the amplifier port impedance, which can simplify the matching circuit design to a certain degree.

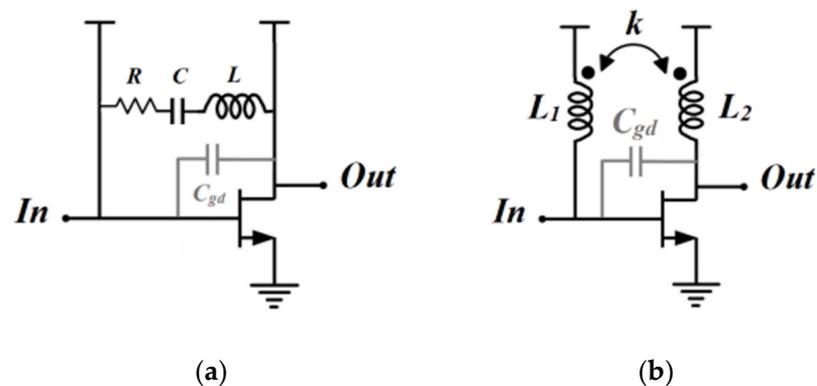


Figure 2. (a) The traditional RLC feedback common source (CS) amplifier; (b) the transformer feedback CS amplifier.

As illustrated in Figure 2b, the TFB amplifier can be configured with an L_1 inductance of 0.9 nH, an L_2 inductance of 0.5 nH, and a coupling coefficient of 0.32. The simulation results, presented in Figure 3a, reveal that by applying the TFB technique, the amplifier’s maximum available gain (MAG) and power gain extend to an ultra-wide range. The amplifier demonstrates an impressively flat frequency response, exhibiting a deviation of less than 1 dB across the range of 6 to 20 GHz. Evidently, the feedback network compensates for the transistor gain roll-off performance, simplifying the wideband matching circuit design as it does not require intentional adjustment of the insertion loss gain roll-off based on transistor performance trends. However, the amplifier’s gain performance is compromised. Without the TFB network, the amplifier’s MAG and power gain are 18.798 dB and 17.31 dB

@12 GHz, respectively. After incorporating the feedback, these values drop to 13.28 dB and 13.35 dB @12 GHz, respectively.

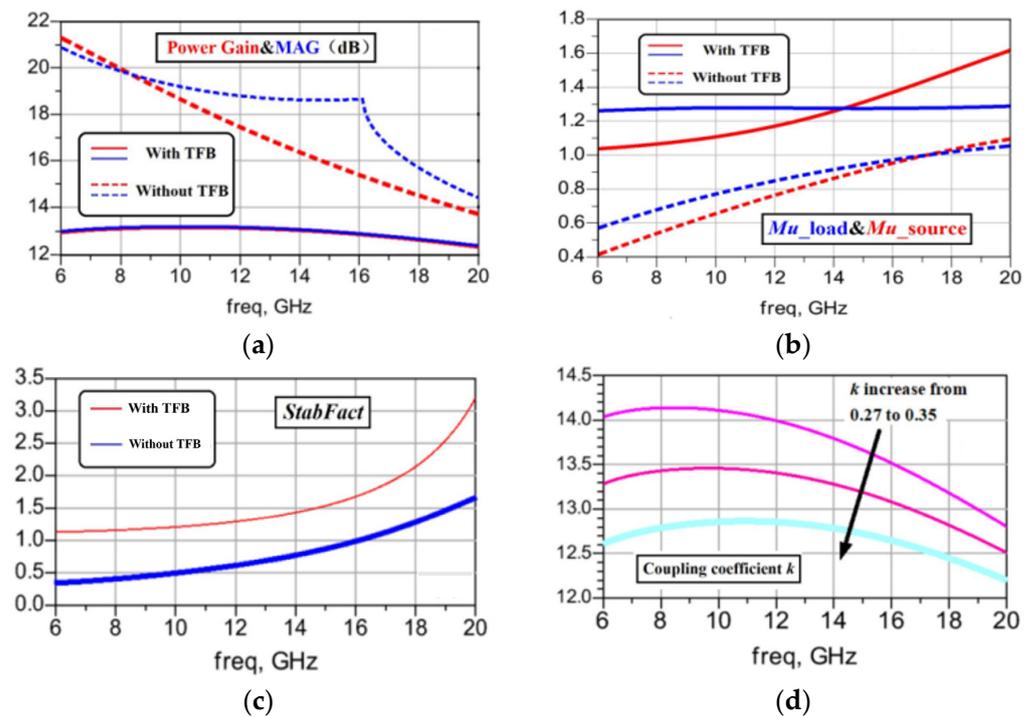


Figure 3. TFB effect to CS amplifier: (a) MAG/power gain; (b) stability factor μ ; (c) stability factor StabFact; (d) MAG vs. coupling coefficient.

In Figure 3b,c, stability factors such as μ and StabFact are shown to be below one. However, after the implementation of the TFB network, these stability factors of the amplifier improve to values above one. The coupling coefficient, represented by k , is utilized to adjust the depth of feedback. As depicted in Figure 3d, when k increases from 0.27 to 0.35, there is a steady reduction in the amplifier's maximum available gain (MAG) from 13.97 dB to 12.85 dB @12 GHz. Additionally, in the lower frequency band, the MAG curve exhibits a more rapid decline than in the high-frequency band, as shown in Figure 3a.

Furthermore, the use of on-chip transformer feedback aids in adjusting the amplifier's input impedance. If the amplifier's gate impedance is brought closer to the 50 Ω impedance range via the feedback network, it can decrease the impedance transformation ratio of the input matching circuit, thus simplifying the design of the input matching circuit. The feedback network's inductance $L1/L2$ and coupling coefficient k can be adjusted to modify the gain and input impedance of the on-chip transformer feedback amplifier. In this particular design, the on-chip transformer feedback network is primarily used to broaden the amplifier's bandwidth and offset the frequency-dependent roll-off characteristics of the transistor. As shown in the Smith chart in Figure 4, the blue line represents the S_{11} of the CG amplifier without the on-chip transformer feedback network, while the red line represents the S_{11} of the amplifier with the on-chip transformer feedback. It is clear that the addition of the on-chip transformer feedback network brings the amplifier's input impedance closer to the center point, Z_0 (50 Ω).

For a more in-depth analysis of the TFB mechanism in broadband PA design, we also examine a four-port transformer model in this paper. The traditional symmetric 2π transformer model [23] is complex, with numerous parameters that need to be fitted. For the sake of simplicity, we opt for a transmission line (TL) theory-based distributed transformer model for our analysis, as depicted in Figure 5.

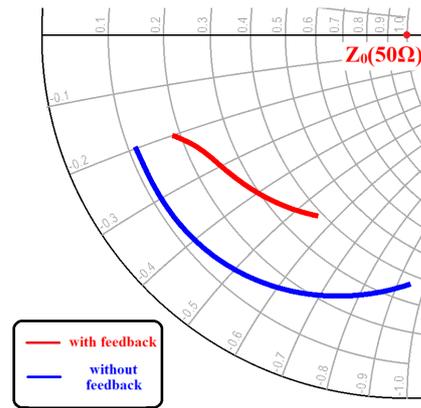


Figure 4. The CS amplifier input return loss S11 trace on the Smith chart.

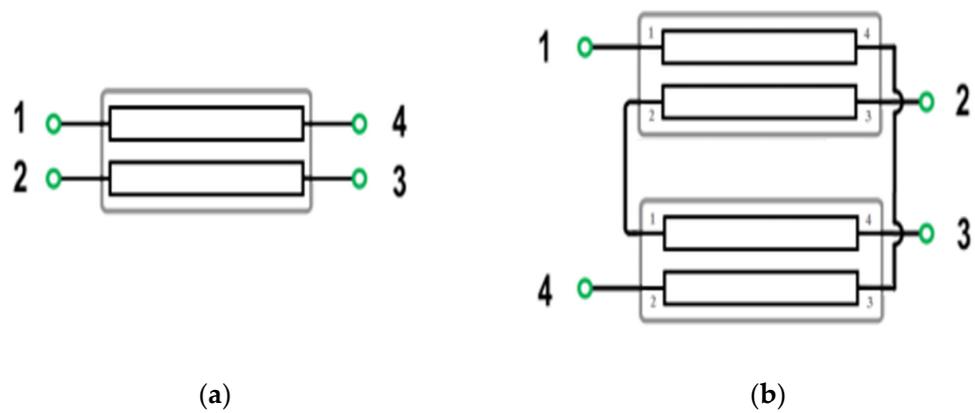


Figure 5. (a) The coupling TL section view; (b) the transformer distribute model based on coupling TL.

The inductance at the biasing circuit can be realized by TL. The coupling effect between the primary and secondary windings of the transformer can be modeled as the coupling TL [24–26], which captures both magnetic (inductive) and electric (capacitive) couplings between the two windings [27]. By employing this method, a four-port coupling TL Y-matrix can be expressed as follows [28]:

$$Y = \begin{bmatrix} -jY_p \cot \theta & -jY_m \cot \theta & jY_m \cot \theta & jY_p \cot \theta \\ -jY_m \cot \theta & -jY_p \cot \theta & jY_p \csc \theta & jY_m \csc \theta \\ jY_m \csc \theta & jY_p \csc \theta & -jY_p \cot \theta & -jY_m \cot \theta \\ jY_p \csc \theta & jY_m \csc \theta & -jY_m \cot \theta & -jY_p \cot \theta \end{bmatrix} \quad (1)$$

where

$$Y_p = \frac{Y_{0o} + Y_{0e}}{2} \quad (2)$$

$$Y_m = \frac{Y_{0o} - Y_{0e}}{2} \quad (3)$$

$$Y_{0e} = \frac{1}{Z_{0e}} \quad (4)$$

$$Y_{0o} = \frac{1}{Z_{0o}} \quad (5)$$

The coupling coefficient, denoted as k , can be expressed as follows:

$$k = \frac{Y_{0o} - Y_{0e}}{Y_{0o} + Y_{0e}} \quad (6)$$

Z_{0e}/Z_{0o} represent TL even/odd characteristic impedance, and θ denotes the electrical length of the transmission line. The transformer can be conceptualized as two pairs of coupled transmission lines (TLs), as depicted in Figure 5b, which makes it a four-port device. The elements of its Y-parameter matrix can be expressed as follows:

$$Y_{11}^* = Y_{44}^* = -Y_{11} + Y_{12} \cdot \frac{Y_{21}Y_{44} - Y_{41}Y_{24}}{2(Y_{22}Y_{44} - Y_{24}Y_{42})} + Y_{14} \cdot \frac{Y_{21}Y_{42} - Y_{41}Y_{22}}{2(Y_{24}Y_{42} - Y_{44}Y_{12})} \quad (7)$$

$$Y_{12}^* = Y_{21}^* = Y_{34}^* = Y_{43}^* = -Y_{13} + Y_{32} \cdot \frac{Y_{21}Y_{44} - Y_{41}Y_{24}}{2(Y_{22}Y_{44} - Y_{42}Y_{24})} + Y_{34} \cdot \frac{Y_{21}Y_{42} - Y_{41}Y_{22}}{2(Y_{24}Y_{42} - Y_{44}Y_{22})} \quad (8)$$

$$Y_{23}^* = Y_{32}^* = Y_{34} \cdot \frac{Y_{23}Y_{42} - Y_{43}Y_{22}}{2(Y_{22}Y_{44} - Y_{24}Y_{42})} + Y_{32} \cdot \frac{Y_{23}Y_{24} - Y_{43}Y_{24}}{2(Y_{22}Y_{44} - Y_{42}Y_{24})} \quad (9)$$

Figure 2b presents a simplified schematic of the transformer feedback (TFB) amplifier stage. If we assume that the transistor's admittance is a 2×2 Y-parameter matrix, we can add the shunt TFB network's Y-matrix to it. Consequently, the open-loop transformer and TFB loop can be expressed as follows [29]:

$$[Y]_{tot} = [Y]_{transistor} + [Y]_f = \begin{bmatrix} y_{11} + y_f & y_{12} - y_f \\ y_{21} - y_f & y_{22} + y_f \end{bmatrix} = \begin{bmatrix} y_{tf11} & y_{tf12} \\ y_{tf21} & y_{tf22} \end{bmatrix} \quad (10)$$

where the feedback admittance, y_f , corresponds to Y_{34}^* in the equation.

The stability factor, referred to as StabFact, and the small-signal gain, denoted as S21, of the transformer feedback (TFB) amplifier can be derived as follows [30]:

$$StabFact = \frac{2\text{Re}(y_{tf11})\text{Re}(y_{tf22}) - \text{Re}(y_{tf12}y_{tf21})}{|y_{tf12}y_{tf21}|} \quad (11)$$

$$S21 = \frac{-2Y_0y_{tf21}}{(Y_0 + y_{tf22}) - y_{tf12}y_{tf21}} \quad (12)$$

The transformer is designed using a 0.25 μm GaN process with a thick MET2 metal layer on top to achieve a higher Q factor and lower insertion loss. Figure 6a illustrates the transformer layout designed using the 0.25 μm GaN process, while Figure 6b presents a sectional view of the 0.25 μm GaN process. In the GaN process, two metal layers, MET1 and MET2, are available with thicknesses of 4 μm and 1.1 μm , respectively.

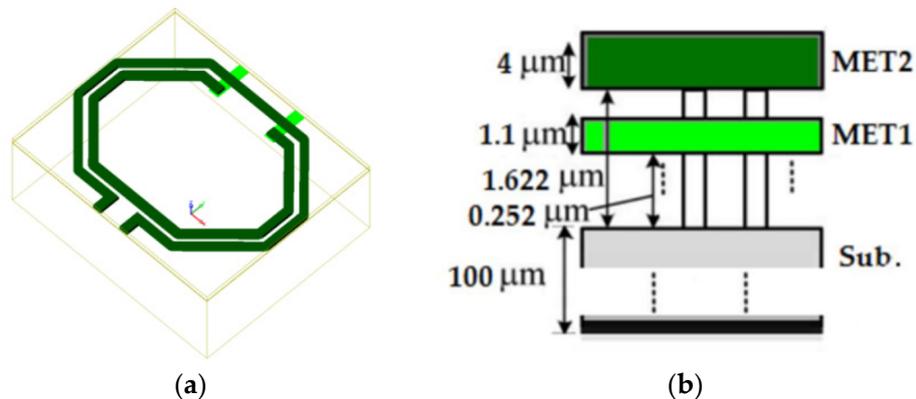


Figure 6. Transformer layout design: (a) the transformer design on 0.25 μm GaN process; (b) cross view of the 0.25 μm GaN process.

Due to the application of heteroepitaxial technology, the GaN metal layers are epitaxially grown on a 100 μm SiC substrate to improve the thermal characteristics of the device and reduce the junction temperature, as shown in Figure 6b. The transformer designed

with this process exhibits a high Q value, as depicted in Figure 7b. The transformer inductance Q value reaches approximately 25 @25 GHz and remains above 20 across the entire band. Figure 7a illustrates the windings of the transformer. The primary winding has an equivalent inductance of 0.414 nH, while the secondary winding has an equivalent inductance of 0.498 nH @10 GHz. The coupling coefficient between the windings is 0.531. Both windings exhibit a self-resonant frequency (fsrf) of 48.8 GHz.

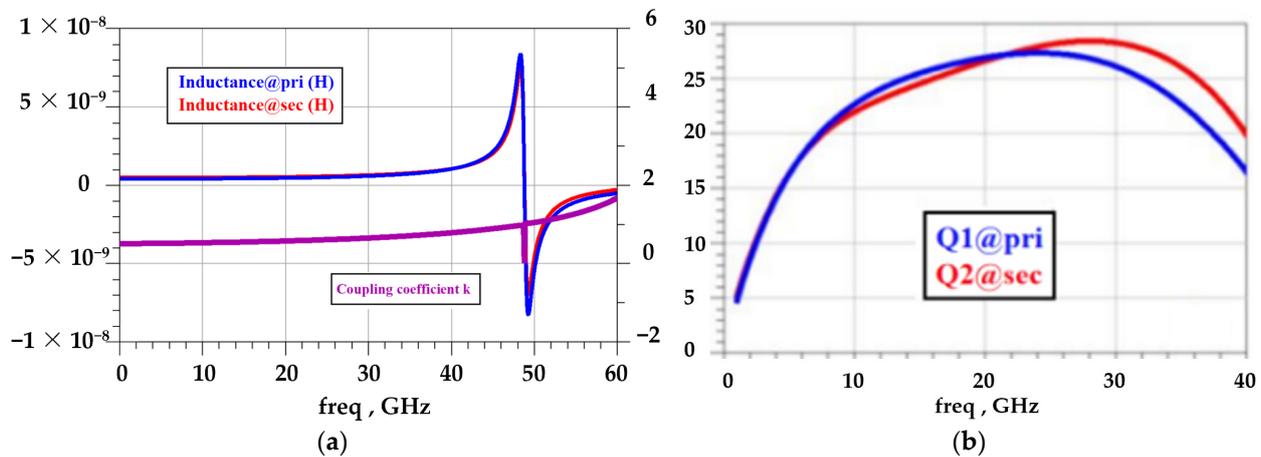


Figure 7. Transformer parameters extracted from EM simulation: (a) equivalent inductance at primary and secondary winding; (b) Q value of primary and secondary winding.

4. Circuit Design and Measurement

This section delves into the discussion of an ultra-wideband power amplifier leveraging the transformer feedback (TFB) technique. The circuit is designed and implemented using a 0.25 μm MMIC GaN process. The circuit schematic is depicted in Figure 8. Both stages of the amplifier structure are biased at $V_g = -2$ V, $V_d = 28$ V, class AB operation, with a quiescent current consumption of 130 mA. The sizes of the two-stage OSV HEMT transistors are $4 \times 70 \mu\text{m}$ and $4 \times 90 \mu\text{m}$, respectively. The driving stage is configured to provide ample power and gain, with the target of enhancing the output power. The feedback network is engineered to compensate for the transistor gain ripple effect and to extend the bandwidth from 6 to 19 GHz. It also serves to address the instability induced by the parasitic capacitance C_{gd} . Employing a feedback network tends to limit transistor gain and output power. To achieve a larger output power, the second-stage amplifier abstains from using a feedback network. All the matching circuits are designed using the port impedance model (PIM) matching the circuit design method [31]. Based on the variation trend of the optimum impedance (Z_{opt}) of the active device, the structure of the reactive matching circuit and the values of its components can be determined.

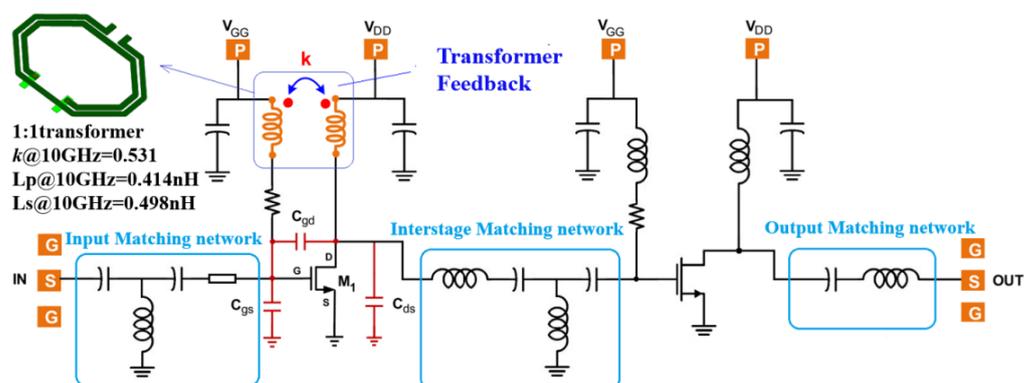


Figure 8. The schematic of proposed TFB power amplifier schematic design.

The designed GaN MMIC process on-chip transformer and all passive matching structures were designed and verified using EM simulation in the ADS 2020 Momentum platform. To ensure the accuracy of the design results, the EM simulation models of the chip PAD and bonding lines are included in this design. The stability factors StabFact, StabMeas, and Mu are shown in Figure 9. The simulation results show that StabFact > 1 is in the extended frequency range with a minimum value of 6.58 @ 9.3 GHz, and $\mu > 1$ and StabMeas > 0. Therefore, the power amplifier of this design is unconditionally stable.

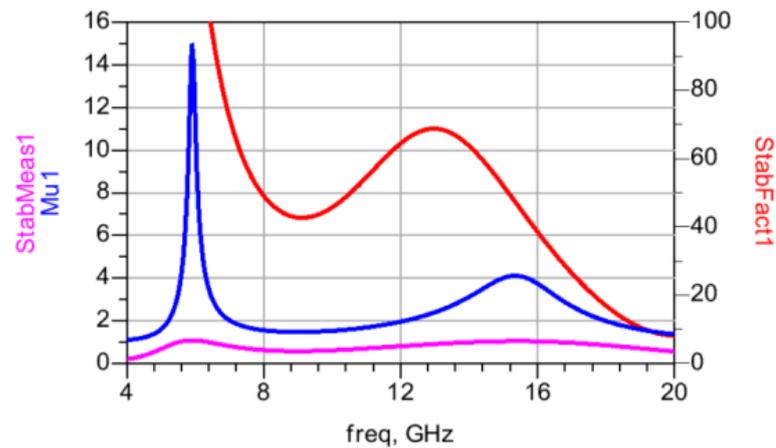


Figure 9. Stability factor StabFact, StabMeas, and Mu of the designed TFB PA.

Figure 10 shows the chip's microphotograph, which occupies an area of 1.570 mm². In Figure 11a, the measured small-signal gain (S₂₁) of the power amplifier (PA) ranges from 13.697 dB to 14.478 dB, exhibiting a flatness of 0.781 dB across a frequency range of 6 GHz to 19 GHz. This corresponds to a relative bandwidth of 104%. The small-signal gain reaches its maximum of 14.476 dB at 9 GHz, and the 1 dB bandwidth extends over a wide range of 13.9 GHz, spanning from 5.9 GHz to 19.8 GHz. The chip's input reflection coefficient S₁₁ is −8.617 dB at 6 GHz, and it improves to better than −10 dB in the frequency range from 7.6 GHz to 19.3 GHz.

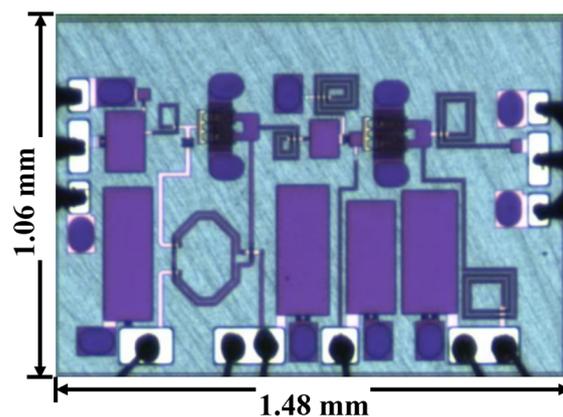


Figure 10. The fabricated chip microphotograph.

During large-signal measurements, the signal generator generates a pulse modulated signal with a 10% duty cycle and 100 μ s pulse. Figure 11b presents the large-signal performance measurement results. The power amplifier achieves a P_{out} ranging from 25.55 to 27.15 dBm, and a PAE ranging from 4.92% to 11.60%.

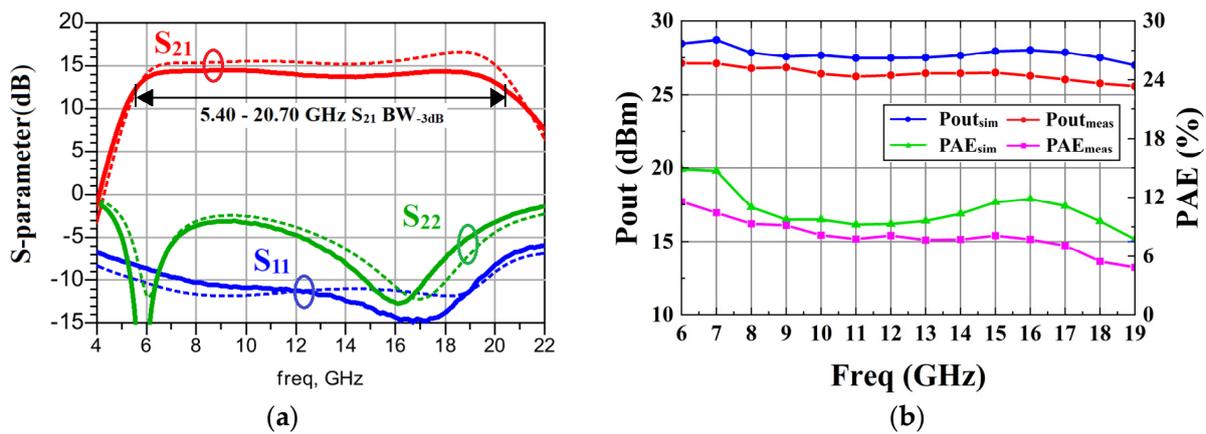


Figure 11. The measured and simulated results of TFB PA: (a) S-parameter; (b) large-signal performance.

To evaluate this PA with the TFB technique, a comparison with other ultra-wideband amplifiers is presented in Table 3. Compared to the feedback amplifiers in the CMOS and GaAs processes, the proposed power amplifier has better input return loss and higher output power. Compared to ultra-wideband GaN power amplifiers, it has a more compact area. What is particularly important is that a gain flatness of 0.78 dB is achieved using the TFB bandwidth enhancement technique, which is much higher than the values obtained.

Table 3. Comparison with ultra-wideband amplifier design.

Reference	[21]	[32]	[33]	[34]	This Work
Technology Process	65 nm CMOS	0.15 μm GaAs	0.2 μm GaN	0.25 μm GaN	0.25 μm GaN
Matching Topology	Transformer Feedback	RLC Feedback	Distributed	Non-Foster	Transformer Feedback
Frequency (GHz)	25–35	6–18	2–18	6–18	6–19
S ₂₁ (dB)	10	17.4	18	15	15
Gain Flatness (dB)	3	2	3	5.6	0.78
Input Return (dB)	−5	−8	−14	NA	−10
Psat (dBm)	14.75	19.2	29	35.7–37.5	25.55–27.15
PAEsat (%)	40–46.4	13–21.7	5–15	13–21	4.92–11.6
Chip Area (mm ²)	0.19	0.982	8	8.77	1.571

5. Conclusions

This paper analyzes the principle of on-chip transformer feedback and proposes a design for an ultra-wideband transformer feedback (TFB) power amplifier (PA) based on GaN 0.25 μm process technology. The C-Ku band broadband power amplifier achieves a relative bandwidth of 117%, a small signal gain of 15 dB, and a saturated output power of 27 dBm under a 28 V power supply condition. Furthermore, by employing the TFB technique, the small signal gain flatness is maintained at only 0.78 dB in the 6 to 19 GHz band, which is suitable for the design of ultra-wideband GaN power amplifiers. Compared with other designs, the on-chip transformer feedback broadband PA has a flatter small signal gain and a more compact topology structure.

Author Contributions: Conceptualization, J.L., J.W. and Y.F.; methodology, J.L., J.W. and Y.F.; Resources, J.L., J.W. and Y.F.; software, J.L., J.W. and Y.F.; validation, J.L., J.W., X.S. and Y.F.; data curation, J.L., J.W. and Y.F.; writing—original draft preparation, J.L.; writing—review and editing, J.L.; project administration, J.W. and X.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Bhagavatula, V.; Rudell, J.C. Analysis and design of a transformer-feedback-based wideband receiver. *IEEE Trans. Microw. Theory Tech.* **2013**, *61*, 1347–1358. [[CrossRef](#)]
2. Zhang, G.; Chang, S.; Chen, S.; Sun, J. Dual mode efficiency enhanced linear power amplifiers using a new balanced structure. In Proceedings of the 2009 IEEE Radio Frequency Integrated Circuits Symposium, Boston, MA, USA, 7–9 June 2009; pp. 245–248. [[CrossRef](#)]
3. Hookari, M.; Roshani, S.; Roshani, S. High-efficiency balanced power amplifier using miniaturized harmonics suppressed coupler. *Int. J. RF Microw. Comput. -Aided Eng.* **2020**, *30*, e22252. [[CrossRef](#)]
4. Ginzberg, N.; Cohen, E. A Wideband CMOS Power Amplifier with 52% Peak PAE Employing Resistive Shunt Feedback for Sub-6GHz 5G Applications. *IEEE Microw. Wirel. Technol. Lett.* **2022**, *33*, 192–195. [[CrossRef](#)]
5. Sapawi, R.; Sahari, S.K.; Kipli, K. A low power 3.1–10.6 GHz ultra-wideband CMOS power amplifier with resistive shunt feedback technique. In Proceedings of the 2013 International Conference on Advanced Computer Science Applications and Technologies, Kuching, Malaysia, 23–24 December 2013; pp. 172–175. [[CrossRef](#)]
6. Nikandish, G.; Medi, A. Transformer-feedback dual-band neutralization technique. *IEEE Trans. Circuits Syst. II Express Briefs* **2016**, *64*, 495–499. [[CrossRef](#)]
7. Luo, X.; Feng, W.; Zhu, H.; Wu, L.; Che, W.; Xue, Q. A 21–41 GHz Compact Wideband Low-Noise Amplifier Based on Transformer-Feedback Technique in 65-nm CMOS. In Proceedings of the 2020 IEEE Asia-Pacific Microwave Conference (APMC), Hong Kong, China, 8–11 December 2020; pp. 92–94. [[CrossRef](#)]
8. Yuan, Y.; Li, J.; Yuan, B.; Zeng, J.; Fan, J.; Yu, Z. Analysis and Design of a Gain-Enhanced 1–20 GHz LNA With Output-Stage Transformer Feedback. *IEEE Trans. Circuits Syst. II Express Briefs* **2023**, *70*, 3539–3543. [[CrossRef](#)]
9. Cassan, D.J.; Long, J.R. A 1-V transformer-feedback low-noise amplifier for 5-GHz wireless LAN in 0.18- μm CMOS. *IEEE J. Solid-State Circuits* **2003**, *38*, 427–435. [[CrossRef](#)]
10. Van Der Heijden, M.P.; de Vreede, L.C.N.; Burghartz, J.N. On the design of unilateral dual-loop feedback low-noise amplifiers with simultaneous noise, impedance, and IIP3 match. *IEEE J. Solid-State Circuits* **2004**, *39*, 1727–1736. [[CrossRef](#)]
11. Li, X.; Shekhar, S.; Allstot, D.J. Low-power $g/\text{sub m}/\text{-boosted}$ LNA and VCO circuits in 0.18/ $\text{spl mu}/\text{m}$ CMOS. In Proceedings of the ISSCC 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, San Francisco, CA, USA, 10 February 2005; pp. 534–615. [[CrossRef](#)]
12. Reiha, M.T.; Long, J.R. A 1.2 V Reactive-Feedback 3.1–10.6 GHz Low-Noise Amplifier in 0.13- μm CMOS. *IEEE J. Solid-State Circuits* **2007**, *42*, 1023–1033. [[CrossRef](#)]
13. Khanpour, M.; Tang, K.W.; Garcia, P.; Voinigescu, S.P. A wideband W-band receiver front-end in 65-nm CMOS. *IEEE J. Solid-State Circuits* **2008**, *43*, 1717–1730. [[CrossRef](#)]
14. Heiberg, A.C.; Brown, T.W.; Fiez, T.S.; Mayaram, K. A 250 mV, 352 μW GPS Receiver RF Front-End in 130 nm CMOS. *IEEE J. Solid-State Circuits* **2011**, *46*, 938–949. [[CrossRef](#)]
15. Roderick, J.; Krishnaswamy, H.; Newton, K.; Hashemi, H. Silicon-based ultra-wideband beam-forming. *IEEE J. Solid-State Circuits* **2006**, *41*, 1726–1739. [[CrossRef](#)]
16. Hashemi, H.; Chu, T.S.; Roderick, J. Integrated true-time-delay-based ultra-wideband array processing. *IEEE Commun. Mag.* **2008**, *46*, 162–172. [[CrossRef](#)]
17. Yeh, H.C.; Liao, Z.Y.; Wang, H. Analysis and design of millimeter-wave low-power CMOS LNA with transformer-multicascode topology. *IEEE Trans. Microw. Theory Tech.* **2011**, *59*, 3441–3454. [[CrossRef](#)]
18. Yeh, H.C.; Chiong, C.C.; Aloui, S.; Wang, H. Analysis and design of millimeter-wave low-voltage CMOS cascode LNA with magnetic coupled technique. *IEEE Trans. Microw. Theory Tech.* **2012**, *60*, 4066–4079. [[CrossRef](#)]
19. Chowdhury, D.; Reynaert, P.; Niknejad, A.M. A 60GHz 1V+ 12.3 dBm transformer-coupled wideband PA in 90 nm CMOS. In Proceedings of the 2008 IEEE International Solid-State Circuits Conference-Digest of Technical Papers, San Francisco, CA, USA, 3–7 February 2008; pp. 560–635. [[CrossRef](#)]
20. Ali, S.N.; Agarwal, P.; Renaud, L.; Molavi, R.; Mirabbasi, S.; Pande, P.P.; Heo, D. A 40% PAE frequency-reconfigurable CMOS power amplifier with tunable gate–drain neutralization for 28-GHz 5G radios. *IEEE Trans. Microw. Theory Tech.* **2018**, *66*, 2231–2245. [[CrossRef](#)]
21. Ali, S.N.; Agarwal, P.; Gopal, S.; Mirabbasi, S.; Heo, D. A 25–35 GHz neutralized continuous class-F CMOS power amplifier for 5G mobile communications achieving 26% modulation PAE at 1.5 Gb/s and 46.4% peak PAE. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2018**, *66*, 834–847. [[CrossRef](#)]
22. Nikandish, G.; Medi, A. Transformer-feedback interstage bandwidth enhancement for MMIC multistage amplifiers. *IEEE Trans. Microw. Theory Tech.* **2014**, *63*, 441–448. [[CrossRef](#)]
23. Cao, Y.; Groves, R.A.; Huang, X.; Zamdmer, N.; Plouchart, J.-O.; Wachnik, R.; King, T.-J.; Hu, C. Frequency-independent equivalent-circuit model for on-chip spiral inductors. *IEEE J. Solid-State Circuits* **2003**, *38*, 419–426. [[CrossRef](#)]

24. Chowdhury, D.; Reynaert, P.; Niknejad, A.M. Design consideration for 60 GHz transformer-coupled CMOS power amplifiers. *IEEE J. Solid-State Circuits* **2009**, *44*, 2733–2744. [[CrossRef](#)]
25. Niknejad, A.M.; Bohsali, M.; Adabi, E.; Heydari, B. Integrated circuit transmission-line transformer power combiner for millimetre-wave applications. *Electron. Lett.* **2007**, *43*, 1. [[CrossRef](#)]
26. Zhao, D.; Zhong, J. Design and modeling of millimeter-wave transformer in silicon: A tutorial. In Proceedings of the 2019 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), Nanjing, China, 28–30 August 2019; pp. 1–3. [[CrossRef](#)]
27. Wang, F. Design of Broadband Linear and Efficient Mm-Wave Power Amplifiers in Silicon for 5g Applications. Ph.D. Thesis, Georgia Institute of Technology, Atlanta, GA, USA, August 2020.
28. Wang, F.; Wang, H. A broadband linear ultra-compact mm-wave power amplifier with distributed-balun output network: Analysis and design. *IEEE J. Solid-State Circuits* **2021**, *56*, 2308–2323. [[CrossRef](#)]
29. Peng, L.; Chen, J.; Zhang, Z.; Huang, Y.; Wang, T.; Zhang, G. Design of broadband high-gain GaN MMIC power amplifier based on reactive/resistive matching and feedback technique. *IEICE Electron. Express* **2021**, *18*, 20210313. [[CrossRef](#)]
30. Hammad, H.F.; Freundorfer, A.P.; Antar, Y.M.M. Feedback for multiband stabilization of CS and CG MESFET transistors. *IEEE Microw. Wirel. Compon. Lett.* **2002**, *12*, 122–124. [[CrossRef](#)]
31. Lin, Q.; Wu, H.F.; Hua, Y.N.; Chen, Y.-J.; Hu, L.-L.; Liu, L.-S.; Chen, S.-J. A 2–20-GHz 10-W high-efficiency GaN power amplifier using reactive matching technique. *IEEE Trans. Microw. Theory Tech.* **2020**, *68*, 3148–3158. [[CrossRef](#)]
32. Lee, H.; Lee, W.; Kim, T.; Helaoui, M.; Ghannouchi, F.M.; Yang, Y. 6–18 GHz GaAs pHEMT broadband power amplifier based on dual-frequency selective impedance matching technique. *IEEE Access* **2019**, *7*, 66275–66280. [[CrossRef](#)]
33. Santhakumar, R.; Thibeault, B.; Higashiwaki, M.; Keller, S.; Chen, Z.; Mishra, U.K.; York, R.A. Two-stage high-gain high-power distributed amplifier using dual-gate GaN HEMTs. *IEEE Trans. Microw. Theory Tech.* **2011**, *59*, 2059–2063. [[CrossRef](#)]
34. Lee, S.; Park, H.; Kim, J.; Kwon, Y. A 6–18 GHz GaN pHEMT power amplifier using non-foster matching. In Proceedings of the 2015 IEEE MTT-S International Microwave Symposium, Phoenix, AZ, USA, 17–22 May 2015; pp. 1–4. [[CrossRef](#)]

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