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Review

Advances in Silicon Based Millimeter-Wave Monolithic Integrated Circuits

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Abstract: In this paper, the advances of the silicon-based millimeter-wave (MMW) monolithic integrated circuits (MMICs) are reported. The silicon-based technologies for MMW MMICs are briefly introduced. In addition, the current status of the MMW MMICs is surveyed and novel circuit topologies are summarized. Some representative MMW MMICs are illustrated as design examples in the categories of their functions in a MMW system. Finally, there is a conclusion and description of the future trend of the development of the MMW ICs.

Keywords: SiGe; CMOS; MMW IC

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1. Introduction

Millimeter-wave Integrated circuits (MMW ICs) are designed to deal with the frequency bands from 30 GHz to 300 GHz that correspond to a wave-length of 10 mm to 1 mm. Recently, applications for all aspects of modern life have been proposed, such as: home entertainment media, consumer electronics, astronomy observations, aerospace communications and cutting-edge research. This draws attention to MMW ICs. The earliest MMW ICs were demonstrated in 1978 [1] and 1981 [2]. Two

decades later, MMW ICs were utilized for the military purpose. Furthermore, in the 1990s, mobile and wireless communications were developed prosperously; many MMICs [3–12] were not only reported for military applications but also for civil applications. Most analog functions of a typical MMW communication system can be performed by monolithic integrated circuits like low noise amplifier (LNA), mixer, voltage-control oscillator (VCO), phase shifter, switch, power amplifier (PA) and so on. In addition, for some applications, which require medium power levels and large quantities of chips, MMW ICs are competitive, especially in large-scale production. Thus, III-V based MMICs such as GaAs and InP were popular at that time due to their superior performances. GaAs-based technologies have higher electron mobility than Si-based technologies and hence transistors can operate above 250 GHz. Also, GaAs transistors have wider bandgap, which leads to a relative insensitivity with respect to heat compared with Si transistors [13]. Most specifically, GaAs devices have relative lower noise than Si devices at high frequencies due to lower parasitics. However, the output power and noise performances of the GaAs-based transistors are still not good enough for some applications. This has resulted in the development of other high electron mobility transistors based on InP and GaN material systems. InP-based technologies have superior electron mobility than the more common semiconductors silicon and GaAs so that they can be utilized in high output power and high frequency MMICs [14]. InP-based technologies are popular in implementing optoelectronic devices such as laser diodes owing to their direct bandgap. Moreover, InP-based technologies are exploited for epitaxial indium gallium arsenide based optoelectronic devices. GaN-based technologies are developed for the applications of high voltage operation and high efficiency. With a reduction of the gate length, GaN-based devices can operate at higher frequencies in excess of W-band [15]. In automotive and electric car applications, GaN-based devices are more popular than other devices. Furthermore, nanotubes of GaN are introduced to realizing circuits for nanoscale electronics, optoelectronics and biochemical-sensing applications [16]. After the year 2000, silicon-based technologies gradually took over GaAs-based technologies in popularity for some III-V niche applications. Advances in silicon-based technologies have been aggressive and rapid. According to Moore's law [17], the period for a doubling in chip performance, that is, a combination of the effect of more transistors and their higher speed or operation frequency is 18 months. Thus, silicon-based technologies are promising and their performances can predictably catch up with those GaAs-based technologies in a short time. Also, silicon-based technologies have much better integration capability [13] than those in GaAs-based technologies. It is easier to integrate the baseband digital circuits into a single chip with MMW circuits in silicon-based technologies rather than that in GaAs-based technologies. Otherwise, an excessively large chip size is required. Note that the III-V based technologies still play an important role due to their superior performances in the field of mmw or sub-mmw circuits [18–21]. Even Si-based technologies could be successively improved in the future.

2. Silicon-Based Technologies

Regarding silicon-based technologies, it is easy to carry out the complete functions of a MMW transceiver due to their natural of high-level integration for putting baseband digital, analog and RF circuits together. Thus, the demonstration of the multi-functions in a MMIC becomes easier, for instance, adaptive bias for a PA, configurable input matching for optimum noise figure (NF) for a

LNA, and so on. Note that the specification of the output power of a transmitter should not be too high or the PA in the transmitter has to be designed in III-V based technologies.

Consequently, silicon-based technologies have attracted a lot of research interest. With the high-level integration capability of the Si-based technologies, system-on-chip (SoC) becomes a popular topic in these two decades. Among the circuit components in a MMW transceiver, radio frequency (RF) and baseband SoCs are of great importance [13,22]. For instances, some W-band image sensing systems [23–27] and V-band transceivers [28–30], which are designed for IEEE 802.15.3c, are implemented in silicon based technologies such as a 65-nm complementary metal oxide semiconductor (CMOS) or a silicon-germanium (SiGe) process.

From the technology point of view, silicon-based technologies include CMOS and BiCMOS technologies. Regarding CMOS technology, the parasitics contribute to inferior performances in implementing MMW or sub-MMW monolithic integrated circuits. However, it has some unique properties that the SiGe BiCMOS technology cannot take over nowadays. In general, the BJTs in SiGe BiCMOS technologies have better noise performance than that in the CMOS technologies [31]. Regarding the low noise characteristic of the SiGe technologies, the reduction of base resistance R_B can be attributed to the lateral scaling and hence, the power gain as well as trans-conductance can be intensified. Thus, the minimum noise figure (NF_{min}) will be improved in SiGe BiCMOS technologies. However, with the aggressive scaling down of the gate length in CMOS technologies, the NF_{min} of the MOS transistor in 65 nm, 40 nm or even 28 nm CMOS process has transcended the record maintained by the SiGe 0.13-μm BiCMOS technologies. Note that 90 nm SiGe BiCMOS technology has been proposed to implement a MMW switch [32]. It demonstrates a comparable performance with 0.15-μm III-V based technologies. Accordingly, the advanced CMOS technologies are perfect matched for the circuits, which are designed for the low-noise applications [27]. Although the devices in 40 nm or even 28 nm CMOS process have higher f_T and f_{max}, they are made for advanced digital circuits. Therefore, the top thick metal, which is for MMW circuits, is not essential in these technologies. On the other hand, the loss of the passives such as transmission line and inductors can be reduced by utilizing thick metal layer, which is provided by the foundry in advanced CMOS process like 65 nm process. 28 nm or 40 nm CMOS process usually do not provide top thick metal layer for the RF designers; hence, the 65 nm CMOS process is still popular for RF circuit designs.

Note that NF_{min} in CMOS technologies is more sensitive than that in the SiGe technologies due to its property of layout dependence [33]. In general, the multi-finger devices are utilized in CMOS technologies and thus result in large parasitic capacitances owing to the parallel combinations. In contrast, SiGe HBTs has low parasitics owing to their physical structure of the devices. In other words, CMOS devices are more sensitive to the parasitics than SiGe HBTs. The measured NF_{min} will not be the same unless the layout of each LNA is identical [14,34].

SiGe BiCMOS technologies have a unique advantage for high temperature operation due to the Ge grading and profile shape at the emitter base boundary [35]. For instance, the devices presented in [35] the f_T reduces by 29% from 125 GHz at 25 °C to 89 GHz at 200 °C, while the f_{MAX} decreased by 23% from 122 GHz to 94 GHz at the same temperature range. Likewise, the devices demonstrate high temperature characterization of SiGe and CMOS MMW circuits [36–38].

3. Current Status of the Circuit Component in the MMW Regime

The circuit topology in MMW IC design should be simple to avoid the parasitics or coupling effect at high frequency as long as it can meet the requirements of the MMW system. In this fashion, the simulation error might be minimized.

In the following paragraphs, the novel and typical circuit topologies will be introduced in the categories of various functions for a current MMW system.

3.1. Low Noise Amplifier (LNA)

The LNA needs to achieve the high gain, low noise and low dc power consumptions under the return loss of both input and output port is matched to 50 Ω (typically better than −10 dB). Among these specifications, NF is one of the most elemental parameters. Therefore, various techniques are proposed for not only the reduction of NF but also improvement of the gain performance. However, for some applications, the linearity and dc power consumptions are not so critical due to the less strictly system link budgets for the LNA.

For LNA implementation, common-source (CS) configuration with inductive source degeneration and transformer feedback technique is usually adopted [39–43] to satisfy low supply voltage requirements. When the operation frequency increases, CS configuration suffers from low power gain. Thus, multi-cascade stage is required. This results in a large chip size. To overcome this, in recent years, a cascode or a multi-cascode topology is adopted for MMW LNA design [44]. However, cascode or multi-cascode topology has some disadvantages. The common-gate (CG) transistors contribute considerable noise at the output port. Also, a high supply voltage is needed.

In order to reduce the noise contributed by CG transistors in cascode or multi-cascode topology, the series resonant inductors [44] or the parallel resonant inductors [45] are designed and placed between the CG devices. However, these solutions enlarge the chip areas. Therefore, the transformer is designed and placed between the multi-cascode devices to form the equivalent inductors [46]. This technique has the same concept as the inter-stage inductors technique used in [44]. It makes a compromise between the NF and the chip size. All reported techniques can reduce the NF, but they still require a high supply voltage in the multi-cascode topology. In order to reduce the NF and the supply voltage of the cascode or multi-cascode configuration simultaneously, a magnetic coupled technique is proposed in our previous work [47]. In this technique, the coupling effect of the transformer is used to couple the RF input signal between CG devices of the cascode or multi-cascode structures, which is different from [44] and [46].

In order to further solve the issues in a MMW LNA, the magnetic coupled technique [48] used in the cascode and the multi-cascode configurations are presented. The transformers minimize the effect of the parasitic capacitances of the cascode or the multi-cascode device in the desired band. Furthermore, the DC path of the cascode or multi-cascode configuration is separated using these transformers. Thus, the NF and the supply voltage of the cascode or multi-cascode configuration are simultaneously minimized. This topology alleviates the design constraints of the LNA and makes the multi-cascode configuration possible to be utilized in a MMW system. Based on the understanding of the topology evolution of a MMW LNA, the current status of the LNA will be introduced in the categories of CMOS and SiGe technologies.

3.1.1. LNA in CMOS Technology

Figure 1 illustrates the measured minimum NF of the recent published MMW LNAs in CMOS technologies. In [49], not only wideband performance but also moderate NF are achieved by using resistive-feedback network, which is composed of a series gate inductor and a parallel tuning capacitor, and inductive-series peaking technique. In [50], a magnetic coupled technique incorporated with the multi-cascode configuration is proposed. The transformers in the multi-cascode configuration resonate the parasitic capacitances of the transistors out. Moreover, a V-band magnetic coupled triple-cascode LNA is proposed in [50], Figure 2 illustrates the circuit topology of the MMW low voltage triple-cascode LNA with magnetic coupled technique and the chip photograph is illustrated in Figure 3. The V-band triple-cascode LNA has a gain of 13.7 dB at 54 GHz and a NF of 5.3 dB at 59.5 GHz, with a power consumption of 14.4 mW at 1.2 V supply voltage. Compared with the conventional cascode LNAs, the use of the magnetic coupled technique in a multi-cascode LNA improves significantly the gain performance with a slight degradation of the NF.

Figure 1. Measured minimum noise figure of the recent published millimeter-wave (MMW) complementary metal oxide semiconductor (CMOS) low noise amplifiers (LNAs). Data taken from [24,46,49–57].

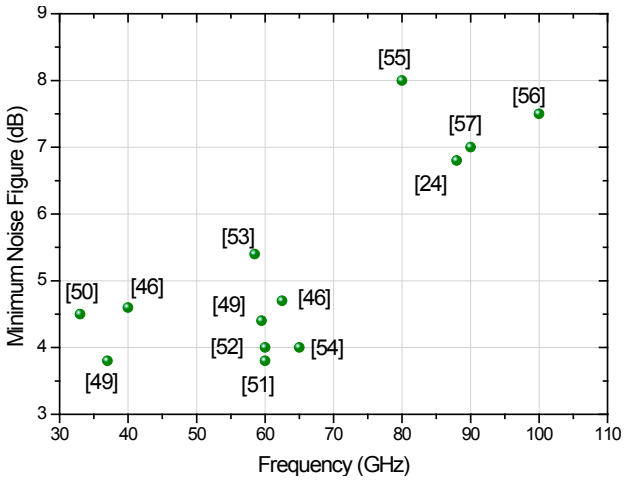


Figure 2. Circuit schematic of the V-band magnetic coupled triple-cascode LNA [50].

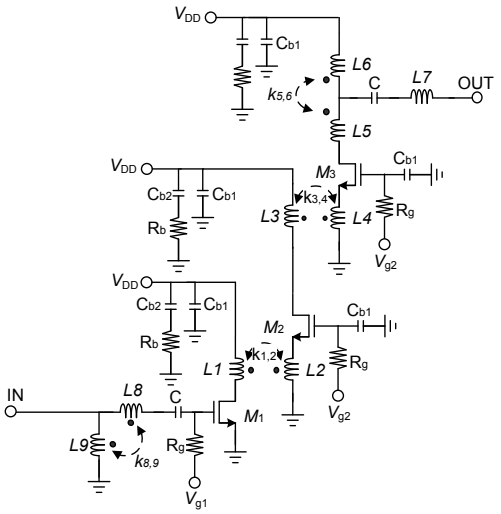
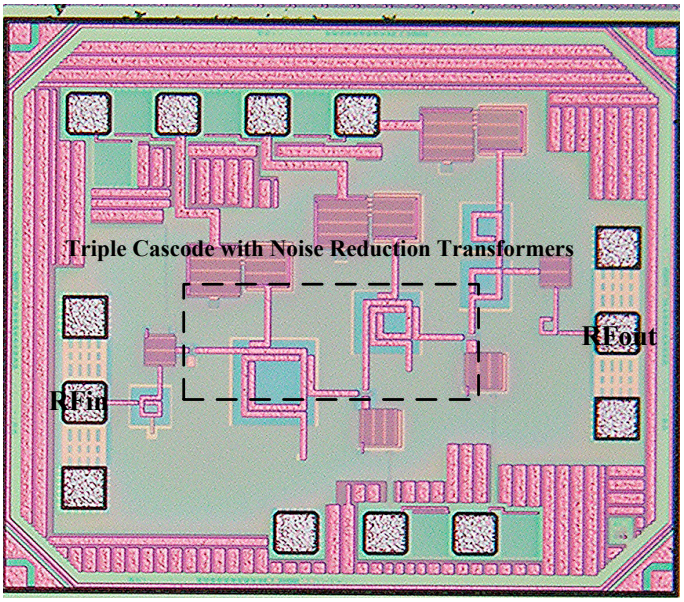


Figure 3. Chip photograph of the V-band magnetic coupled triple-cascode LNA with a size of 0.6 × 0.48 mm^2 including all testing pads [50].

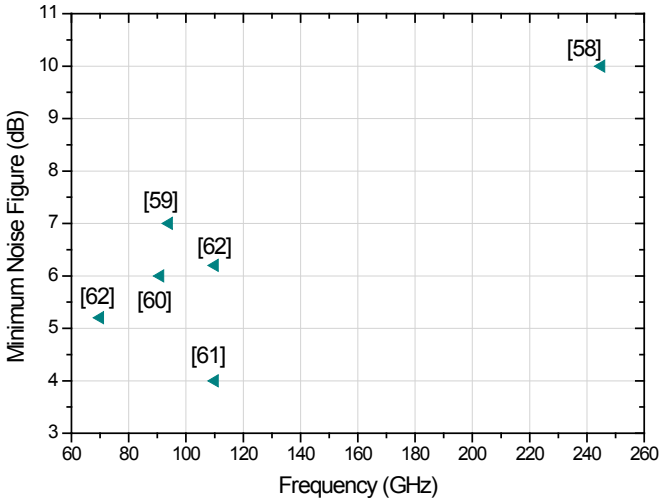


In [46], the transformer multi-cascode topology is proposed to maximize the gain-bandwidth products, minimize the area and noise figure of the amplifier. These transformers in the multi-cascode configuration eliminate the effect of the parasitic capacitances of the transistors in the desired band, and thus the NF can be improved. In [51], the NF is reduced by the proposed voltage-voltage transformer feedback technique within the operation bandwidth of 6 GHz owing to the neutralization of the Miller capacitance. In [52], a novel gain-boosting technique is proposed. A 180° transformer is adopted to form the capacitive feedback path. In this manor, a high gain and low power LNA is designed and implemented with more degree of freedom compared with the conventional designs. In [53], the transformer between the gate and the source of the first stage results in simultaneous input impedance and noise matching. For further reduction of the path losses between the input and the output of the LNA, the drain-source transformers replace the matching networks, which are consisted of thin film transmission line or lump components. In [56,57], the slow-wave CPW transmission line is utilized to reduce the loss of the thin-film transmission line in this frequency range; this leads to a low noise figure performances of the amplifier. In [24], the parasitic capacitances in the cascode configuration are resonated out for further reducing the noise figure of the five stages amplifier.

3.1.2. LNA in SiGe Technology

Figure 4 illustrates the measured minimum noise figure of the published MMW LNAs in SiGe technologies. In [58], the transformers are adopted in the amplifier to alleviate the loss of the passive components in the matching networks at 245 GHz. Therefore, the noise figure can be reduced. In [59], the improvement of the gain and NF are achieved by using the Q-enhanced cascode mechanism with a filter synthesis passband-forming technique. Also, the measured minimum noise figure of the amplifier is 6 dB at 92 GHz. In [60], with the source degeneration inductors and careful modeling of the passive components, the amplifier has a measured minimum NF of 4 dB at 110 GHz. In [61], a T-type matching topology is utilized to achieve the wide bandwidth and minimum noise figure performances.

Figure 4. Measured minimum noise figure of the recent published MMW SiGe LNAs. Data taken from [58–62].



3.2. Power Amplifier (PA)

In these two decades, the published works about MMW PAs are mainly about enhancement of output power and gain with power combining, reduction of passive components and neutralization of the parasitic capacitances with inductive components like transmission line, and the improvement of efficiency by linearization techniques [63–72].

The power handling capability decreases with the downscaling of the advanced CMOS technologies owing to the reduction in breakdown voltage of the CMOS transistors. This leads to the significant decrement in output power. In order to achieve higher output power, the transistors can be combined by direct shunt combining 3-dB couplers and transformers [73–81]. Direct shunt combining is the simplest combining architecture to combine the current of each PA cell, in turn; the output power is enlarged. However, it is more difficult to match the output with a number of combined transistors owing to lower impedance. The lower output impedance at the output of PA, the more difficult to match with the system impedance (50 Ω). A solution for this issue is to design the pre-matching network behind the combined transistors but the area is huge while the combining number is high. At MMW frequencies, binary combining is popular because the phase of each transistor should be equal to maximum the output power.

An effective mechanism to double the output power is to exploit 3-dB coupler with the same PA units and 3-dB couplers. In-phase 3-dB couplers (e.g., Wilkinson coupler) and 90° 3-dB couplers (e.g., Lange coupler, branch-line couplers, and a pair of 3-dB coupled-lines with 90° electrical length) are successfully adopted in PA combining to gain high output power even with multilevel 3-dB couplers. Wilkinson coupler [82], which can divide input power equally in-phase into the input ports of two amplifiers and combine the output power at the two output ports. It is one simplest structure, which is composed of two quarter-wavelength lines and one isolation resistor, in turn, results in a good phase and amplitude balance at input and outputs. A common way to form a quadrature coupler is to use two adjacent quarter-wavelength transmission lines. For example, in CMOS technology, broadside coupled transmission lines are usually adopted owing to the multilevel dielectric and metal layer environment above the lossy silicon substrate. Thus, broadside-coupled quadrature couplers can be implemented using two metal layers with the thin dielectric between them. Broadband 3-dB coupler is achieved by

adjusting the overlap area of the coupled lines. A balanced amplifier [83] takes advantage of the quadrature couplers to achieve good input and output return losses. The aforementioned combing techniques have some limitations. The chip size is at least doubled because the identical PA units are used. In addition, the losses of the couplers become severe when multi-stage PA units are utilized. Since the quarter-wavelength lines are exploited, the 3-dB couplers usually have large size.

Currently, transformers are popular in MMW PA design [64,72,81,84] since dc voltage can be fed to the transistors via this transformer, bypass capacitors or RF chokes can be eliminated as well as RF grounding can be achieved with the virtual ground. By using transformer combing, a large number of on-chip components are eliminated. Consequently, the PA can be realized with a compact size; the higher output power can be achieved. One issues for transformer combining is that the optimum load impedance for high output power will be very low when a lot of transistors are combined. Another is the higher insertion loss due to the multi-mental layers, especially in CMOS technologies. The top metal layer is thicker and hence the lower loss it has compared with the other metal layers in CMOS technologies. This is an important issue in MMW PA design. The effect of combing transistors to gain higher output power may not be significant for the high combing loss from transformers.

According to aforementioned combing techniques, the difficulties in gaining higher output power is to reduce the loss of the passive components by combining multi-metal layers or investigating different ground shield patterns, which are utilized to isolate the lossy substrates and the passive components.

In addition, with the demanding of the complex digital modulation schemes like quadrature phase-shift keying (QPSK), n-quadrature amplitude modulation (n-QAM), and orthogonal frequency-division multiplexing (OFDM), linearity of the PA becomes more important than last two decades. For improving the linearity, a bias mechanism is proposed an implemented to a cascode configuration. This contributes to the improvement of the power added efficiency (PAE) at output 1 dB compression point (P_{1dB}) [85]. Except for the method in [85], a V-band PA adopts with the proposed pre-distortion linearizer using body bias technique is successfully implemented with improved P_{1dB}, PAE at P_{1dB} and the third order intermodulation distortion (IMD_3) [86].

Regarding different specifications of the target systems, the correspondent circuit topologies can be utilized to implement the PAs. Meanwhile, this shows the possibility of the integration of the PAs with the MMW front-end system in silicon-based technologies.

3.2.1. PA in CMOS Technology

Figure 5 illustrates the saturation power performance of the published MMW CMOS PAs. In [87], a 2-D distributed power-combining network with right/left-handed transmission line is proposed to offer distributed amplification and power combining for low loss and wideband performances of the PA. In [88], a Q-band stack PA is reported. The more transistors stack, the more supply voltage and output power allow. However, the high supply voltage is still an issue for this topology. In [89], a parallel power combiner based on a transmission-line transformer is proposed. Also, a cascode power cell structure with the inter-stage matching inductor is exploited to gain high output power and efficiency. In [90], a 45 GHz Doherty PA was reported. A cascode amplifier and slow-wave coplanar waveguides are exploited to improve the performances. The efficiency is boosted 8% compared with the conventional Doherty PA. In [91], the high output power is achieved by 32 ways combining differential PA. Wilkinson

combiners, and a multi-port argyle transformer are deployed to minimize the path loss for high output power. In [92], a lumped-element λ/4 combiner is proposed. The inductor can realize higher Z_0 and lower loss with respect to the thin high-Z0 transmission lines owing to their self-magnetic coupling. Note that the combiner poses a 50 Ω load to each PA. In [93], the novel devices layout is presented to minimize the parasitics of the transistors. By utilizing the transistors in the proposed transformer-based power combining MMW PA, which operates in Class AB, the efficiency is boosted. Moreover, one of the amplifier cell in this PA will be turned off while operating in low power mode. In this fashion, the efficiency and the loss of the combiner will be further reduced. In [94], the stability, broadband width are achieved by using cascode drain-source neutralization while implementing the CMOS 28 nm 60 GHz PA. Except for the recent published works, a representative MMW PA will be illustrated.

A three-stage, six-way combining CS W-band PA is presented with 14.8-dBm P_{sat} with 65-nm CMOS technology [73]. The peak gain is 12 dB and the 3-dB bandwidth is from 79 to 106 GHz with a chip size of 0.28 mm^2. Likewise, an eight-way combing matching networks is proposed to achieve the impedance transformation [74]. With the proposed method, a CS D-band 65-nm CMOS PA is implemented with 13.2-dBm P_{sat} at 140 GHz. Figure 6 shows the chip photo, and the chip size is 0.38 mm^2.

Figure 5. Saturation power of the recent published MMW CMOS PAs. Data taken from [87–95].

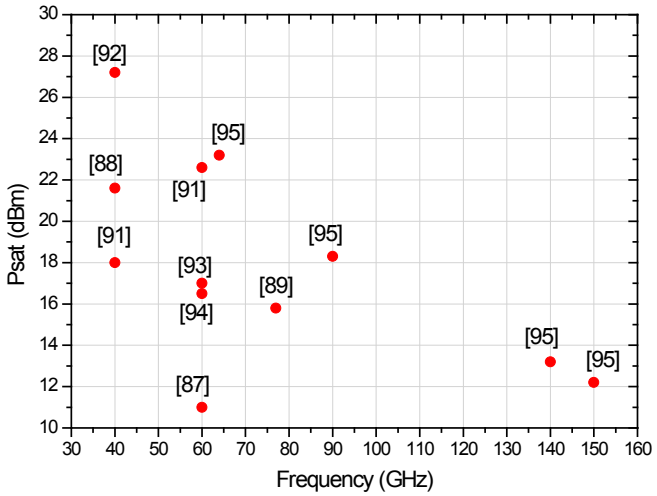
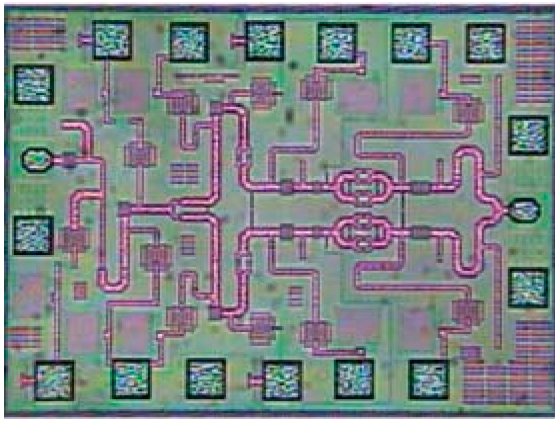


Figure 6. Chip photo of the D-band eight-way combining common-source power amplifier (CS PA) [74].

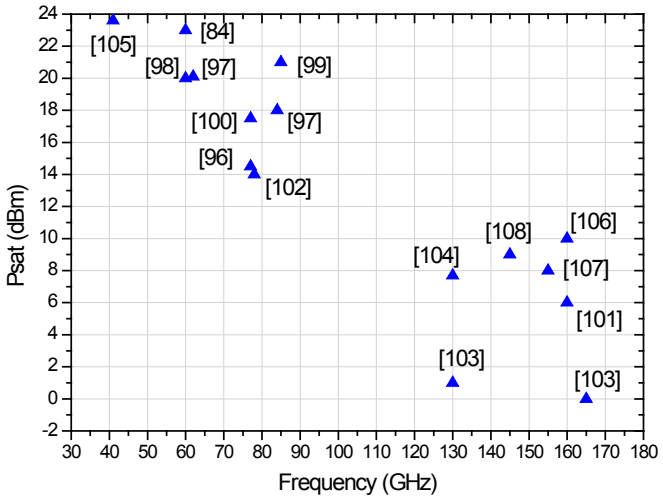


3.2.2. PA in SiGe Technology

Figure 7 illustrates the saturation power performance of the published MMW SiGe PAs. In [96], the efficiency and gain of the PA are enhanced by using the transformer-coupling current-reuse technique. Also, this inter-stacked transformer improves the output loss owing to the differential-to-single-ended conversion. In [97], the collector-emitter breakdown beyond BV_{CEO} is achieved with the differential common-base pairs and stability and reverse isolation are improved by the cross-coupled, collector-emitter neutralization. Furthermore, the novel transformer power combiner improves the uniformity of the load impedance while transforming to each primary port. Thus, the undesired coupling will be minimized. In [98], the adaptive bias control V-band PA is reported. The main insight is that a fully-integrated on-chip RMS power detector for automatic level control (ALC), build-in self-test and voltage standing wave ratio (VSWR) protection incorporate with the PA to improve the performances. In [84], the distributed active transformer, which is realized with tacked coupled wires as opposed to slab inductors, performs a high coupling coefficient of 0.8 at 60 GHz. The possibility of efficient power combining and impedance transformation for the operation in MMW frequencies is exemplified. In [99], a novel two-dimensional passive propagation media is proposed for power combining and impedance transformation. By exploiting this media, the W-band PA delivers 125 mW at 85 GHz in the SiGe technology. In [100], improvement of the isolation between adjacent lines and better integration of the PA is achieved by utilizing the conductor-backed coplanar waveguide transmission line. As a result, this PA has a compact area and high output power due to the reduction in path losses with this transmission line structure. In [101], the differential cascode topology incorporates with the center-tapped microstrip lines are proposed. The path losses can be reduced by using center-tapped microstrip lines, especially for long quarter-wave RF chokes. In [102], the novel combiner is proposed to enhance the power transformation efficiency (reduce the loss) and eliminate the necessaries of the additional baluns in differential circuits because it behaves like a balanced-to-unbalanced converter. In [103], the 140 GHz and 170 GHz PA are reported. Both of the PAs are measured over 125 °C. The 140 GHz PA has a measured output power of +1 dBm with a gain of 17 dB whereas the 170 GHz PA has a measured output power of 0 dBm with a gain of 15 dB.

In [104], the proposed PA utilizes the transformers for power combining and inter-stage matching networks. The bias condition of the proposed cascode HBT configuration is optimized fot highest output power and gain performance. In [105], the proposed Q-band high power-added efficiency stack PAs exhibit the high power-added efficiency operation over the collector-emitter breakdown voltage. The active devices are designed to turn ON and OFF at the same time to make sure the voltage swing across the transistors add up in phase resulting in larger overall output voltage swing and power of the PA. In [106], a state-of-the art PA, which operates beyond 120 GHz, is reported. The highest power performance is achieved by optimizing the design in device sizing, EM modeling and layout techniques. In [107], the D-band amplifier has a measured saturation output power of 8 dBm at 155 GHz. In [108], another state-of-the-art PA is presented by adopting the staggered tuning mechanism. In this manor, the peak gain of the individual or group of individual stages can tuned at offset frequencies, in turn; combining these individual or group stages could perform a broadband operation. This PA has largest operation bandwidth among all silicon D-band PAs.

Figure 7. Saturation power of the recent published MMW SiGe PAs. Data taken from [96–108].



3.3. Mixer

Mixer in MMW systems is utilized to offer frequency translation from the input signal to the output signal. It can be used to up-convert the baseband signals to the carrier frequencies, in turn; the signals transmit via antenna [109]. In this case, the input is IF and the output is RF; for down-conversion the opposite is true. In most cases, conversion gain (CG), pumping LO power at optimum CG and port-to-port isolations are more crucial than others such as linearity [110–112], image rejection [112–116] and power consumptions [116–120] among all the specifications of a mixer. The reported works of mixer can be roughly categorized according to its features like wideband, miniature, and so on.

Operation bandwidth and CG are important specifications of the mixer for a modern multi-band receiver. Thus, the one of the mixer features wideband performance with flat CG. In this kind of the mixer, the turn-on resistance and the parasitic capacitance of the transistor, which is related to the device size, limit of the bandwidth of a mixer [121]. Consequently, the device sizes have to be selected as careful as possible for the consideration of bandwidth, power consumptions, conversion gain and port-to-port isolations.

Another primary limitation of the bandwidth of a mixer is the passive comments [122–124] in the input or output port of a mixer especially for the case of an active mixer utilizing with the Gilbert-cell [125–127] in CMOS technologies. Therefore, the passive components should be designed as broadband as possible for achieving wideband performance.

Besides the various core circuit configurations of the mixer such as Gilbert cell, anti-parallel diode, single FET, distributed type, and so on; the passive components like balun, power divider, matching networks, filters that might have more impact than that of on the performances of a mixer [128]. For example, low conversion gain (CG) can be attributed to one possibility of lossy passive components. Nevertheless, the narrow band frequency response of the low loss passive components gives rise to the narrow band performances of a mixer under the design requirement of keeping the CG as high as possible. As a result, minimizing the passive components in a mixer design and remaining the wide band performances as possible should be achieved, simultaneously, in an excellent design.

In addition, the main idea of miniaturization is producing equivalent electrical length with more compact components in silicon-based technologies [129]. For instance, in silicon-based technologies,

there are multi-metal layers for routing or other applications. With this benefit, the equivalent electrical length can be created by either stacking the baluns, power dividers, inductors, and so on [110]; or enhancing the coupling coefficients, that means smaller inductances, shorter electrical length or novel winding methods than the original design without this technique [111], between the transformers, inductors even transmission lines.

Another concept for minimizing the area of the passive components is generating the accurate model for them [110]. In this fashion, the critical design parameters can be observed from the derivation of their frequency responses (S-parameters), in turn, the area of the passive components could be minimized. Namely, some design parameters of the passive components are not so sensitive to their frequency responses like amplitude/phase imbalance, which result in low CG, isolations in some designs that can be minimized for reducing the area.

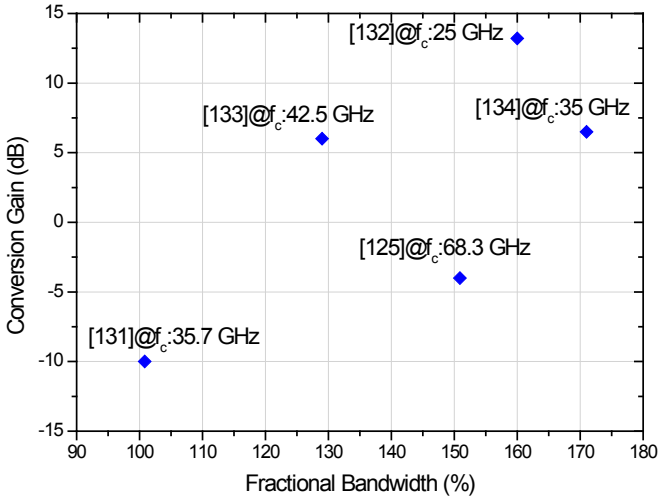
Also, isolation between LO port and RF port is critical because their frequencies are close, in turn, will interfere with each other, especially for a down-conversion mixer design. Thus, in general, the filter, which performs a short circuit to LO frequency is inserted at the RF port whereas the other filter, which performs a short circuit to RF frequency is put at the LO port. Also, the IF band-pass filter is deigned at the IF port. After finishing these filters, the mixer achieves good performances in LO to RF isolations [130]. The same concept can be applied to a sub-harmonic mixer design to achieved good 2LO to RF isolations [130].

One method to improve the isolation between LO port and RF port is illustrated in [130]. In [130], drain-body feedback technique is applied to the sub-harmonic mixer design to reduce the 2LO-to-RF leakage. For up-conversion, sub-harmonic gate resistive mixer leads to more leakage of the 2LO signal due to a stronger IF input. When IF signal is strong, the charges will accumulate in drain parasitic capacitor, and result in the drain voltage variation. The 2LO unwanted signal in drain increases. To resolve this problem, we connect the body to drain to build a discharging path, and the variation of drain voltage will be moderate and the 2LO-to-RF leakage will be reduced [130].

3.3.1. Mixer in CMOS Technology

Figure 8 illustrates the conversion gain *versus* fractional bandwidth of the published MMW CMOS mixers. In [125], for a broadband performance, a compact asymmetrical broadside-coupled balun is proposed. Also, a moderate conversion gain and low power consumption can be achieved by using the forward body biased technique. In this case, the threshold voltage and the supply voltage can be reduced for a transistor, which operates in weak inversion region. In [131], the wide-band performance of the mixer is achieved by utilizing the miniature symmetric offset stack Marchand single and dual baluns; meanwhile, the measured conversion loss is 12 dB. In [132], the distributed topology incorporates with a cascode complementary switching pair are utilized for broadband and high conversion gain performances. In [133], the broadband performance is attributed to the g_m of the switching core itself. The input impedance of the switching core is $1/g_m$ and is not heavily dependent on the operation frequency. Thus, a broadband performance is achieved. In [134], a Darlington cell and a wideband Lange coupler, which is composed of the microstrip-line, constitute the mixer. The proposed mixer has a measured CG of 6 dB with a power consumption of 4.2 mW. Note that the maximum CG is 6.5 dB at 36 GHz.

Figure 8. Common-gate (CG) *versus* fractional bandwidth of the recent published MMW CMOS mixers. Data taken from [125,131–134].



Except for the recent published works, some representative MMW mixers are illustrated later.

A 5 to 45 GHz wideband distributed mixer is designed and implemented with a standard 180 nm CMOS process [132]. Also, the port-to-port isolation is improved by taking the advantage of a cascoded complementary switching pair as illustrated in Figure 9. The distributed mixer is composed of the four-stage distributed topology to carry out a wide bandwidth and minimize its conversion loss. The distributed mixer has a 40 GHz operation bandwidth that is from 5 to 45 GHz with the conversion loss of 11 to 13.2 dB. All port-to-port isolations are better than 30 dB at a LO power level of 8 dBm with a 1.4 mW dc power consumptions. Note that the chip size is 0.92 mm × 0.72 mm as shown in Figure 10.

Compact balanced mixers that consist of three miniature asymmetric broadside Marchand baluns are designed, implemented and reported in order to demonstrate the utility of the CMOS technology [135]. There are two baluns, which are analyzed in [135], both have compact chip size of 0.06 mm^2. Besides, the compact asymmetric broadside balun with low-loss broadband characteristics are suitable for the mixer designs. These baluns take advantage of the two asymmetric multilayer meander coupled lines; as a result, the size can be minimized. Moreover, from 10 to 60 GHz, the balun has an insertion loss better than 4.1 dB around 35 GHz with an amplitude imbalance less than 1 dB and a phase imbalance less than 5°. Furthermore, there are three circuits in [135] for the demonstration of the design concept with the proposed miniature technique. The first circuit is a mixer, which is designed to operate in Ku-band. It incorporates with a miniaturized balun. The size of the miniaturized balun can be reduced about 80% compared with the conventional balun. This Ku band mixer has a conversion loss better than 6.8 dB with a chip size of 0.24 mm^2.

The second circuit is a 15–60 GHz broadband single-balanced mixer, which has a conversion loss better than 15 dB with a chip area of 0.24 mm^2 as well. Finally, a three-conductor miniaturized dual balun is designed and adapted in the third mixer. This star mixer (the third mixer) incorporates with two miniature dual baluns to achieve a conversion loss of better than 15 dB from 27 to 54 GHz with a chip area of 0.34 mm^2. From the above design examples, the key concept of the miniaturization is verified for MMW mixer design.

Figure 9. Schematic of the distributed mixer with cascoded complementary switching pairs [132].

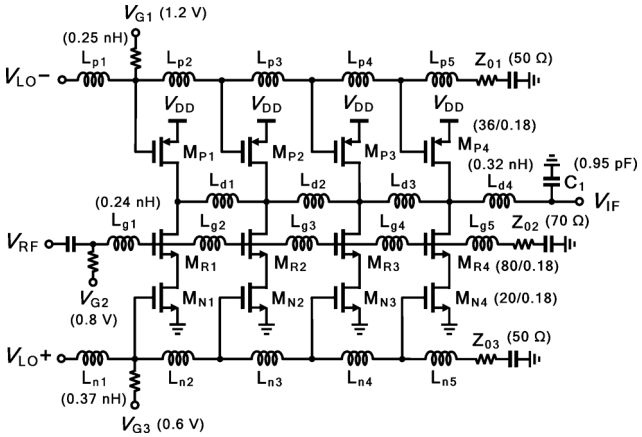
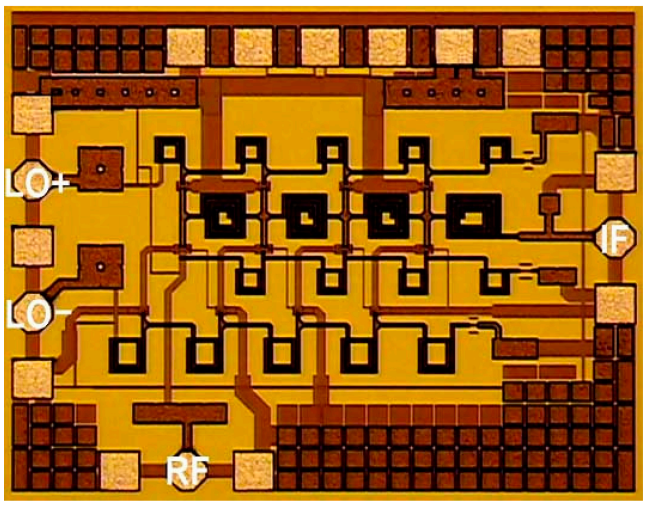


Figure 10. Chip photograph of the distributed mixer with area 0.92 mm × 0.72 mm [132].



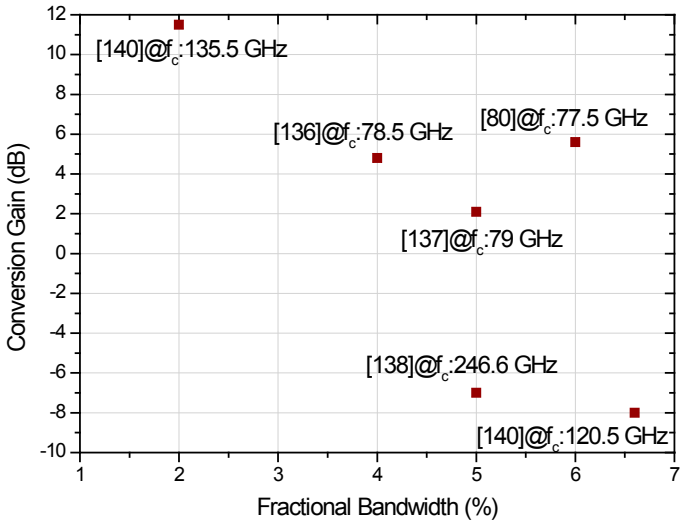
A 56 to 66 GHz high isolation sub-harmonic resistive mixer using 0.13 μm CMOS technology is presented in [130] This mixer exhibits a flat conversion loss of about −12 and −13 dB and good isolations between ports from 56 to 66 GHz for both down and up-conversion with a lowest LO power of 0 and −1 dBm. The 2LO-RF isolation is more than 27 dB even if IF input power exceeds 4 dBm, which results from the mechanism of connecting drain and body of the device. Besides, this mixer has a relatively high input P_{1dB}. Therefore, this mixer can be used in the system, such as the system, which is compatible with IEEE 802.15.3c standard.

3.3.2. Mixer in SiGe Technology

Figure 11 illustrates the conversion gain *versus* fractional bandwidth of the published MMW SiGe mixes. In [80], with careful design of the degeneration resistors of the transconductance stage in the Gilbert cell topology, the linearity and the conversion gain can be improved. In [136], according to the multi-tanh triplet principal, the linearity of the transcoductance stage in the Gilbert cell mixer is able to be mended as well. In [137], the dc power consumption is reduced by the current injection technique and the conversion gain is enhanced by the dual negative resistance compensation technique. In [138], the 245 GHz subharmonic balanced mixer has a measured conversion loss of −7 dB with a fractional

bandwidth of 5% in 130 nm SiGe technology. In [139], two cross-couple pairs with four base-emitter external capacitances are combined by the dual balun. The voltage across the base and emitter junction will increase owing to the four base-emitter external capacitances, and thus; the conversion gain is boosted. In [140], the common mode noise can be reduced owing to the natural of the anti-parallel diode subharmonic mixer. Moreover, it has a measured conversion gain of 8 dB with a fractional bandwidth of 6.6%.

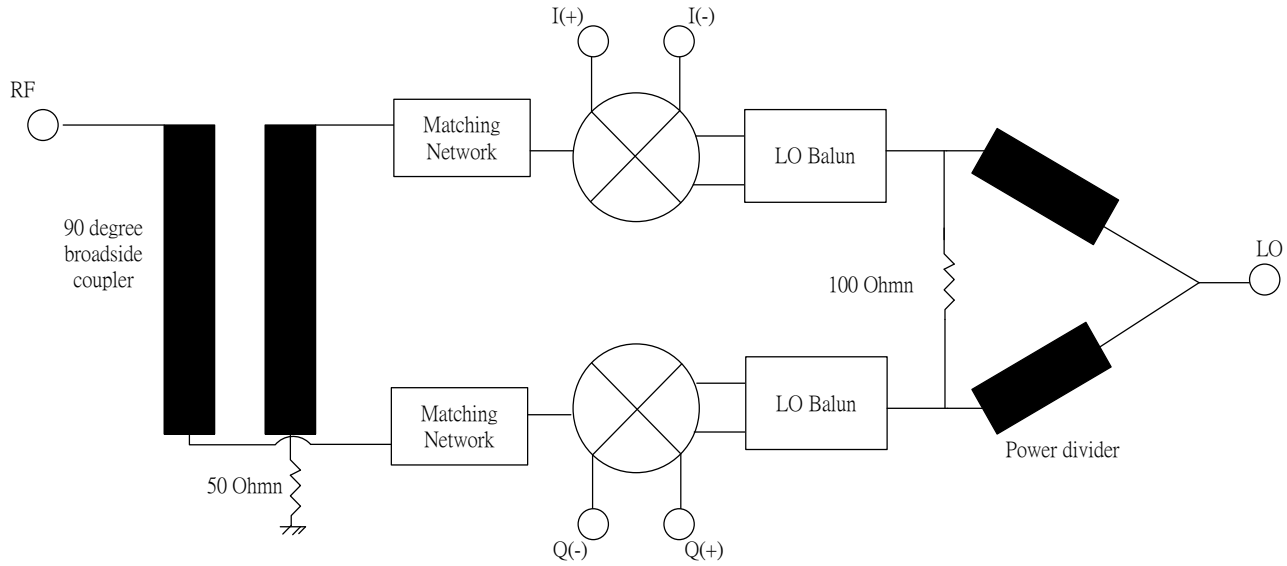
Figure 11. CG *versus* fractional bandwidth of the recent published MMW SiGe mixers. Data taken from [80,136–140].



3.4. Modulators

Quadrature phase (I/Q) modulator (or demodulator) [141,142] is composed of two mixers, which are combined with a 90° hybrid at the input port; meanwhile, an in-phase power divider is utilized at the output (Figure 12).

Figure 12. Block diagram of the MMW I/Q modulator.



The Marchand balun is designed to provide the differential LO signal for the double-balanced mixer architecture. The Wilkinson power divider furnish a good isolation between the LO port and the other two mixers. The modulator (demodulator) can perform the modulation (demodulation) of the received (or transmit) RF signal by following the design procedures in the textbook [143]. However, there are some design challenges for the modulator or demodulator.

The Wilkinson power divider at the output port, which limits the overall bandwidth of the modulator (demodulator), should be designed carefully. The performances could be further improved in both the area and bandwidth. Moreover, the bandwidth extension techniques such as right/left hand transmission line and naturalization can be applied to the circuit for improving the bandwidth of the passive components and maintaining good isolation performances [144].

The other concern is that the mixer core is the most critical part of the modulator (demodulator). It dominates the critical performances like CG. Furthermore, the better mixer core is developed, the less LO power is needed to drive the modulator (demodulator). For example, in a passive mixer, adjusting the bias condition of the mixer core can intensify the CG. The transistors in mixer core can be biased around their threshold voltage to increase the CG due to their low channel resistance in this operation region. As for the low LO power driven mixer core, it is able to achieve by reducing the number of transistors in the mixer cores of the modulator (demodulator).

Furthermore, in the upcoming communication standard for V-band, it is desire to have a 64-quadrature amplitude modulation (64-QAM) [145]. The nonlinearity and IQ mismatch damage the RF signal especially for high QAM modulators. However, the IQ mismatch can be reduced by proper selection of the circuit topology. Likewise, power back-off can be leveraged the linearity constrain [146].

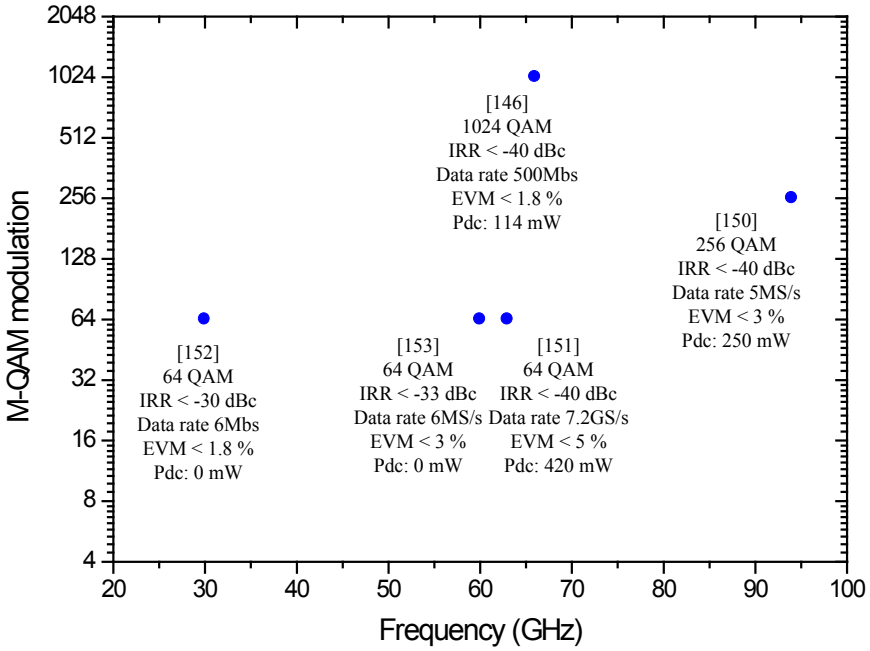
The solution to the IQ mismatch can be provided by a type of calibration technique [116,147–151]. For the in-phase/quadrature (IQ) mismatch of the IF path, digital [147,148] and mixed-mode [149] techniques are exploited below 2 GHz. However, more power consumption and area are necessary for the digital compensation technique as well as the additional control circuits. Also, the limitation of bandwidth are the major issue for most IF compensation techniques. For MMW wideband communication, IQ magnitude mismatches can be achieved with phase calibration mechanisms on the local oscillator (LO) signal path and variable gain amplifiers (VGAs) on the IF path [150]. The image rejection ratio (IRR) can be suppressed below 40 dBc with this calibration mechanism at W-band. A 256-QAM constellation with 3% error vector magnitude (EVM) is demonstrated at 90 GHz. In addition, the 60-GHz direct conversion transmitter with 33-dB conversion gain and the 11-dBm saturated power enlarges the dynamic range for the measurement consideration. By using the characteristics of the high image rejection and good LO signal suppression, the direct-conversion transmitter MMIC demonstrates a 1024-QAM modulated signal (modulation capability) with a data rate of 500 Mb/s and the EVM results are within 1.7% at 65 GHz. Figure 13 shows a comparison between our design and other works of MMW high-order QAM modulation [150–153].

Those solutions for improving the performances in the major categories are introduced. Among the wideband, miniature, and high isolation, the point is mainly about the passive such as balun, combiner, filter, power divider and matching networks. Note that in [152] and [153], there's no active device in both of the architectures; therefore, no dc power consumptions are required.

Different from the published MMW mixers in decades ago, modern MMW mixers have mixed features as well as topologies for the multi-standards or complex modern communication MMW

systems. As a result, they could not be easily compared according to a single feature. With the aforementioned background of the MMW mixers, some representative MMW mixers, which were recently reported, will then be exemplified.

Figure 13. Comparison of the MMW high-order quadrature amplitude modulation QAM modulation. Data taken from [146,150–153].



3.5. Voltage Control Oscillator (VCO)

LC-tank oscillator [154], distributed oscillator [155–157] and harmonically pushed oscillator [158–161] are popular topologies in MMW regime. These topologies will be introduced as follows.

LC-tank oscillator is widely adopted due to its simplicity. The resonate frequency is dominated by the inductor and capacitor. Moreover, the loss of the passive components is compensated by the negative resistance, which is attributed to the cross-couple pair of the oscillator. A resonant circuit and an amplified stage constitute the LC tank VCO. The resonate circuit is usually consisted of the inductors and a variable capacitor for the purpose of tuning mechanism. This can alleviate the effects of the process variation and give some margins for the operation frequency. For instance, in most of case, there is a frequency shift between the designed frequency and the measured result. Thus, the variable capacitor makes us to adjust the resonate frequency of the VCO to fit the target frequency, in turn, minimize the difference between simulation and measured result. Moreover, the amplified stage cannot only be the cross-couple pair but also the other amplified configurations like a single transistors or cascode configuration. Similarly, there are three major factors, which affect the performance of the phase noise in this topology. The thermal noise from the inductors, the noise from the tail current of the VCO and the noise from the transistors are the major concerns while minimizing the phase noise in the topology [154].

Although silicon-based technologies provide higher f_T and f_{max}, passive components limit the frequency generation with low phase noise in MMW regime [162,163]. The distributed oscillator is treated as a possible solution for silicon-based VCO for high frequency operation. There are two

popular topologies for distributed VCO: Standing wave oscillator and traveling wave oscillators. The main concept of the standing wave oscillator is to design the position-dependent tailoring of conductive and resistive losses along the trans-mission line [155]. On the other hand, traveling wave oscillator means to utilize a distributed circuit to propagate the oscillation around a transmission line ring [156,157]. Furthermore, the combination of these two topologies is rotary-wave oscillator [164].

Harmonically pushed oscillator [158–161] is another potential mechanism to generate signal above MMW frequencies. It generates N times fundamental frequency with the disadvantage of lower power level compared with the oscillator, which generates fundamental frequency. The LC-tank is designed to resonate at the harmonic of the target output frequency. The oscillation condition is easy to be satisfied for the low gain characteristic of the transistor at MMW or even higher frequencies. Additionally, the on-chip inductors and MOS-varactors have high quality factors at low frequencies; therefore, the better phase noise can be achieved. In contrast, the imperfect differential output of the VCO is the issue due to the process variation. As a result, an extra amplifier is necessary for compensating the loss, which is generated from the mismatch. More dc power consumption is required.

3.5.1. VCO in CMOS Technology

Figure 14 illustrates the measured phase noise of the published MMW CMOS VCOs. In [165], a CMOS MMW low voltage VCO with the AC-coupled LC tank is reported. Wide tuning range and pushing by the high order harmonics are achieved by using the AC-coupled LC tank, simultaneously. The differential tuning is performed by an extra varactor biasing terminal without large resistors for a differential PLL. In [166], a fundamental double-stacked cross-coupled VCO were implemented in 32 nm SOI CMOS technology. The additional negative source degeneration resistance improves the overall negative resistance of this oscillator, in turn; the loss of the varactor at high frequencies is compensated. As a result, the phase noise and the loop gain will be improved. In [167], a high tuning range and high output power VCO is proposed. The tuning range is enlarged by exploiting either a variable capacitor or controlling the phase/delay between the coupled oscillators. In [168], a novel varactorless VCO is presented. Between the source and drain nodes of the cross-coupled pair, source degeneration and capacitors are adopted to alter the frequency of the VCO. In [169], according to the nonlinear dynamic theory, the phase shift and frequency are dominated by the coupling between the cores. The harmonic power, which is generated by the coupling of the two multiple oscillators, will be transfer to the output without varactors. In [170], the conventional cross-coupled 38 GHz VCO with a doubler was implemented in 65 nm CMOS with a phase noise of −88 dBc/Hz at 1 MHz offset and a measured output power of 6 dBm at 77 GHz. In [171], the extension of the output frequency range and reduction of the phase noise are achieved by standing-wave transmission line resonators. The VCO, which exploits the standing-wave transmission line resonators, has lower phase noise instead of the one, which does not use.

Except for the recent published works, some representative MMW VCOs will be illustrated.

A V-band VCO and a Q-band VCO are reported in [172]. The tuning range of the V-band VCO is 16% and the Q-band DCO has 18 bits and 14% tuning range with the variable inductor techniques. The tuning mechanism of the variable inductor, which is composed of a transformer and a variable resistor, is to changing the variable resistor to adjust the inductance. In this fashion, wide frequency

tuning range and multi-band operation can be achieved without lowering the operation frequencies. Figure 15. See also, Figure 16. The VCO and DCO are both fabricated in 90 nm CMOS technology. The tuning range of VCO is 9.1 GHz that is from 52.2 GHz to 61.3 GHz. The measured phase noise is about 118.75 dBc/Hz at 10-MHz offset at 61.3 GHz with the output power of −6.6 dBm. The dc power consumption is 8.7 mW with a 0.7-V supply, and the chip size is 0.28 × 0.36 mm^2. S for the DCO, it has a tuning range about 5.8 GHz that is from 37.6 to 43.4 GHz. The measured phase noise is about −109 dBc/Hz at 10-MHz offset with the output power is −11 dBm at 43 GHz. The dc power consumption of the DCO is 19 mW with a 1.2-V supply. It has a chip size of 0.5 × 0.15 mm^2.

Figure 14. Phase noise of the recent published MMW CMOS VCOs. Data is taken from [165–171].

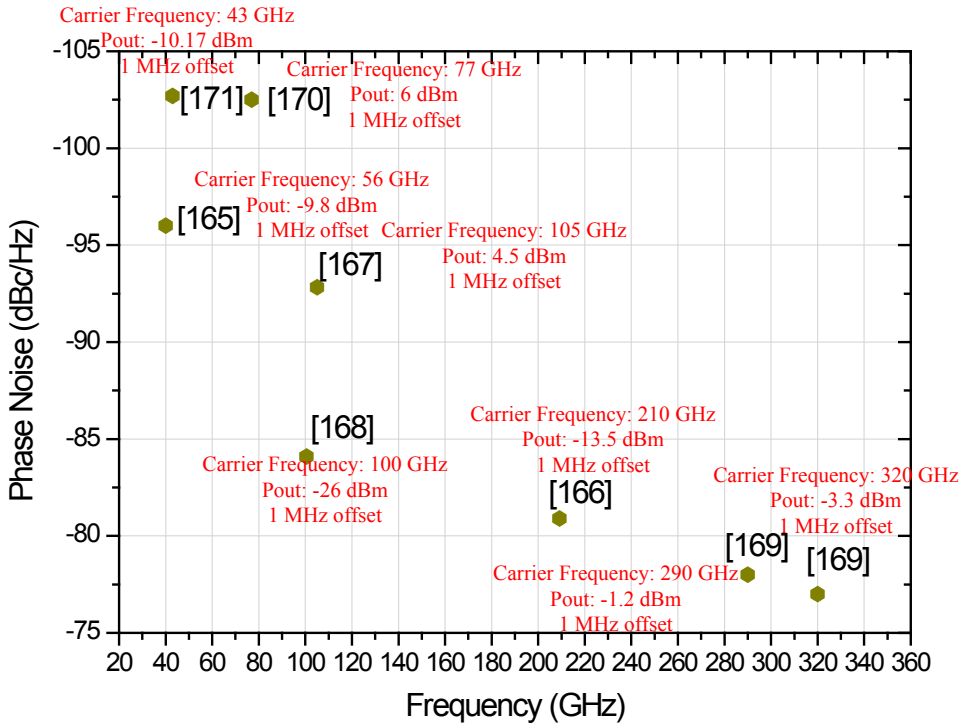


Figure 15. VCO schematic [172].

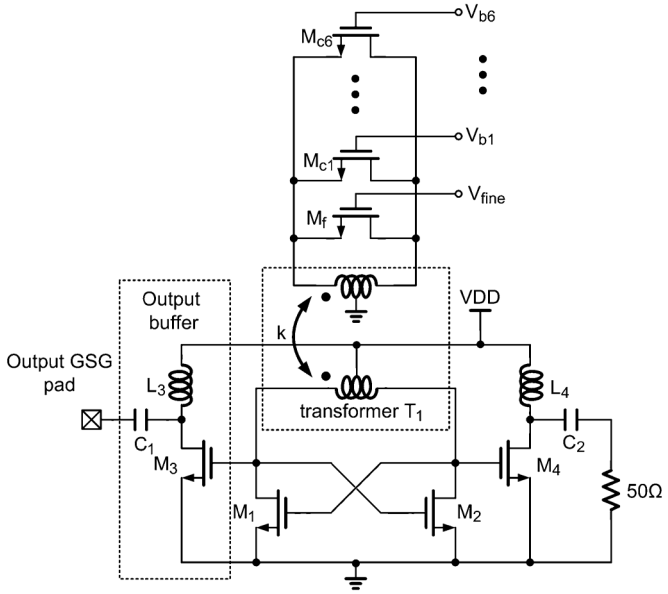
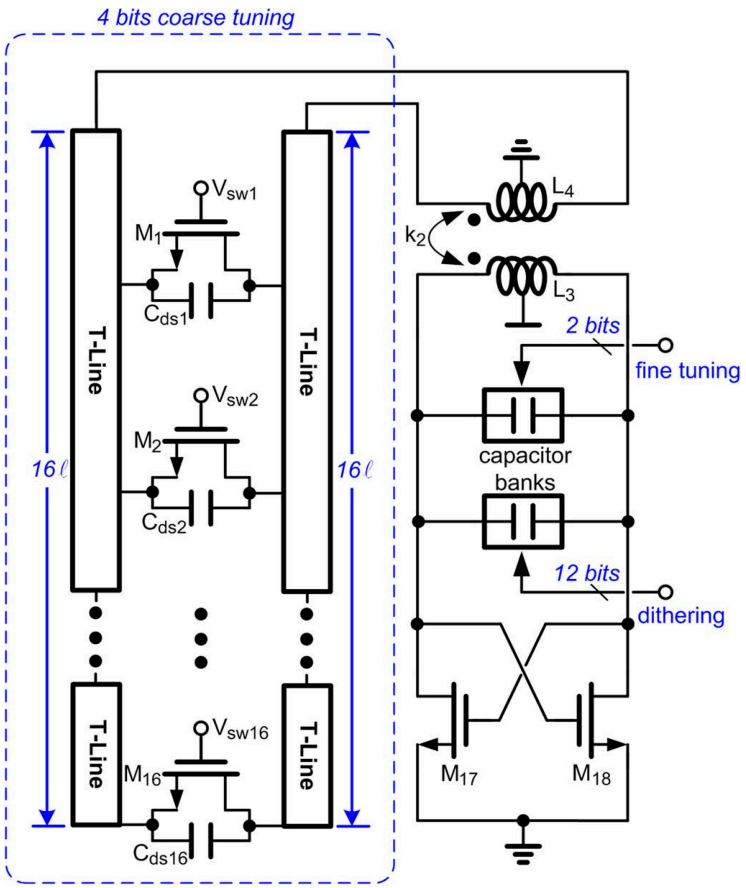


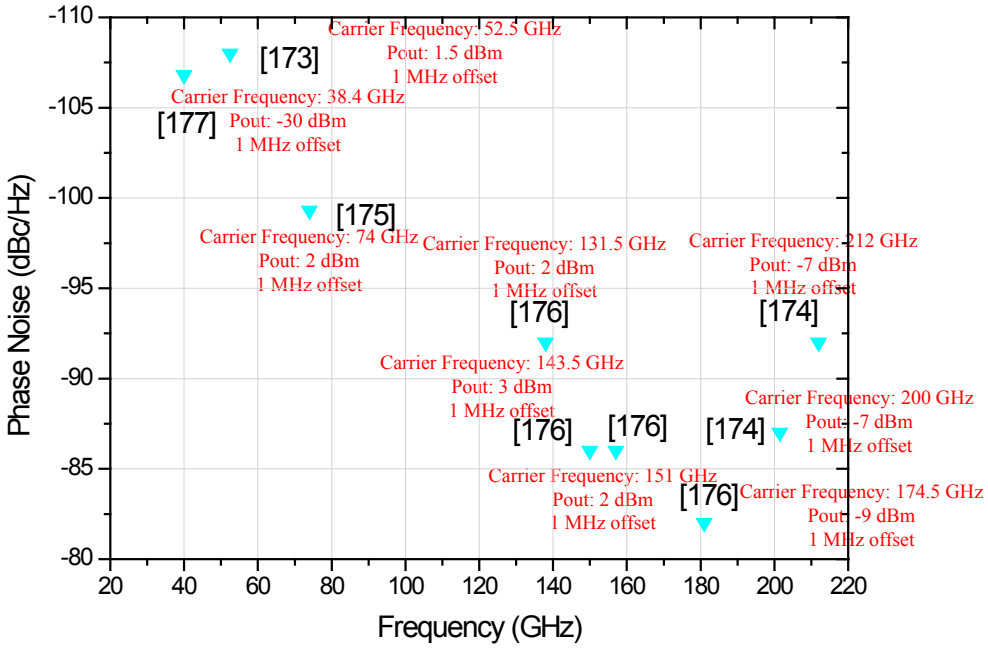
Figure 16. The circuit schematic of DCO [172].



3.5.2. VCO in SiGe Technology

Figure 17 illustrates the measured phase noise of the MMW SiGe VCOs. In [173], a 52 GHz VCO, which employs loop-ground transmission line, is proposed to enlarge the tuning range and output power without sacrificing phase noise. In [174], a high power efficiency inductive tuning VCO was reported. The base-degenerated inductor and resistor lead to a high quality factor and high tuning range. By controlling the bias current of the base-degenerated resistor, the tuning mechanism of the inductor is achieved. Also, the negative resistance of the cross-coupled pair is compensated. In [175], the tuning range and the output power are improved by utilizing the transformer. The primary winding of a transformer tank attracts the signal from the switching transistor bases, meanwhile, the output buffer is driven by the secondary winding. Thus, the tuning range and the output power will increase without leveling the supply voltage. In [176], the earliest broadband SiGe-based VCO/divider combination at 180 GHz is presented. With a divide by 32 prescaler, the total tuning range of the four fundamental VCOs is 56 GHz, which ranges from 125 to 181 GHz. In [177], the low phase noise common-collector Colpitts VCO is reported. With the fixed voltage swing, more current will flow into the tank due to the low impedance of the resonate tank. This results in a lower phase noise than the conventional MMW VCO.

Figure 17. Phase noise of the recent published MMW SiGe VCOs. Data is taken from [173–177].



3.6. Other MMW Control Circuits

3.6.1. Switch in Si-Based Technology

MMW switches, which include SPST switches and SPDT switches [178–184], are essential for a MMW communication system. For a MMW switch, most important design considerations are low insertion loss and high isolation. However, in Si-based technologies, higher loss and parasitics are still challenges instead of their high-level integration and low cost natural. In MMW switch design, the shunt-series and traveling wave (transmission line integrated) techniques are popular.

The series-shunt technique offers appropriate performance of single port single throw (SPST) switches in MMW [178]. As for the single port double throw (SPDT) switch design; the drain-to-source capacitance has great influence on the transistor performance both in the series and parallel path. In [182], the effect of the parasitic capacitance can be reduced by the LC-tuned technique for a narrow band CMOS SPDT switch design.

The transmission-line integrated switches are promising in MMW frequency due to good performances [180,183]. Also, in [179], a 90 nm CMOS switch exploits traveling wave concept to exhibit a wideband performance in 50–94 GHz. It is worth mentioning that a filter-integrated switch concept is proposed with better sideband rejection for the undesired bands [185,186] in GaAs HEMTs. The body-floating technique was reported to increase the power handling capacity of CMOS switches [187].

In [188], a 60 to 110 GHz SPDT switch with traveling wave concept and body bias technique is implemented in the 90 nm CMOS technology. It has a measured insertion loss of 3–4 dB and a measured isolation better than 25 dB. In [189], a low insertion loss and high isolation 90 nm CMOS switch is implemented. In order to achieve a low insertion loss and high Tx-to-Rx isolation, the double-shunt switch on the transmitter side and the matching-network switch on the receiver side are adopted. The switch exhibits a measured insertion loss and Tx-to-Rx isolation of 1.9 and 39 dB, respectively, at 60 GHz.

3.6.2. Circulator and Isolator in Si-Based Technology

Circulator, which is a three ports component, is usually utilized to provide simultaneously transmit and receive signals without diplexer filters or RF switches [179,188,190–196]. An active circulator has wider operation bandwidth, lower insertion loss and smaller area than a passive circulator. In an active circulator, isolation can be enhanced by couplers with the cost of its operation bandwidth [190]. By using common-drain or common source configurations, the operation bandwidth of the active circulator can be extended; however, it demonstrates a high insertion loss and NF [191]. Moreover, good port-to-port isolation can be achieved by phase compensating technique, which is proposed in [192] with complex matching network and large chip area. These can be solved by active balun and current combiner [193] with the cost of reduction in operation bandwidth. Two quasi-circulators exploiting CMOS technology are presented to demonstrate high port-to-port isolations, but the bandwidth of these quasi-circulators were narrow and consume considerable power [194,195]. In addition, current-reuse technique can be applied to an active circulator to save dc power consumptions, nevertheless, the narrow band performances is inevitable [196]. In [189], a 90 nm CMOS 60 GHz quasi-circulator is implemented with distributed amplifiers. By taking advantages of distributed amplifier and Lange couplers, the quasi-circulator has god insertion gain, low NF as well as high isolation performances. As a result, it is suitable for MMW communication systems. In addition, a novel 24-GHz MMIC isolator is developed in TSMC 0.18-μm CMOS. A new topology using the nonreciprocal common-source amplifier and the directional coupler is proposed to realize an isolator without ferrite. This isolator achieves 36-dB isolation with 1.8-dB insertion loss. The dc power consumption is only 3.6 mW. The performance of this isolator is comparable to those of the ferrite isolators except for the bandwidth [197].

3.7. Recent Works of SoC in MMW Regime

Silicon-based technologies add more appeal to the MMW IC designers owing to the trend of higher-level integration. Nevertheless, high substrate loss of silicon is more severe than that of in GaAs technologies. Also, the conductive substrate of silicon-based technologies leads to the leakage signals from the local oscillator or mixed-mode circuits. This has to be taken into layout considerations. N-well and guard ring, which are available in silicon-based technologies, can be utilized to isolate the leakage signals between circuits [198]. In addition, low efficiency of the on-chip antennas and low output power of power amplifier (PA) are still challenging with silicon-based technologies in MMW regime. However, beam-forming architecture like phased array and system in packaging (SIP) are promising for high integration of antennas and output power PA in silicon-based technologies.

3.7.1. CMOS MMW Transceivers

CMOS technologies are popular in implementing MMW ICs for various applications owing to their high-level integration with the baseband circuitry. This contributes to the prosperity of the research in CMOS MMW circuit designs. As a result, in recent years, MMW transmitters and receivers are reported in CMOS technologies including multi-port transceiver [199], direct-conversion transceiver [191,200], Doppler radar transceiver [201–203], phased-array transceiver [204,205] and differential transceiver [166]. The earliest 60 GHz CMOS transceiver for gigabit software-defined transceivers was demonstrated

using 0.13-μm bulk CMOS technology in [199]. It has a 5 dB conversion gain and measured EVM of the BPSK signal is lower than 4% with an input power of −30 dBm. Based on 90 nm CMOS technology, an integrated, energy-efficient 60 GHz transceiver was implemented including baseband circuitry [191], it has a BER of $<10^{-11}$ was measured up to 6 Gb/s in QPSK mode. Wireless testing was also performed using 25 dBi horn antennas over 1 m distance, and the measured BER at 4 Gb/s is $<10^{-11}$. In [163], the 130 nm CMOS 280 GHz imager is reported with a measured NEP of 29 and a responsivity of 5.1 kV/W. LNAs and passive pixels are put outside. The fully integrated array incorporates with the pixels increases 20% NEP. With the backend process, the 130 nm CMOS 860 GHz single sideband detector has a measured NEP of 42 $pW/Hz^{1/2}$ by reducing the number of unit cells in the diode and using the efficiency improvement of patch antenna with frequency. In [201], the 90 nm direct-conversion transceiver has been implemented. The transmitter has an output power of 3.3 to 6.3 dBm in the frequency range from 73.5 to 77.1 GHz. The conversion gain of the receiver is 2 ± 1.5 dB in the RF input range from 76 to 77 GHz, and the output power at the 1 dB compression point is −17 dBm. In [203], a 90 nm CMOS V-band transceiver for sensing the vital signals was reported. It demonstrates the first-pass success of human vital-sign detection at 0.3 m. The small mechanical vibration with a displacement of 0.2 mm can be detected up to 2 m away. A 90 nm CMOS 60 GHz direct-conversion transceiver was reported [200]. In this work, the transceiver was implemented with both 90 nm and 40 nm CMOS technologies. The transmitter has a EIRP of +8.5 dBm and EVM of −22 dB. The carrier and image leakages are −39 dBc and −37.7 dBc, respectively. After the DC/IQ calibration, the transmitter provides more than 14 dB improvement. The receiver has a wide dynamic range of 53 dB (−78–−25 dBm) with a noise figure of 7.1 dB at its peak gain. This chipset has the MAC throughput of 1.8 Gb/s for up to 40 cm and 1.5 Gb/s for up to 1 m. It also shows the capability for 60 GHz mobile applications.

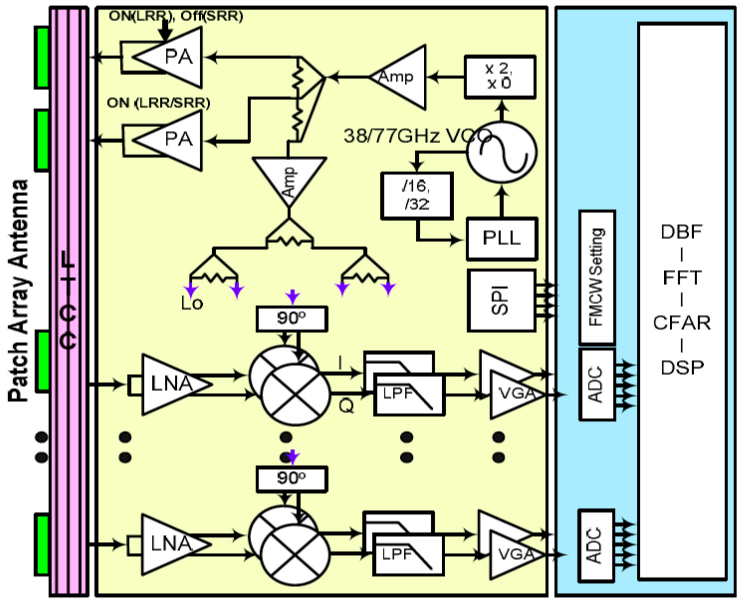
Regarding 65 nm CMOS technologies, some MMW transceivers has been implemented. For instances, in [205], a 65 nm CMOS 4-element phased array was reported. The measured peak output power of the transmitter is −5 dBm whereas the conversion gain of the receiver is 20 dB. In [204], a phased array transceiver was proposed. A 200 m detection with angular resolution below 2° and 60 m detection with FoV of ±45° within one cycle time of 46 ms multi-slope FMCW waveform is designed and implemented.

Figure 18 illustrates the system block diagram of the transceiver. It is composed of eight channel I/Q receivers and one channel transmitter with frequency generation/power divider block. The transceiver is implemented in 65 nm CMOS technology and the patch antenna array is implemented on LTCC substrate. The chip size of single channel and two transmitters are 1.8 × 2.0 mm^2, 1.9 × 0.93 mm^2 and 0.8 × 0.6 mm^2, respectively.

The LNA has a measured gain of 20.1 dB and NF of 8.7 dB (sim.) at 77 GHz and conversion gain of I/Q receiver is 22 dB with 134 mW power consumption. Tuning range of 38 GHz VCO with doubler and 77 GHz VCO shows 69.6–81 GHz and 75.2–79.2 GHz, respectively. Moreover, the PA has a gain of 14.3 dB and P_{1dB} of 10 dBm with 236 mW power consumption.

Furthermore, in [202], the Doppler radar transceiver has a down-conversion gain of 16 dB and an NF of 7–9 dB over an IF bandwidth of 17 GHz. The transmitter output power, as measured at the output of one of the two PAs, varies between +1 and +3 dBm over the VCO tuning range of 90.6–93.5 GHz.

Figure 18. Block diagram of proposed CMOS centric phase array transceiver architecture for radio on a chip and radar on a package [204].



Regarding 32 nm CMOS technology, a SOI CMOS 210 GHz fully differential transceiver was implemented [166]. The receiver has a sensitivity of −47 dBm with a noise figure of 12 dB. The transmitter has an EIRP of 5.13 dBm with a 3 dB bandwidth of more than 14 GHz. This chip demonstrates the possibility of advanced CMOS technologies for implementing the transceivers beyond 200 GHz.

3.7.2. SiGe MMW Transceivers

SiGe HBT and BiCMOS technologies are promising for carrying out the MMW transceivers in these two decades. In the past few years, many MMW transceivers are implemented with SiGe HBT and BiCMOS technologies [103,127,206–212] involving the system architecture of phased array transceivers [150,212–214], sub-harmonic imaging array receiver [215], FMCW radar transceivers [31,216,217], fully differential transceiver [218] and dual-frequency transceiver [103].

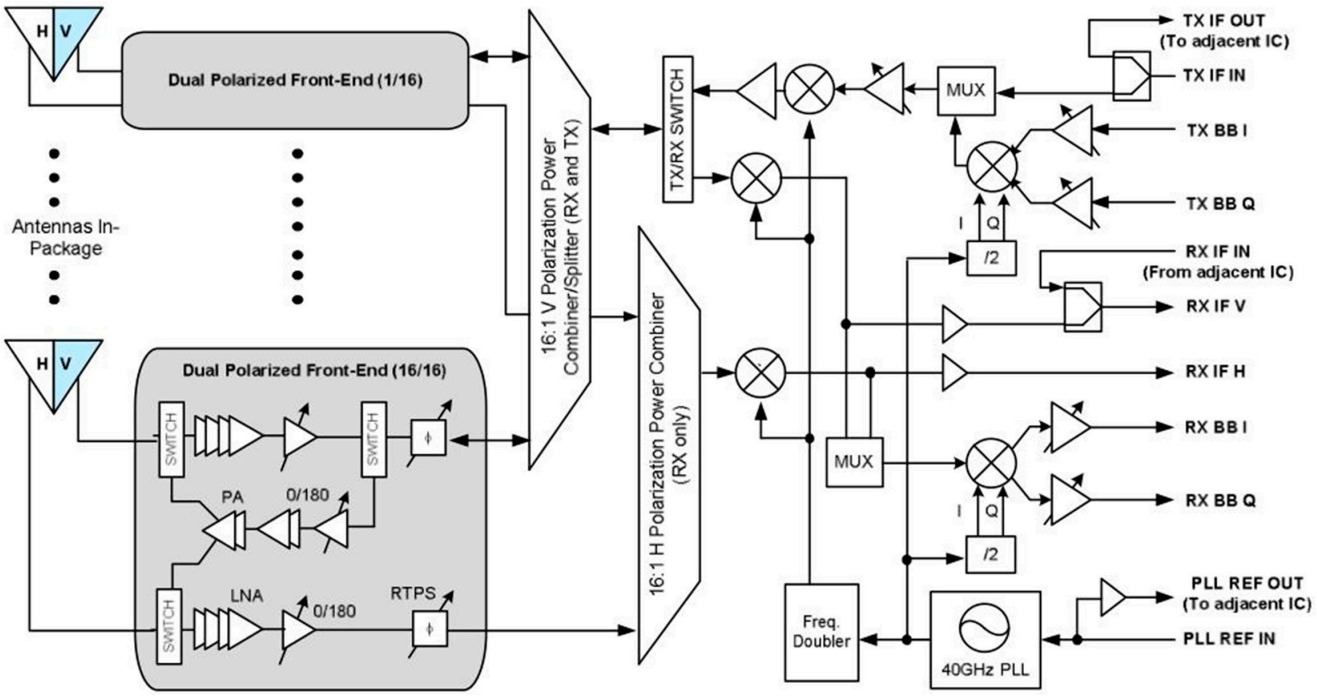
A multi-channel FMCW radar sensor, which is designed and implemented in 0.25-μm SiGe process [31]. The receiver has a measured conversion gain of 7 dB, NF of 16.5 dB whereas the IP_{1dB} is −30 dBm. The transmitter has an output power of 6.5 dBm and the OP_{1dB} of 6.5 dBm. The supply voltage of the transceiver is 3.3 V and the total power consumption is 1.584 W (VCO chip, four transceivers with one transmitter active and down-converter).

In [150], a W-band phased array transceiver is implemented with the 0.18-μm SiGe technology. The receiver has a measured conversion gain of 37 dB corresponding to a bandwidth of 20 GHz. The average NF between 75 and 95 GHz is 7 dB. Between 70 and 102 GHz, the input P_{1dB} is better than −35 dBm. The phase and amplitude imbalance remain better than ±2° and ±0.5 dB between 81.5 GHz and 100.5 GHz, respectively. The I/Q transmitter has a measured maximum saturated output power of 8.5 dBm for each element and higher than 5 dBm between 70 and 100 GHz. The image rejection at 90 GHz is better than 40 dB with the calibration. The transceiver demonstrates a transmitted 256-QAM constellation with 3% EVM.

Based on 0.13-μm SiGe technology, a sub-harmonic pumped 650 GHz receiver was reported [215]. It demonstrates the capability of SiGe technology in sub-MMW regime. The receiver has a measured conversion gain of −13 dB and a noise figure of −13 dB at 650 GHz. Also, when the LO power is −18 dBm. In [216], a 0.38 THz FMCW radar transceiver was implemented in 0.13-μm SiGe technology. The measured EIRP ranges from 11 to 14 dBm. The transceiver demonstrates the FMCW function when the modulation frequency is 20 kHz at the 5 cm distance. Moreover, the measurements are also performed for a target at 10 cm distance from the FMCW radar transceiver. The measured beat frequency of the peak is 210 kHz with 92.47 dBm. In [217], a miniature 0.13-μm SiGe 120 GHz FMCW/CW radar transceiver was presented. The receiver has a measured conversion gain of 12–36 dB with a measured noise figure 9.5 dB. The measured IP_{1dB} of the receiver is −11 dBm. The transmitter has a measured output power of 0 dBm. The power consumption of the whole transceiver is 350 mW. In [214], a 0.13-μm SiGe dual-polarization W-band phased array transceiver was reported. Figure 19 illustrates the system block diagram of the dual-polarization W-band phased array transceiver. The receiver is composed of 32 phase-shifters and one for each antenna polarization (H and V). The transmitter is consisted of the double-conversion superheterodyne architecture, which is the same with the receiver. The local oscillator signal of the transmitter and receiver is provided by the same LO generation with the passive combiners. Depending on the desired polarization direction, only one of these paths will be activated. The beam-steering operations and calibration of the overall array can be bring about by the phase-shifting RF front ends in both transmitter and receiver with local memory arrays with a chip size of 6.6 × 6.7 mm^2.

The receiver has a measured maximum conversion gain of 43 dB and a measured noise figure of 8.2 dB. Also, the measured saturated output power of the transmitter is larger than 2 dBm with a measured maximum conversion gain of 23 dB.

Figure 19. The system block diagram of the dual-polarization W-band phased array transceiver [214].



In [218], a fully differential 240 GHz sub-harmonic transceiver was implemented in 0.13-μm SiGe technology. This transceiver has a measured EIRP of −1 dBm and a measured tuning range of 61 GHz whereas the measured phase noise is −84 dBc/Hz at 1 MHz offset at 240 GHz. Furthermore, the 240 GHz mixer has a simulated conversion gain of better than 5 dB, and an IP_{1dB} of −1.3 dBm.

In [103], a dual-frequency transceiver in 0.13-μm SiGe technology was presented. The transceiver has a measured maximum output power of 3.5 dBm at 165 GHz. The conversion gain of it is 27 dB with the 3-dB bandwidth of 9 GHz. In addition, the temperature effect is also measured. It is observed that the receiver gain is reduced to 11 dB at 75 °C, and to 25 dB at 125 °C, but the transceiver is still functional. The receiver has a P_{1dB} of −20 dBm, the linearity, like the receiver gain, degrades significantly above 100 °C. The transmitter has a measured output power from 23.5 dB to 3 dB, and from 10 dBm to 3.5 dBm, respectively. Moreover, the oscillator at 82.5 GHz drives the static frequency divider and the two amplifiers.

Based on 0.12-μm SiGe technology, the 16-elements phased array transmitter [212] and receiver [213] were reported. For the transmitter [212], the measured OP_{1dB} for the single-element is 9 dBm, corresponding to a 16-element total generated power of 21 dBm and allowing for an EIRP of 33 dBm under ideal spatial power combining excluding unit antenna gain. With increased PA bias conditions the OP_{1dB} per element and total generated power increase to 13.5 dBm and 25.5 dBm, respectively. The OP_{1dB} has a measured variation of ±0.25 dB across different phase settings and adjacent elements. For the receiver [213], it has an input P_{1dB} of 59 dBm at 47 dB gain and 37 dBm at 20 dB gain. An adjacent-channel IIP_3 of 26.5 dBm with the Rx gain is set to be 35 dB (single channel). The noise figure is 7.4 dB at the highest gain mode and 11.6 dB when the receiver gain is set to be 15 dB. The sensitivity at 30 dB Rx gain setting is 86 dBm under the assumption of 2 GHz noise bandwidth and a 12 dB improvement in SNR while the input power is −44 dBm. Also, the measured phase noise is 90 dBc/Hz at 1 MHz offset.

4. Conclusions and Future Trends

Silicon-based MMW ICs look more promising to fit the requirements of mixed signal and SoC applications. However, for the applications of ultra low noise and high output power, III-V based technologies are still more popular than the Si-based technologies.

The future trend of the MMW ICs tends to fit more sophisticated and strictly specifications with multi-features in a single chip or a single circuit component like LNA, PA, mixer, VCO and so on. For the MMW LNAs will be low dc power, low supply voltage, high gain, high linearity as well as low NF. In MMW PA development, especially for modern communication systems, linearity and output power becomes more important due to the requirements for high quality communication. The output power has to be increased without sacrificing too much linearity performance. The future trend of the development of MMW mixers will equip both mixed-multi-features and outstanding performances among wide operation bandwidth, high isolations, CG, linearity, lower dc power consumptions and compact chip size. MMW VCOs nowadays have to fit low supply voltage, wide tuning range, large output power with good phase noise performance. As for other MMW control circuits, the main concept is to replace the passive components with active ones. In this manor, the area will be significantly reduced with moderate trade-off between their performances.

In order to fit those strictly specifications and multi-features in MMW ICs, digitally assisted techniques are developed to solve the emergences. For the future MMW PA designs, digitally assisted techniques incorporate 3-dimensional power combing structures may be useful. The MMW mixer might be designed to be programmable to alleviate the number of mixer for different narrow-bandwidth standards in a MMW system or a time-consuming project cycle of MMW IC designs. Likewise, digitally assisted MMW circuit will be a hot research topic in this decade. This can be solved by the digital compensation techniques in the IF path [120] or LO path. Similarly, self-healing circuits, which can detect, isolate, and repair their own faults produced by the process variations, incorporate with the MMW mixers will possibly become popular [219]. With the evolution of the communication systems, multi-features with digital control mechanism in a MMW VCO are essential. Except for the varactors, inductors or even transformers in a MMW VCO become tunable and thus, wide frequency tuning range and multi-band operation can be achieved without lowering the operation frequencies [172].

As for current MMW transceivers, it is possible to integrate the antenna, a medium-power amplifier, a transceiver, a frequency synthesizer, and baseband circuits into a single chip. Also, high-efficiency antenna is still needs to develop while implementing the transceiver in silicon based technologies. Thus, flip-chip design with LTCC will be essential for high performance antennas, multi-chip modules and the MMW ICs of high power dissipations in order to lower the temperature of the device junctions. Also, three-dimensional MMW ICs will worth further developments to achieve higher level of integrations particularly in SiGe and will find a various applications in MMW regime.

To the author's best knowledge, some silicon-based MMICs emerge in the past few years, for instance, high performance 60 GHz wireless chipsets are available from Silicon Image for the application of a wireless, high-definition video and audio connection, with near-zero latency for wired-quality performance and reliability. These chipsets feature embedded on-chip antennae and proprietary beam-forming algorithms on the low-cost CMOS processes. In most challenging environments, these 60 GHz wirelessHD products still provide a robust wireless connection to support cable-like video connections [220].

Finally, the temperature-compensation for Si-based technologies might be an emerging issue, which needs to be solved. Some temperature compensation techniques are proposed to solve this issue for Si-based MMIC, especially for PA.

In order to suppress the gain variation and the degradation of linearity due to temperature change, a PA with a simple on-chip temperature compensation circuit consisting of diodes and resistors has been reported [221]. In [221], the temperature compensation circuit, which is consisted of a few diodes and resistors, is utilized in the PA. By decreasing the threshold voltage of the diode while the temperature increases. With this temperature compensation circuit, the gain variation of the PA has been improved from 5.5 to 1.3 dB in the temperature range between −10 °C and 80 °C.

A power detector can be adopted in the PA to improve the temperature issue, however, the output load will be increased but the performances will be degraded with this mechanism [222]. In [222], low dc power consumption and high linear P_{out} can be achieved with the dynamic bias control mechanism by reducing the bias current and enhancing the PAE at low P_{out}.

Moreover, in [223], temperature compensation for a CMOS PA based on quadratic temperature feedback is proposed. The temperature sensor is composed of a p-n diode. Only the second stage of the

PA is controlled for minimizing the effects on saturation output power and output power at 1-dB compression point.

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Author Contributions

This paper is organized by Han-Chih Yeh and revised by Huei Wang. Ching-Chau Chiong and Ming-Tang Chen give a lot of comments about the references for recent development either in single circuit component or MMW transceivers while organizing.

Conflicts of Interest

The authors declare no conflict of interest.

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