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# A Suspended Six-Port Transformer-Based Power Divider for 2.4 GHz Applications

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Academic Editor: Jeong-Bong Lee Received: 25 January 2017; Accepted: 5 April 2017; Published: 8 April 2017

Abstract: This paper presents a transformer-based power divider with six-port suspending structure for 2.4 GHz wireless applications. The proposed power divider, which is featured with chip size (2.9 mm  $\times$  2.8 mm  $\times$  21 µm), was constructed by an 8-µm-thick Cu bottom electrode, a 5 µm-height supporting copper post, and an 8-µm-thick suspended spiral copper conducting layer with a 13 µm air gap. The main structure included two transformers and six input/output matching capacitors for simultaneously achieving two single-to-differential paths so that the chip size of the complex multiple-ports transceiver could be reduced. According to the results, the proposed divider has characteristics of the radio frequency (RF), and its input return losses are around -10 dB, output return losses are beneath -10 dB, and minimum amplitude imbalance is below 1.5 dB and less than 1° phase imbalance at 2.4 GHz operating frequency.

Keywords: transformer-based; power divider; six-port; suspending structure; wireless applications

## 1. Introduction

Increased demands for high transmission speed for wireless communication system have led to the popularity of transceivers with in/quadrature (I/Q) architecture [1,2]. However, to achieve higher data rate, new designs of transceivers are necessary for applications such as industrial, scientific and medical (ISM) radio band (emerging low-power appliances), long term evolution (LTE) mobile networks, multimedia (video streaming, e-commerce), wireless internet access (WLAN, WiFi, WiMax) and wireless body area sensor networks (WBANs) with multi-input multi-output (MIMO) topologies [3]. Figure 1 depicts the diagram for the  $2 \times 2$  MIMO transceiver [4], which comprises two receivers (Rx) and two transmitters (Tx), and both Rx and Tx path have the double conversion architecture [5]. The duplicate functional components are required, that is, passive items with compact size are important after the MIMO architectures are adopted in the transceiver.

Power splitter is an essential and critical component widely used in RF wireless systems [6–12] to provide balanced outputs from an unbalanced input for antenna array [6], or to reduce the reflected wave as an impendence matching network in low-noise amplifiers (LNAs) [7–9]. Power dividers also have been applied to mitigating image rejection [10] and improving voltage conversion [11] in mixers, and are often used in voltage-controlled oscillators [12] to enhance phase noise characteristic.

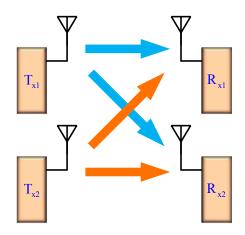
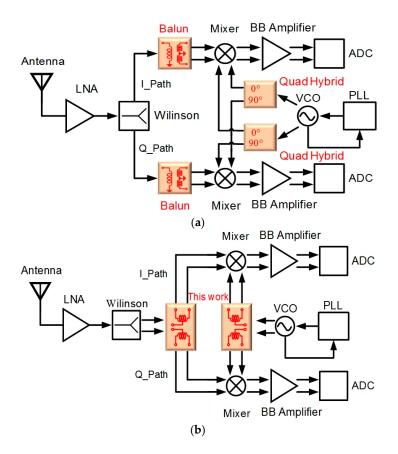


Figure 1. Diagram for the 2 × 2 multi-input multi-output (MIMO) transceiver.

The reported power dividers [13–23] can be classified into active and passive types. Active power dividers usually use two common-drain FETs [13] or Darlington cell [14] topologies to achieve single-to-differential outputs by adopting advanced processes. Despite the advantage of compact size, active dividers are unsuitable for portable systems due to extra power dissipation. Passive dividers, on the other hand, are mostly realized in monolithic microwave integrated circuit (MMIC) technology [15–18] and are seldom performed in MEMS process [19] to split unequal power signal into differential. However, it is still a challenge to implement a power divider with miniaturized size by cause of the limitation of wavelength. Some techniques were proposed to reduce the size of power dividers, such as capacitive loading technique [20] and lumped components based on Method of Least Squares (MLS) technique [21], but they do not have multiple ports to simultaneously realize two differential outputs. So, six-port splitters were proposed using a Wilkson power divider combined with three quadrature hybrid couplers (or three branch-line couplers) [22], and a rat-race coupler incorporated with three branch-line couplers [23]. Although the mentioned splitters are suitable for I/Q transceivers, they are still too large to be integrated with RFIC chips.

In the receiver front-end architecture shown in Figure 2a, mixer is an indispensable component with differential configuration since it has better port-to-port isolation and noise immunity [24], and the passive blocks, such as single to differential baluns and 90° phase shifters, are required to realize the differential signal. However, passive blocks always dominate the entire receiver chip size, let alone the MIMO transceiver system. Figure 2b presents the implemented suspended six-port transformer-based power divider adopted in the receiver front-end, which provides two differential outputs for simultaneously reducing the passive blocks and the complicated multiple Rx or Tx MIMO chip dimension.

The implemented suspended six-port transformer-based power divider is featured with compact size and good phase imbalance for multiple components on silicon substrate utilizing surface micromachining technology. In the main structure, multilayer transformer configurations were used to shorten the dimension of the power divider, and the MIM capacitors located at input/output ports were used to improve the impedance match. The proposed power divider is suitable for multiple Rx or Tx MIMO applications. In the following sections, we will show the structure of the proposed six-port transformer-based power divider, the manufacture of fabrication processes, the measured results of divider, and its comparison with simulated performances.



**Figure 2.** The receiver front-end architecture with: (a) conventional passive device (b) six-port transformer-based power divider.

### 2. The Structure of the Six-Port Power Divider

The six-port transformer-based power divider consisted of two inner symmetric transformers, ground ring and six exterior metal-insulator-metal (MIM) capacitors (C), and the top and cross-section views of the divider is shown in Figure 3. Power incident at input port (port 1) was coupled to the output ports (port 3 and port 4), and the phases at port 3 and port 4 were 90° and -90°, respectively. Similarly, the power incident in port 2 was coupled to ports 5 and 6, and there were two 180° phase differences between each output ports (port 3 and 4, port 5 and 6). The layer thicknesses of power divider were calculated according to the skin effect equation [25], and the skin depth ( $\delta$ ) was defined as

$$\delta = \sqrt{\frac{2}{\omega \cdot \mu \cdot \sigma}} \tag{1}$$

where  $\omega$  is the angular frequency,  $\mu$  is the permeability and  $\sigma$  is conductivity, and the computed result is around 1.5  $\mu$ m. Since thickness is usually five times higher than the skin depth for reducing conductor loss, the thickness of inner symmetric transformers has to be higher than 7.5  $\mu$ m, and we set the thickness as 8  $\mu$ m to avoid structure collapse while the devices were released. Free-standing symmetric transformers was also used to reduce the substrate loss with 13  $\mu$ m air-gap by surface micromachining technique. To minimize the proximity effect [26], the windings of transformers need to be as short as possible, and the turns need to be spaced apart to separate the signal lines. Therefore, we used the full-wave electromagnetic (EM) commercial software (Ansoft HFSS) to optimize the signal lines (W) and space (S) between each lines, which were 60 and 25  $\mu$ m, respectively. The inner symmetric transformers contained three differential ground (G), signal (S), ground (G), signal (S) and ground (G) lines, and the widths (S<sub>1</sub>) of each pad were 60  $\mu$ m. The ground ring structure was used to connect all the ground terminals of this transformer, and the line width (W<sub>1</sub>) was 115 µm. To further approach the characteristic impedance (Z<sub>0</sub>) and to reduce the propagation of the reflected wave at high frequency, we adopted the input/output ports of this power divider with matching MIM capacitors, and the dimensions of the input/output MIM capacitors were 550 (W<sub>c1</sub>) × 550 (l<sub>c1</sub>) µm<sup>2</sup> and 530 (W<sub>c2</sub>) × 1225 (l<sub>c2</sub>) µm<sup>2</sup>, respectively.

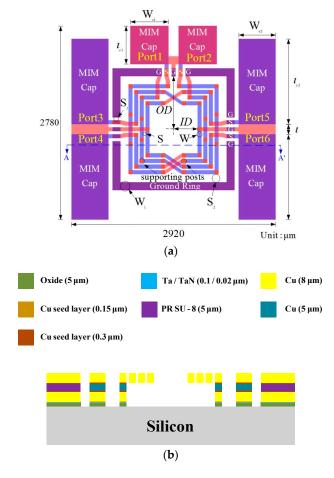


Figure 3. (a) Top and (b) cross-section views of the six-port transformer-based power divider.

Air, nitride (Si<sub>3</sub>N<sub>4</sub>) [27,28], oxide (SiO2) [29,30] and polymer (SU-8) [31,32] have been used as the material of the insulator of MIM capacitor, but the relative permittivity (~1) of air is too low to achieve the smaller dimensions of capacitors, and nitride and oxide capacitors have higher relative permittivity. In addition, the temperature required for both materials has to be above 200 °C, which leads to difficulty in dislodging the sacrificial layer (AZ 4620) under the insulator layer. So, we chose polymer, which has moderate relative permittivity (~3) and high compatibility, as the material for MIM capacitor.

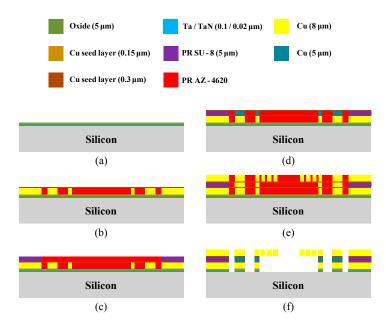
The inside diameters (ID) and outside diameters (OD) of six-port transformer-based power divider were 345  $\mu$ m and 760  $\mu$ m, respectively. The chip dimension including test pads was 2920  $\times$  2780  $\mu$ m<sup>2</sup>, and Table 1 lists the major design parameters of the proposed six-port transformer-based power divider.

Table 1. The parameters of the proposed power divider.

Parameter	w	s	$S_1$	$W_1$	W <sub>c1</sub>	l <sub>c1</sub>	W <sub>c2</sub>	1 <sub>c2</sub>	ID	OD
(µm)	60	25	60	115	550	550	530	1225	345	760

### 3. Fabrication of the Six-Port Transformer-Based Power Divider

The proposed power divider, whose structure is shown in Figure 4, was fabricated utilizing surface micromachining technology with four photomasks. The 5000-Å-thick silicon dioxide isolation layer was grown on a 525-µm-thick 4-inch silicon wafer using a low-pressure chemical vapor deposition system (LPCVD). A 200-Å-thick TaN, a 1000-Å-thick Ta and a 1500-Å-thick Cu multilayers were continually deposited onto silicon oxide layer by RF-sputter system to enhance the adhesion between silicon oxide and Cu layer (Figure 4a). An 8-µm-thick bottom copper conducting layer structure was patterned and deposited by one photolithography process and one electroplating process, and a 3000-Å-thick copper seed layer was deposited by RF magnetron sputtering (Figure 4b). A 5-µm-thick polymer insulator configuration layer of MIM capacitor on seed layer was coated by spin coater and patterned by wet etching (2.38%  $C_4H_{13}NO$ ), as shown in Figure 4c. In addition to the insulator layer, a 5-um-thick copper supporting layer was also deposited and patterned by electroplating system and photolithography process onto the same seed layer and a 3000-Å-thick copper seed layer for electroplating, as illustrated in Figure 4d. Figure 4e depicts the final deposited thin layer, an 8-µm-thick top copper symmetric conducting layer, which was deposited and patterned by electroplating and photolithography process, respectively. The photoresist (AZ 4620) etchant (persulfate) and Cu etchant (persulfate and  $H_2SO_4$ ) were used to remove the sacrificial and cooper seed layers, and Ta/TaN thin layers were etched out in 40 wt % and 90°C KOH etching solution for 30 min to fully release the suspended micro structure. Finally, the whole power divider consisted of six thin-film of various materials, including one 0.5-µm-thick silicon oxide isolation layer, one 0.27-µm-thick TaN/Ta/Cu bottom electrode, 5-µm-thick supporting posts and both of the 8-µm-thick bottom and top conducting layers. The total thickness of the power divider was 21.87  $\mu m.$ 

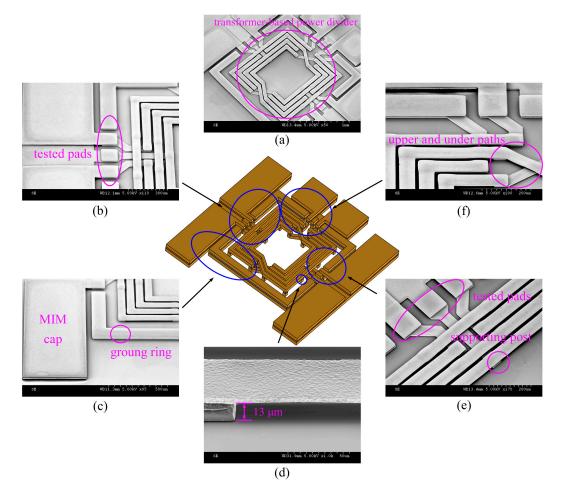


**Figure 4.** Main processing steps of the proposed power divider: (**a**) 5000/200/1000/1500-Å-thick silicon dioxide/TaN/Ta/Cu multilayers deposition, (**b**) electroplating 8-µm-thick bottom copper conducting layer and 3000-Å-thick copper seed layer deposited, (**c**) 5-µm-thick polymer insulator layer coated and patterning, (**d**) electroplating 5-µm-thick copper supporting layer and 3000-Å-thick copper seed layer deposited, (**e**) electroplating 8-µm-thick top copper symmetric conducting layer, and (**f**) remove the sacrificial and cooper seed layers.

#### 4. Results and Discussion

The major portion and scanning electron microscope (SEM) micrographs (with an enlarged view) of the fabricated six-port transformer-based power divider is shown in Figure 5. Figure 5a

presents a free-standing copper symmetric structure well suspended by copper supporting posts on the silicon substrate with a 13- $\mu$ m air-gap underneath. Figure 5b,e present the output GSGSG tested pads. Figure 5d shows high magnification SEM micrograph of the 13- $\mu$ m-tall copper supporting post between the Cu suspended structure and the substrate. The MIM capacitor and 21- $\mu$ m-thick copper ground ring are illustrated in Figure 5c, and 5- $\mu$ m air-gap distance from the under path to the upper path is shown in Figure 5f.



**Figure 5.** Scanning electron microscope (SEM) optical micrographs: (**a**) free-standing symmetric structure of the six-port power divider, (**b**) GSGSG tested pads, (**c**) MIM capacitor and copper ground ring, (**d**) 13-μm-tall copper supporting post, (**e**) GSGSG tested pads and supporting post, and (**f**) 5-μm air-gap distance from the under path to the upper path.

The six-port transformer-based power divider with 2.4 GHz operating frequency was measured on-wafer using an Agilent N5247A to directly obtain the S-parameter data, and the input and output ports were connected with the Cascade Z040-K3N-GSGSG-100 probes. Moreover, the optical image of the micromachined power divider denotes the port numbers for distinguishing the measured S-parameter results, as shown in Figure 6. Since the power divider has six network ports with a differential port considered as two network ports, the power divider is measured between one-side (ports 1, 3 and 4) and the other side (ports 2, 5 and 6) in configurations of three different network ports, whereas the remaining network ports are consistently and simultaneously matched with  $50-\Omega$  terminations.

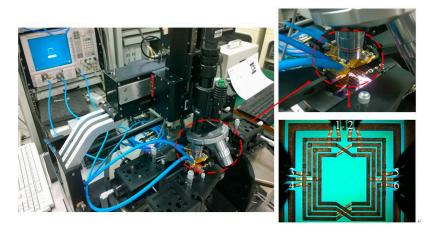


Figure 6. Radio frequency (RF) characteristics measurement environment.

Since the measured operating frequency is often lower than simulated frequency, the optimum simulated high-frequency characteristics were set at 2.7 GHz. Figure 7 illustrates the measured input return losses (S11 and S22) with simulation results versus frequency. Although the nadir S11 and S22 are -17.7 dB at 2 GHz and -19.2 dB at 2.1 GHz, the moderate input return losses are around -10 dB at 2.4 GHz. The simulated and measured output return losses (S33, S44, S55 and S66) ranging from 0 to 5 GHz are shown in Figure 8a,b, in which all the simulated performances are below -15 dB at 2.7 GHz. The measured output return losses are beneath -10 dB and are close to the operating frequency. The frequency difference of input and output return losses between simulated and measured frequency is caused by the material, copper, which may undergo quality changes during electroplating. However, in simulation, we set copper as an ideal conductor. Moreover, the operating frequency of the implemented six-port power divider is 2.4 GHz, and it is susceptible to signal interference from other nearby wireless networks and devices when measured in open spaces. Since the proposed divider uses an up-and-down coupler to transmit signals, the first dip of the output return loss was due to the zero point caused by the self-inductance of the divider and the capacitance between the internal metals and the conductor, whereas the lower dip was resulted from the resonance between the internal inductance and external capacitance. The resonant frequency was set as the operating frequency of the power divider. Figure 9 presents the performance of insertion losses (S31, S41, S52 and S62), and the simulated results are about -8 to -6.6 dB from 2.4 to 2.7 GHz. Measured insertion losses of S31, S41, S52 and S62 are -12.9, -9.3, -10.6 and -9.1 dB. The measured average results are lower than -8 dB due to poor input/output matches and some remains such as photoresist or particle that might not be completely removed. Besides, Figure 10 displays the comparison between the measured amplitude and phase imbalances with the simulated ones at frequency range from 1.5 to 3.5 GHz. According to the two output ports (port 3 and 4, port 5 and 6) of the proposed power divider, the minimum amplitude imbalance is 1.5 dB (port 5 and 6), whereas the maximum is below 3.6 dB (port 3 and 4). Phase imbalances are both less than 1°, which denotes moderate amplitude imbalance but excellent phase imbalance output at 2.4 GHz operating frequency. Moreover, there is an important characteristic of common-mode rejection ratio (CMRR) indicating the performance of differential device, and the simulated results reveal that both the CMRRs are larger than 30 dB, as shown in Figure 11.

Based on the nearby operating frequency, Table 2 tabulates a performance comparison between the proposed six-port transformer-based power divider and prior state-of-the-art approaches. The power divider with two single-to-differential paths than the other literatures. Our design also attains a phase imbalance of 1° and chip area of  $2.9 \times 2.8 \text{ mm}^2$ . Although the prior power splitters in [16,33] exhibit a lower amplitude imbalance, they consume a larger chip area. It is obvious that the proposed power divider has a good phase imbalance.

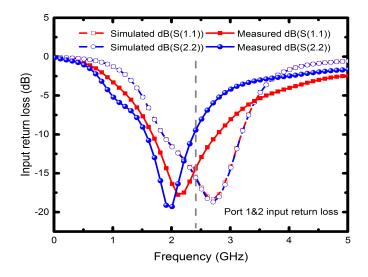


Figure 7. Input return losses of the proposed power divider.

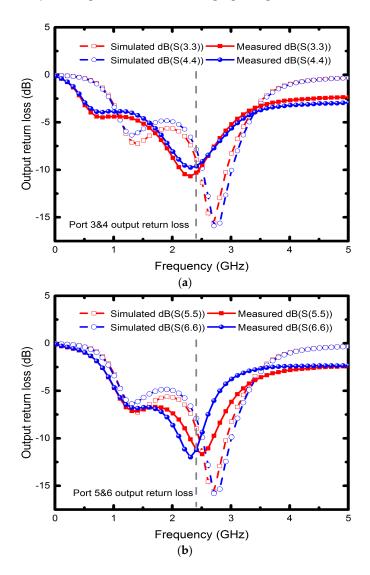


Figure 8. Output return losses of the (a) port 3 and 4; (b) port 5 and 6.

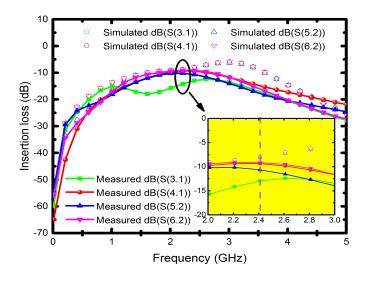


Figure 9. Insertion losses of the six-port power divider.

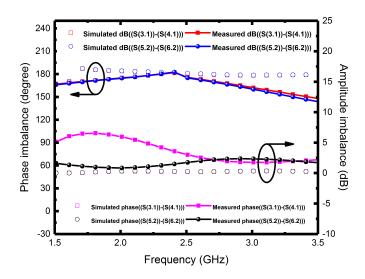


Figure 10. Phase and amplitude imbalances of the six-port power divider.

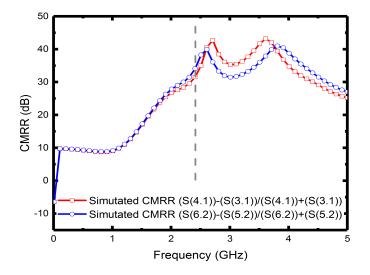


Figure 11. CMRRs of the of the power divider.

Reference	16	19	33	This Work	
Technology	Microstrip Line	Microstrip Line and MEMS	Microstrip Line	MEMS	
Single-to-diff. path	1	1	1	2	
Operating frequency (GHz)	2	2.5	2.1	2.4	
Return loss (dB)	N/A	N/A	-15	-10	
Amplitude imbalance (dB)	1.3	2.4	0.6	1.5	
Phase imbalance (degree)	5.24	5	N/A	1	
Chip area (mm <sup>2</sup> )	$117.2\times37.7$	20  imes 16	83.8  imes 102.3	2.9 imes2.8	

 Table 2. Performance comparison.

## 5. Conclusions

We have proposed a suspended six-port transformer-based power divider with two simultaneously sampled single-ended input and differential-ended outputs for multiport transceivers. With low input/output return losses (S11, S22, S33, S44, S55 and S66), which are -10 dB, minimum transmission imbalance (1.5 dB) and excellent phase imbalance output (1°), the realized six-port power divider is well suited for complex wireless networks and applications.

**Acknowledgments:** The authors thank the Ministry of Science and Technology and National Sun Yat-sen University of the Republic of China, Taiwan, for financially supporting this research under Contract Nos. MOST 105-2221-E-110-080, MOST 105-2622-E-006-018-CC2 and MOST 105-2218-E-110-006. The authors are indebted to the National Nano Device Laboratories (NDL) in Taiwan for their assistance in providing access to their processing facilities.

**Author Contributions:** Wei-Hui Huang and Wun-Hong Syu contributed to the specifications of six-port power divider, the design of experiments and the data analysis. I-Yu Huang proposed the idea of the power divider. Chia-Lung Sung fabricated the device. Chia-Hsu Hsieh wrote this manuscript. All authors contributed in conceiving of, designing and performing the experiments.

**Conflicts of Interest:** The authors declare no conflicts of interest.

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