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Review

Vertical Transistors Based on 2D Materials: Status and Prospects

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Received: 15 December 2017; Accepted: 29 January 2018; Published: 31 January 2018

Abstract: Two-dimensional (2D) materials, such as graphene (Gr), transition metal dichalcogenides (TMDs) and hexagonal boron nitride (h-BN), offer interesting opportunities for the implementation of vertical transistors for digital and high-frequency electronics. This paper reviews recent developments in this field, presenting the main vertical device architectures based on 2D/2D or 2D/3D material heterostructures proposed so far. For each of them, the working principles and the targeted application field are discussed. In particular, tunneling field effect transistors (TFETs) for beyond-CMOS low power digital applications are presented, including resonant tunneling transistors based on Gr/h-BN/Gr stacks and band-to-band tunneling transistors based on heterojunctions of different semiconductor layered materials. Furthermore, recent experimental work on the implementation of the hot electron transistor (HET) with the Gr base is reviewed, due to the predicted potential of this device for ultra-high frequency operation in the THz range. Finally, the material sciences issues and the open challenges for the realization of 2D material-based vertical transistors at a large scale for future industrial applications are discussed.

Keywords: graphene; 2D materials; van der Waals heterostructures; vertical field effect transistors; hot electron transistors

1. Introduction

In 2004, the pioneering works on the field effect in atomically thin carbon films [1], from then on named graphene (Gr), gave birth to an entirely new research branch of solid-state electronics, focused on the use of two-dimensional (2D) materials and their heterostructures for electronics/optoelectronics devices with unconventional or improved performances compared to traditional semiconductor devices. Due to its excellent carrier mobility (up to ~10^5 cm^2 V^{-1} s^{-1}) [2,3] and micrometer electron mean free path [4–7], Gr has been considered since the first studies as the channel material for fast field effect transistors (FETs) [8]. Essentially, the Gr field effect transistor (GFET) resembles the classical metal-oxide-semiconductor FET architecture, where lateral transport in the channel is modulated by a gate electrode separated from Gr by a thin insulator. As a matter of fact, the lack of a bandgap in the electronics band structure of Gr results in a poor ON/OFF current ratio in GFETs, making them unsuitable for digital (logic) or switching applications [9]. On the other hand, GFETs can be of interest for radio frequency (RF) applications, where fast current modulation of the device operated in the on-state is required and switch-off is not necessarily needed [9,10]. To date, RF GFETs allowing current amplification at very high frequencies (>400 GHz) have been demonstrated [11]. However, the same devices suffer from limited performances in terms of voltage and power amplification, mainly due to the high output conductance resulting from the lack of a bandgap. On the other hand, the peculiar

symmetric ambipolar conduction of GFETs has been exploited to demonstrate novel device concepts, such as the RF mixer [12].

To overcome the Gr fundamental limitations arising from the missing bandgap both in digital and RF electronics, new solutions have been explored inside the wide family of 2D materials. In particular, two routes have been followed by scientists working in this field.

The first route was replacing Gr as the channel material in lateral FETs with semiconducting 2D materials, such as some members of the transition metal dichalcogenides (TMDs) family (MoS_2, WS_2, $MoSe_2$, WSe_2) [13] or phosphorene (a 2D lattice composed of phosphorus atoms) [14]. The second route has been to introduce novel device architectures based on van der Waals (vdW) heterostructures obtained by the stacking of 2D materials (such as Gr, hexagonal boron nitride (h-BN), TMDs) [15,16] or by 2D material heterojunctions with thin conventional 3D (i.e., bulk) semiconductors [17]. These devices rely on quite different working principles than traditional lateral FETs and mainly exploit vertical current transport across the interfaces of these materials. They include the tunneling field effect transistors (TFETs) [18,19], the band-to-band tunneling transistor [20], the transistor based on the field effect modulation of the Gr/semiconductor Schottky barrier (barristor) [21] and the hot electron transistor (HET) with the base made with a 2D material [22–25]. These devices typically show high ON/OFF current ratios, not reachable by conventional lateral GFETs, that make them suitable for logic and switching applications. Furthermore, some of these device concepts, like the HET with a Gr base, are especially targeted to operate at ultra-high frequencies up to THz.

This paper reviews recent developments in 2D material-based vertical transistors. Section 2 discusses the open issues of Gr and TMD lateral FETs, and it serves to introduce some of the potential advantages of vertical architectures. Therefore, the main vertical device structures considered so far are presented in the Section 3, where the working principles and the targeted application fields for each structure are discussed. In particular, recent implementations of TFET based on 2D materials are overviewed due to their interest in beyond-CMOS digital electronics. Furthermore, recent experimental activity on the HET with Gr base is presented, considering the predicted potential of these devices in ultra-high frequency electronics. In Section 4, the materials science issues and the open challenges for the realization of 2D material vertical transistors at a large scale are illustrated. Finally, the last section includes a summary and some prospects for future industrial applications of the discussed device structures.

2. Lateral Field Effect Transistors

Due to the proper bandgap (in the range from 1–2 eV), combined with a good stability under ambient conditions, semiconductor TMDs are very promising candidates as channel materials for digital electronics [13]. As an example, MoS_2-channel FETs have been fabricated with large I_{on}/I_{off} ratios (>10^4) and small subthreshold swings (SS < 80 mV/decade) [26], approaching the desired requirements of FETs for CMOS digital circuits. The energy gap of TMDs comes, however, at the cost of a relatively low mobility. As an example, the upper theoretical limit for the mobility of monolayer MoS_2 at room temperature is about 400 $cm^2\ V^{-1}\ s^{-1}$ [27], whereas the experimental values reported so far are in the range of a few tens of $cm^2\ V^{-1}\ s^{-1}$ [28,29].

Besides TMDs, also phosphorene has recently attracted interest as a semiconducting channel material for FETs. A mobility of 286 $cm^2\ V^{-1}\ s^{-1}$ has been reported for few-layer phosphorene [14], whereas values up to ~1000 $cm^2\ V^{-1}\ s^{-1}$ have been shown for multilayer phosphorene with an ~10 nm thickness [30]. However, the main disadvantage of phosphorene (as compared to TMDs) is its chemical reactivity under ambient conditions, which can represent a serious concern for practical applications.

The ultimate thin body of TMDs can be very beneficial for the scaling prospects of lateral FETs for CMOS applications, as discussed in many simulation works [31–34]. As an example, Liu et al. [33] predicted that MoS_2 FETs can meet the requirements of the International Technology Roadmap for Semiconductors (ITRS) [35] down to a minimum channel length of 8 nm. For such aggressively reduced geometries, the low mobility of MoS_2 is not a real issue, because transport can be considered as almost

ballistic for channel lengths below 10 nm. Although most of these predictions are based on simulations, some experimental work has been also reported, where the challenges of channel length scaling in TMD lateral transistors down to the nanometric limit started to be addressed [36].

Concerning high frequency applications, the first Gr-based FET capable of RF operation, fabricated using exfoliated Gr from graphite, was reported in 2008 [37]. Later on, the development of advanced synthesis methods, such as epitaxial growth of Gr on SiC by controlled high temperature graphitization [38–41] or chemical vapor deposition (CVD) on catalytic metals [42], provided high quality Gr of a large area for device fabrication. Ultra-scaled transistors with interesting RF performances have been demonstrated both using transferred CVD Gr [43] (see, e.g., Figure 1a) and epitaxial Gr on SiC (see, e.g., Figure 1b) [43,44].

RF transistors are typically used for the amplification of a high frequency input signal (current or voltage), and the amplifier gain decreases with increasing frequency. Hence, the two main figures of merit for RF transistors are the cut-off frequency f_T (i.e., the frequency for which current gain is reduced to unity) and the maximum oscillation frequency f_{MAX} (i.e., the frequency for which power gain is reduced to unity). As in the case of more conventional RF transistors, the f_T of GFETs was found to increase with reducing the channel length L (see, as an example, Figure 1c). A record value of f_T = 427 GHz has been reported for scaled devices obtained with a self-aligned fabrication process [11].

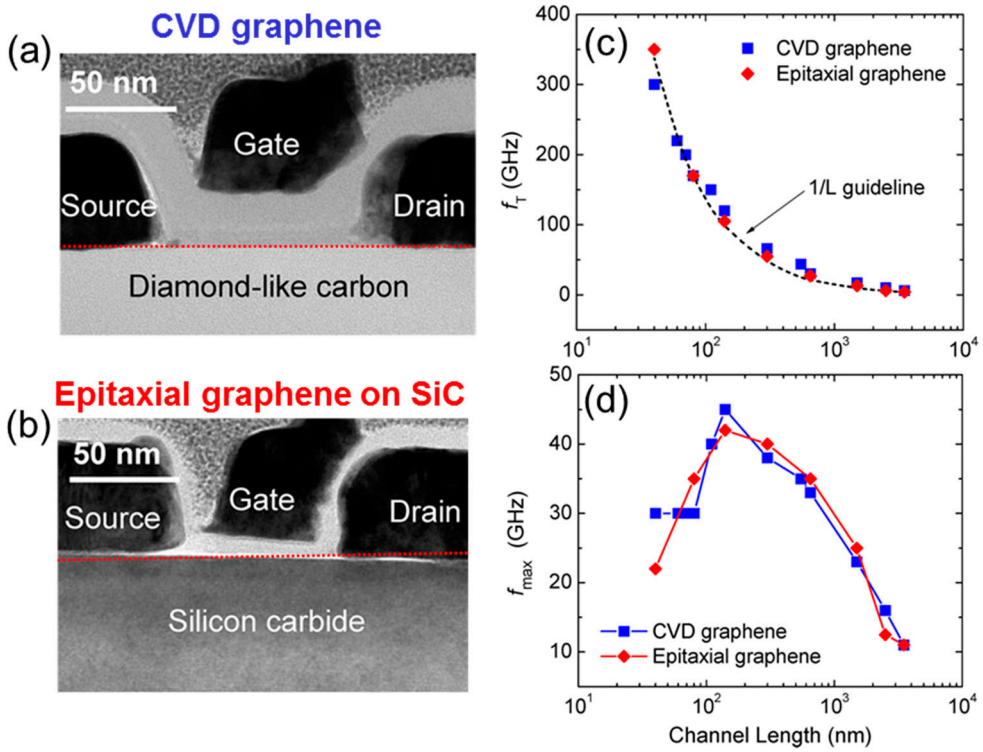

Figure 1. Cross-sectional TEM micrographs of scaled RF graphene (Gr) field effect transistors (GFETs) fabricated with transferred CVD Gr (**a**) and with epitaxial Gr grown on SiC(0001) (**b**); behavior of the cut-off frequency f_T (**c**) and of the maximum oscillation frequency f_{MAX} (**d**) as a function of channel length. Figures adapted with permission from [43].

These values of f_T are comparable with those achieved by the state of the art InP high electron mobility transistors (HEMTs) with similar channel lengths. However, for most RF applications, both high f_T and high f_{MAX} are required, and unfortunately, f_{MAX} values measured for GFETs are significantly smaller than f_T values, as illustrated in Figure 1d [43]. Furthermore, contrary to common expectations for RF FETs, f_{MAX} shows a non-monotonic behavior with the channel length L. In fact, it reaches a peak value around 150 nm and decreases for lower L values.

The reason for these poorer power gain performances can be argued by comparing the theoretical expressions of f_T and f_{MAX} for RF transistors:

$$f_T = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)}\left[\frac{1}{1+g_d(R_s+R_d)+g_m\frac{C_{gd}(R_s+R_d)}{C_{gs}+C_{gd}}}\right] \quad (1)$$

$$f_{MAX} = \frac{f_T}{2\sqrt{g_d\left(R_s+R_{gs}\right)+2\pi f_T R_{gs} C_{gd}}} \quad (2)$$

Here, C_{gs} and C_{gd} are the gate-source and gate-drain coupling capacitances, R_s and R_d are the source and drain series resistances, R_{gs} is the gate-source resistance, $g_m = \mathrm{dI_D/dV_G}$ is the transconductance and $g_d = \mathrm{dI_D/dV_D}$ is the output conductance.

The drain current $\mathrm{I_D}$ of an FET is proportional to the saturated velocity $\mathrm{v_s}$ and to the sheet concentration $\mathrm{n_s}$ of the carriers in the channel. Hence, the two prerequisites to achieve a high transconductance are a high $\mathrm{v_s}$ and a high $\mathrm{dn_s/dV_G}$, i.e., an effective modulation of the carrier density with the gate bias.

If the R_s and R_d resistance contributions in Equation (1) are properly minimized, the expression of f_T can be approximated as $f_T \approx g_m/[2\pi(C_{gs} + C_{gd})]$, and it results in being independent of the output conductance $\mathrm{g_d}$. For this reason the high carrier mobility and saturation velocity of Gr results in a high transconductance g_m and, hence, in a high f_T. On the other hand, from Equation (2), it is evident that, even minimizing R_s, the output conductance g_d still plays a role in the expression of f_{MAX}. As a matter of fact, the output characteristics of Gr channel FETs exhibit a poor saturation behavior, i.e., a large $\mathrm{g_d}$. This overcompensates the effect of a large g_m, ultimately resulting in degradation of f_{MAX}. The non-monotonic behavior of f_{MAX} in Figure 1d has been also ascribed to the competing contributions from f_T, g_d and R_{gs} as L decreases [43].

The poor saturation of the output characteristics is mainly a consequence of the missing bandgap in the Gr band structure. Hence, this peculiar physical property of Gr not only hinders its application in digital electronics, but severely limits also the high frequency performances of GFETs in terms of power amplification and f_{MAX}. Finally, the high off-state current ($\mathrm{I_{off}}$) of GFETs results in a high power dissipation and represents a significant concern in terms of energy efficiency.

Besides Gr, single and multiple layers of MoS_2 have been also investigated as channel materials in lateral FETs for RF applications. Thanks to an electron saturation velocity $\mathrm{v_s} > 3 \times 10^6$ cm/s [45] and to a high bandgap (resulting in a high ratio $g_m/g_d > 30$), MoS_2 FETs can achieve, in principle, both current and power amplification [46–49]. However, quite low values of f_T and f_{MAX} have been reported to date. Initial work on exfoliated monolayer MoS_2 RF FETs yielded f_T = 2 GHz and f_{MAX} = 2.2 GHz at a gate length of 240 nm [48]. Figure 2 shows a cross-sectional TEM micrograph (a) and the DC output (b) and transfer (c) characteristics of an FET fabricated with multilayer MoS_2 flakes. For these devices, the scaling behavior of f_T and f_{MAX} with the channel length is illustrated in Figure 2d,e, showing how f_T = 42 GHz and f_{MAX} = 50 GHz are achieved at a gate length of 68 nm [47]. More recently, RF $\mathrm{FET_S}$ fabricated with monolayer MoS_2 deposited by CVD showed f_T = 6.7 GHz and f_{MAX} = 5.3 GHz at a gate length of 250 nm [49].

Several issues still need to be addressed to evaluate the real potentialities of TMDs both in digital and RF electronics. Besides the issues related to the lattice defects (such as chalcogen vacancies) [50–52] and impurities [53] commonly present in these compound materials, some critical processing steps need to be developed. These include the fabrication of low resistance source/drain contacts [54,55] and doping [56–58].

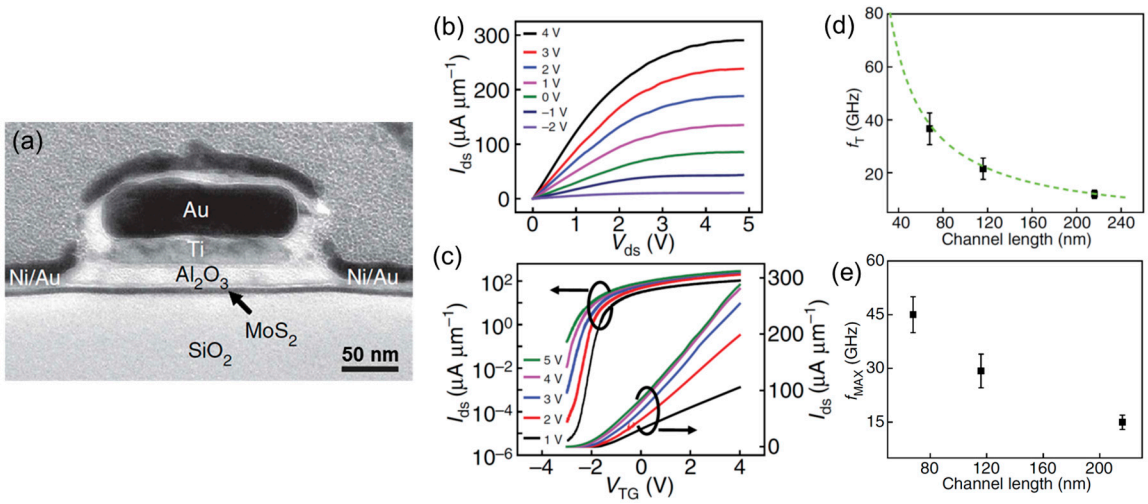

Figure 2. Cross-sectional TEM micrograph (**a**); DC output (**b**) and transfer (**c**) characteristics of an FET fabricated with multilayer MoS_2. Scaling behavior of f_T (**d**) and f_{MAX} (**e**) with the channel length. Figures adapted with permission from [47].

As an example, MoS_2 thin films are typically unintentionally *n*-type doped. Furthermore, most of the elementary metals exhibit a Fermi level pinning close to the MoS_2 conduction band, resulting in a small (but not negligible) Schottky barrier height (SBH) for electrons' injection and a high SBH for holes' injection. The origin of this Fermi level pinning is still a matter of debate, although some nanoscale electrical investigations highlighted the possible role of the defects present at the MoS_2 surface [59,60]. As a matter of fact, this Schottky barrier results in a significant source/drain contact resistance [54,61], which degrades the intrinsic performances of the transistor. Furthermore, the high injection barrier for holes makes it difficult to achieve *p*-type or ambipolar transport in MoS_2 FETs [62,63]. On the other hand, ambipolar transistors can be useful not only for logic (CMOS) applications, but also for some RF circuits. To date, *p*-type MoS_2 transistors have been fabricated by using high work function MoOx contacts [64]. Recently, multilayer MoS_2 transistors with ambipolar behavior have been demonstrated by selective-area *p*-type doping in the source/drain regions with O_2 plasma [65]. Besides MoS_2, other TMDs have been also considered for FETs' fabrication. As an example, WSe_2 is a slightly *p*-doped semiconductor, allowing the fabrication of both *p*-type and *n*-type FETs by proper selection of the metal contacts [66–68]. However, the problem of the contact resistance still holds also in the case of WSe_2.

Most of the TMD-based FETs have been fabricated using metals as source-drain contacts and high permittivity (high-k) dielectrics as gate insulators. Recently, some attempts at fabricating FETs with all components formed by 2D materials have been reported. As an example, Roy and co-workers have demonstrated an FET including MoS_2 as the channel material, h-BN as the dielectric layer for top electrode isolation and Gr for semi-metal contacts (see the schematic and the optical microscopy in Figure 3a,b) [69]. An optimal Ohmic contact between Gr and MoS_2 is possible by tuning the Gr Fermi level by the SiO_2/Si back-gate bias. Due to its large bandgap, h-BN acts as a top-gate dielectric, allowing current modulation over several orders of magnitude (see Figure 3c). Furthermore, thanks to its atomically-smooth surface without charge trapping, h-BN forms an ideal interface with the MoS_2 channel [3]. One of the most relevant advantages of this smooth interface is that the channel mobility of this device remains constant at high gate bias values (see Figure 3d), different from that in common FETs, where a decrease of mobility is observed at high fields due to the effect of the interface roughness.

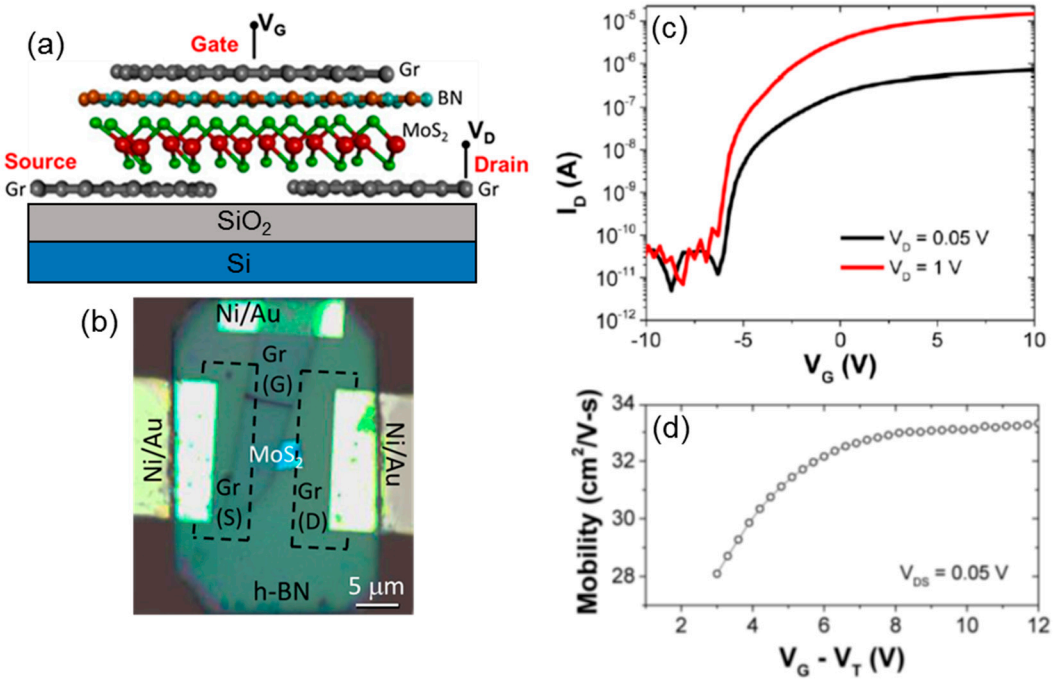

Figure 3. Schematic (**a**) and optical microscopy (**b**) of an FET with all components formed by 2D materials, where MoS_2 works as the channel, hexagonal boron nitride (h-BN) as the dielectric layer for top electrode isolation and Gr for semimetal source/drain contacts. Transfer characteristics (**c**) and mobility vs. gate bias behavior (**d**) of this transistor. Figures adapted with permission from [69]

3. Vertical Transistors

3.1. Tunneling Field Effect Transistors

One of the main issues for modern digital electronics is the dramatic increase of power consumption with the increase in the device integration density. As a matter of fact, the minimum supply voltage to switch an MOSFET from the OFF to the ON state is determined by the thermionic emission mechanism of carrier injection over the energy barrier at the source. This mechanism results in a theoretical limit of 60 mV/decade for the minimum subthreshold swing (SS) for MOSFET devices. On the other hand, tunneling field effect transistors (TFETs), based on quantum mechanical tunneling across an energy barrier, have the potential of reduced supply voltage, since a pure tunneling process is not thermally activated. Numerous studies have been conducted in the last decade to implement this device concept using bulk (3D) semiconductors, such as Ge, III-V and Si [70,71], and sub-thermionic SS values have been reported with TFETs based on these materials. However, the demonstrated performances have not been good enough for practical applications. In particular, one of the main limitations is that SS < 60 mV/decade (at room temperature) is typically obtained only at low drain currents, whereas it would be desirable to get such a behavior over a current range of several orders of magnitude. One of the reasons for the difficulty in obtaining sharp switching over a wide current range is the presence of band-tail states in bulk semiconductors [72]. Under this point of view, 2D materials with sharp band edges even at a thickness of a monolayer can represent an interesting platform to implement TFETs.

Britnell and co-workers first reported a TFET with the vertically-stacked heterostructure composed of Gr and thin h-BN [18]. Figure 4a schematically shows the layer stacking (1); the energy band diagram under equilibrium (2); under the effect of the back-gate bias V_g (3); and under the effect of V_g and of a bias V_b between the two Gr layers (4). The basic principle of this vertical transistor is the quantum tunneling between the two Gr electrodes separated by the thin h-BN barrier. Current tunneling was controlled by tuning the density of states in Gr and the associated barrier by the external gate

voltage. Figure 4b shows the tunneling current density J vs. the bias V_b for different values of V_g. Figure 4c shows the conductance dJ/dV_b (at $V_b = 0$) as a function of V_g, from which an ON/OFF ratio of ~50 was deduced.

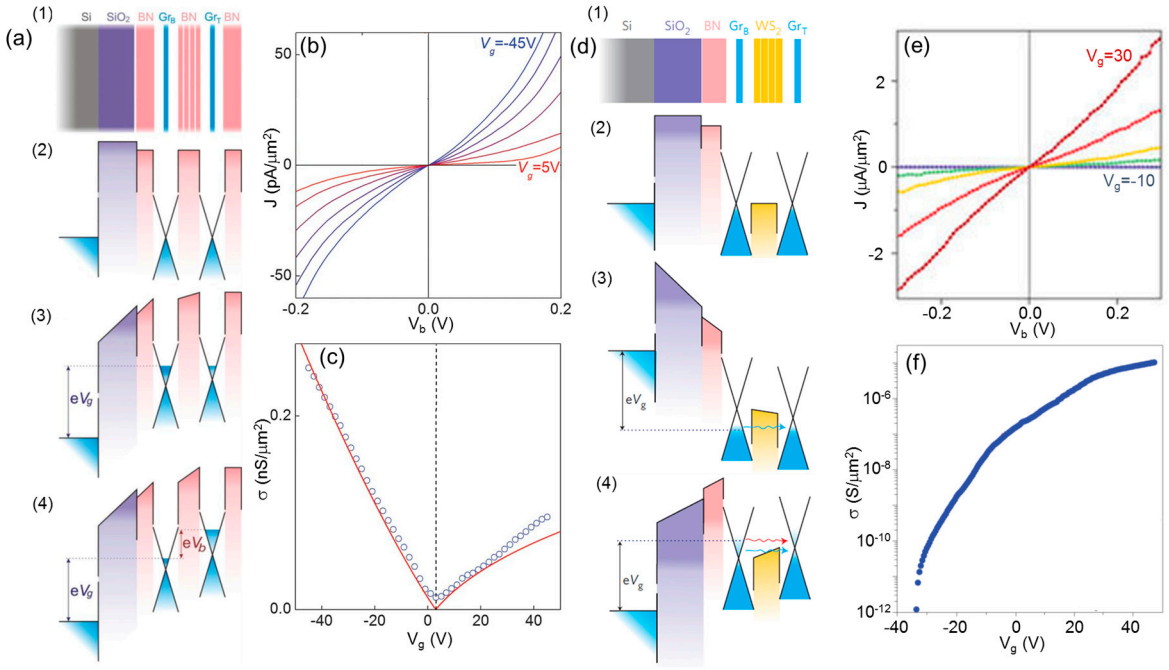

Figure 4. (**a**) Schematic illustration of a Gr/h-BN/Gr field effect tunneling transistor: (1) layer stacking; (2) energy band diagrams under equilibrium; (3) under the effect of the back-gate bias V_g; and (4) under the effect of V_g and of a bias V_b between the two Gr layers; (**b**) tunneling current density J vs. V_b for different values of V_g; (**c**) conductance $\sigma = dJ/dV_b$ as a function of V_g; (**d**) schematic illustration of a Gr/WS_2/Gr field effect tunneling transistor: (1) layer stacking; (2) energy band diagrams under equilibrium; (3) under the effect of $V_g < 0$; and (4) under the effect of $V_g > 0$; (**e**) tunneling current density J vs. V_b for different values of V_g; (**f**) conductance $\sigma = dJ/dV_b$ as a function of V_g. Figures adapted with permission from [18,19].

As the transit time associated with tunneling is very low, the field effect tunneling transistor can be potentially suitable for high speed operation. On the other hand, as a result of the direct tunneling mechanism, this device suffers from very low current density (in the order of 10–100 pA/μm^2), making it not useful for practical applications. Starting from the same idea, Georgiou and co-workers reported a Gr vertical FET with WS_2 layers as the barrier [19]. Figure 4d schematically shows the layer stacking (1); and the energy band diagrams under equilibrium (2); under the effect of $V_g < 0$ (3); and under the effect of $V_g > 0$ (4). Due to the smaller band gap of WS_2, current transport between the two Gr layers occurs by direct tunneling for $V_g < 0$ and by tunneling or thermionic emission for $V_g > 0$. Figure 4e shows the tunneling current density J vs. the bias V_b for different values of V_g, whereas Figure 4f shows the conductance as a function of V_g. As compared to the Gr/h-BN/Gr prototype, this device exhibits much higher ON current (in the order of 1 μA/μm^2) and better current modulation, with an ON/OFF current ratio up to 10^6.

3.1.1. Resonant Interlayer Tunneling Transistors

Progress in the alignment and transfer techniques of 2D materials permitted the demonstration of resonant tunneling phenomena in TFETs. Devices showing gate-tunable negative differential resistance (NDR) of the output characteristics due to resonant tunneling were first obtained by Gr/h-BN/Gr stacks with a precise rotational crystallographic alignment between the two Gr monolayers [73,74]. Since carriers in a Gr monolayer are populated near the *K*-point on the periphery of its Brillouin zone,

conservation of both energy and momentum in the tunneling from one layer to the other is allowed only in the presence of a rotational alignment in momentum space.

Following the first demonstrations with double monolayer Gr, resonant TFET using bilayer Gr as the top and bottom electrodes and h-BN as the interlayer tunnel barrier were also demonstrated [75,76]. Due to the more complex band structure of bilayer Gr (with two sub-bands both in the conduction and valence bands at the *K*-point), additional NDR peaks occur at higher interlayer bias [75]. In fact, when the first sub-band of one bilayer energetically aligns with the second sub-band of the opposite bilayer, a second resonant tunneling condition is established. More recently, experimental results for resonant TFETs with multilayer Gr electrodes separated by an h-BN tunnel barrier have been also reported [77]. With an increase in the Gr electrode layer thickness, from bilayer to pentalayer Gr, the resonance peaks have been shown to become narrower in width and stronger in intensity, mainly due to the increase in the density of states with the increase in the Gr thickness. On the other hand, due to the increased complexity in the band structure with multiple sub-bands for thicker Gr, multiple resonance conditions arise in the output characteristics.

h-BN has been widely used as the interlayer in resonant TFETs with symmetric Gr electrodes, due to its good insulating properties and chemically-inert and atomically-flat surface. However, its wide energy bandgap (~5.8 eV) severely limits the peak current at resonance in Gr/h-BN/Gr TFETs [77]. In this context, using TMDs with a smaller bandgap as tunnel barriers may enhance the peak-to-valley ratio of the resonances in the electrical characteristics. Recently, Burg et al. [78] demonstrated gate-tunable resonant tunneling and NDR between two rotationally-aligned bilayer Gr sheets separated by a bilayer WSe_2. Remarkable large interlayer current densities of 2 $\mu A/\mu m^2$ and NDR peak-to-valley ratios of ~4 were observed at room temperature in these device structures.

Recently, the possibility of realizing resonant TFETs using TMD electrodes instead of Gr has been also considered [79,80]. Theoretical reports indicate that vertical heterostructures consisting of two identical monolayer MoS_2 electrodes separated by an h-BN barrier can result in a peak-to-valley ratio several orders of magnitude higher than the best that can be achieved using Gr electrodes [79]. However, practical implementation of resonant tunneling TFETs with identical electrodes (different than Gr) proved to be difficult.

On the other hand, many vertical transistor demonstrators have been implemented with differing bottom and top electrode layers, exploiting the principle of band-to-band tunneling, as discussed in the following.

3.1.2. Band-To-Band Tunneling Vertical Transistor

Roy et al. [81] first experimentally demonstrated interlayer band-to-band tunneling in vertical MoS_2/WSe_2 vdW heterostructures using a dual-gate device architecture. The electric potential and carrier concentration of the MoS_2 and WSe_2 layers were independently controlled by the two symmetric gates. Depending on the gate bias, the device behaves as either an Esaki diode with NDR, a backward diode with large reverse bias tunneling current or a forward rectifying diode with low reverse bias current. Notably, the weak electrostatic screening by the atomically thin MoS_2 and WSe_2 layers resulted in a high gate coupling efficiency for tuning the interlayer band alignments. Later on, Nourbakhsh et al. [82] further investigated band-to-band tunneling in the transverse and lateral directions of the MoS_2/WSe_2 heterojunctions. The room-temperature NDR in a heterojunction diode formed by few-layer WSe_2 stacked on multilayer MoS_2 was attributed to the lateral band-to-band tunneling at the edge of this heterojunction.

A band-to-band tunneling vertical transistor has been demonstrated also using the vdW heterojunction between differently-doped layered semiconductors as WSe_2 and $SnSe_2$, where WSe_2 worked as the back-gate-controlled *p*-layer and $SnSe_2$ was the degenerately *n*-type-doped layer [83].

Yan et al. [84] demonstrated room temperature Esaki tunnel diodes using a vdW heterostructure made of two layered semiconductors with a broken-gap energy band offset: black phosphorus (BP) and tin diselenide ($SnSe_2$). The presence of a thin insulating barrier between BP and $SnSe_2$ enabled the

observation of a prominent NDR region in the forward-bias current voltage characteristics, with a peak to valley ratio of 1.8 at 300 K and a weak temperature dependence, indicating electron tunneling as the dominant transport mechanism.

Another recently demonstrated very interesting device concept is based on the field effect modulation of current transport across the *p*-*n* heterojunction between 3D and 2D semiconductors. The 3D semiconductor component of the heterojunction is heavily doped in equilibrium by substitutional dopants, whereas the doping level of the 2D semiconductor component can be tuned by the field effect. Therefore, gate-tunable 2D–3D *p*-*n* heterojunctions provide a unique opportunity to realize band-to-band tunneling devices. As an example, Sarkar and co-workers have recently demonstrated a band-to-band tunnel FET with a vertical heterojunction between a *p*-type Ge and an *n*-type bilayer MoS_2 [20] (see the schematic representation in Figure 5a). The band diagrams for the device in the OFF and ON states are illustrated in Figure 5b and the transfer characteristics in Figure 5c. By gating the MoS_2 into the high *n*-type doping regime, direct tunneling occurs from the Ge valence band to the MoS_2 conduction band. Figure 5d illustrates the values of the SS at room temperature as a function of the drain current for this bilayer MoS_2/*p*-Ge TFET and for a conventional MOSFET fabricated with a bilayer MoS_2 channel. Different from the conventional FET, this TFET exhibits an SS lower than the thermionic limit of 60 mV/decade in the considered drain current range (from 10^{-13} to 10^{-9} A). On the other hand, for larger drain currents, significantly larger SS values are obtained.

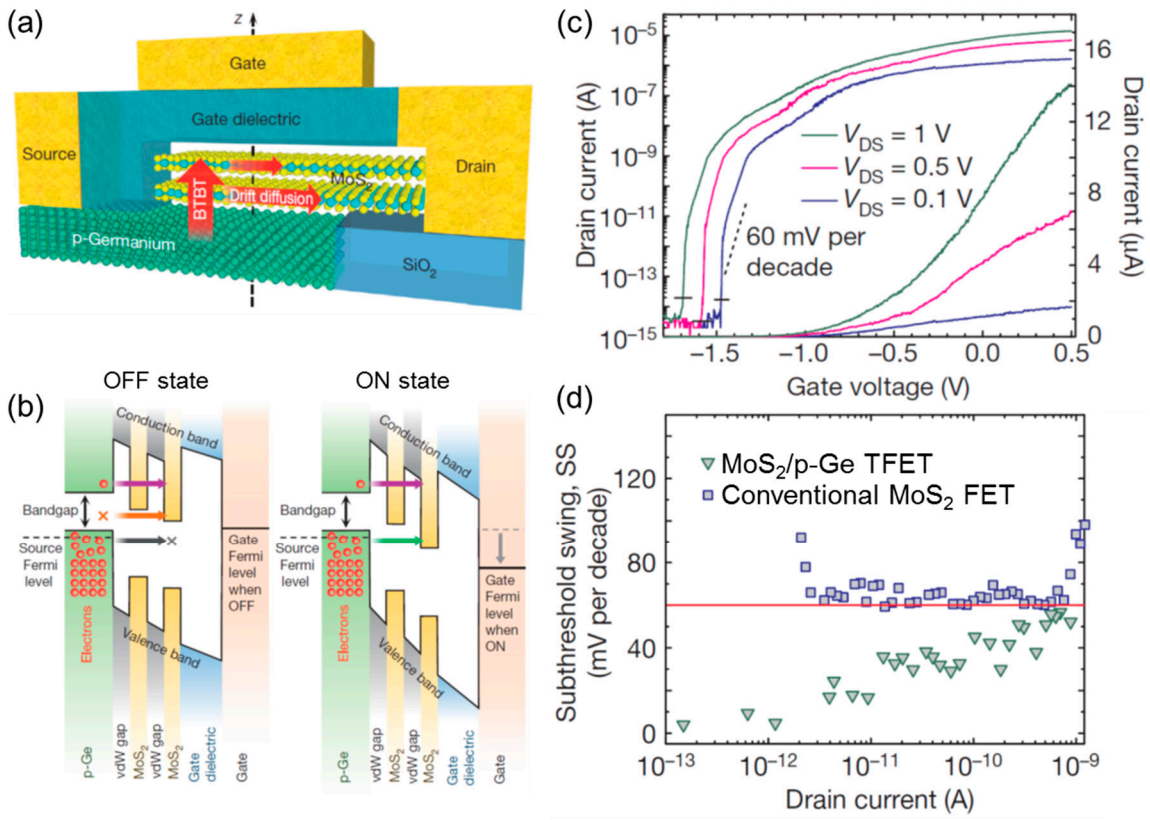

Figure 5. (**a**) Schematic cross-section of a gate-modulated bilayer MoS_2/*p*-Ge junction; (**b**) band diagrams of the device in the OFF and ON state; (**c**) transfer characteristics of the device for different V_{DS}; (**d**) comparison of the subthreshold swing (SS) of this bilayer MoS_2/*p*-Ge tunneling field effect transistor (TFET) with that of a conventional FET with a bilayer MoS_2 channel. Figures adapted with permission from [20].

3.2. Gate Modulated Schottky Barrier Transistor (Barristor)

The Barristor device concept is based on the tunability of the Schottky barrier height of a Gr contact with a semiconductor by an external electric field. Clearly, a nearly ideal interface between Gr and the semiconductor, without interface states responsible for Fermi level pinning, is required to achieve an efficient field effect modulation of the Schottky barrier height. The first Barristor was demonstrated by transferring CVD graphene onto hydrogen-passivated Si, thus obtaining a nearly ideal Schottky diode behavior both with *n*- and *p*-type Si [21]. Figure 6a illustrates a cross-sectional schematic of a Gr/Si barristor, and Figure 6b shows the band diagram for the Gr/*n*-Si Schottky junction for $V_g > 0$ and $V_g < 0$. The modulation of the Gr/*n*-Si Schottky barrier height with the gate bias is shown in Figure 6c, and the resulting output characteristics of the device (for different V_g values) are reported in Figure 6d. A current ON/OFF ratio of ~10^5 under forward bias was achieved, which is suitable for digital logic applications.

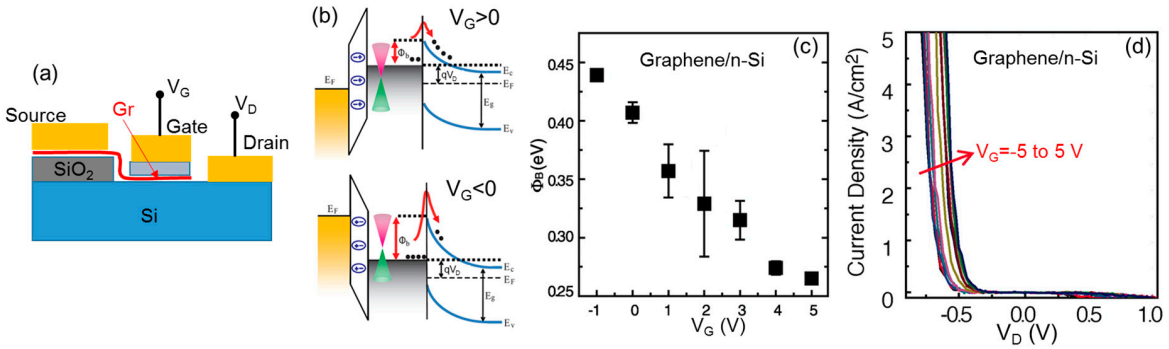

Figure 6. (**a**) Schematic cross-section of a Gr/Si Barristor; (**b**) band-diagrams of the Gr/*n*-Si device for $V_g > 0$ (**a**) and $V_g < 0$; (**c**) behavior of the Gr/*n*-Si Schottky barrier height vs. the gate voltage V_g; (**d**) Current density vs. V_D for different V_g from −5 to 5 V. Figures adapted with permission from [21].

The early demonstration of the Barristor was based on the vdW heterostructure between a 2D material (i.e., Gr) and a 3D material (i.e., Si). More recently, a vertical transistor working on the same principle has been demonstrated using the 2D/2D vdW heterostructure between Gr and a TMD. Also in this case, current modulation was obtained by electric-field tuning of the Schottky barrier between Gr and the TMD, whereas a proper metal layer provides an Ohmic contact with the TMD. Yu and coworkers have demonstrated such a device with a Gr/few-layer MoS_2/metal heterostructure. This FET showed an ON/OFF ratio larger than 100 and a high current density of 5000 A/cm^2 [85]. Moriya and co-workers further improved the current modulation to >10^5 and current density up to 10^4 A/cm^2 with a similar structure, but better interface fabrication [86]. The advantages of this type of vertical transistor are the large current density and the small device scale, providing high potential for future high density integration circuits.

3.3. Hot Electron Transistor

The hot electron transistor (HET) is a three-terminal (i.e., emitter, base and collector) heterostructure device where the ultra-thin base layer is sandwiched between two thin insulating barriers (i.e., the emitter-base and base-collector barriers), as schematically illustrated in Figure 7a. For a sufficiently high forward bias V_{BE} applied between the base and the emitter, electrons are injected into the base by Fowler–Nordheim (FN) tunneling through the barrier or by thermionic emission above the barrier, depending on the barrier height and thickness. A key aspect for the HET operation is that the injected electrons (hot electrons) have a higher energy compared to the Fermi energy of the electrons' thermal population (cold electrons) in the base. Ideally, for a base thickness lower than the scattering mean free path of hot electrons, a large fraction of the injected electrons can traverse the base ballistically, i.e., without losing energy, and finally reach the edge of the base-collector barrier.

This barrier is aimed to act as an energy filter, which allows the hot electrons to reach the collector and reflects back the electrons with insufficient energy. These reflected electrons eventually become part of the cold electrons' population in the base and contribute to base current (I_B), whereas the hot electrons reaching the collector give rise to the collector current (I_C). Besides transmitting hot electrons, the base-collector barrier must be thick and high enough to block the leakage current I_{BCleak} of cold electrons from the base to the collector.

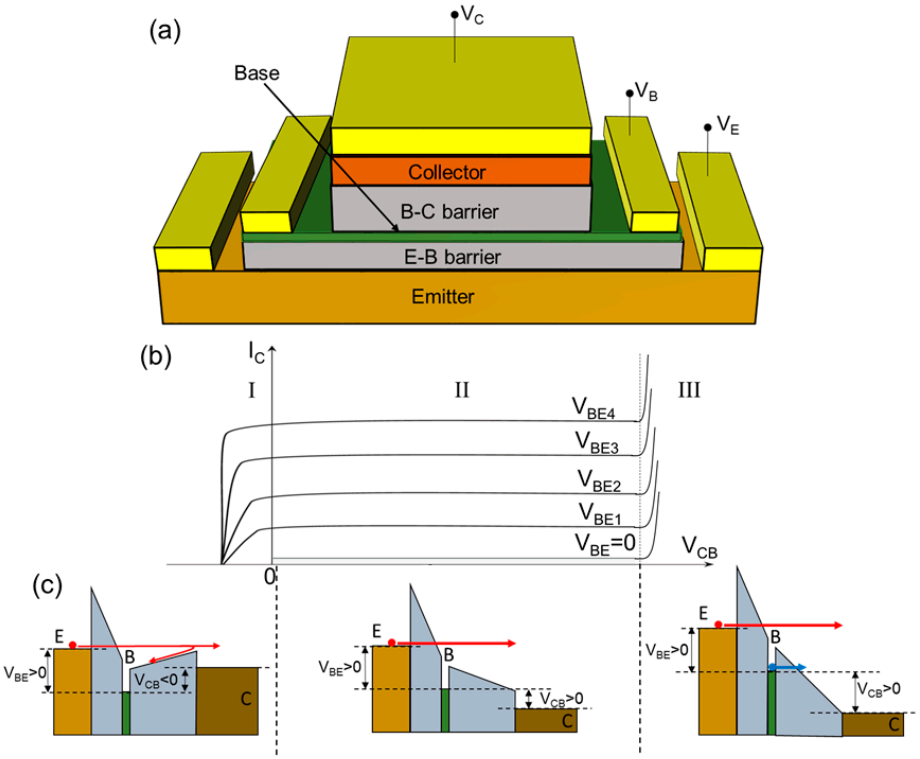

Figure 7. (**a**) Schematic illustration of a hot electron transistor (HET); (**b**) ideal output characteristics I_C-V_{CB} for the transistor biased in the common-base configuration ($V_B = 0$ and $V_{BE} = V_B - V_E > 0$) for different V_{BE} values; (**c**) energy band diagrams for different V_{CB} biasing regimes.

Figure 7b,c illustrates the DC electrical characteristics and the band diagrams for an HET biased in the common-base configuration (i.e., with $V_B = 0$ and $V_{BE} = V_B - V_E > 0$). Depending on the values of the potential difference $V_{CB} = V_C - V_B$, three current transport regions can be observed in the output characteristics I_C-V_{CB} (Figure 7b). For $V_{CB} > 0$ (Region II), I_C is almost independent of V_{CB}, i.e., all the injected hot electrons are transmitted above the B-C barrier (current saturation regime of the transistor). For $V_{CB} < 0$ (Region I), the collector edge of the B-C barrier is raised up, and part of the hot electrons is reflected back in the base, resulting in a decrease of I_C with increasing negative values of V_{CB}, up to device switch-off. For large positive values of V_{CB} (Region III), the leakage current (I_{BCleak}) contribution of cold electrons injected by FN tunneling through the B-C barrier becomes large, and this leads to a rapid increase of I_C as a function of V_{CB}.

The main figures of merits for DC operation of an HET are the common-base current transfer ratio $\alpha = I_C/I_E$ and the common-emitter current gain $\beta = I_C/I_B$. For good DC performances, $\alpha \approx 1$ and β as large as possible are needed.

In the case of an HET, the high-frequency figures of merit, i.e., the cutoff frequency f_T and the maximum oscillation frequency f_{MAX}, can be expressed as follows:

$$f_T = \frac{1}{2\pi\left(\tau_d + \frac{C_{EB}+C_{BC}}{g_m}\right)} \quad (3)$$

$$f_{MAX} = \sqrt{\frac{f_T}{2\pi R_B C_{BC}}} \quad (4)$$

where τ_d is the total delay time associated with electrons' transit in the E-B barrier layer, in the base and in the B-C filtering layer, C_{EB} and C_{BC} are the capacitances of the two barriers, $g_m = dJ_C/dV_{BE}$ is the transconductance and R_B is the base resistance. Clearly, the most effective way to maximize f_T is the increase of g_m. In fact, a reduction of the barrier layer capacitances would imply an increase of the E-B and B-C barrier thicknesses, with a consequent impact on the transit delay times across these barriers. Under saturation conditions, when all the hot electrons injected from the emitter reach the collector ($J_C \approx J_E$), the transconductance $g_m \approx dJ_E/dV_{BE}$. As the emitter current is injected over a barrier, it exhibits an exponential dependence on V_{BE}, i.e., $J_E \propto \exp(qV_{BE}/kT)$. As a result, $g_m \propto qJ_E/kT$. This means that a high injection current density is one of the main requirements to achieve a high cut-off frequency f_T. The R_B term in Equation (4) is the resistance associated with "lateral" current transport in the base layer from the device active area to the base contact. Hence, R_B is the sum of different contributions, i.e., the "intrinsic" base resistance $R_{B\_int} \propto \rho/d_B$ (with ρ the base resistivity and d_B the base thickness), the resistance of the Ohmic metal contact with the base and the access resistance from this contact to the device active area. All these contributions should be minimized to achieve a low R_B. Of course, the most challenging issue to obtain high f_{MAX} is to fabricate an ultra-thin base (allowing ballistic transport of hot electrons in the vertical direction) while maintaining low enough intrinsic and extrinsic base resistances. However, for most of the bulk materials, reducing the film thickness to the nanometer or sub-nanometer range implies an increase of the resistivity, due to the dominance of surface roughness and/or grain boundaries' scattering, as well as to the presence of pinholes and other structural defects in the film.

Indeed, the HET device concept was introduced more than 50 years ago by Mead [87]. Since then, several material systems have been considered for HET implementation, including metal thin films [87–90], complex oxides [91], superconducting materials [92], III-V and III-nitride semiconductor heterostructures [93–97]. However, the successful demonstration of high-performance HETs has been limited by the difficulty to scale the base thickness below the electron mean free path of the carriers. In this context, 2D materials, in particular Gr and TMDs, can represent ideal candidates to fabricate the base of HETs, since they maintain excellent conduction properties and structural integrity down to single atomic layer thickness, allowing one to overcome the base scalability issue.

Theoretical studies have predicted that, with an optimized structure, f_T and f_{MAX} up to several terahertz [98], I_{on}/I_{off} over 10^5, high current and voltage gains can be achieved with a Gr-based HET (GBHET). The first experimental prototypes of GBHETs were reported by Vaziri et al. [22] and by Zeng et al. [23] in 2013. Those demonstrators were fabricated on Si wafers using a CMOS-compatible technology and were based on metal/insulator/Gr/SiO_2/n^+-Si stacks, where n^+-doped Si substrate worked as the emitter, a few nm thick SiO_2 as the E-B barrier, a thicker high-k insulator (Al_2O_3 or HfO_2) as the B-C barrier and the topmost metal layer as the collector. Figure 8a shows a schematic of the device structure, while Figure 8b illustrates the band diagrams in the OFF and ON states. The measured common-base output characteristics of this device are reported in Figure 8c, showing a collector current I_C nearly independent of V_{CB} and strongly dependent on V_{BE}.

In spite of the wide modulation of I_C as a function of V_{BE}, these first prototypes suffered from a high threshold voltage and a very poor injected current density (in the order of $\mu A/cm^2$) due to the high Si/SiO_2 barrier, hindering their application at high frequencies.

In order to improve the current injection efficiency, other materials have been investigated as E-B barrier layers in replacement of SiO_2 [99]. As an example, using a 6 nm-thick HfO_2 (including a 0.5-nm interfacial SiO_2) deposited by atomic layer deposition results in an improved threshold voltage and a higher injected current density. Further improvements have been obtained using a TmSiO/TiO_2 (1 nm/5 nm) bilayer, where the thin TmSiO layer (with low electron affinity) in contact with the Si emitter allows high current injection by step tunneling, while the thicker TiO_2 layer (with higher electron affinity) serves to block the leakage current from the Si valence band. For this GBHET

with a $TmSiO/TiO_2$ E-B barrier, a collector current density $J_C \approx 4$ A/cm^2 (more than five orders of magnitude higher than in the first prototypes) was obtained at $V_{BE} = 5$ V and for $V_{BC} = 0$. However, the device still suffers from low values of $\alpha \approx 0.28$ and $\beta \approx 0.4$, which can be due to the insufficient quality of the interface between Gr and the deposited B-C barrier.

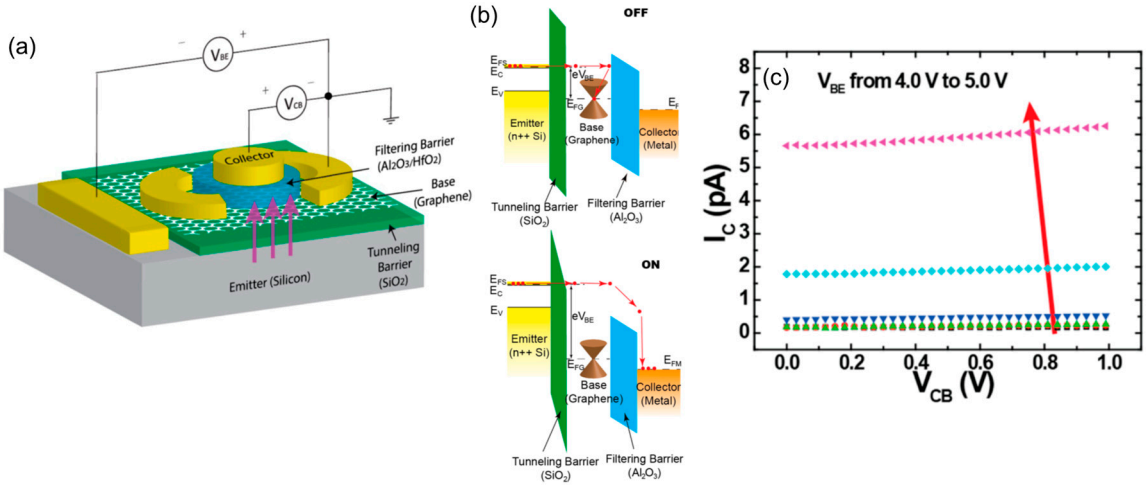

Figure 8. (**a**) Schematic illustration of a $Si/SiO_2/Gr/Al_2O_3/Ti$ Gr-based hot electron transistor (HET) (GBHET) biased in the common base configuration; (**b**) band diagrams in the OFF and in the ON state; and (**c**) output characteristics I_C-V_{CB} of the device. Figures adapted from [23].

Besides Gr, monolayer MoS_2 has been also considered as the base material. As an example, Torres et al. [25] demonstrated an HET device based on a stack of $ITO/HfO_2/MoS_2/SiO_2/n^+$-Si, where the n^+-doped Si substrate worked as the emitter, thermally-grown SiO_2 (3 nm) as the E-B tunneling barrier, a monolayer of CVD-grown MoS_2 as the base, the HfO_2 layer (55 nm thick) as the B-C barrier and the topmost ITO as the collector electrode. This device showed an improved value of $\alpha \approx 0.95$ with respect to the previously described Gr-base HET prototypes, mainly due to the lower conduction band offset between MoS_2 and HfO_2 (1.52 eV), with respect to the cases of Gr/HfO_2 (2.05 eV) and Gr/Al_2O_3 (3.3 eV). In spite of this, the collector current density of these devices was still poor (in the order of $\mu A/cm^2$), due to the high E-B barrier between Si and SiO_2.

The above discussed attempts to implement the GBHET device using Si as the emitter material have been mainly motivated by the perspective of integrating this new technology with the state-of-the-art CMOS fabrication platform. More recently, the possibility of demonstrating GBHETs by the integration of Gr with nitride semiconductors has been investigated. GaN/AlGaN or GaN/AlN heterostructures are excellent systems to be used as emitter/emitter-base barriers, due to the presence of high density 2DEG at the interface and to the high structural quality of the barrier layer. Thermionic emission has been demonstrated as the main current transport mechanisms in GaN/AlGaN/Gr systems with a thick (~20 nm) AlGaN barrier layer [100–102].Very efficient current injection by FN tunneling has been recently shown in the case of GaN/AlN/Gr heterojunctions with an ultra-thin (3 nm) AlN barrier [103].

Figure 9a,b illustrates a cross-sectional schematic and the band diagram of a recently-demonstrated GBHET based on a $GaN/AlN/Gr/WSe_2/Au$ stack [103]. The 3-nm AlN tunneling barrier was grown on top of a bulk GaN substrate (n^+-doped), working as the emitter. In order to circumvent the problems related to the poor interface quality between Gr and conventional insulators or semiconductors deposited on top of it, an exfoliated WSe_2 layer (forming a vdW heterojunction with Gr) was adopted as the B-C barrier layer. The resulting Gr/WSe_2 Schottky junction is characterized by a low barrier height due the small band offset (~0.54 eV) between Gr and WSe_2. Figure 9c shows the common-base output characteristics (I_C-V_{CB}) for different values of the emitter injection current I_E in the case of a GBHET with a 2.6 nm-thick WSe_2 barrier. Furthermore, Figure 9d plots the common-base current transfer ratio

$\alpha = I_C/I_E$ as a function of V_{CB} in the same bias range. Three current transport regimes can be identified in Figure 9c,d. At intermediate V_{CB} bias (Region II), I_C is almost independent of the V_{CB} and $\alpha \approx 1$, indicating that almost all the injected hot electrons are able to overcome the Gr/WSe_2 Schottky barrier and reach the collector. For $V_{CB} < 0$ (Region I), the injected electrons from the emitter are reflected back by the elevated B-C potential barrier, resulting in a reduced I_C and $\alpha < 1$. Finally, at higher positive V_{CB}, current starts to increase due to the increasing contribution of cold electrons' leakage current from the base. Although this device showed excellent DC characteristics in terms of α, its operating V_{BC} window was very limited (~0.3 V), due to the poor blocking capability of the B-C junction with an ultrathin WSe_2 barrier. Increasing the WSe_2 thickness improved the blocking capability of the B-C barrier, but resulted in a reduced value of α. As an example, $\alpha = 0.75$ was evaluated for a GaN/AlN/Gr/WSe_2/Au GBHET with a 10 nm-thick WSe_2 barrier [103].

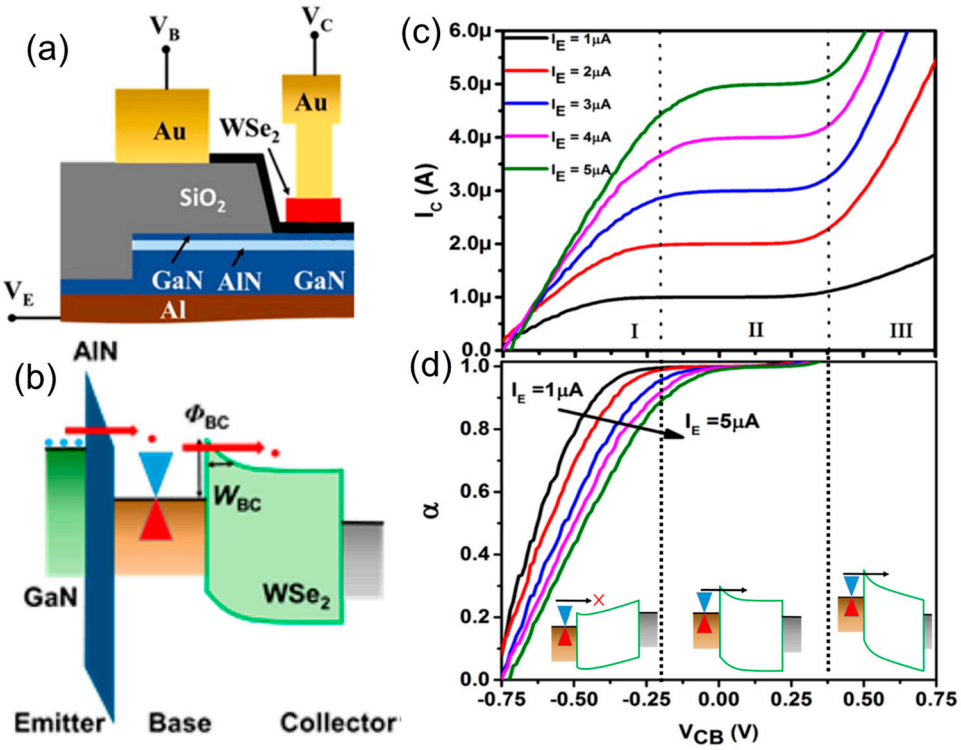

Figure 9. (**a**) Cross-section schematic and (**b**) band diagram of a GBHET based on the GaN/AlN/Gr/WSe_2/Au stack; (**c**) common-base output characteristics (I_C-V_{CB}) for different values of the emitter injection current I_E in the case of a GBHET with a 2.6 nm-thick WSe_2 barrier; (**d**) plots of $\alpha = I_C/I_E$ as a function of V_{CB} in the same bias range. Images adapted with permission from [103].

Table 1 reports a comparison of the main DC electrical parameters (i.e., the collector current density J_C, the common-base current transfer ratio α and the common-emitter current gain β) for the HETs with a Gr or MoS_2 base reported in the literature. Some examples of HETs fully based on nitride-semiconductors with a sub-10-nm base thickness are reported for comparison. In spite of the theoretically-predicted superior performances (related to ballistic transport in the atomically-thin Gr base), GBHETs still suffer from reduced values of J_C, α and β with respect to HETs fabricated by bandgap engineering of III-N semiconductors (even with a thicker GaN base). This reduced GBHET performance can be due to the non-ideal quality of Gr interfaces with the emitter and collector barriers, indicating that further work will be necessary in this direction.

Table 1. Comparison of J_C, α and β for the-state-of-the-art HETs with a Gr or MoS_2 base and for nitride semiconductor-based HETs with a sub-10-nm base thickness

Emitter/Emitter-Base Barrier	Base (Thickness)	Base-Collector Barrier	J_C (A/cm^2)	α	β	Reference
Si/SiO_2	Gr (0.35 nm)	Al_2O_3	~1×10^{-5}	~0.06	~0.06	[22]
Si/SiO_2	Gr (0.35 nm)	Al_2O_3, HfO_2	~5×10^{-5}	~0.44	~0.78	[23]
$Si/TmSiO/TiO_2$	Gr (0.35 nm)	Si	~4	~0.28	~0.4	[99]
GaN/AlN	Gr (0.35 nm)	WSe_2 (10 nm)	~50	~0.75	4–6	[103]
Si/SiO_2	MoS_2 (0.7 nm)	HfO_2	~1×10^{-6}	~0.95	~4	[25]
$GaN/Al_{0.24}Ga_{0.76}N$	GaN (10 nm)	$Al_{0.08}Ga_{0.92}N$	~5×10^3	~0.97		[95]
GaN/AlN	GaN/InGaN (7 nm)	GaN	~2.5×10^3	>0.5	>1	[97]
GaN/AlN	GaN (8 nm)	AlGaN/GaN	~46×10^3	~0.93	~14.5	[96]

4. Materials Science Issues and Challenges

The device structures reviewed in this paper are based on vdW heterostructures of 2D materials (Gr, TMDs, h-BN) [15] or on mixed-dimensional vdW heterostructures [17] formed by the integration of 2D materials with 3D semiconductors and insulators (bulk or thin films). In many cases, proof of concept devices have been fabricated by the transfer of the individual 2D components, obtained by mechanical or chemical exfoliation of flakes from layered bulk crystals. As a matter of fact, the large area growth method of electronic quality 2D materials and heterostructures are mandatory to move from proof-of-concept devices to industrial applications.

Nowadays, high quality Gr can be grown on a large area by CVD on catalytic metals, such as copper [42], followed by transfer to arbitrary substrates [104]. Although this is a very versatile and widely-used method, it suffers from some drawbacks related to Gr damage and polymer contaminations during the transfer procedure, as well as of possible adhesion problems between Gr and the substrate. Furthermore, it typically introduces undesired metal (Cu, Fe) contaminations [105] originating from the growth substrate and the typically used Cu etchants. An intense research activity is still in progress to optimize Gr transfer procedures to minimize Gr defectivity and contaminations associated with Gr manipulation [106–109].

Notwithstanding the above-mentioned issues, large area (cm^2) Gr heterojunctions with semiconductors are currently fabricated by optimized transfer of CVD-grown Gr. These have been used for the fabrication of device arrays using semiconductor fab-compatible approaches. As an example, Gr junctions with AlGaN/GaN heterostructures showing excellent lateral uniformity have been reported [100,110] and are currently investigated as building blocks for HET devices. Figure 10a,b reports two representative morphologies of the AlGaN surface without (a) and with (b) a single-layer Gr membrane on top. Figure 10c,d shows two arrays of local current-voltage characteristics measured by conductive atomic force microscopy (CAFM) at the different positions on bare AlGaN- and Gr-coated AlGaN, respectively. In both cases, all the I-V curves exhibit a rectifying behavior, with a lower Schottky barrier height for the Gr/AlGaN junction. Noteworthy, a very narrow spread between different curves is observed for the Gr/AlGaN junction, indicating an excellent lateral homogeneity of the Gr/AlGaN Schottky contact.

Under many respects, the direct growth/deposition of Gr on the target substrate would be highly desirable. However, to date, high quality Gr growth has been demonstrated only on a few semiconducting or semi-insulating materials, such as silicon-carbide [38–40,111,112] and, more recently, germanium [113]. Single or few layers of Gr can be obtained on the Si face (0001) of hexagonal SiC, either by controlled sublimation of Si at high temperatures (typically > 1650 °C) in Ar at atmospheric pressure or by direct CVD deposition at lower temperatures (~1450 °C) using an external carbon source (such as C_3H_8) with H_2 or H_2/Ar carrier gases [111]. Gr grown on SiC(0001), commonly named epitaxial graphene (EG), generally exhibits a precise epitaxial orientation with respect to the substrate, which originates from the peculiar nature of the interface, i.e., the presence of a carbon buffer layer with mixed sp^2/sp^3 hybridization sharing covalent bonds with the Si face of SiC [114,115]. This buffer layer has a strong impact both on the lateral (i.e., in plane) current transport in EG, causing a reduced carrier mobility, and on the vertical current transport at the EG/SiC interface [116,117].

Hydrogen intercalation at the interface between the buffer layer and Si face has been demonstrated to be efficient in increasing Gr carrier mobility and tuning the Schottky barrier and, hence, the vertical current transport across the Gr/SiC interface [118]. Recently, CVD growth of Gr from carbon precursors on nitride semiconductor (AlN) substrates/templates has been also investigated. Gr deposition on these non-catalytic surfaces represents a challenging task, as it requires significantly higher temperatures as compared to conventional deposition on metals. The first experimental works addressing this issue showed the possibility of depositing a few layers of Gr both on bulk AlN (Al and N face) and on AlN templates grown on different substrates, such as Si(111) and SiC, at temperatures >1250 °C using propane (C_3H_8) as the carbon source, without significantly degrading the morphology of AlN substrates/templates [119,120]. In spite of the very promising results of these experiments, further work will be required to evaluate the feasibility and the effects of CVD Gr growth onto AlN/GaN or AlGaN/GaN heterostructures. Moreover, the possibility of integrating these high temperature processes in the fabrication flow of GBHETs with the GaN/AlN (or GaN/AlGaN) emitter needs to be investigated.

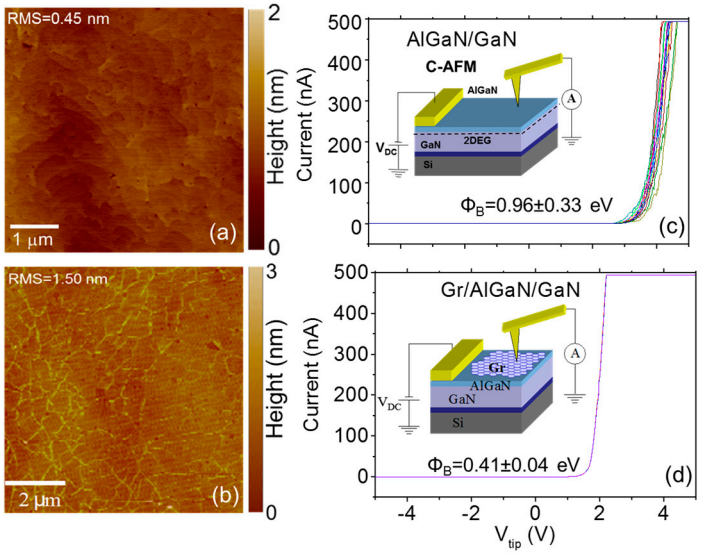

Figure 10. AFM morphologies of an AlGaN/GaN heterostructure (**a**) and of Gr transferred onto AlGaN/GaN (**b**). Current-voltage characteristics measured by conductive atomic force microscopy (CAFM) on an array of different positions on the bare AlGaN surface (**c**) and on the Gr-coated AlGaN surface (**d**). Figures adapted with permission from [100].

Although most of TMD-based devices are still fabricated using exfoliated flakes, much progress has been made in the last few years in the CVD deposition of MoS_2 and other TMDs, both on insulating substrates, such as SiO_2 [121,122] and sapphire [123], and on semiconductors, such as GaN [124]. Noteworthy, an epitaxial registry with the substrate has been observed for CVD-grown MoS_2 on sapphire and on GaN.

High quality thin insulating layers are key components for most of the above-discussed lateral and vertical devices based on Gr and TMDs. In this context, due to the layer-by-layer deposition mechanism, atomic layer deposition (ALD) has been considered as method of choice to grow thin high-k dielectrics (such as Al_2O_3 and HfO_2) on Gr and TMDs [125]. The main challenge related to ALD on the chemically inert and dangling-bonds' free surface of 2D materials is the activation of nucleation sites from which the growth can initiate. Several approaches have been explored so far to this aim, like ex situ deposition of metal or metal-oxide seed layers [126] or pre-functionalization of Gr [127]. Recently, highly uniform Al_2O_3 films with very low leakage current and a high breakdown field have been deposited on Gr by a two-step thermal ALD process, resulting in minimal degradation of the Gr electronic/structural properties [128]. As a matter of fact, the interface between Gr and TMDs with

common insulators is not atomically flat. Furthermore, interface or near-interface defects are typically present in the oxide and act as trapping states for electrons/holes.

In this respect, due to its atomically-flat crystal surface, excellent insulating properties and chemical inertness, h-BN represents an ideal ultra-flat substrate and interlayer dielectric for Gr (to which it is closely lattice matched, within 1.6%) and, by extension, other 2D semiconductor materials [3]. Although single and multilayer h-BN used for device demonstration are still mainly obtained by exfoliation from the bulk crystal, significant progress has been also made towards the controlled synthesis of large-area, high-quality h-BN films by CVD on metal catalysts, such as Ni [129], Cu [130] and Ni/Cu alloys [131]. Recently, Sonde et al. reported a detailed study clarifying the mechanisms of CVD h-BN growth on Ni and Co thin films on SiO_2/Si substrates [132], which could lead to large area (up to wafer scale) growth of h-BN thin films on arbitrary substrates in a transfer-free manner. As schematically illustrated in Figure 11a, after exposure to ammonia (NH_3) and diborane (B_2H_6) precursors at high temperature (~1050 °C), diffusion of boron (B) and nitrogen (N) in Ni occurs, followed by segregation/precipitation of h-BN multilayers both on the upper and the buried face of the Ni film. These h-BN films showed excellent insulating properties, with a breakdown field of 9.34 MV·cm^{-1}, as determined from current-voltage characteristics measured by CAFM (see Figure 11b). Finally, the quality of h-BN as a substrate for back-gated Gr field effect transistors has been evaluated. The Gr resistance measured under forward and backward gate bias sweep is reported in Figure 11c, showing minimal hysteresis associated with the absence of charge trapping at the Gr/h-BN interface.

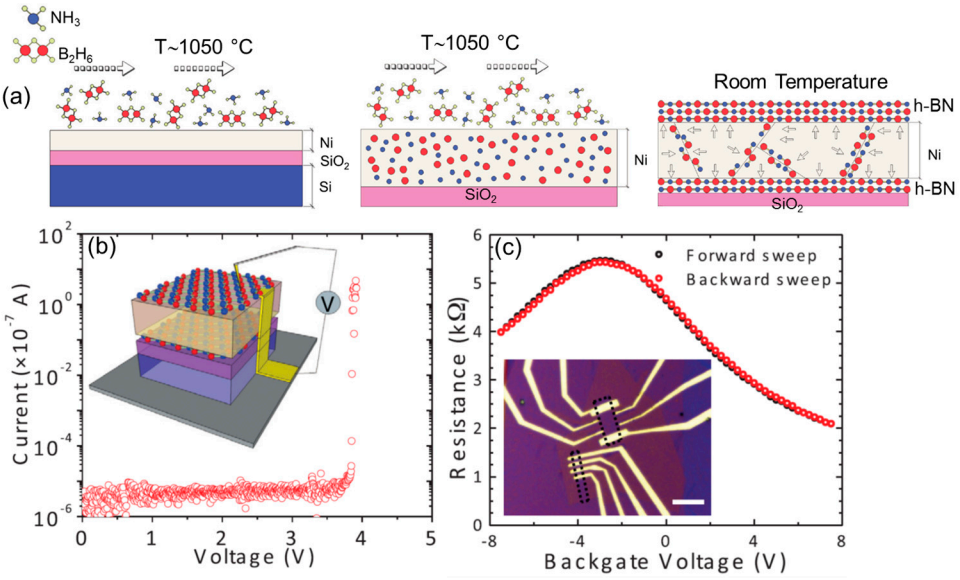

Figure 11. (**a**) Schematic illustration of the mechanism of h-BN CVD growth on Ni thin films by ammonia (NH_3) and diborane (B_2H_6) precursors at high temperature (~1050 °C); (**b**) estimation of the breakdown field (9.34 MV·cm^{-1}) of the multilayer h-BN (10–11 layers) by current-voltage measurements with CAFM; (**c**) resistance of a Gr field effect transistor with an h-BN back-gate, showing minimal hysteresis between forward and backward gate bias sweep. Figures adapted with permission from [132].

PMMA-assisted transfer is the simplest way to construct arbitrary 2D heterostructures. However, the quality of the interface can be affected by the trapping of polymer, solvents or chemicals used for transfer. This represents a major issue, especially for large-area 2D heterostructures. In this respect, the direct synthesis of vertically-stacked 2D heterojunctions, obtained by CVD growth of one 2D material on another, would be highly desirable, as the direct growth would result, in principle, in clean heterojunction interfaces. The early van der Waals epitaxy experiments started from Gr and h-BN, which share a similar lattice constant. Yang et al. reported a plasma-assisted deposition method for

the growth of single domain Gr on the h-BN substrate [133]. Gr grows with a preferred orientation with respect to the h-BN lattice, and the size of the domain is only restricted by the area of underlying h-BN. Furthermore, Shi et al. have obtained a vertically-stacked MoS_2/Gr heterostructure via thermal decomposition of ammonium thiomolybdate precursors on Gr surfaces [134]. In spite of the 28% mismatch between MoS_2 and Gr lattice constants, Gr is still a good growth platform for MoS_2, as the growth of MoS_2 on Gr involves strain to accommodate the lattice mismatch. Lin et al. demonstrated the direct growth of MoS_2, WSe_2 and h-BN on epitaxial Gr on SiC through CVD methods [135], showing how the morphology of the underlying Gr strongly affects the growth and the properties of top heterostructures. In particular, strain, wrinkling and defects on the surface of Gr provide the nucleation centers for the upper layer material growth.

5. Summary and Outlook

We have reviewed the state-of-the-art of 2D material-based vertical transistors for logic and high frequency electronics.

Regarding logic applications, vdW heterostructures obtained by 2D/2D or 2D/3D material stacking have been explored by several research groups as a platform to implement tunneling field effect transistors (TFETs). Resonant TFETs have been demonstrated by rotationally-aligned Gr monolayers or bilayers separated by a tunnel barrier (h-BN or TMD). However, although these prototypes permitted exploring interesting physical phenomena, the possibility of realizing vdW heterostructures with a precise crystallographic alignment on a large area represents a big challenge, making real applications of resonant TFETs in the near future difficult. On the other hand, TFETs relying on the band-to-band-tunneling across the interface of different semiconducting layered materials could have more realistic prospects of practical applications, once further progress in van der Waals epitaxy of TMDs is achieved.

Regarding high frequency applications of 2D materials, lateral Gr FETs with a very high cut-off frequency (f_T > 400 GHz) have been demonstrated, exploiting the high Gr channel mobility. However, these devices suffer from a lower maximum oscillation frequency f_{MAX}, due to the poor saturation of the output characteristics mainly originating from the missing bandgap of Gr. Vertical transistors based on 2D/2D or 2D/3D material heterostructures can represent an alternative to lateral Gr FETs to realize RF functions. In particular, the hot electrons transistor (HET) has been theoretically predicted to be suitable for ultra-high-frequency applications, with f_T and f_{MAX} values in the THz range. The main requirement for the implementation of this device concept, i.e., an ultrathin base allowing both ballistic transport in the vertical direction and low base resistance in the lateral direction, can be fulfilled by 2D materials, in particular Gr. However, although much progress has been made in the last few years in the fabrication of Gr-based HETs, the electrical performances of these demonstrators are still lower than those of previously-reported HET devices fabricated with III-V heterostructures (even with a thicker base) and far from the state-of-the-art RF HEMTs (which represent the benchmark for any competing RF device concept). Further improvements in the emitter-base and base-collector barrier layers and interfaces are still required to achieve the theoretical DC and RF performances of HETs.

Generally speaking, the perspective of industrial applications of 2D material-based devices is strongly related to the possibility of growing individual 2D layers and, possibly, vdW heterostructures on a large area.

Acknowledgments: The authors want to acknowledge all of the following colleagues for useful discussions and participation in the experiments: Gabriele Fisichella., Emanuela Schilirò, Salvatore Di Franco, Patrick Fiorenza, Raffaella Lo Nigro, Ioannis Deretzis, Antonino La Magna, Giuseppe Nicotra, Corrado Bongiorno, Corrado Spinella (CNR—Institute for Microelectronics and Microsystems (CNR-IMM), Catania, Italy); Sebastiano Ravesi, Stella Lo Verso, Ferdinando Iucolano (STMicroelectronics, Catania, Italy); Eric Frayssinet, Roy Dagher, Adrien Michon, Yvon Cordier (CNRS—Centre de Recherche sur l'Hétéro-Epitaxie et ses Applications (CNRS-CRHEA), Valbonne, France); Mike Leszczynski, Piotr Kruszewski, Pawel Prystawko (TopGaN, Warsaw, Poland); Rositza Yakimova, Anelia Kakanakova (Linkoping University, Linkoping, Sweden); Bela Pecz (Institute for Technical Physics and Materials Science Research, Centre for Energy Research, Hungarian Academy of Science,

Budapest, Hungary); and Luigi Colombo (Texas Instruments, Texas, TX, USA). This paper has been supported, in part, by the Flag-ERA project "GraNitE: Graphene heterostructures with Nitrides for high frequency Electronics".

Conflicts of Interest: The authors declare no conflict of interest.

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