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*Article*

# Optimization of Fluorine Plasma Treatment for Interface Improvement on $HfO_2/In_{0.53}Ga_{0.47}As$ MOSFETs

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**Abstract:** This paper reports significant improvements in the electrical performance of $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistors (MOSFET) by a post-gate $CF_4/O_2$ plasma treatment. The optimum condition of $CF_4/O_2$ plasma treatment has been systematically studied and found to be 30 W for 3–5 min. Approximately 5× reduction in interface trap density from $2.8 \times 10^{12}$ to $4.9 \times 10^{11}$ $cm^{-2}eV^{-1}$ has been demonstrated with fluorine (F) incorporation. Subthreshold swing has been improved from 127 to 109 mV/dec. Effective channel mobility has been enhanced from 826 to 1,144 $cm^2/Vs$.

**Keywords:** InGaAs; $HfO_2$; fluorine plasma treatment; high-k dielectrics

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## 1. Introduction

$In_{0.53}Ga_{0.47}As$ based-III-V compounds have attracted a great deal of attention for their advantages in high electron mobility over their Si-based counterparts. However, poor interface quality between $In_{0.53}Ga_{0.47}As$ and high dielectric constant (high-k) gate dielectrics has imposed an enormous challenge for implementing inversion-type enhancement mode metal-oxide-semiconductor field-effect transistors (MOSFETs). Proper surface pre-treatment and insertion of interface passivation layer [1–3] have generally employed to achieve improved interface quality. Those approaches usually performed prior to high-k deposition, however, interface state traps created during the high-k deposition need to be passivated by a post-oxide treatment.

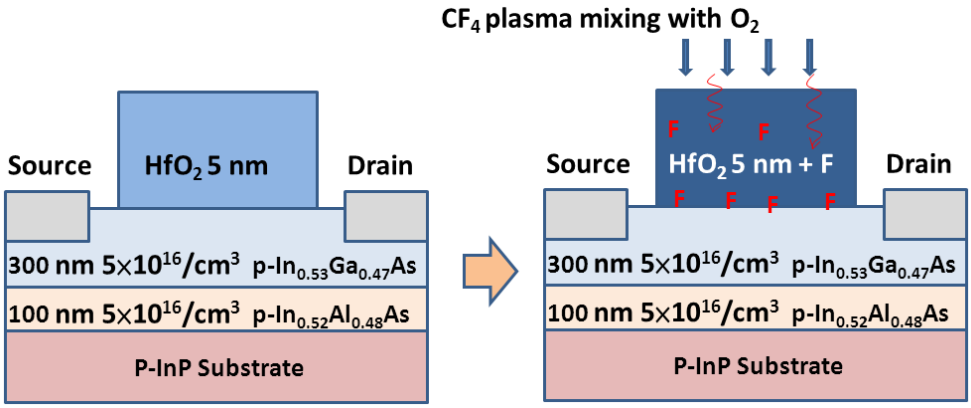
It can be expected that fluorine (F) will be an effective passivation agent for $In_{0.53}Ga_{0.47}As$ because F has high binding energy with In (5.25 eV), Ga (5.99 eV), and As (4.26 eV), respectively [4]. F incorporation has been demonstrated on Si, Ge, and $In_{0.53}Ga_{0.47}As$ substrates. It has been found that F can passivate high-k bulk traps and interface defects at high-k/substrates (Si, Ge and $In_{0.53}Ga_{0.47}As$) interface [5–9]. Although previous reports showed that the insertion of a thin interface passivation layer could improve interface quality [10], those layers usually have relative lower k value [11]. This may hinder equivalent oxide thickness (EOT) scaling and as a result, hardly meet the requirement for the sub 22 nm nodes.

In this paper, we systematically studied the effects of $CF_4/O_2$ plasma power wattage and treatment time on $HfO_2/In_{0.53}Ga_{0.47}As$ gate stack. The condition of $CF_4/O_2$ plasma has been optimized, which significantly improves the effective channel mobility ($\mu_{eff}$), transconductance ($G_m$), drive current ($I_d$), and subthreshold swing (SS). With F incorporation, we have successfully developed excellent interface quality of $HfO_2$ directly on $In_{0.53}Ga_{0.47}As$ without using interface passivation layer. Fluorinated samples exhibit low interface trap density ($D_{it}$) of $4.9 \times 10^{11}$ $cm^{-2}eV^{-1}$, which is the lowest value compared to prior reported $HfO_2/In_{0.53}Ga_{0.47}As$ gate stacks.

## 2. Experimental Section

Figure 1 shows the device structure and the illustration of F incorporation. The wafers used in our study were molecular beam epitaxy grown by a vender. P-type (Zn-doped, $3 \times 10^{18}/cm^3$) InP wafers were the starting substrates. P-type (Be-doped, $5 \times 10^{16}/cm^3$) $In_{0.52}Al_{0.48}As$ of 100 nm thick was grown as a buffer layer, followed by a 300 nm p-type $In_{0.53}Ga_{0.47}As$ layer (Be-doped, $5 \times 10^{16}/cm^3$), which was used as the channel layer. The native oxides were removed with 1% diluted HF solution, followed by 20% $(NH_4)_2S$ solution for sulfur passivation. To protect gate stack from the source and drain (S/D) activation annealing, the gate-last process was adopted: A 10-nm-thick atomic-layer-deposited (ALD) $Al_2O_3$ was deposited at a substrate temperature of 200 °C as an encapsulation layer. S/D regions were selectively implanted with a Si dose of $2 \times 10^{14}/cm^2$ at 35 keV. The S/D activation annealing was performed in nitrogen ambient at 700 °C/10 s. The encapsulation layer was then removed using buffered oxide etch solution. A 5 nm-thick ALD $HfO_2$ film was deposited after the same surface preparation (HF and $(NH_4)_2S$). Some samples were treated *ex situ* with $CF_4$ plasma with varied RF wattages and treatment times. A mixed flow of $CF_4$ and $O_2$ gas (ratio ~10:1) was introduced into the chamber with pressure of 100 mTorr. The purpose of $O_2$ flow was to avoid carbon contamination. Control samples without $CF_4/O_2$ plasma treatment were also fabricated as references. Post-deposition annealing was then performed for all the samples at 500 °C for 60 s in a nitrogen ambient. Subsequently, a 200 nm TaN was sputtered and patterned as gate electrode. AuGe/Ni/Au alloy was deposited by E-beam evaporation and a liftoff process to form S/D Ohmic contacts; backside contact was made by E-beam evaporation of Cr/Au, followed by annealing at 400 °C for 30 s in nitrogen ambient.

**Figure 1.** The device cross-sectional structure of $HfO_2/In_{0.53}Ga_{0.47}As$ gate stack. Samples were treated in a mixed flow of $CF_4$ and $O_2$ gas (ratio ~10:1) with varied RF power and treatment time.




Figures 2 and 3 show the X-ray photoelectron spectroscopy (XPS) spectra of Hf 4*f* and F *1s* for the $HfO_2/In_{0.53}Ga_{0.47}As$ gate stack with and without $CF_4/O_2$ plasma treatment. All the scanned binding energy was calibrated by the C 1*s* signal at 284.5 eV.

**Figure 2.** X-ray photoelectron spectroscopy (XPS) analysis of the Hf 4*f* electronic spectra for the samples with and without fluorine (F) incorporation.

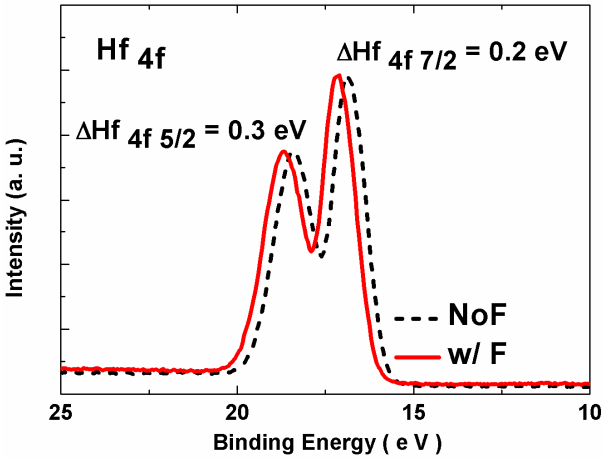
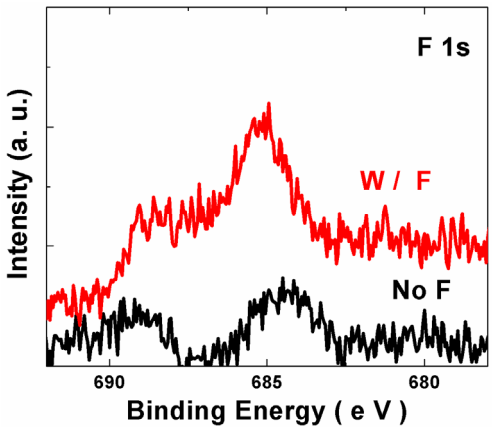


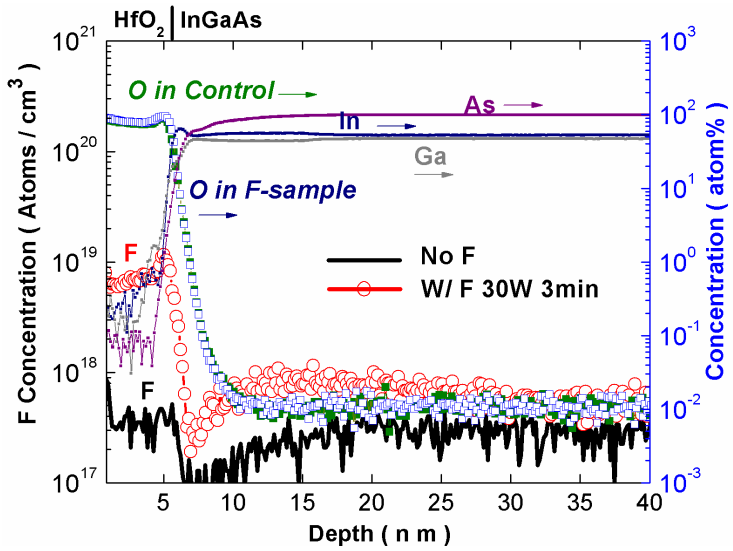

**Figure 3.** XPS analysis of the F 1*s* electronic spectra for the control sample and fluorinated sample.



Compared to the control sample, the fluorinated sample has an increased binding energy by 0.2 eV and 0.3 eV for the Hf $4f_{7/2}$ and Hf $4f_{5/2}$ signal, respectively. This suggests that parts of the oxygen vacancies were terminated by the incorporated F atoms to form stronger Hf-F bonds with higher binding energy. In Figure 3, the peak signal located at ~685 eV corresponds to the F bonds in the bulk $HfO_2$, indicating that F was incorporated into the $HfO_2$ after $CF_4/O_2$ plasma treatment.

In order to search the F distribution in the $HfO_2/In_{0.53}Ga_{0.47}As$ gate stack, the secondary ion mass spectrometry (SIMS) technique was examined, as shown in Figure 4. A considerable amount of F was incorporated into the $HfO_2$ gate stacks with $CF_4/O_2$ plasma treatment while the oxygen concentration remained similar. Due to sudden structural transition at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface, the density of defective bonds at the interface is much higher than that in the $HfO_2$ bulk. F tends to pile up at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface passivating interface traps, resulting in a better interface quality (discussed later in this paper).

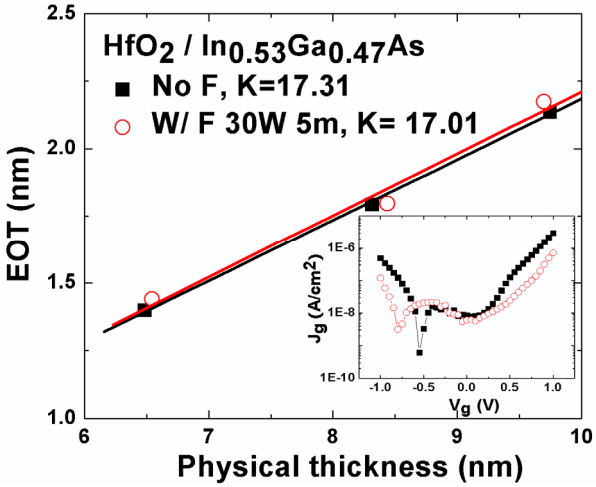
**Figure 4.** Secondary ion mass spectrometry (SIMS) profile of elements in the $HfO_2/In_{0.53}Ga_{0.47}As$ gate stack with and without $CF_4/O_2$ plasma treatment. The $CF_4/O_2$ plasma condition is 30 W for 3 min.




The composition and stoichiometry of $HfO_2$ were determined by XPS analysis (data not shown). For the control sample, $HfO_2$ was in good stoichiometry (Hf:O = 1:2) and it became oxygen-rich ($HfO_{2.25}$) after $CF_4/O_2$ plasma treatment. One possibility of improvements could be due to the oxygen vacancies passivation during the plasma treatment. The effect of $O_2$ plasma treatment is under investigation.

One concern of doping F into gate oxide is that dielectric constant of the gate oxide would decrease with heavy F incorporation. From XPS, the F concentration in our fluorinated $HfO_2$ is estimated to be 2.7 at.%, which is lower than that used in the low-k technology [12]. Therefore, the dielectric constant of $HfO_2$ remains similar (~17) after F incorporation, as shown in Figure 5. The inset of Figure 5 compares the gate leakage current of samples with and without F incorporation. The gate leakage current is slightly reduced with F incorporation.

**Figure 5.** Equivalent oxide thickness (EOT) *versus* physical thickness for the samples with and without F incorporation. Inset: the gate leakage current comparison of samples with and without F incorporation.




One objective of this work is to investigate the optimum condition of $CF_4/O_2$ plasma. The RF power and the plasma treatment time are two critical factors that affect the electrical characteristics significantly. Insufficient plasma treatment might not improve the gate dielectric quality, whereas excessive plasma treatment possibly causes plasma damage and corrodes the improvement. To study the effects of RF power on $HfO_2$ gate dielectrics, some samples were treated in $CF_4/O_2$ plasma for 3 min at different RF power in the range from 20 to 40 W. It was found that the samples treated by the power of 30 W improved most in terms of $G_m$, $I_d$ and SS. With the fixed RF power of 30 W, we continued to study the effect of $CF_4/O_2$ plasma treatment time. Some samples were treated in $CF_4/O_2$ plasma at different treatment times ranging from 1 to 7 min with a fixed RF power of 30 W. It was found that 5 min plasma treatment further improved SS.

## 3. Results and Discussion

### *3.1. Optimization of $CF_4/O_2$ Plasma*

The maximum $G_m$ and $I_d$ as a function of different RF power ($CF_4/O_2$ plasma treatment time: 3 min) are shown in Figure 6 (W/L = 600/20 μm, at $V_d$ = 50 mV and 0.5 V). The maximum $G_m$ and $I_d$ of the control sample are 3.1 mS/mm and 1.3 mA/mm ($V_d$ = 50 mV), and 20.3 mS/mm and 12 mA/mm ($V_d$ = 0.5 V), respectively. With F plasma treatment of 30W, the maximum $G_m$ and $I_d$ reach 3.7 mS/mm and 1.7 mA/mm ($V_d$ = 50 mV), and 26 mS/mm and 16.2 mA/mm ($V_d$ = 0.5 V), respectively. However, the maximum $G_m$ and $I_d$ roll back with power larger than 30 W indicative of possible plasma damage. SS data with different RF power are shown in Figure 7. $In_{0.53}Ga_{0.47}As$ MOSFETs have similar EOT (~1.4 nm, data not shown) with different RF power treatment. With F incorporation, SS has been improved from 127 to 118.1 mV/dec (as shown in the inset of Figure 7), which suggests that the interface quality has been improved. For the RF power of 40W, SS increases to 127.5 mV/dec, indicating that excessive $CF_4/O_2$ plasma treatment degrades the interface quality.

**Figure 6.** Maximum $G_m$ and $I_d$ as a function of $CF_4/O_2$ plasma RF power (W/L = 600 μm/20 μm at $V_d$ = 50 mV and 0.5 V). $CF_4/O_2$ plasma treatment time: 3 min.

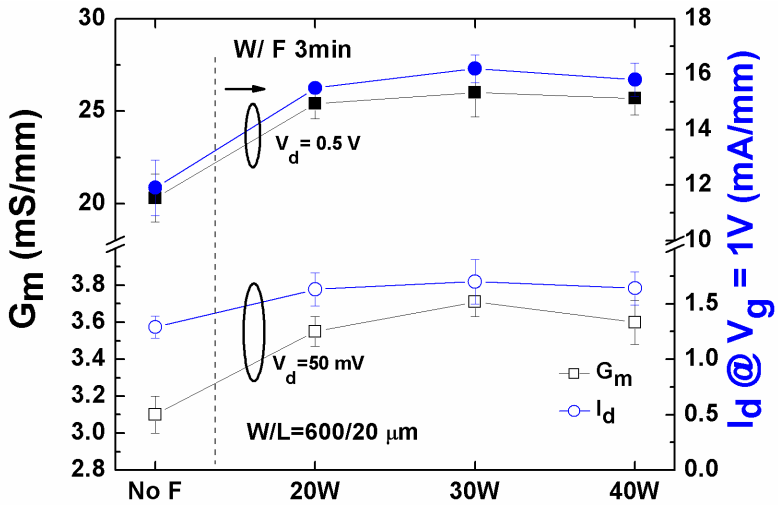



**Figure 7.** Subthreshold swing (SS) as a function of $CF_4/O_2$ plasma RF power. $CF_4/O_2$ plasma treatment time: 3 min. Inset: $I_d$-$V_g$ comparison of the control sample and the sample with $CF_4/O_2$ plasma treatment for 30 W/3 min.

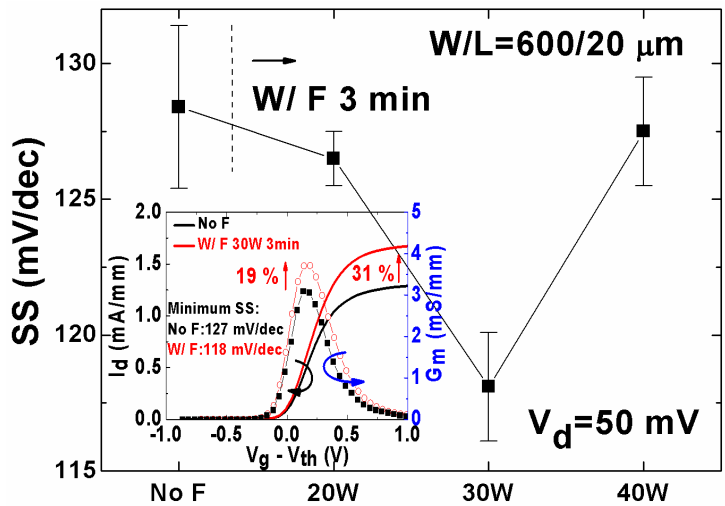



Figure 8 compares the maximum $G_m$ and $I_d$ as a function of plasma treatment times ranging from 1 to 7 min with a fixed RF power of 30W (W/L = 600 μm/20 μm at $V_d$ = 50 mV and 0.5 V). 3 min plasma treatment reaches the peak values of the maximum $G_m$ and $I_d$, whereas 5 min plasma treatment achieves the lowest SS value (Figure 9). The inset of Figure 8 compares the $I_d$-$V_g$ curves (in log-linear scale) of the control sample and the sample with F treatment 30 W/5 min. A steeper SS slope is clearly observed.

**Figure 8.** Maximum $G_m$ and $I_d$ as a function of $CF_4/O_2$ plasma treatment time (W/L = 600 μm/20 μm at $V_d$ = 50 mV and 0.5 V). RF power: 30 W.

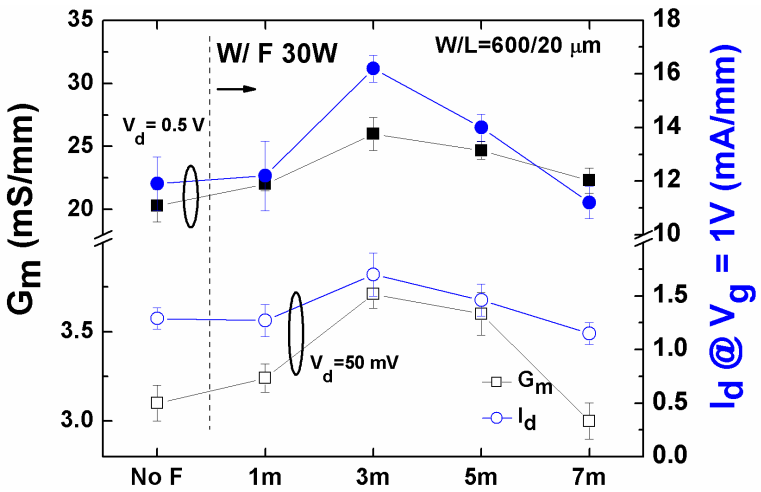
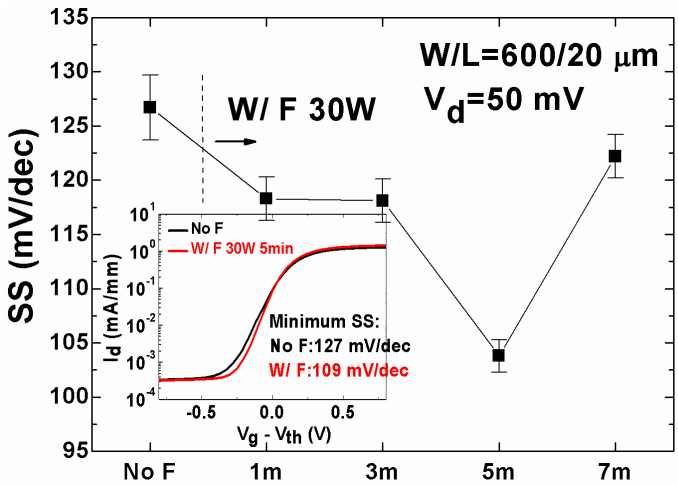
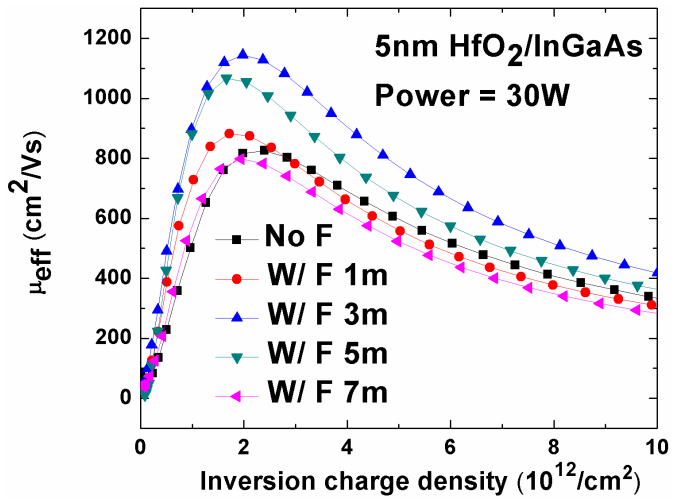



**Figure 9.** SS as a function of $CF_4/O_2$ plasma treatment time. RF power: 30 W. Inset: $I_d$-$V_g$ comparison of the control sample and the sample with $CF_4$ plasma treatment for 30 W/5 min.




Effective channel mobility ($\mu_{eff}$) of $In_{0.53}Ga_{0.47}As$ MOSFETs with different plasma treatment times are plotted in Figure 10. The peak $\mu_{eff}$ of 30 W/3 min reaches 1,144 $cm^2/Vs$, which is 38% improvement compared to the control samples (826 $cm^2/Vs$). The improvements in the $I_d$, $G_m$, SS and $\mu_{eff}$ are believed to be due to the improved interface quality by an appropriate amount of $CF_4/O_2$ plasma post-$HfO_2$ treatment.

**Figure 10.** Effective channel mobility *versus* inversion charge density as a function of $CF_4/O_2$ plasma treatment time. RF power: 30 W.




We noticed that the plasma damage occurred if excessive plasma (either plasma wattage or treatment time) was applied. The plasma damage could come from disordering, surface roughening, and fluorine contamination [13]. The disordering layer contains dangling bonds and broken bonds, which would scatter the electrons underneath (in the channel) and lower the electron mobility. Severe disordering would lead to surface roughness, which results in more dangling bonds and broken bonds. If the F concentration is too high (>5 at.%, [12]), the dielectric constant of $HfO_2$ decreases, resulting in lowering drive current.

### *3.2. Electrical Characterization of the Interface Trap Density*

Charge pumping measurements were conducted to accurately evaluate the interface quality of the control and fluorinated MOSFETs. The charge pumping characterization was performed by sweeping the base level voltage ($V_{base}$, −2.3 V to 1 V in a step of 50 mV) of the trapezoidal gate pulse (with a constant-amplitude, 1 V) at 200 KHz. The S/D terminals were grounded. The region of the bandgap probed was from electron emission energy level to hole emission energy level, which was around the midgap. The charge pumping current ($I_{cp}$) is plotted as a function of $V_{base}$ for equal trapezoidal pulse rise time ($t_R$) and fall time ($t_F$), as shown in Figure 11. $t_R$ and $t_F$ are varied from 100 to 800 ns. Lower $I_{cp}$ for the fluorinated sample is indicative of reduced $D_{it}$. The mean $D_{it}$ value can be extracted according to the following equation [14,15],

$$\frac{I_{cp}}{f} = 2qD_{it}AkT\left\{\ln\sqrt{t_R t_F} + \ln\left(\frac{|V_{fb}-V_t|}{|\Delta V_g|}V_{th}n_i\sqrt{\sigma_n\sigma_p}\right)\right\}$$

where $q$ is the electronic charge, $A$ is the transistor gate area ($2.08 \times 10^{-4}$ cm$^2$ in our devices), $k$ is the Boltzmann constant, $V_{fb}$ is the flat band voltage, $V_t$ is the threshold voltage, $\Delta V_g$ is the gate pulse amplitude, $V_{th}$ is the thermal velocity of the carriers, $n_i$ is the surface concentration of minority carriers, and $\sigma_n$ and $\sigma_p$ are the capture cross sections of electrons and holes, respectively. The mean $D_{it}$ values were extracted from the slope of $I_{cp}/f$ *versus* $\ln[(t_R \times t_F)^{1/2}]$, as shown in Figure 12. It has been found that the mean $D_{it}$ value was reduced ~5× from $2.8 \times 10^{12}$ to $4.9 \times 10^{11}$ cm$^{-2}$eV$^{-1}$ after F plasma

treatment. F atoms possibly passivate dangling bonds and oxygen vacancies in the $HfO_2/In_{0.53}Ga_{0.47}As$ interface and thereby reduce $D_{it}$ value.

**Figure 11.** Charge pumping measurement with rise/fall time dependence. Samples with F incorporation show much smaller $I_{cp}$. $V_{base}$: −2.3 V to 1 V in a step of 50 mV and the pulse amplitude is 1 V.

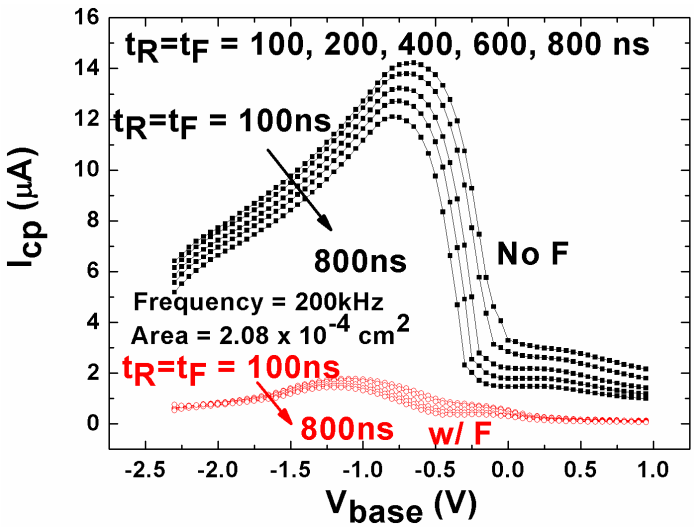



**Figure 12.** $Q_{cp}$ (=$I_{cp}$/f) *vs*. $\ln[(t_R \times t_F)^{1/2}]$. The mean $D_{it}$ value is extracted by linear fitting according to References [14,15]. Samples with F incorporation show less $D_{it}$ value of $4.9 \times 10^{11}$/eVcm$^2$.

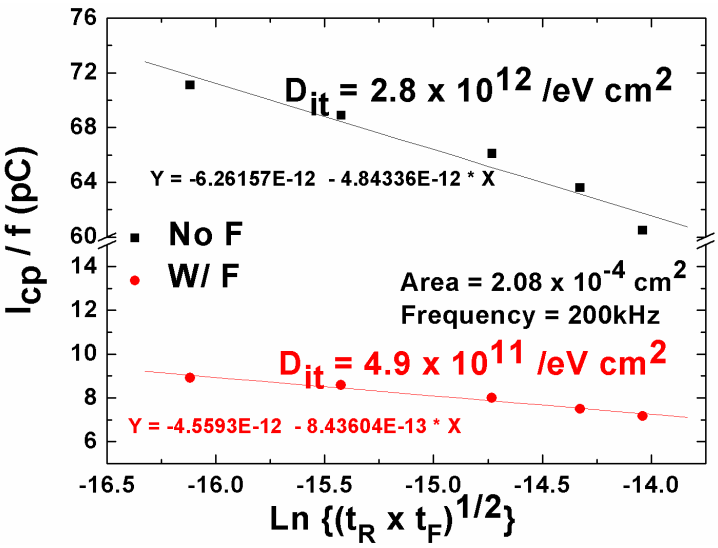



Table 1 compares the device performance and interfacial properties of $In_{0.53}Ga_{0.47}As$ MOSFETs reported in this paper and other high-k/$In_{0.53}Ga_{0.47}As$ gate stacks in recent publications. The $D_{it}$ value reported in this paper is the lowest value compared to prior reported $HfO_2/In_{0.53}Ga_{0.47}As$ gate stacks.

**Table 1.** Comparison of the electrical and interfacial properties of this work with some recently reported paper.

| High k | Passivation method | Channel material | $L_G$ | EOT or thickness of high-k | $D_{it}$ ($cm^{-2}eV^{-1}$) | SS (mV/dec) | Ref. |
|---|---|---|---|---|---|---|---|
| $Al_2O_3$ * | - | $In_{0.53}Ga_{0.47}As$ | - | 4.2 nm | $5 \times 10^{11}$ | - | [16] |
| $Al_2O_3$ | - | $In_{0.53}Ga_{0.47}As$ | - | 10 nm of $Al_2O_3$ | $2.5 \times 10^{11}$ | - | [17] |
| $Al_2O_3$ | - | $In_{0.53}Ga_{0.47}As$ | 1.5 μm | 8 nm of $Al_2O_3$ | $1 \times 10^{12}$ | >200 | [18] |
| $Al_2O_3$ | - | $In_{0.53}Ga_{0.47}As$ | 0.5 μm | 30 nm of $Al_2O_3$ | $1.4 \times 10^{12}$ | 240 | [19] |
| $HfO_2$ * | - | $In_{0.53}Ga_{0.47}As$ | - | 2.1 nm | $1 \times 10^{12}$ | - | [16] |
| $HfO_2$ * | - | $In_{0.53}Ga_{0.47}As$ | - | 7.8 nm of $HfO_2$ | $2 \times 10^{12}$ | - | [20] |
| $HfO_2$ * | Al-doped | $In_{0.53}Ga_{0.47}As$ | - | 8–9 nm of $HfO_2$ | $6 \times 10^{12}$ | - | [21] |
| $HfO_2$ * | $PH_3$ | $In_{0.53}Ga_{0.47}As$ | 4 μm | 1.7 nm | $8.6 \times 10^{11}$ | 103 | [22] |
| HfAlO | $SiH_4$+$NH_3$ | $In_{0.53}Ga_{0.47}As$ | 2–10 μm | 3.8 nm | $6.5 \times 10^{11}$ | 155–210 | [2] |
| $ZrO_2$ | $LaAlO_3$ | $In_{0.53}Ga_{0.47}As$ | 5 μm | 1.63 nm | $7.5 \times 10^{11}$ | 116 | [23] |
| $HfO_2$ | $CF_4/O_2$ post treatment | $In_{0.53}Ga_{0.47}As$ | 5–20 μm | 1.4 nm | $4.9 \times 10^{11}$ | 109 | This work |
| $HfO_2$ | Control | | | 1.35 nm | $2.8 \times 10^{12}$ | 127 | This work |

* Capacitor structure.

## 4. Conclusions

The effects of post-oxide $CF_4/O_2$ treatment on $HfO_2/In_{0.53}Ga_{0.47}As$ gate stack have been systematically investigated. The condition for the $CF_4/O_2$ plasma is optimized to be 30 W for 3–5 min. The gate stack interface quality has been notably improved by F incorporation. The mean $D_{it}$ value has been reduced ~5× from $2.8 \times 10^{12}$ to $4.9 \times 10^{11}$ $cm^{-2}eV^{-1}$. As a result, enhanced electrical performances have been presented: steeper SS from 127 to 109 mV/dec, enhanced $\mu_{eff}$ from 826 to 1,144 $cm^2/Vs$, and improved $G_m$ and $I_d$ from 3.1 to 3.7 mS/mm and from 1.3 to 1.7 mA/mm, respectively (at $V_d$ = 50 mV, 20 μm channel length). These results suggest that the post-$HfO_2$ F treatment could be a key technique to implement high performance III-V MOSFETs for the sub 22 nm nodes.

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