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Capacitive Power Transfer System with Reduced Voltage Stress and Sensitivity

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Featured Application: In this paper, we introduce a wireless power transfer system based on electric field coupling (capacitive coupling) with less voltage across the coupling interface and circuit quality factor by using a DC–DC converter, which resulted in a safer and less sensitive system while maintaining sufficient delivered power and high efficiency. The introduced system has a wide application range with different power needs and transmission distances, such as charging mobile devices including mobile phones, pads, laptops, drones, cameras, and wireless sensors. The system use can also be extended to supplying power to robots, smart walls, screens, lighting, indicative signs, and oil and gas applications.

Abstract: This paper introduces a DC–DC buck converter on the secondary side of the capacitive power transfer system to reduce the voltage and electric field across the interface, and to reduce the circuit Q , and thus the system sensitivity. The system is mathematically analyzed to study the improvement in sensitivity and voltage stress. The leakage electric field emissions around the plates are investigated by simulation. The analytical and simulation results show that by reducing the duty cycle of the buck converter at a constant output power, the voltage across the plates can be significantly reduced and the circuit becomes less sensitive to the variations in parameters. Experimental results demonstrated that Q and the voltage stress over the capacitive interface are reduced by changing the duty cycle of the buck converter. For delivering 10 W of power, the maximum voltage stress across one pair of the coupling plates is reduced from 211 V in the conventional system without using a DC–DC converter, to 65 V and 44 V at duty cycles of 30% and 20%, respectively. The system achieves an end-to-end power efficiency of 80% at an output power of 10 W and a duty cycle of 30%.

Keywords: capacitive wireless power transfer; DC–DC buck converter; quality factor; voltage stress; wireless power transmission

1. Introduction

Since the 1890s, efforts have focused on the wireless transfer of power [1], and the most successful approach has been inductive power transfer (IPT), which is based on magnetic field coupling. Inductive power transfer has been widely used for powering industrial machines [2,3], charging mobile devices [2,4] and electric vehicles [5,6], and powering biomedical implants [7]. However, IPT has clear limitations with regard to high eddy current losses to the surroundings especially with metals, high standing losses, and complicated design, requiring bulky and expensive magnetic materials and electromagnetic interference (EMI) shielding [8,9]. Also, given its nature, IPT is unable to transfer power across metal barriers. Capacitive power transfer (CPT), a technology that uses a

varying electric field to transfer power, has been introduced as a good alternative to IPT for near field power transfer due to its unique features, such as design flexibility of coupling structure, ability to transfer power across electrically isolated metal barriers, low standing losses and EMI, and low cost and weight [10–14]. Capacitive power transfer can be used in various applications, such as integrated circuits (IC) [15], biomedical devices [16], consumer electronics [11,12,17–19], and electric vehicles (EVs) [20].

The conventional CPT system is illustrated in Figure 1, where the capacitive interface is typically in the range of hundreds of picofarads (pF) when the plates are almost touching with an insulation layer in between and 1–2 mm air gap, and few tens of picofarads when there is a wide air gap, e.g., 150 mm to 300 mm air gap is usually considered for EV charging applications [21]. This results in a high-quality factor and voltage stress across the capacitive interface. For example, if the operating frequency f is 1 MHz, the load resistance R_L is 12.3 Ω , the capacitive interface $C_{c1} = C_{c2} = 2C_c = 1$ nF and the tuning inductor L is 50.7 μ H, which provides the quality factor [22] Q_{conv} of $8/\pi^2 R_L (\text{sqrt}(L/C_c)) \cong 32$ and provides the maximum voltage stress across the single pair of the capacitive interface V_{c_conv} of 320 V for an AC input voltage V_{in_conv} of just 20 V. Consequently, practically attaining tuning is challenging, and the system is highly sensitive to coupling variation and load change. The high voltage stress across the coupling interface increases the probability of dielectric breakdown and sparks occurrence. In addition, system safety becomes an issue as the related leakage electric field emissions around the plates increase beyond the safety margins as will be detailed in Section 4. These matters result in lower efficiency, decreased ability to deliver power, and increased difficulty in offering commercially accepted systems.

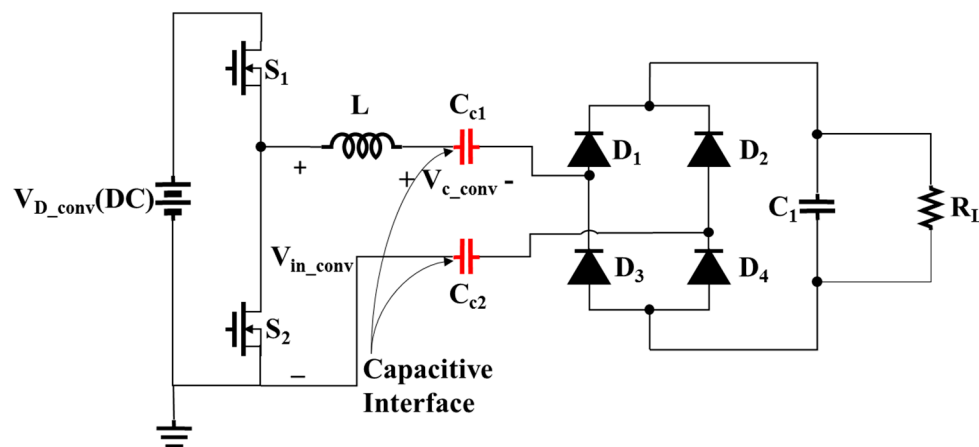


Figure 1. The conventional capacitive power transfer (CPT) system.

Previous studies introduced a partial solution for the previously mentioned issues [10,21,23–25]; however, no comprehensive design overcomes both issues simultaneously. For instance, one pulse switching active capacitor (OPSAC) was proposed to overcome the sensitivity issue [24]; however, the system is complicated and the voltage stress across the coupling interface is high. Tuning the operating frequency [25] is an effective method to mitigate the sensitivity issue and even with a high-quality factor, the system can still transfer the power with high efficiency, but by changing the frequency, following the regulations becomes challenging and the design is complex, costly, and cannot avoid the high voltage stress.

In this paper, a CPT system with a DC–DC buck converter on the secondary side is introduced to simultaneously reduce the system sensitivity and the voltage stress across the capacitive interface. The proposed system can also keep the leakage electric field low, which improves the safety of CPT systems.

The rest of the paper is arranged as follows. Section 2 describes the structure of the proposed CPT system. The mathematical model and analysis are covered in Section 3. In Section 4, the leakage electric field simulation is outlined. A prototype is implemented for evaluation in Section 5. The conclusions are drawn in Section 6.

2. Proposed System Structure

The structure of the proposed CPT system is shown in Figure 2a. Switches (S_1 – S_2) construct a half-bridge inverter (full bridge can be used) to convert DC input voltage (V_D) into an AC signal. Inductor L is placed in series to compensate for the capacitive interface, where C_{c1} and C_{c2} represent the capacitive coupling interface. Diodes (D_1 – D_4) construct the full wave rectifier to obtain DC voltage. The DC–DC buck converter supplies the voltage and current to the load.

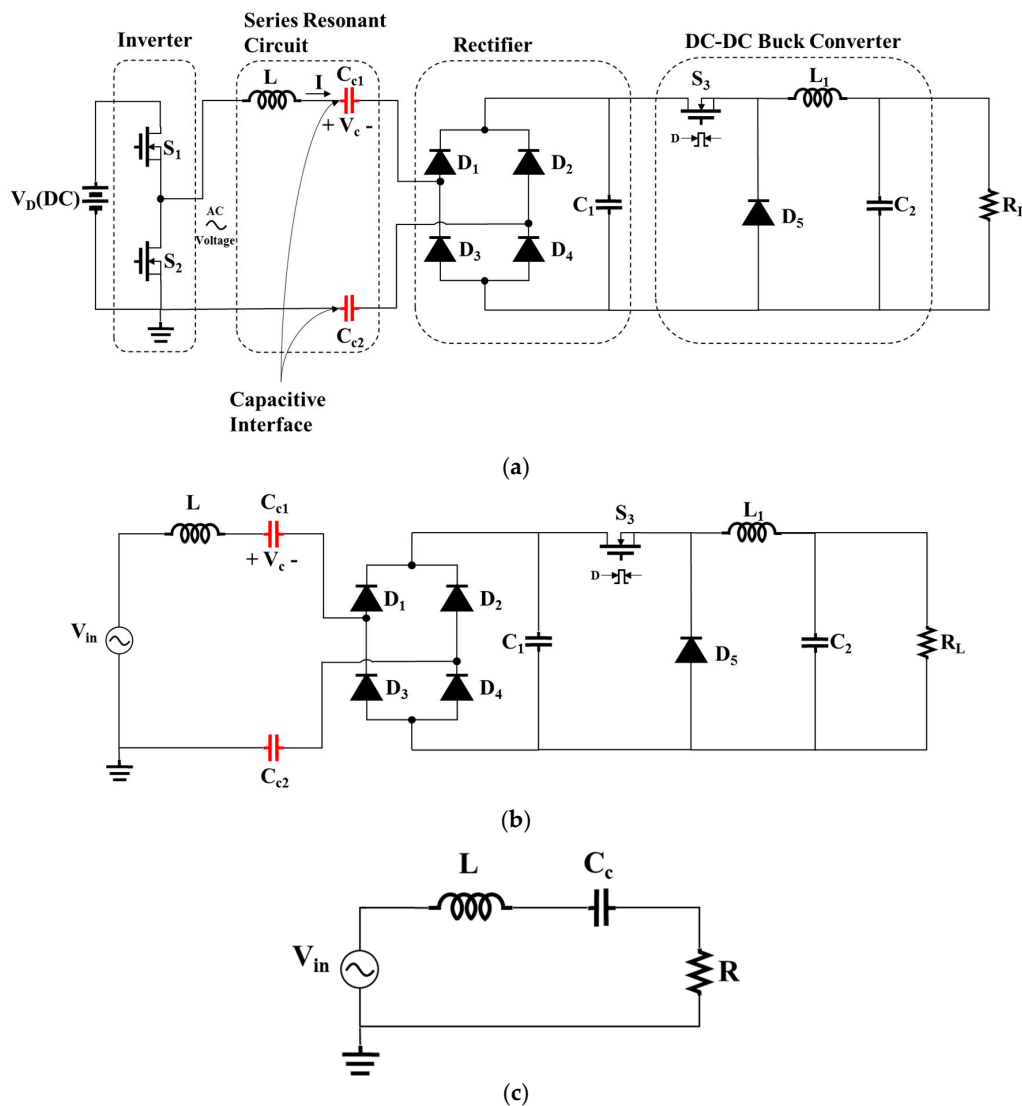


Figure 2. The proposed system: (a) CPT system with a DC–DC buck converter; (b) circuit simplification by the sinusoidal approximation, and (c) equivalent circuit used for analysis.

3. Mathematical Modelling and Analysis

For analysis, the system topology of Figure 2a was rearranged assuming the parasitic resistances are neglected for all components, as shown in Figure 2c. The inverter in Figure 2a produces a square wave voltage. This voltage is applied to the input terminal of the resonant circuit. The resonant

circuit frequency is tuned to the fundamental component of the inverter square wave, i.e., to the switching frequency f . As a result, the resonant circuit current and the resonant circuit output voltage and current have essentially sinusoidal waveforms at the fundamental frequency f , with negligible harmonics. Accordingly, the sinusoidal approximation was first considered where V_{in} can be obtained from Equation (1), as shown in Figure 2b.

The two series interface capacitances were replaced by C_c as shown in Equation (2). The series compensation inductor L is obtained from Equation (3). The equivalent AC load R [26], assuming the rectifier and the buck converter are ideal, is described in Equation (4).

$$V_{in} = \frac{2V_d}{\pi} \sin(\omega t), \quad (1)$$

$$C_c = \frac{C_{c1} C_{c2}}{C_{c1} + C_{c2}}, \quad (2)$$

$$L = \frac{1}{C_c \omega^2}, \quad (3)$$

$$R = \frac{8}{D^2 \pi^2} R_L = \frac{R_{load}}{D^2}, \quad (4)$$

where ω is the angular switching frequency; R_{load} is the effective load resistance at the AC side; which is equal to 81% of the actual load resistance R_L at the DC side after the rectifier; and D is the buck converter duty cycle. The values in Table 1 were used as a design example to prove the concept.

Table 1. Parameters used for modelling.

Parameter	Unit	Value
P_{load}	Watt	10
f	MHz	1
$C_{c1} = C_{c2} = 2C_c$	nF	2
L	μ H	25
R_{load}	Ω	10

The equivalent circuit shown in Figure 2c would not be applicable for analysis if the cross coupling or the leakage capacitance is too high due to the complicated coupling configuration [27] or if the operating frequency is increased to a very high level. In these cases, more accurate modelling [14] for the capacitive interface should be used.

To fairly compare the system sensitivity and the voltage stress over the capacitive coupling interface in the proposed system and the conventional system previously described, we assumed that the same amount of power was delivered to the load and the input voltage would change according to the value of the duty cycle (D) of the buck converter. When D was 100% represented the conventional system. Figure 3 shows the needed input voltage for the design example to deliver 10 W to the load depending on D , as shown in Equations (5) and (6):

$$V_{in} = \frac{V_{in_conv}}{D}. \quad (5)$$

From Equation (1), we obtain:

$$V_D = \frac{V_{D_conv}}{D}, \quad (6)$$

where V_D and V_{in} are the DC input voltage and AC input voltage needed to deliver a specific amount of power to the load, respectively. The DC input voltage and AC input voltage for the conventional system are represented by V_{D_conv} and V_{in_conv} , respectively.

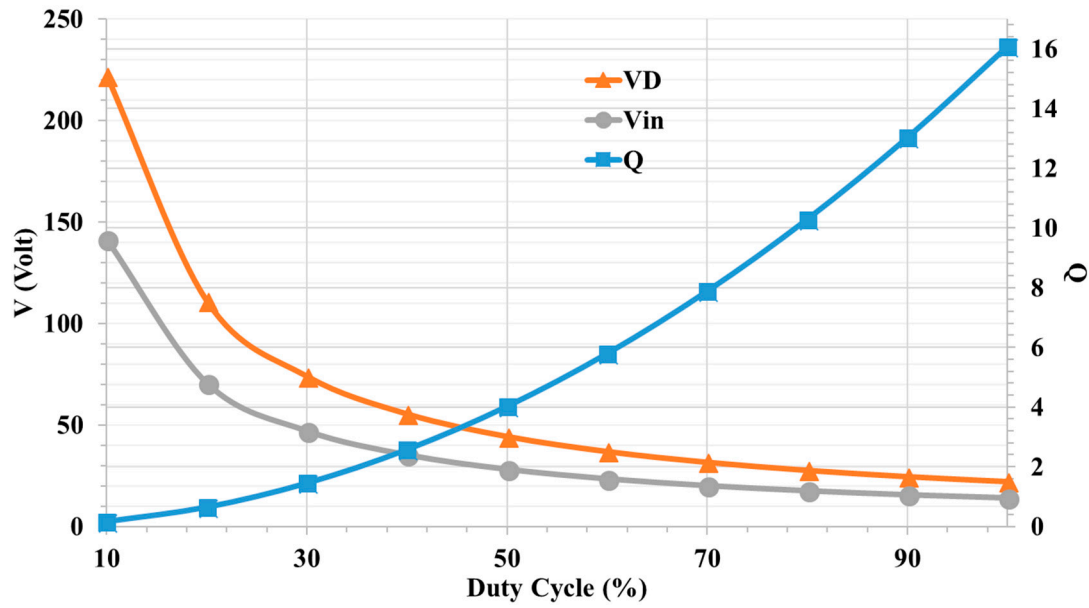


Figure 3. Input voltage needed to deliver 10 W to the load and the change in the quality factor of the circuit Q with different duty cycles D .

3.1. System Sensitivity

Figure 4 illustrates the frequency response of the output power with different duty cycles. The instantaneous real power transferred to the load is provided in Equation (7) and the average power in Equation (8). By reducing D , the output will have a wider response that is reflected in lower sensitivity. The quality factor of the proposed system (Q) as expressed in Equation (9) decreases proportionally to D^2 , as shown in Figure 3. By lowering Q , the sensitivity decreases and tuning at resonant frequency will be more obtainable practically. For a less sensitive system, we recommend using $Q \leq 6$, which can be easily achieved by choosing $D \leq 50\%$ for the chosen values of this design example. The recommended D will change depending on the situation and the system design parameters.

$$P_{\text{load}} = \frac{\left(\frac{C_c R V_{in} D s}{C_c L s^2 + C_c R s + 1} \right)^2}{2 R_{\text{load}}}, \quad (7)$$

$$|P_{\text{load}}| = \frac{C_c^2 D^2 R^2 V_{in}^2 \omega^2}{2(R_{\text{load}} + C_c^2 L^2 R^2 R_{\text{load}} \omega^6)}, \quad (8)$$

$$Q = \frac{1}{R} \sqrt{\frac{L}{C_c}} = Q_{\text{conv}} D^2, \quad (9)$$

where s is $j\omega$, P_{load} is the real power delivered to the load for the CPT system with the DC–DC buck converter added, and Q_{conv} denotes the quality factor of the conventional system.

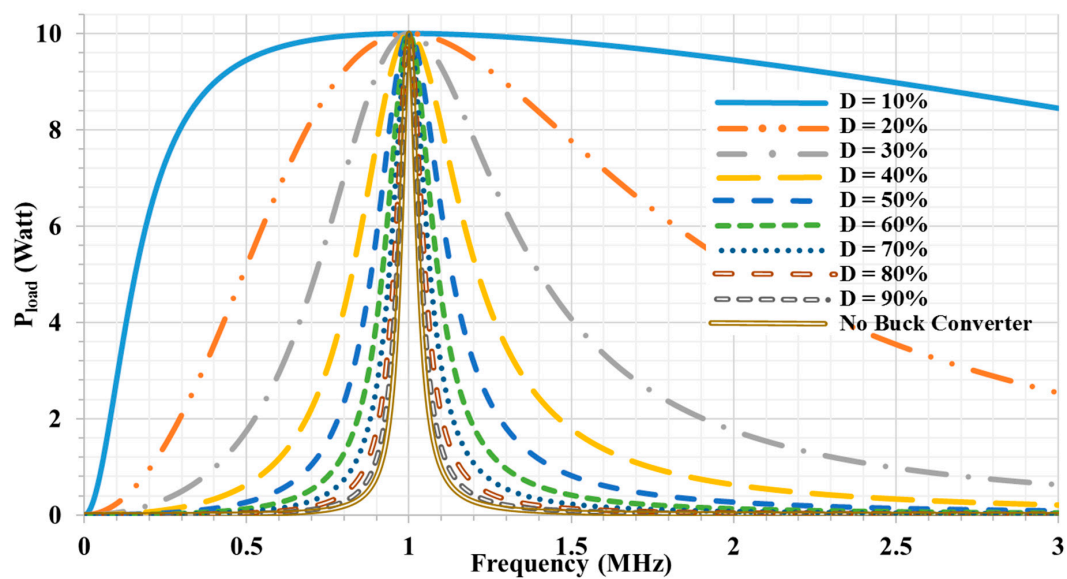


Figure 4. The frequency response of the output power at different duty cycles D .

By reducing the system sensitivity, the system's ability to transfer power becomes impervious to large parametric variations. Figure 5 shows the impacts on output power with changes in the capacitive coupling interface. For the conventional system, by changing the interface value by only 10% of its original value, no power will transfer to the load and resonance frequency will vary considerably due to the high Q . Conversely, by using the DC–DC buck converter on the power receiving side, the system becomes immune to parameter changes and the ability to transfer the power increases even under extreme conditions. For instance, if $D = 10\%$ is used, the power can be transferred with almost the same amount for any increase in the interface value from 250% more to 55% less than the original interface value by using DC–DC buck converter as a part of the secondary side. As such, the misalignment issue is of less concern.

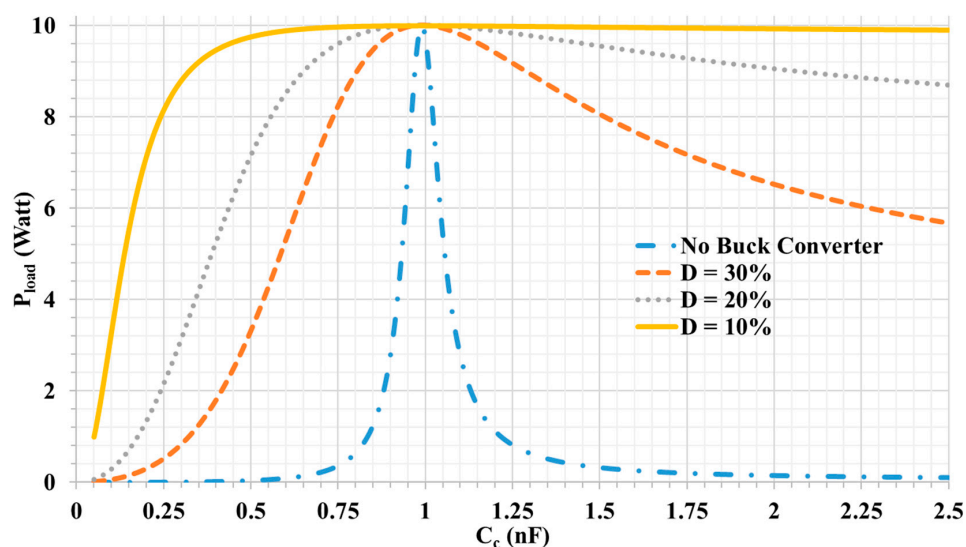


Figure 5. The tolerance of the output power with the change in the capacitive interface value using different duty cycles D .

By adding the buck converter, the Q value remained low for any value of the interface, as shown in Figure 6, which guarantees the system robustness. On the contrary, the previous system Q is

susceptible to variations in the coupling interface, especially when the coupling capacitance is reduced to less than 0.5 nF.

The load can be a parameter that affects the system by changes that may occur due to the change in the battery under charge at the DC level, for example. Figure 7 shows that the Q value is stable and low for a wide range of changes in the load, unlike the case without DC–DC buck converter added where the Q reaches to more than 100 for some load values.

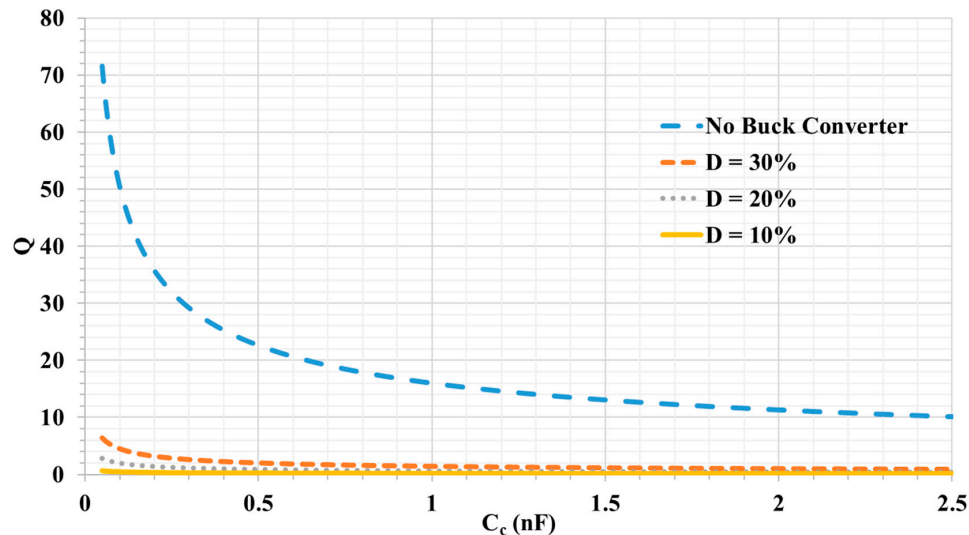


Figure 6. The change in the capacitive interface value effect on the Q value.

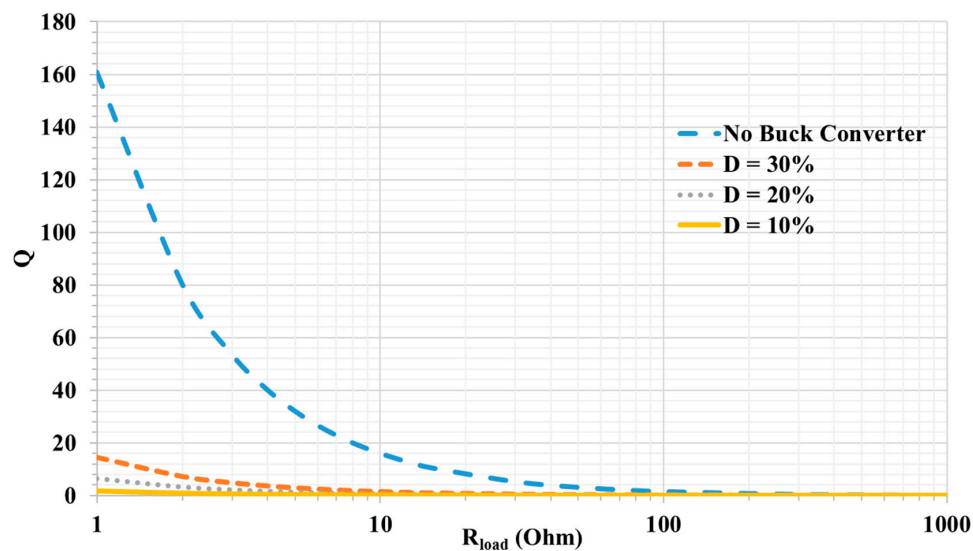


Figure 7. Q value change with the load.

3.2. Voltage Stress Across the Capacitive Interface

By having the DC–DC buck converter on the secondary side in the proposed system, the equivalent AC load increased with decreasing D as expressed in Equation (4). Therefore, the input voltage had to be boosted accordingly per Equation (5) and the power could be transferred with smaller current (I) to the load in the same amount of transferred power. The current flowing through the interface (I) can be found using Equation (10), which can be expressed as a function of the duty cycle and the interface current of the conventional system at the resonance frequency, as shown in Equation (13).

The reduction in the current through the circuit results in less voltage stress V_c across the one pair of the coupling plates as described in Equations (11) and (12). Figure 8 that shows how V_c varies with the duty cycle of the DC–DC converter. The voltage stress across one pair of the coupling plates (V_c) decreases proportionally with D at the resonant frequency, as given in Equation (14). At low frequencies, the terms $2 C_c L \omega^2$ and $C_c^2 \omega^2 (R^2 + L^2 \omega^2)$ can be neglected and V_c can be determined, as shown in Equation (15), which explains the high V_c at the low frequencies. According to these results, the probability of having safety issues or the occurrence of sparks and dielectric breakdown is much lower, and can be totally neglected if D is sufficiently low.

$$I = \frac{C_c V_{in}}{C_c L s^2 + C_c R s + 1} \quad (10)$$

$$V_c = \frac{I}{2 C_c s} = \frac{V_{in}}{2 C_c L s^2 + 2 C_c R s + 2} \quad (11)$$

$$|V_c| = \frac{1}{2} V_{in} \sqrt{\frac{1}{1 - 2 C_c L \omega^2 + C_c^2 \omega^2 (R^2 + L^2 \omega^2)}} \quad (12)$$

If the switching frequency = the resonance frequency,

$$I = I_{conv} D, \quad (13)$$

$$V_c = V_{c_conv} D. \quad (14)$$

If the switching frequency « the resonance frequency,

$$V_c \approx \frac{1}{2} V_{in}, \quad (15)$$

where I_{conv} and V_{c_conv} are the current flowing through the interface and the voltage across a single pair of the capacitive coupling interface plates for the conventional system, respectively.

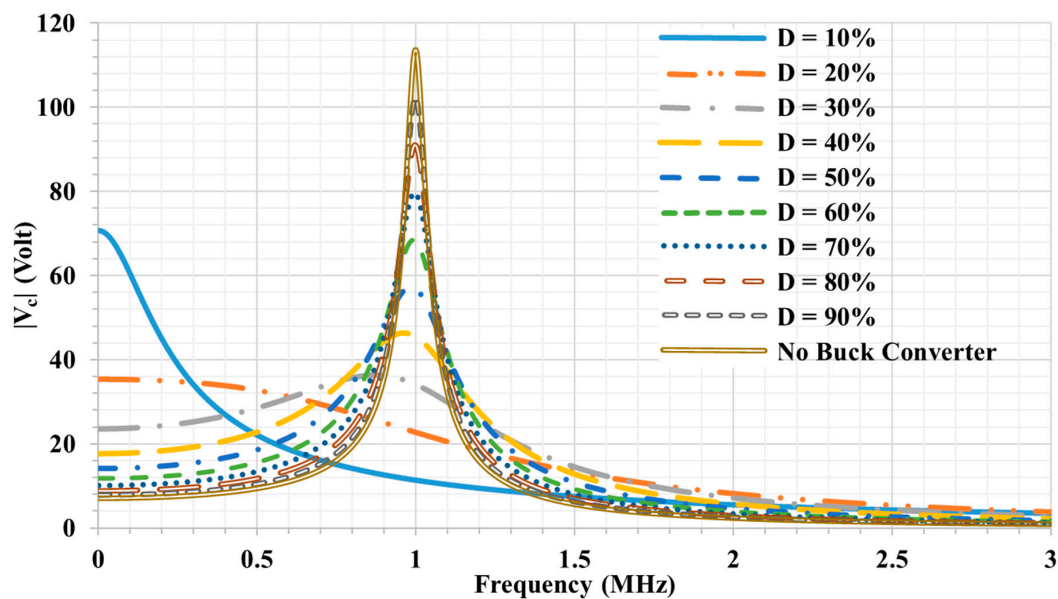


Figure 8. The frequency response of the voltage V_c across one pair of the coupling plates at different duty cycles D .

4. Electric Field Simulation

As discussed in the previous section, the proposed system has lower voltage stress over the capacitive coupling interface. Accordingly, the electric field in between the coupling plates, including the leakage electric field emissions, should decrease as well. In this section, the transient E field analysis in Maxwell software from Ansys, Pennsylvania, USA, was used to simulate the electric field strength between and around the plates. Figure 9 shows the experimental modelling used as the coupling interface with the same dimensions and materials. Measurement points were assigned between and at different distances around the plates as listed in Table 2.

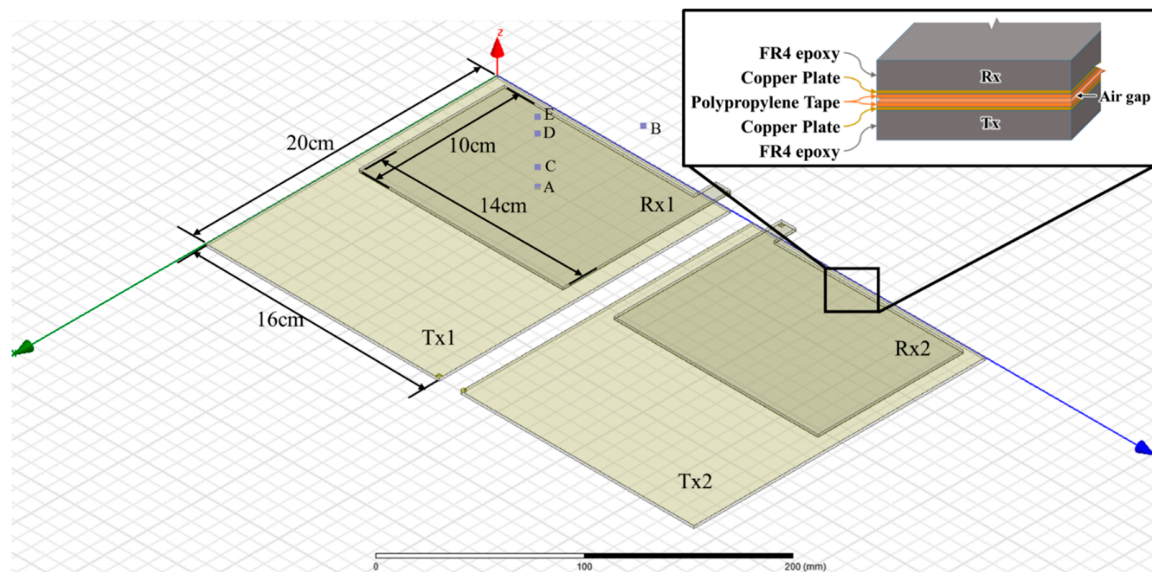


Figure 9. Plates modelling in Ansys Maxwell.

Table 2. Measurement points coordination.

Point	Distance to the Plates (cm) X, Y, Z
A	In the center between Tx1 and Rx1
B	2, 0, 0 (in front of Tx1 and Rx1)
C	0, 0, 1 (above the center of Tx1 and Rx1)
D	0, 0, 3 (above the center of Tx1 and Rx1)
E	0, 0, 4 (above the center of Tx1 and Rx1)

Figure 10 shows that the electric field between the single pair coupling interface plates reduced by D factor, which results in a reduction in the electric field emission to the surrounding space as illustrated in Figures 11 and 12.

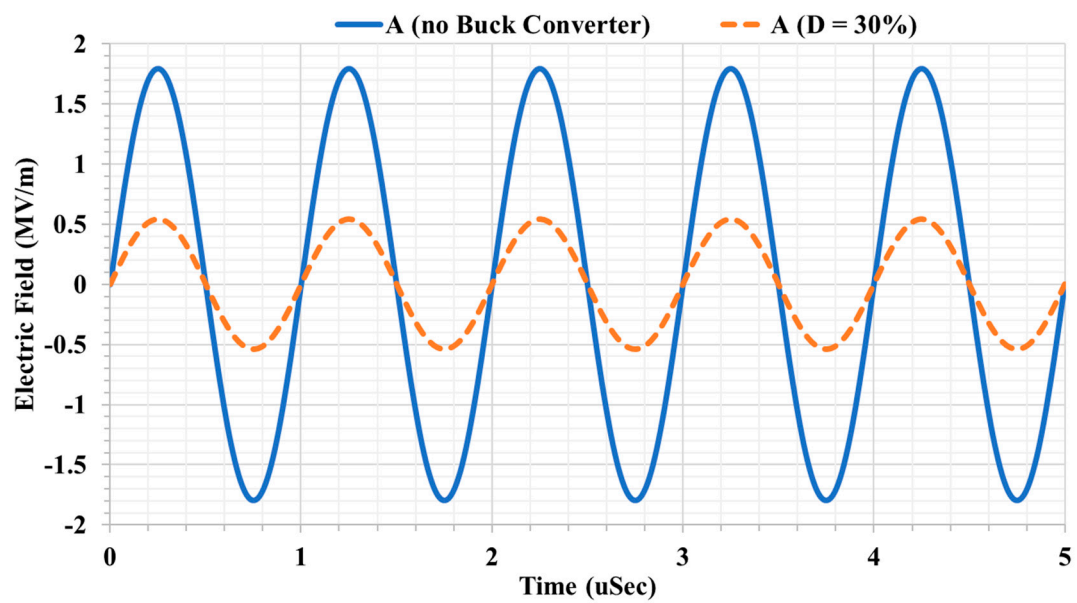


Figure 10. Simulated electric field at measure point A between Tx1 and Rx1.

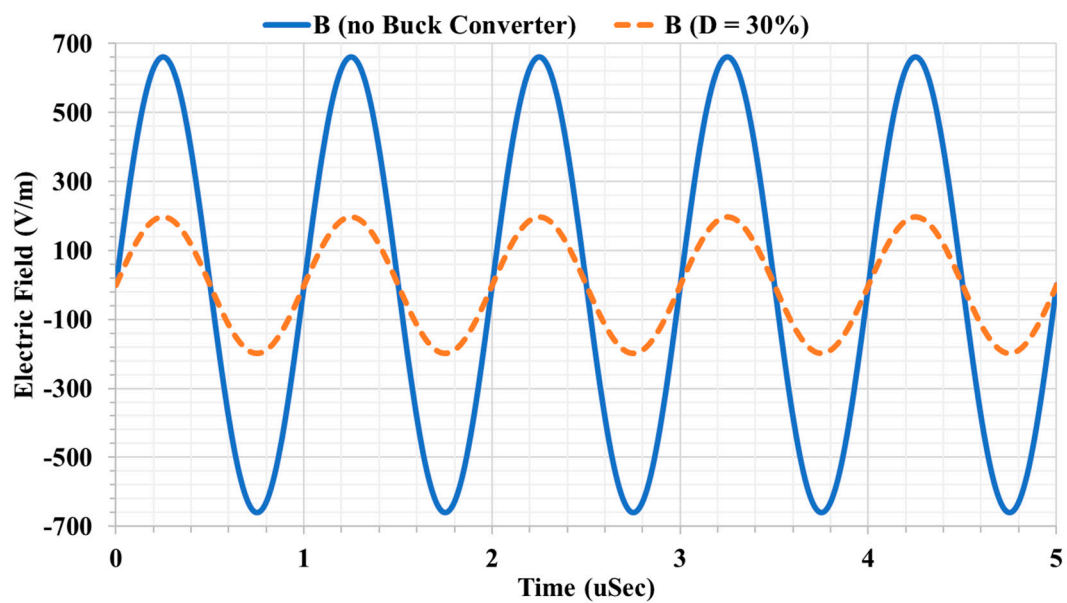


Figure 11. Simulated electric field at measurement point B in front of Tx1 and Rx1.

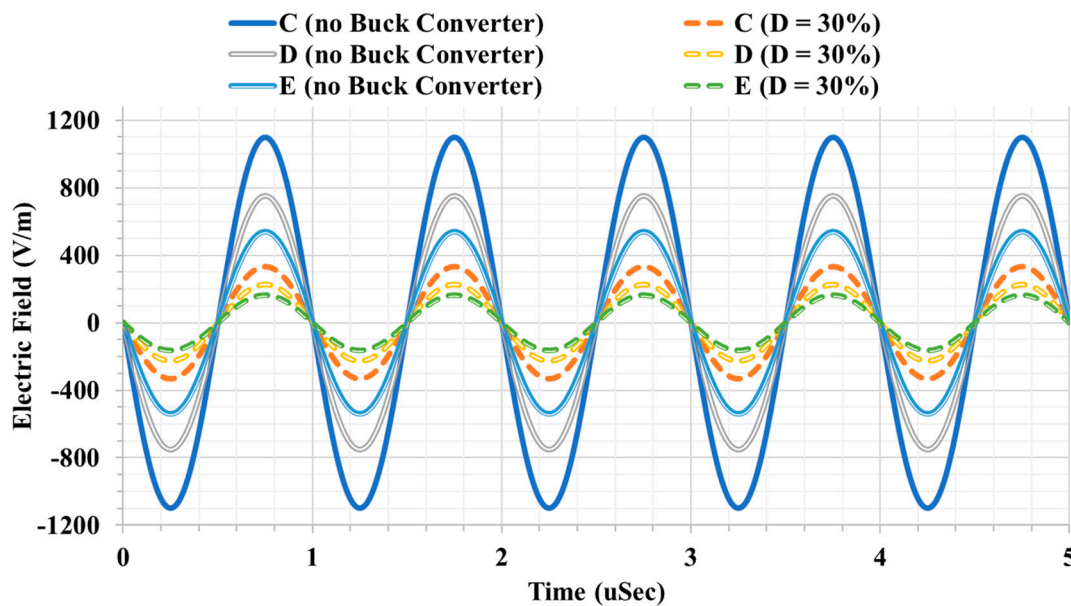


Figure 12. Simulated electric field at measurement points C, D, and E above the center of Tx1 and Rx1.

According to the Institute of Electrical and Electronics Engineers (IEEE) standard for safety levels with respect to human exposure to radio frequency electromagnetic fields of 3 kHz to 300 GHz [28], the field strength emissions for any system should be lower than 614 V/m for 0.03–1.34 MHz to ensure safe operation without harm to the human body. According to Figure 11, for the conventional CPT, the safe region starts after 2.5 cm in the X and Y directions from the plates by adding a buck converter electric field lower than 614 V/m anywhere in the XY plane around the plates. Figure 12 shows that the safe region for the conventional system, where the electric field is acceptable, is 3.5 cm above the plates. Notably, the system with a buck converter has sufficiently low electric field levels to be used safely. The proposed system helps to safely use CPT technology without the need for shielding or living object detection systems.

5. Experimental Results

A prototype was built, based on parameters listed in Table 3, as shown in Figure 13. The capacitive coupling interface was made of copper boards and the metal faces are covered by the polypropylene tape (relative permittivity is about 2.5) as a dielectric material. The dimensions of the pickup plates were chosen to suit the back side of an Apple 10-inch iPad, 10 cm × 14 cm each. Four Schottky diodes were used to compose the rectifier for its high-frequency abilities, and Litz-wire was used for inductors to reduce skin effect. Duty cycles 20%, 30% and 100% (system without buck converter) of DC–DC buck converter were examined. The input voltage value was determined according to the duty cycle used in the DC–DC buck converter for delivering 10 W of power to the load. The frequency was swiped from 0.35 MHz to 2.5 MHz to show the frequency responses of the output power and the voltage stress across the interface.

For kilowatt (kW) level high power applications, silicon-carbide (SiC) field effect transistors (FETs) can be used instead of conventional power metal oxide semiconductor field effect transistor (MOSFETs) used in this experiment; while at low power high frequency operations at several tens of MHz, gallium-nitride (GaN) FETs provides a good option [29].

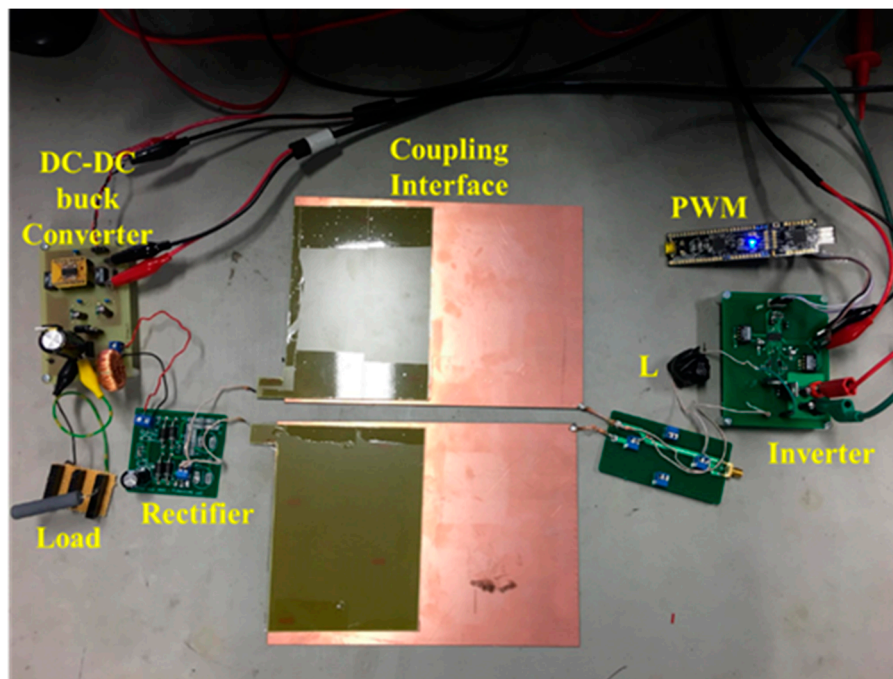


Figure 13. The system prototype. PWM: pulse-width modulation.

Table 3. Circuit parameters and system specifications.

Parameter	Unit	Value
P_{load}	Watt	10
$freq.$	MHz	1
C_{c1}	nF	~2.1
C_{c2}	nF	~1.9
Duty Cycle	%	20, 30, 100
L	μ H	25
R_{load}	Ω	10

Figure 14 shows the frequency response of the DC output power at different duty cycles. Q reduction is confirmed by reducing the duty cycle of the buck converter as predicted from the analysis. The main reason for the shift in the response is the change in the value of the total impedance of the load and the parasitic capacitance of the diodes that constructs the rectifier by changing the duty cycle. As proved in the analysis section, by reducing Q , the system's tolerance to misalignment improves, as shown in Figure 15. Figure 16 shows the amplitude of voltage stress measured across the single pair of the capacitive interface (C_{c1}). A differential probe was used to eliminate the common ground effect. The voltage stress is proportionally decreasing with the duty cycle which follows Equation (14) from the mathematical analysis. The maximum voltage stress across the capacitive interface (C_{c1}) is reduced to about 65 V at $D = 30\%$ and 44 V at $D = 20\%$, corresponding to an output power of 10 W, while 211 V is measured for the no buck converter used case. The values of the experimental results of V_c is higher than the calculated ones due to the non-ideal components in the system and the switching losses which decrease the efficiency, so a higher input voltage is needed to deliver 10 W resulting in higher voltage stress across the interface. By using 64 V DC input voltage (V_D), the system could deliver 10 W of power at the duty cycle of 30% and operating frequency 1 MHz, while the end-to-end system efficiency reached 80%. Figure 17 shows the measured V_{in} , V_c , and V_{out} .

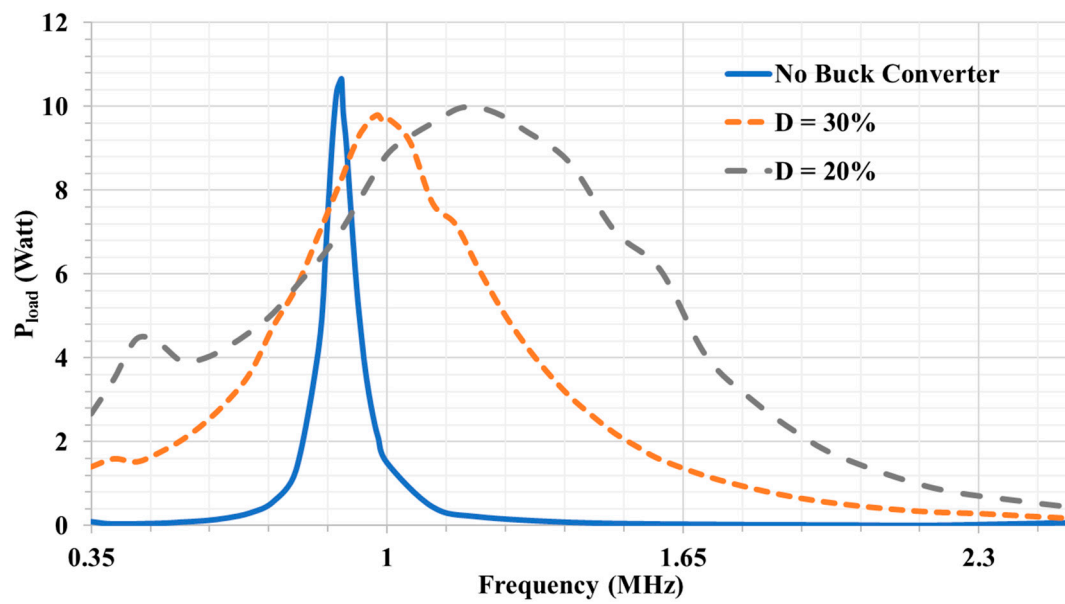


Figure 14. Frequency response of the DC output power.

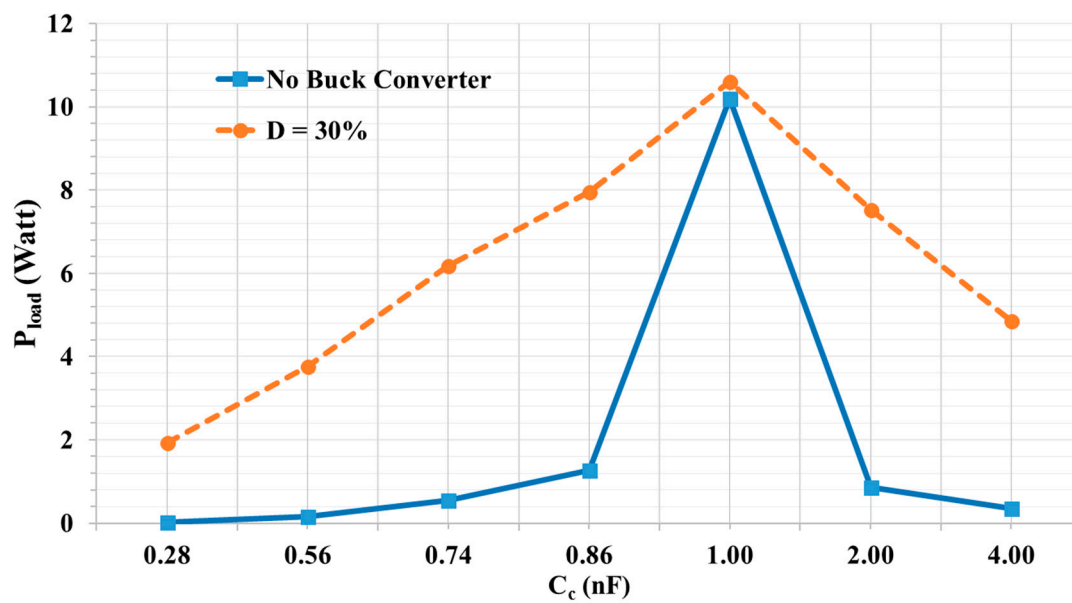


Figure 15. The tolerance of the output power with the change in the capacitive interface equivalent series value.

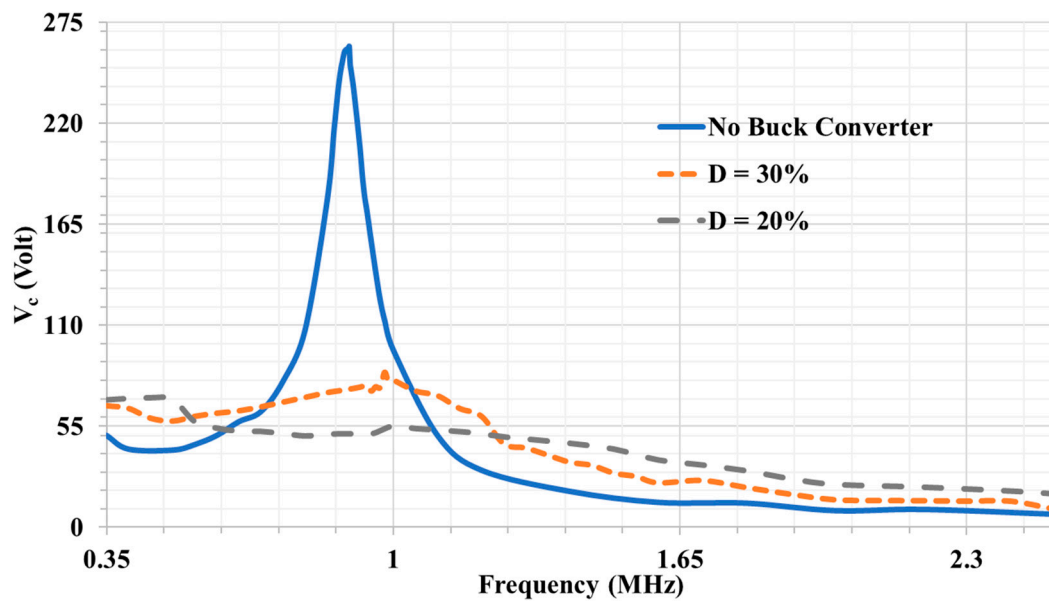


Figure 16. Frequency response of the voltage across the single pair of the capacitive interface C_{c1} (amplitude).

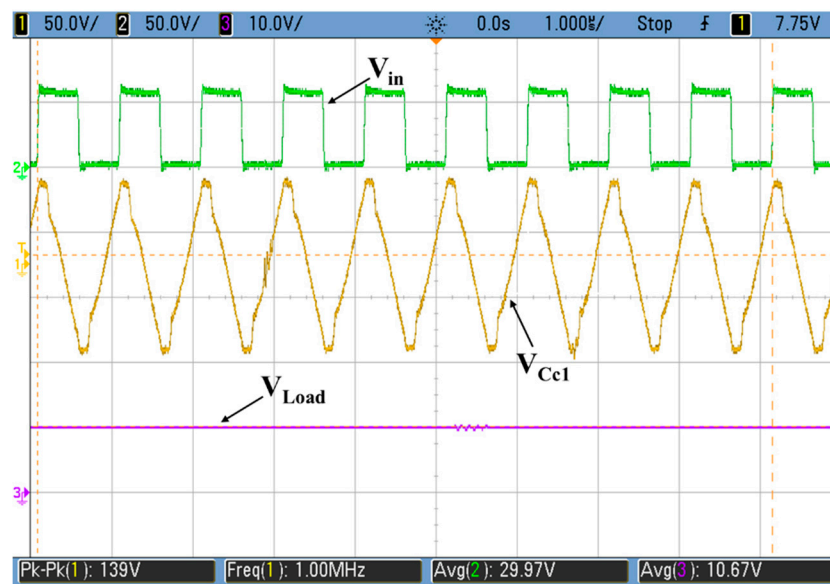


Figure 17. Waveforms of the input AC voltage, voltage across the coupling capacitor, and the DC output voltage.

6. Conclusions

This paper proposed a novel method for reducing the voltage stress and sensitivity of a CPT system by using a DC–DC buck converter. Mathematical analysis of the proposed system has been carried out to investigate the change in the system's Q and the voltage stress across the coupling interface. The leakage electric field emissions were simulated by using the Maxwell software package. It is found that by reducing the duty cycle of the DC–DC buck converter, the system Q reduces proportionally to D^2 . Accordingly, the system tolerance to the change in the system parameters has improved. While transferring the same amount of power, the voltage stress is reduced proportionally to D and the related leakage electric field around the plates is drastically shrunk so the system becomes safer and the probability of dielectric breakdown or spark occurrence becomes much less.

The experimental results from a 10 W CPT prototype demonstrated that by adding the buck converter, Q and voltage stress could effectively be reduced by changing the duty cycle. The maximum voltage stress across one pair of the coupling plates has been reduced to 65 V and 44 V at duty cycles of 30% and 20%, respectively, compared to 211 V for the conventional system without using a DC–DC converter. By applying 64 V input DC voltage and 30% buck converter duty cycle the system has achieved a system input to output (end-to-end) power efficiency of 80% at an output power of 10 W.

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