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Design of Three Phase Solid State Transformer Deployed within Multi-Stage Power Switching Converters

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Abstract: This paper presents a symmetrical topology for the design of solid-state transformer; made up of power switching converters; to replace conventional bulky transformers. The proposed circuitry not only reduces the overall size but also provides power flow control with the ability to be interfaced with renewable energy resources (RESs) to fulfill the future grid requirements at consumer end. The proposed solid-state transformer provides bidirectional power flow with variable voltage and frequency operation and has the ability to maintain unity power factor; and total harmonic distortion (THD) of current for any type of load within defined limits of Institute of Electrical and Electronics Engineers (IEEE) standard. Solid state transformer offers much smaller size compared to the conventional iron core transformer. MATLAB/Simulink platform is adopted to test the validity of the proposed circuit for different scenarios by providing the simulation results evaluated at 25 kHz switching frequency.

Keywords: decoupled controller; ferrite material; proportional integral (PI); solid state transformer (SST); space vector pulse width modulation (SVPWM); voltage source converter (VSC); voltage source inverter (VSI)

1. Introduction

The main consideration, currently, is to supply a cheap, clean and sustainable supply of power to end consumers in the future. To meet this goal, the most significant and required change is the design of the distribution transformer. Traditional transformers are heavy, occupy a large volume and possess fix voltage and frequency operation. Traditional transformers are sensitive to transients, voltage disturbances, harmonics and inter harmonics due to non-linear and unbalanced loads [1,2]. This creates power quality issues, as effects of the load from consumer side travel to the power distribution network. Distribution transformers have a poor transformer utilization factor as the magnetic core saturates due to the harmonic nature of the load. The presence of harmonic current due to nonlinear and unbalanced loads also influences the primary side current, thus creating power quality issues [3]. Besides power quality improvement and a continuous supply of power to the customers, an advanced type of transformer needs to be introduced to cope with the future grid requirement.

Over the past decade, power electronic converters have played a vital role in the well-known high voltage direct current transmission (HVDC) and flexible alternating current transmission (FACT) systems in the form of static volt ampere reactive (VAR) compensators (SVCs), static synchronous

compensators (STATCOMs) and unified power flow controllers (UPFCs) and so on [4]. Since renewable energy resources (RESs) such as wind, fuel cells and solar have penetrated into the industry, so power electronic converters also find their applications in them [5,6]. Energy resources like natural coal or gas are limited and the use of RESs is growing constantly with the aim to exchange electric power with the grid by net metering. Owing to the fact that the conventional transformer cannot be interfaced with RESs and the progress made in the field of power electronics, have led to the evolution of another power electronic converter named the solid state transformer, also known as the power electronic transformer, that has gained a lot of attention [7–11].

With the progress made in the field of the semiconductor industry, high-frequency controlled switches with high-power ratings have been developed. With these advancements and to cope with the future requirement of distributed energy sources integration, research is being carried out in the field of power electronics, which targets the use of solid state transformers (SSTs) in applications of a high-power level. One of the key interests of researchers is to develop a dynamic architecture of SST acquiring minimum controlled switches; the other approach is the integration of SSTs with RESs and other power applications.

Solid state transformers respond to control signals but their designs are not simple due to the presence of power electronic converters. The basic principle of operation of SST is that it first transforms low-frequency (50 Hz) AC voltage to high-frequency (frequency more than 20 kHz) voltage. After that isolated dual active DC–DC high frequency converter regulates secondary direct current (DC) voltage, whose size is much smaller because of high frequency operation. The multi-stage power electronic converters use controlled power electronic switches in series. In the first stage active rectifier is used, which converts and controls grid voltage to DC grid voltage and provides extended control of active and reactive power [12]. Thus, it provides the control of power and power factor. One of the most important benefits provided by SST is that it isolates both the primary and secondary side, thus eliminating the coupling effects. Ride through capabilities, and compatibility between RESs and the grid make SST superior to conventional transformers [12]. The ability of SST to generate any variable frequency and voltage enables it to perform better and be efficient in industry applications as it removes the requirement of using variable frequency drives (VFDs). SSTs, in future, will not only replace the conventional bulky transformers dominating at charge stations, locomotive and traction applications, smart grids and at secondary distribution sides, but also provide additional functions, such as the control of the active-reactive power and distribution source integration. Reduced-volume SST with aforementioned features also plays a key role in improving the power quality [13,14].

Various two-level and multilevel switching converter topologies can be employed in SSTs as discussed in [15]. Some recent configurations of SST are also reported in [16–19]. SSTs in the form of direct Alternating Current (AC) to AC matrix converters directly convert three-phase alternating current to three phase alternating voltage [20]. SSTs without a DC link are impossible to be interfaced with RESs and fuel cells [21]. However, SST with a DC link [22] offers advantages such as the availability of DC port, and much reduced size due to high frequency operation over [20,21]. However, all aforementioned topologies involve a large number of converter valves. The isolated type topology, presented in this paper, involves the least possible number of controlled switches, completely isolates the grid from load, and provides independent control of the voltage, frequency, power flow and power factor. A very few instances (no instance, in fact) in the literature are reported where such a kind of topology can accomplish all the above-mentioned tasks. This justifies the applicability and validation of the proposed research. The suggested topology of SST also can maintain a clean voltage and current waveforms of utility supply irrespective of the type and nature of the load. This is what that has been stressed upon in this paper.

The paper is constructed in the following way. Section 2 pinpoints the proposed SST circuit topology, specifications and complete control layout. In Section 3, detailed simulation results are presented to investigate the role of SST as a variable frequency drive, power factor improvement

device and renewable interface with bidirectional power flow. An active power flow mechanism with balanced and unbalanced load is also simulated in this section. Conclusions are drawn in Section 4.

2. Proposed SST Circuit, Specifications and Control Layout

Vector control (decoupled controller) was used for a three-phase rectification purpose. Vector control employing controlled switches such as insulated gate bipolar junction transistors (IGBTs) maintains total harmonic distortion (THD) of the input current within IEEE defined limits and provides a ripple free DC output voltage. Obtained DC voltage $V_{DC,mes}$ was converted to a high frequency square wave using a full-bridge inverter, which was stepped down using a ferrite core high frequency transformer. This stepped down voltage was rectified again with the help of a full-bridge converter as shown in Figure 1. In the last stage, DC voltage V_x was converted back to the variable three-phase voltage with frequency and voltage control using the space vector pulse width modulation (SVPWM) technique.

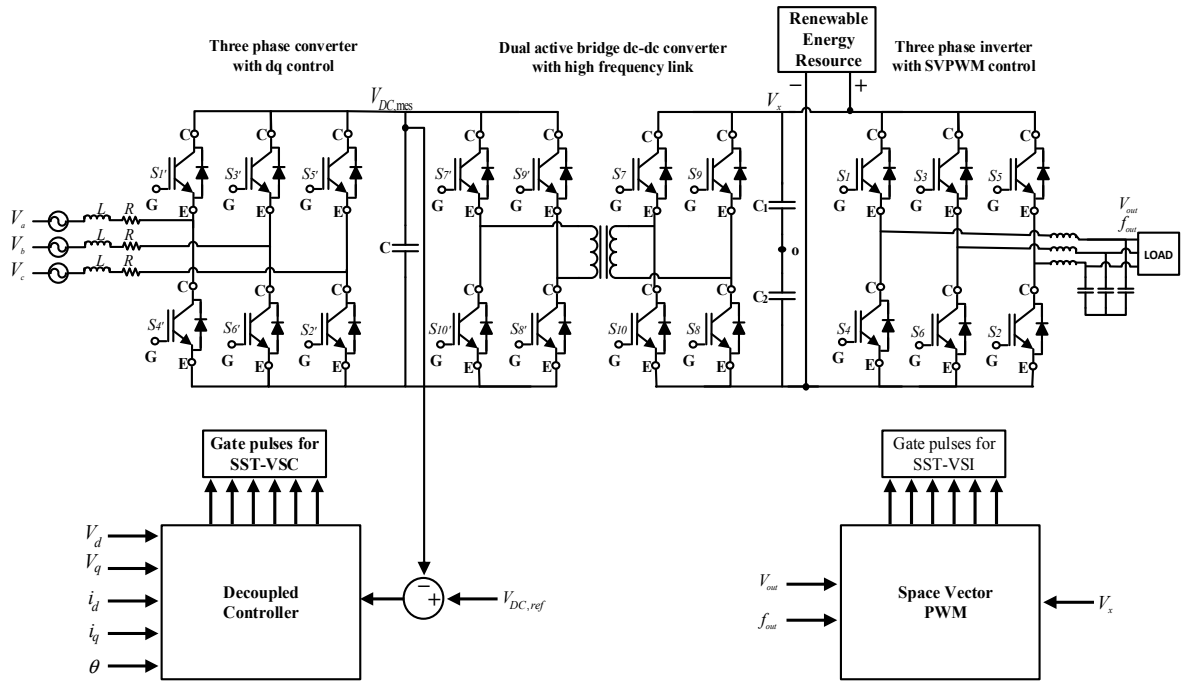


Figure 1. Proposed circuit diagram of the solid-state transformer.

2.1. Control Layout of the SST-Voltage Source Convereter

Flux-oriented vector current control (VOC), based on two control layers: Outer current control layer (OCC) and inner current control layer (ICC), was used to control the operation of voltage source converters (VSCs) [23]. The outer layer satisfied the DC voltage, active power and reactive power demands of the VSCs while the inner layer used the decoupling control method to regulate the q-axis and d-axis currents. Both control loops had a proportional and integral (PI) controller as a common element in them. DC link voltage $V_{DC,mes}$ was regulated using the voltage droop control [24]. Through the investigation of the bi-layer control architecture deployed within a multi-input multi-output (MIMO) voltage source converter, it can be realized that the operation of SST-VSC becomes a bit complex [25]. This complex control architecture has many variables, which need to be controlled precisely using PI controllers [26]. Therefore, it is the requirement of the system that PI controllers should be optimally tuned to provide both transient and steady state desired responses. However, tuning PI parameters of the nonlinear system like the voltage source converter, is a challenging task within itself [27].

Vector current control was used at the point of common coupling, which regulates the DC voltage control at VSC and power flow control with ac voltage regulation [28]. In this technique, ac voltage

and current of the VSC were converted into a rotating d–q reference frame, which was synchronized with ac grid voltages using a phase locked loop (PLL). This methodology not only regulated DC and ac voltage but also provided the decoupled control of both active and reactive power. The layout of the d–q control architecture-based SST-VSC is shown in Figure 2. The outer control loop produced reference currents for the inner current loop, which then provided the reference voltage for the d–q reference frame.

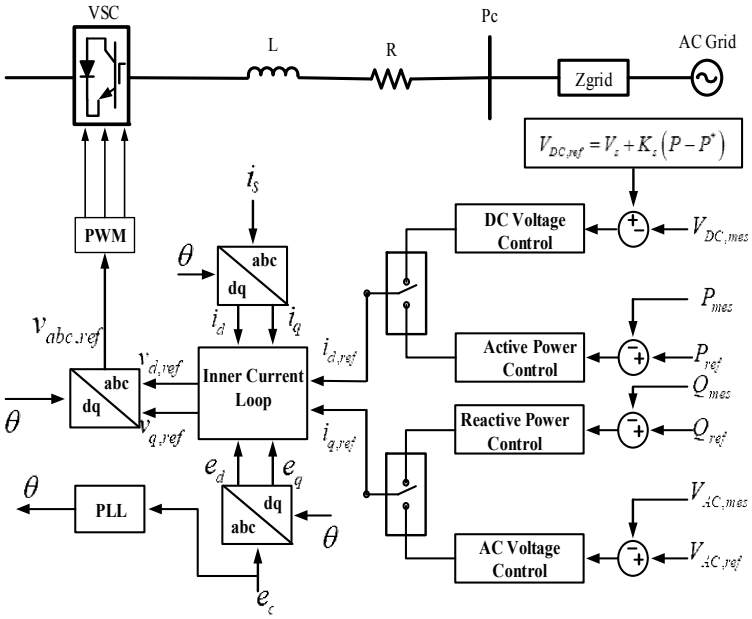


Figure 2. The d–q control architecture of solid state transformers-voltage source converters (SST-VSC).

By taking the d–q control frame into consideration, the internal control loop used the PI controllers, which generated the reference current and maintained the required voltage for the VSCs. Voltage expression at the point of common coupling (p_c) and the voltage source converter side (v_s) can be given as:

$$e_C - v_S = R \times i_S + L\frac{di_S}{dt}, \tag{1}$$

where R and L represent the resistance and inductance between SST-VSC and point of common coupling (PCC), while i_S is the current from the grid to the SST-VSC.

From Park's transformation:

$$e_d - v_d = Ri_d - \omega Li_q + L\frac{di_d}{dt}. \tag{2}$$

$$e_q - v_q = Ri_q + \omega Li_d + L\frac{di_q}{dt}. \tag{3}$$

Here ω represents the angular frequency at the PCC of ac system. Based on (2) and (3), the ICC control layout is shown in Figure 3. The reference signals (V_{d_ref} and V_{q_ref}) were transformed back to the *abc* frame, which were used to generate switching pulses for IGBTs of VSC.

In this research, the classical tuning method was used to tune the PI controller parameters. The transfer function of the simple PI controller is:

$$F(s) = k_p + \frac{k_i}{s}. \tag{4}$$

According to internal model control (IMC) method as presented in [29], we can write:

$$F(s) = k_p + \frac{\alpha_{ICC}}{s}\widehat{G}^{-1}(s) = \frac{\alpha_{ICC}}{s}(R + sL).$$

$$F(s) = \alpha_{ICC} L + \alpha_{ICC}\frac{R}{s}. \tag{5}$$

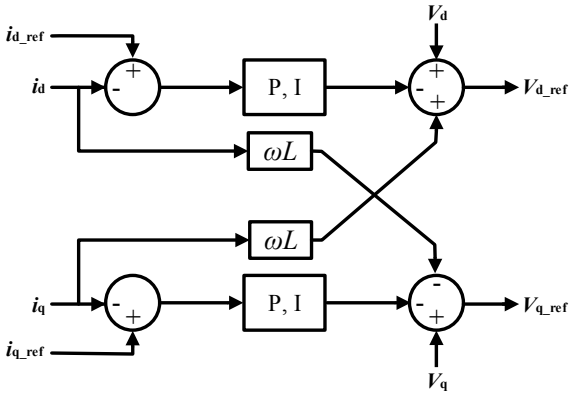


Figure 3. Inner current control loop of SST-VSC.

Here α_{ICC} (rad/s) represents the bandwidth of the current controlled system; $\widehat{G}(s)$ is the estimation of $G(s)$. Comparison of (4) and (5) yields the range of PI controller coefficients for ICC as:

$$k_p, ICC \leq \alpha_{ICC} L. \tag{6}$$

$$k_i, ICC \leq \alpha_{ICC} R. \tag{7}$$

The bandwidth α_{ICC} for the ICC must be selected such that it is ten times lesser than the switching frequency [30,31]. That is to say:

$$\alpha_{ICC} \leq \frac{2\pi Fs}{10}. \tag{8}$$

The PI controller parameters for the OCC can also be tuned using the same procedure as for ICC but with a constraint that OCC must be ten times slower than the ICC to achieve the non-oscillatory response of the closed loop system. This is achieved by selecting the bandwidth of the OCC such that it is 10 times smaller than the bandwidth of the ICC. As presented in [32], the OCC PI controller parameters are given as:

$$k_p, OCC \leq \alpha_{OCC} C. \tag{9}$$

$$k_i, OCC \leq \alpha_{OCC}{}^2 C. \tag{10}$$

$$\alpha_{OCC} \leq \frac{\alpha_{ICC}}{10}. \tag{11}$$

The outer control loop is responsible for controlling the ac and DC voltage, both active and reactive powers at PCC. As shown in Figure 2, d-channel controlled the DC link voltage or active power control, while the q-channel regulated the ac voltage or controlled the reactive power. These relations are mathematically represented as:

$$P = V_d i_d + V_q i_q. \tag{12}$$

$$Q = V_q i_d - V_d i_q. \tag{13}$$

Using PLL, the d-axis of vector control was synchronized with the phasor voltage of the ac system, so, $V_q = 0$. This reduced (12) and (13) to:

$$P = V_d i_d. \tag{14}$$

$$Q = -V_d i_q. \tag{15}$$

From (14) and (15), the active power and reactive power is regulated by controlling the d–q axis currents. At PCC, ac voltage is regulated by the q-axis current or can also be controlled by injecting the required reactive power to the system. Likewise, the DC link voltage is maintained via the exchange of real power with an ac system or by modifying the d-axis current.

The specifications of the VSC used within SST are given in Table 1:

Table 1. VSC specifications for SST.

	Nominal Voltage	Specifications	Impedance
Ac grid	11 kV	200 kVA	$R = 1\ \Omega\ L = 100$ mH
DC -link	20 kV		
DC -capacitor	20 kV	Single 880 μF	

2.2. Control Layout of the SST-Voltage Source Inverter

Three phase two level voltage source inverters (VSIs), consisting of two power electronic switches in each leg, have penetrated in the industry as they provide various speed control demands of induction motor drives. A two level VSI has six active states and two null states. Various PWM techniques are proposed in [33,34] to reduce the VSI output waveform distortions at a given switching frequency. The most popular one is the space vector PWM as it provides low output current ripple and provides maximum utilization of the DC -link voltages [35,36]. It provides 15% higher ac voltage, lower current and voltage harmonics distortions as compared to conventional PWM [37]. This is the reason that SVPWM as a modulation technique is employed in this research. The active states divide the space vector plane into six sectors of equal magnitude as shown in Figure 4. Switching states for all eight (six active and two null) vectors are shown in Table 2.

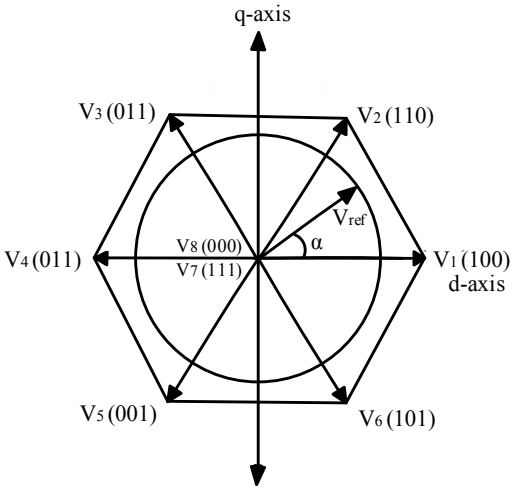


Figure 4. Vector representation of the SVPWM signal.

Using SVPWM, desired three phase voltages are provided by the voltage vector controlled in the d–q rotating frame as shown in Figure 4, whose rotation is sampled in every sub-cycle T_s. Figure 5 shows the component of the reference voltage vector of magnitude V_{ref} along the α and β-axis in sector

I whereas, T_1, T_2 and T_z are dwell times for which the active voltage vector V_1, active voltage vector V_2 and null vectors are applied in a sub-cycle T_s, such that the following relation is always satisfied.

$$T_S = T_1 + T_2 + T_Z. \tag{16}$$

Table 2. Space vectors state and the switching sequence.

Vector	Sector & Vector Combination		Line to Line Voltage			State
			V_{ab}	V_{bc}	V_{ca}	
V_0 (000)			0	0	0	Zero
V_1 (100)	I	V_0, V_1, V_2, V_7	$+V_d$	0	$-V_d$	Active
V_2 (110)	II	V_7, V_2, V_3, V_0	0	$+V_d$	$-V_d$	Active
V_3 (010)	III	V_0, V_3, V_4, V_7	$-V_d$	$+V_d$	0	Active
V_4 (011)	IV	V_7, V_4, V_5, V_0	$-V_d$	0	$+V_d$	Active
V_5 (001)	V	V_0, V_5, V_6, V_7	0	$-V_d$	$+V_d$	Active
V_6 (101)	VI	V_7, V_6, V_1, V_0	$+V_d$	$-V_d$	0	Active
V_7 (111)			0	0	0	Zero

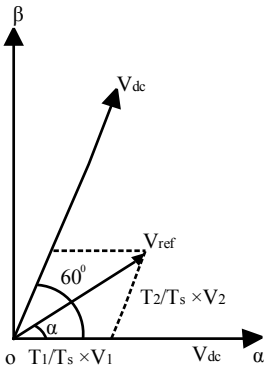


Figure 5. Vector representation of the SVM signal in sector 1.

Consequently, the applied gating sequence of sector I is depicted in Figure 6.

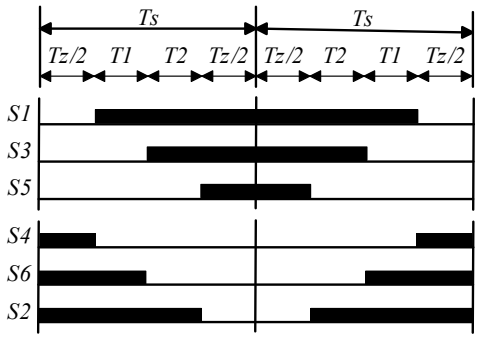


Figure 6. Gating sequence for the switches.

Volt-second balance equations along the α-axis and β-axis are given as:

$$V_{ref} \times T_S \times \cos(\alpha) = \frac{2}{3} V_{dc} \left\{ T_1 + T_2 \times \cos(\frac{\pi}{3}) \right\}. \tag{17}$$

$$V_{ref} \times T_S \times \sin(\alpha) = \frac{2}{3} V_{dc} \times T_2 \times \sin(\frac{\pi}{3}). \tag{18}$$

Solving (17) and (18) gives dwell time for each vector as:

$$T_1 = m \times \frac{\sin\left(\frac{\pi}{3} - \alpha\right)}{\sin\left(\frac{\pi}{3}\right)} \times \frac{1}{f_s}, \tag{19}$$

$$T_2 = m \times \frac{\sin\left(\alpha\right)}{\sin\left(\frac{\pi}{3}\right)} \times \frac{1}{f_s}, \tag{20}$$

$$T_Z = T_S - (T_1 + T_2), \tag{21}$$

where 'm' represents the modulation index, which is equal to $V_{ref}/(2/3\,V_{dc})$ and $f_s = 1/T_s$ represents the switching frequency.

The specifications of the VSI used within SST are given in Table 3.

Table 3. Voltage source inverter (VSI) specifications for SST.

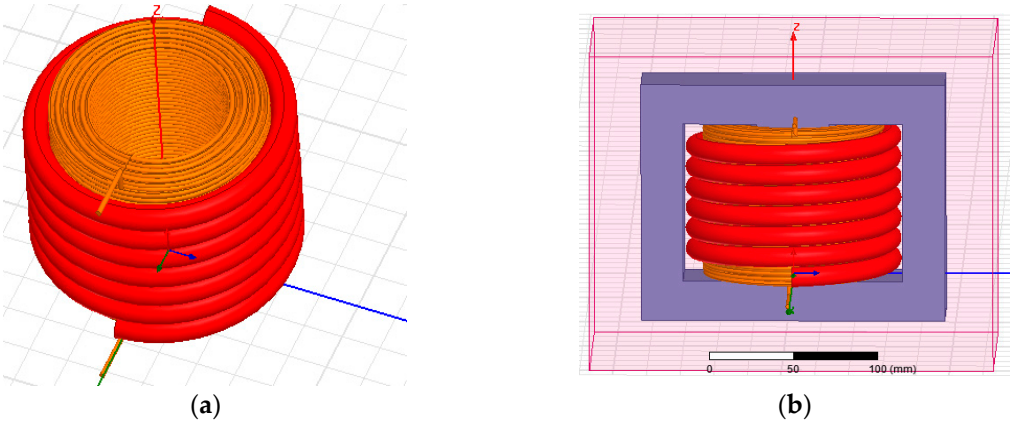
	Quantity	Specifications
DC-link	Input DC Voltage	500 V
DC-capacitors	2- DC capacitors in series	Each 250 V & 20 mF
V_{out}	Output Voltage	Variable
F_{out}	Output Frequency	Variable

2.3. Ferrite Core High Frequency Transformer Design

The importance of ferrite materials is worth mentioning in modern power and industrial electronics application. Design constraints of ferrite materials and losses incorporated in soft magnetic materials due to high switching frequency are already discussed in literature [38,39]. More elaborate models that discuss the modeling and dependence of ferrite losses at high flux densities and high frequencies are also discussed in [40].

The operation of ferrites at square waves with 50% duty cycle offer 0%–15% smaller losses as compared to sinusoidal signals of the same peak and frequency [41–44]. These properties and performance make ferrite materials suitable for many switching applications where square wave switching is desired without using any auxiliary filter circuits.

In this research work ferrite medium, operated at 50% duty cycle within DAB, is used not only to provide galvanic isolation but also to decrease voltage levels. The ANSYS/Maxwell platform is chosen to design the high frequency ferrite core transformer. The specified design parameters of the simulated Maxwell model, as shown in Figure 7, are tabulated in Table 4.



(**a**) (**b**)

Figure 7. High frequency ferrite core transformer. (**a**) Primary and secondary coil. (**b**) Complete transformer model placed within an air medium.

Table 4. Parameters of a high frequency ferrite transformer.

Units	Quantity	Values
3F3	Ferrite (MnZn), P-Type	9997 (nH/T^2)
B	Magnetic flux density	3200 Gauss (core losses <100 mW/cm^3)
W_aA_c	Product of Core Area and Window Winding Area	1006.7857 cm^4
A_c	Core Area	25 cm^2
W_a	Window Winding Area	40.271429 cm^2
P_o	Power	200 kVA
F	Frequency	25 kHz
J	Current Density	3.5 A/mm^2
K	Filling Factor	0.6
V_p	Primary Voltage	20 kV
I_p	Primary Current (with 5% increase in input power to cover losses)	10.5 A
V_s	Secondary Voltage	500 V
I_s	Secondary Current	400 A
N_p	Primary Turns	250 Turns
N_s	Secondary Turns	7 Turns
R_p	Primary Winding Resistance	0.299947 Ω
L_p	Primary Winding Inductance	26676.98 μH
R_s	Secondary Winding Resistance	0.34242 mΩ
L_s	Secondary Winding Inductance	400.904 μH
A_{pw}	Primary Winding Wire Area (with skin effect compensation)	4.399 mm^2
A_{sw}	Secondary Winding Wire Area (with skin effect compensation)	122.23 mm^2

The parameters of a high frequency transformer, simulated using ANSYS/Maxwell software, tabulated in Table 4, were used in MATLAB/Simulink to carry out the simulation of SST.

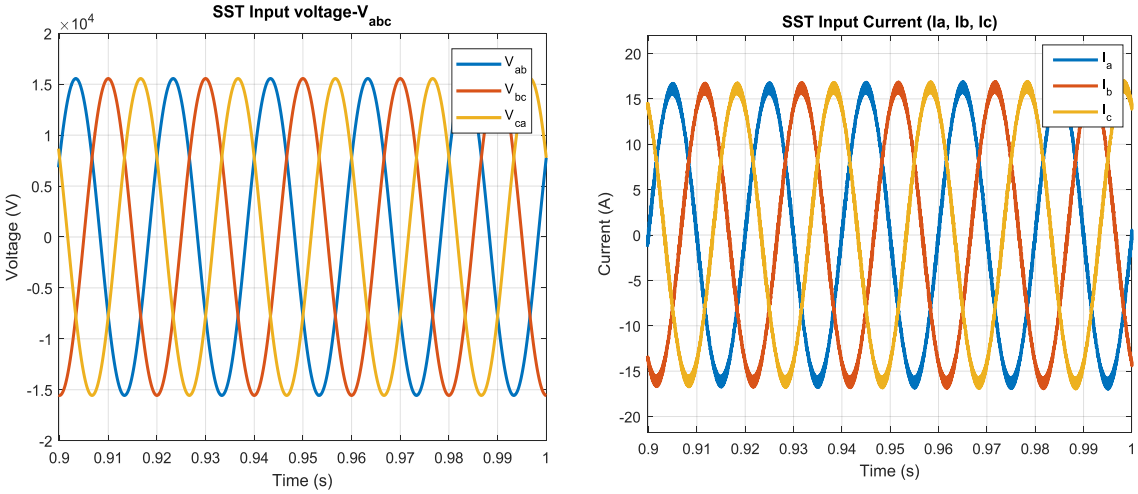
3. Simulation Results

The SST-VSC incorporated within the inner–outer control loops and voltage droop control maintained both active and reactive power requirements while the SST-VSI fulfilled variable frequency control requirements at the consumer end. The SST-VSC connected with the 11 kV grid, maintained a DC -link $V_{DC,mes}$ at 20 kV whose specifications are already given in Table 1, while the SST-VSI, specifications given in Table 2, generated variable voltage and variable frequency at the load end.

Since the proposed circuit was symmetric, so the bidirectional power flow could be achieved just by changing the gate pulses only without any amendment in the circuit. To assess the flexibility and validity of the proposed circuit, simulations using the MATLAB/Simulink environment were carried out for four different test cases: SST to deliver active power, SST as a variable frequency drive, bidirectional power flow interfacing RES and SST as a power factor improvement (PFI) device.

3.1. Case 1: Active Power Flow

Simulation results were presented at various stages of the proposed SST based on multi-stage power switching converters after the transient period was elapsed. Three phase voltage and current at the grid side, for a three-phase balanced load, are shown in Figure 8. As can be observed from Figure 9, SST input voltage (phase A) and current (phase A) at the grid side remained in-phase even though active power demand was varied from 0.0 p.u. to 1.0 p.u, thus delivering power at unity power factor. Results show that presented SST model drew balanced three phase current from the grid. Input current (phase A) had very less harmonic content (THD = 2.16%) as shown in Figure 10. Same results were valid for other phases as well.



(**a**) (**b**)

Figure 8. (**a**) SST input voltage at the grid side. (**b**) SST input current at the grid side.

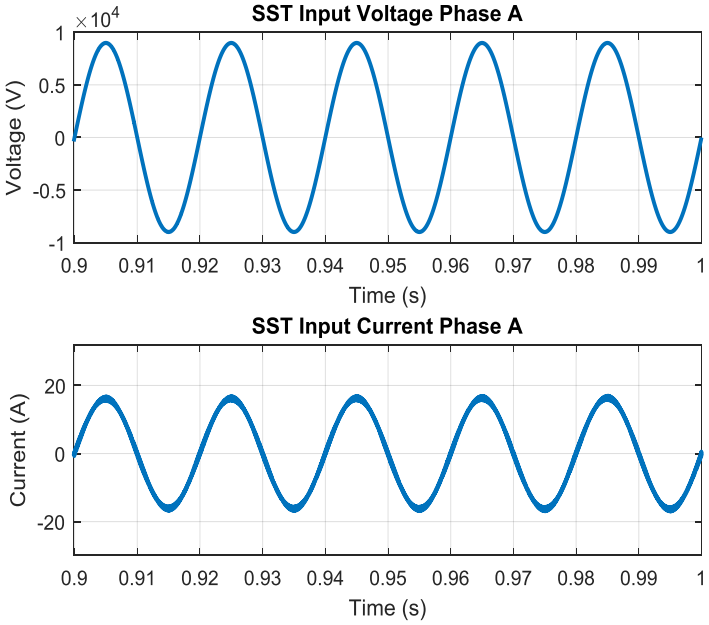
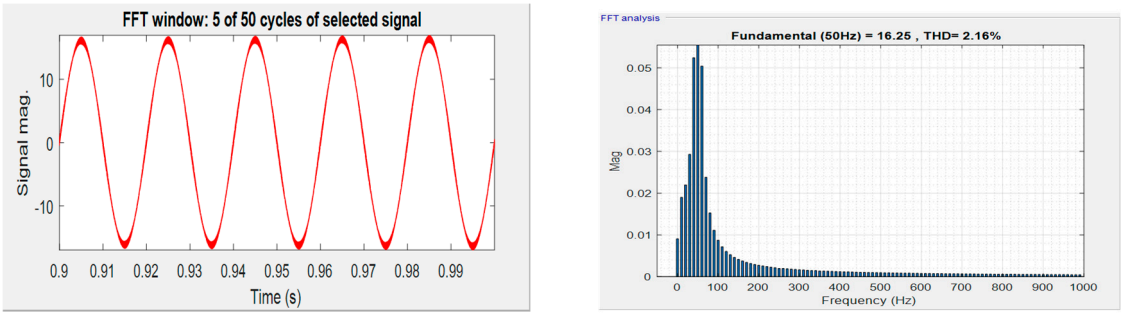


Figure 9. Result displaying that phase A voltage and current are in phase with each other.



(**a**) (**b**)

Figure 10. (**a**) Phase A current drawn from utility. (**b**) Total harmonic distortion (THD) analysis of phase A current.

In the dual active bridge (DAB) circuit, the full bridge square wave inverter cascaded at SST-VSC generated a square wave voltage of 25 kHz for the high frequency transformer (HFT), which reduced the voltage level. The other full bridge square wave converter used within DAB, rectified the voltage at the secondary side of HFT. The voltage and current response of the SST-VSC at the DC -link $V_{DC,mes}$ side is given in Figure 11. Voltage at the primary and secondary side of HFT are shown in Figure 12.

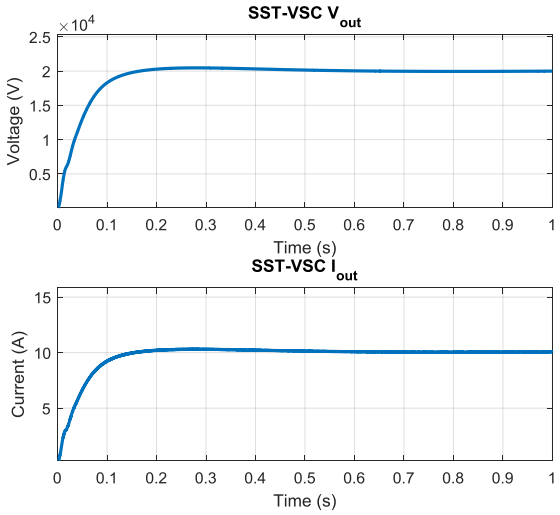


Figure 11. SST-VSC voltage and current at the DC -link.

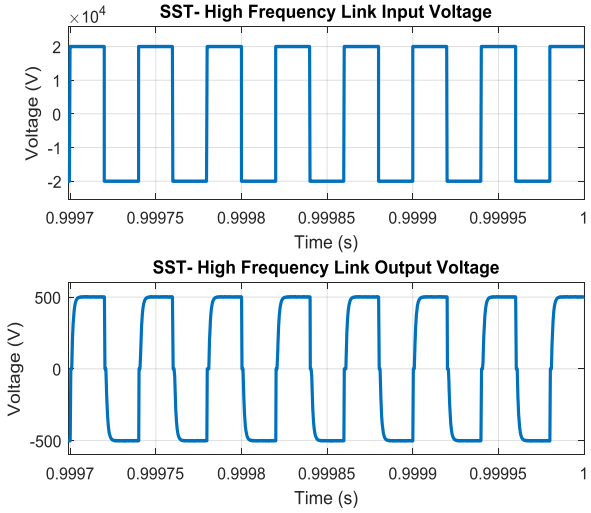


Figure 12. Primary and secondary voltage of the high frequency transformer.

At the DAB end, the DC -capacitor decreased the ripple content while the SST-VSI cascaded used SVPWM pulses to generate a three phase voltage with variable frequency and amplitude for the consumer end. When the generated frequency was 50 Hz, the SST-VSI output Line to Neutral (L-N) voltage before and after filter circuits are shown in Figure 13.

The same was true for the case of a 1.0 p.u. three-phase unbalanced load. Figures 14 and 15 display that SST delivers unbalanced current to the unbalanced load while keeping the SST input voltage (phase A) and current (phase A) in-phase at the grid side, thus ensuring power at the unity power factor.

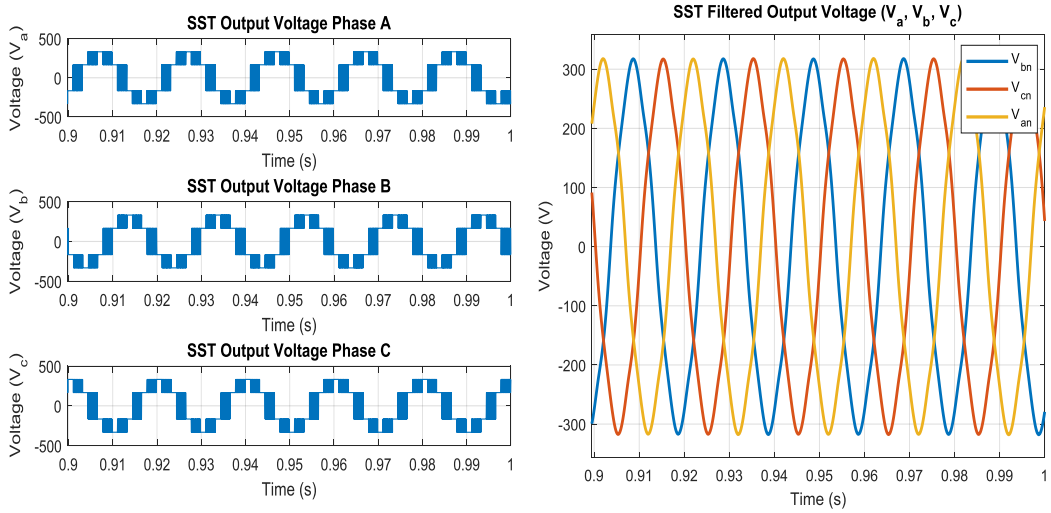


Figure 13. (**a**) SST-VSI output voltage without filter. (**b**) Filtered SST output voltage.

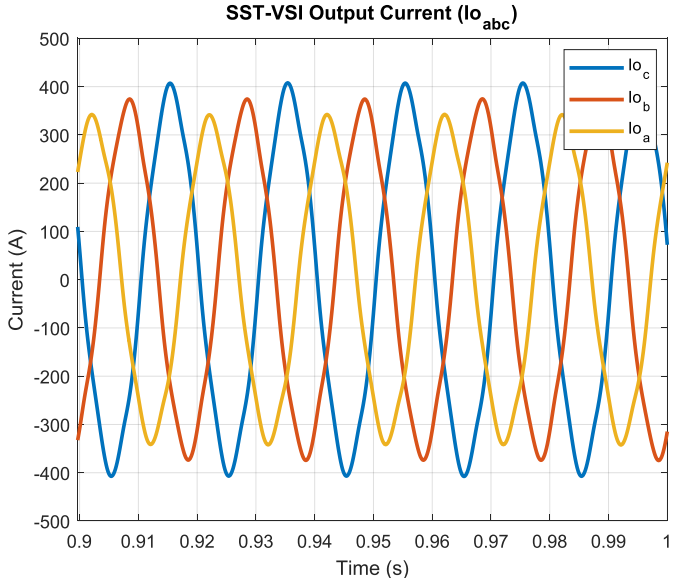


Figure 14. SST output current to the unbalanced load.

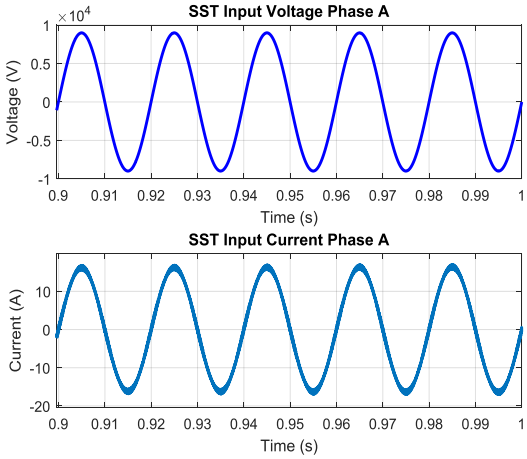
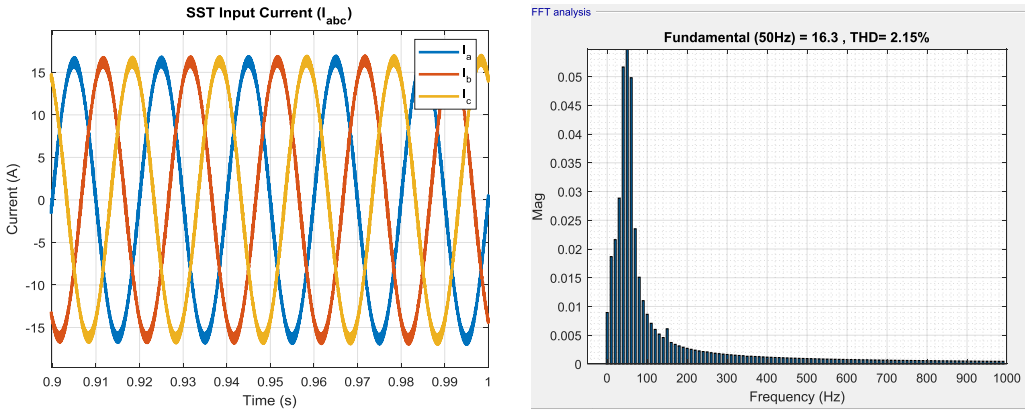


Figure 15. Result displaying that phase A voltage and current are in phase.

In addition, for unbalanced loaded SST, results presented in Figure 16 show that presented SST model drew a balanced three phase current from the grid with a harmonic content of 2.15% only for each phase current.



(**a**) (**b**)

Figure 16. (**a**) SST input current at the grid side. (**b**) THD analysis of phase A input current.

The voltage and current response of SST-VSC at DC -link $V_{DC,mes}$ with unbalanced loading is given in Figure 17.

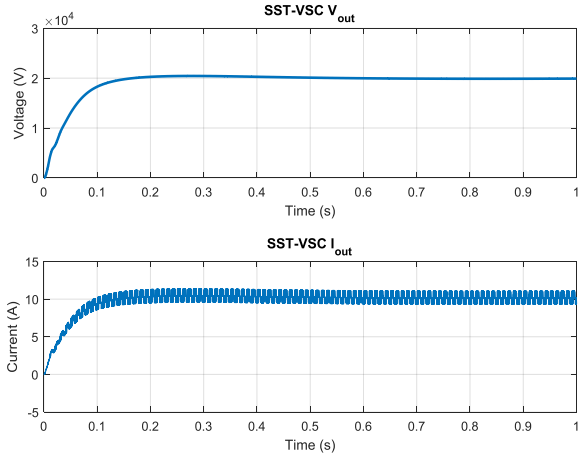


Figure 17. SST-VSC voltage and current at the DC -link.

3.2. Case 2: SST as a Variable Frequency Drive

When the operation of SST as VFD was evaluated for the case when SST delivered power to an induction motor with 1.0 p.u mechanical loading, the obtained results showed satisfactory results. SST maintained the unity power factor. The grid side current harmonic contents were within IEEE defined THD limits. With the induction motor at the rated loading, the settling time of SST-VSC at the DC -link increased by 0.15 s, as shown in Figure 18. SST-VSC took a little bit more (0.32 s) time to settle for the inductive load.

For the case when SST generated the voltage signal of 50 Hz for the inductive load, it could be observed from Figure 19 that the SST input current and the voltage were in phase, thus ensuring the unity power factor. For this case, filtered SST output voltage is shown in Figure 20.

When SST generated 60 Hz voltage signal for the load, the same parameters were evaluated, as in the previous case, and are displayed in Figure 21. Similarly, a voltage signal of other frequencies can be generated using the proposed SST for the resistive as well as the inductive load.

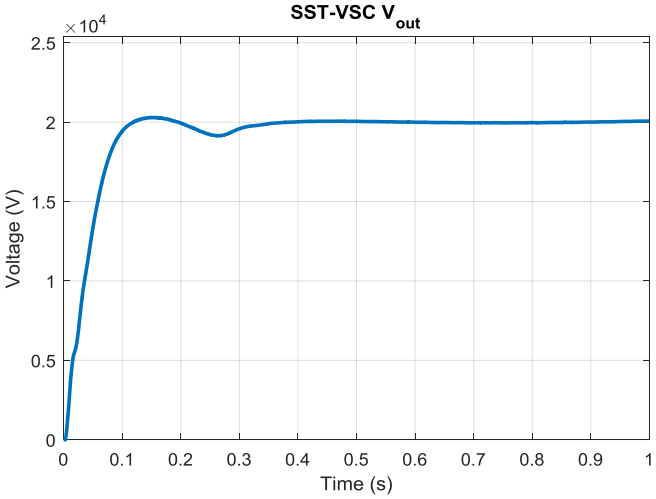


Figure 18. SST-VSC response with induction motor loading.

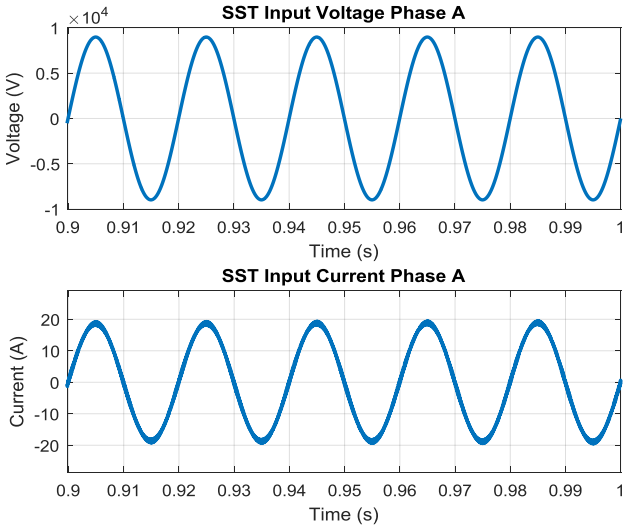


Figure 19. Result displaying that phase A voltage and current are in phase.

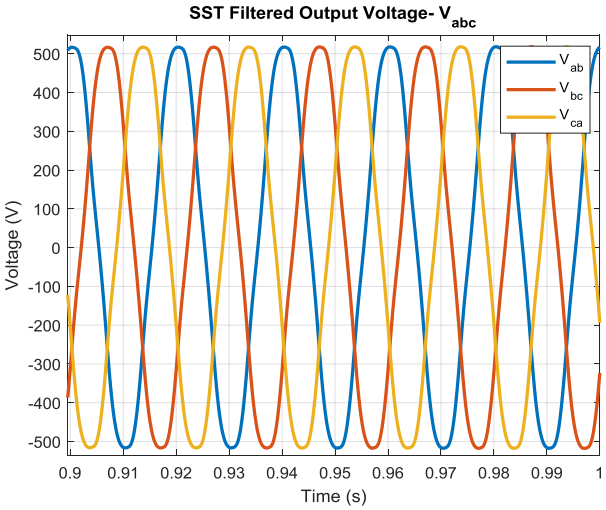
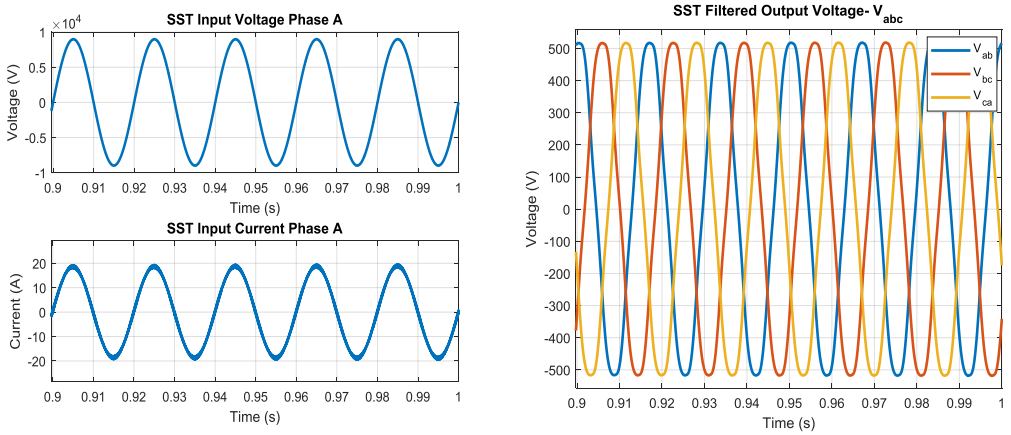


Figure 20. SST 50 Hz filtered output voltage.



(**a**) (**b**)

Figure 21. SST simulation results for 60 Hz output. (**a**) Phase A voltage and current in phase. (**b**) SST 60 Hz filtered output voltage.

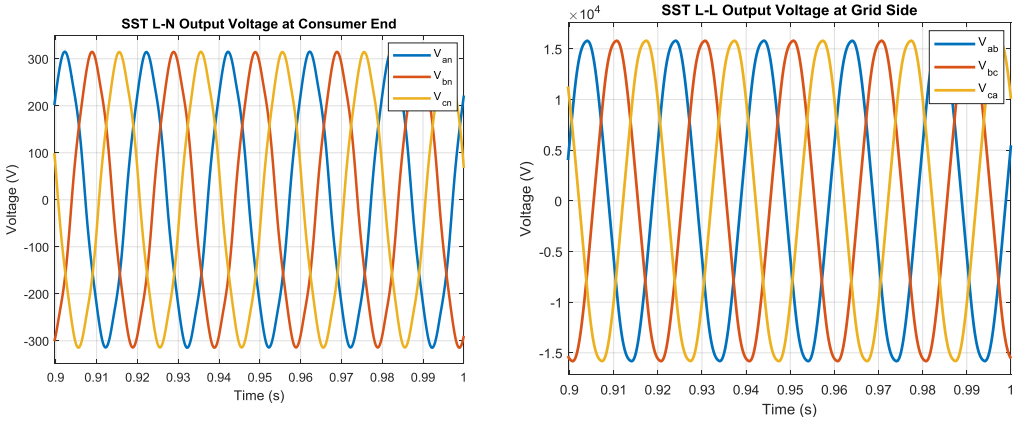
3.3. Case 3: SST with a Renewable Interface

To cope with the increasing trend of using RESs, SST provides a very handy infrastructure. RES integrated with SST, as shown in Figure 1, can be used solely to provide power to the consumer, making SST working as stand-alone system. The proposed topology also makes bidirectional power flow possible just by changing the gate pulses of the SST-VSC to make it perform as SST-VSI.

A high frequency transformer, which in previous cases was used to reduce the voltage level, now in this scenario, was working as a step up HFT. DAB, in this case, would maintain the DC -link for the SST-VSC. The SST-VSC, now working as SST-VSI, used SVPWM pulses to generate a three phase voltage. In this scenario SST was working as a grid-tied inverter, feeding power to the utility.

The RES block, represented in Figure 1, would be any single RES or the hybrid-RES incorporating batteries as well. In this research work, only the design of controlled multi-input multi-output circuitry of SST is under investigation, so, no specific constraints regarding the RESs were taken into consideration.

When a constant DC source was used as RES, simulations show that SST provided power not only to consumer but also to the utility as well, as shown in Figure 22, so, this architecture provided by SST would be a solution to all problems that will be faced in the future when smart and super grids will be kicked in the power system.



(**a**) (**b**)

Figure 22. SST simulation results when integrated with renewable energy resource. (**a**) SST line to neutral voltage at the consumer end. (**b**) SST line to line voltage at the grid end.

3.4. Case 4: SST as a Power Factor Improvement Device

In the ICC of SST-VSC, the quadrature component of current was maintained at zero using PI regulation, which forced SST not to draw reactive power from the grid, thus maintaining unity power factor at the grid side. When the *q*-component of current in ICC was maintained at any positive value, SST drew leading VAR from the grid, making SST as a PFI device, and at the same time maintaining its own feature of transformer.

When the current at the grid side was set to 45° leading, the simulation result shows that SST maintained its function of the PFI device when it was delivering power to a 1 p.u. rated inductive load. As compared to the conventional transformers, this is a remarkable achievement of the proposed SST design. The proposed circuit as a part of the interconnected system had the ability to improve the overall power factor of the system while meeting the lagging reactive power requirement of the load. However, the current at the grid side increased as expected. Figure 23 shows the voltage and current of phase A at the grid side, and filtered output voltage of the SST.

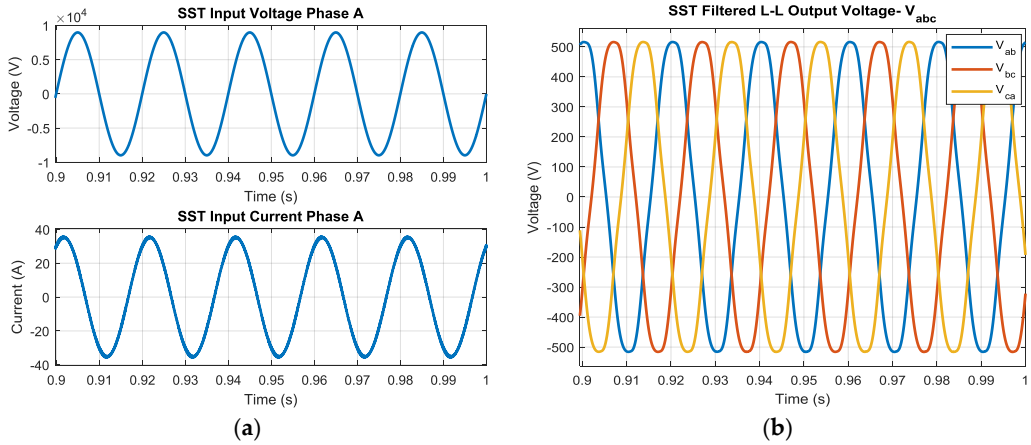


Figure 23. SST simulation results as the power factor improvement (PFI) device. (**a**) The input current leads the input voltage. (**b**) SST filtered output voltage.

When SST as a PFI device was investigated by the pre-tuned PI controller parameters, simulation results show that SST-VSC took more time (0.7 s) to settle its steady state value (see Figure 24). The voltage droop control at the outer layer of the SST-VSC could be re-tuned to reduce the settling time of the SST-VSC.

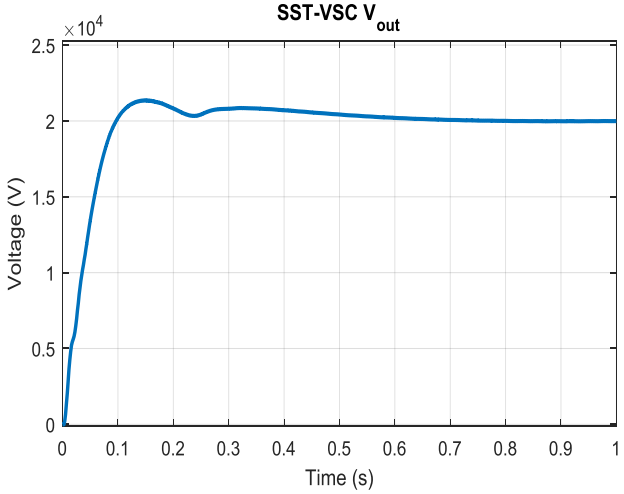


Figure 24. SST-VSC response working as the PFI device with induction motor loading.

3.5. Case 5: SST Supplying Power to Instantly Shifted Different Loads

In order to verify the stable performance of the proposed SST, simulation results were presented at various stages for different shifts of loads. The simulation was performed for 1.0 p.u three different test loads, which were resistive, inductive and capacitive in nature. Just like case 1, when the system was energized, it provided only the active power to the load. The test scenario was created such that at 0.7 s, the resistive load was disconnected and the pure inductive load was connected instantly. As simulation goes on, at 0.14 s, the pure inductive load was disconnected and the pure capacitive load was connected instantly. These shifts of loads where SST instantly shifted to provide lagging VARs and leading VARs to the load are depicted in Figure 25.

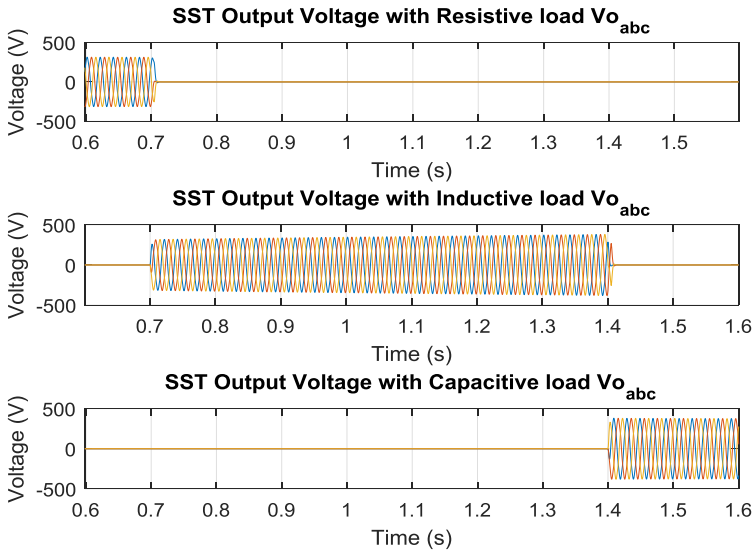


Figure 25. Filtered SST output voltage to resistive, inductive and capacitive load.

When SST was energized with the resistive loading, this scenario was analogous to Case 1. When the resistive load was disconnected and the pure inductive load was connected at 0.7 s, the output current of the inverter to the load is displayed in Figure 26. At 0.7 s from Figure 26, a shift of 90 degrees in the output current can be seen clearly.

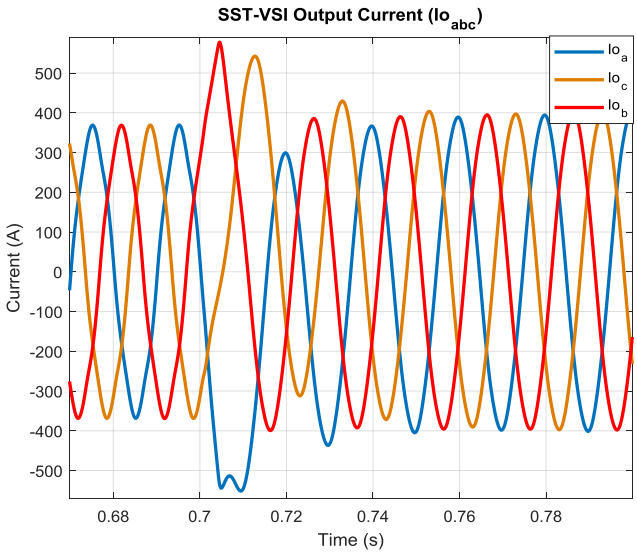


Figure 26. SST output current to the load. The figure is displaying the shift in phase of the current from the resistive load to inductive load at 0.7 s.

As the load shifted at 0.7 s, output current increased for a cycle to fulfill the instant lagging reactive power demand of the load and then settled down. During and after this transition time, the SST input voltage (phase A) and current (phase A) at the grid side remained in phase, as shown in Figure 27, thus supplying power at the unity power factor just like the previous scenario. The three phase supply current to the SST at the grid side was still balanced and harmonic content was still low. These results are depicted in Figure 28.

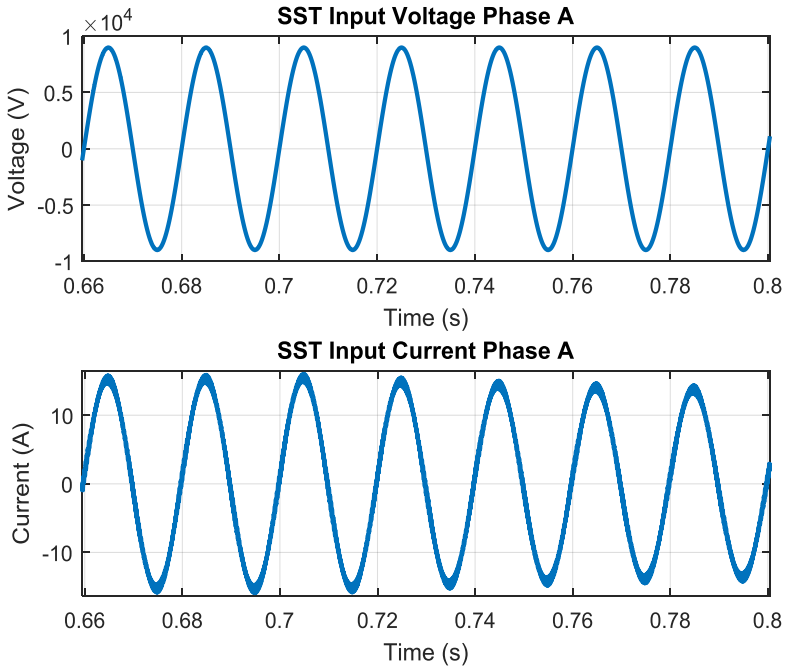
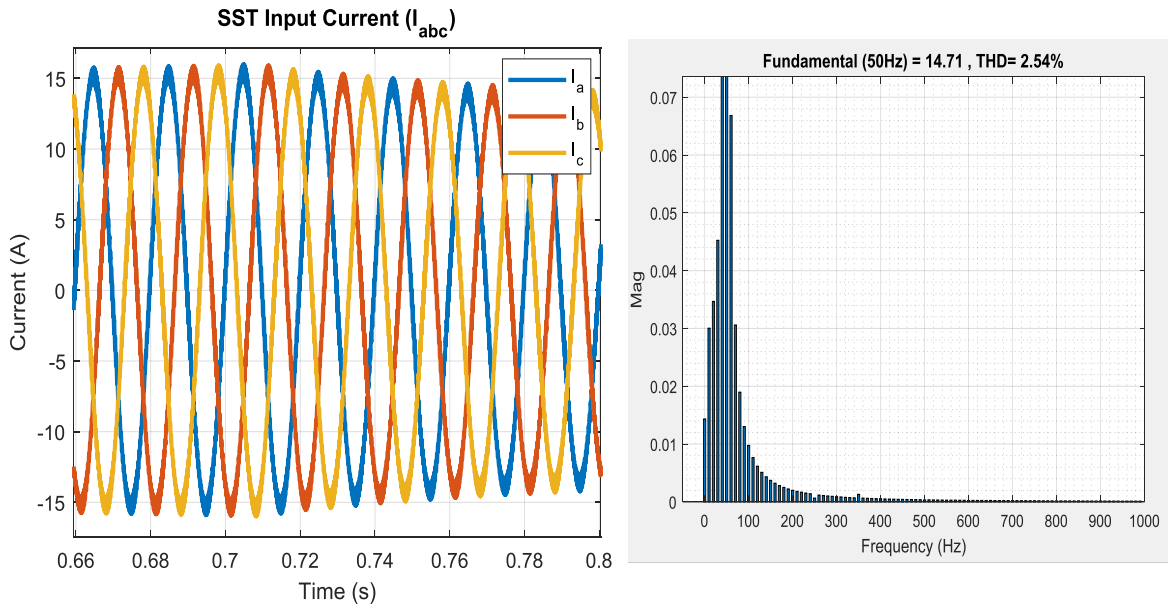


Figure 27. Result displaying that phase A voltage and current are in phase.



(**a**) (**b**)

Figure 28. (**a**) SST input current at the grid side. (**b**) THD analysis of phase A input current.

Figure 29 shows the output current of the SST at the instant when the pure inductive load was disconnected at 1.4 s, and pure capacitive load was connected instantly. Again from Figure 29, the phase shift in the output current could be visualized easily. As the load was instantly shifted to capacitive

nature, the instant leading reactive power demand caused the output current of the SST to be increased at 1.4 s. The current settled down when the transient period of one cycle elapsed.

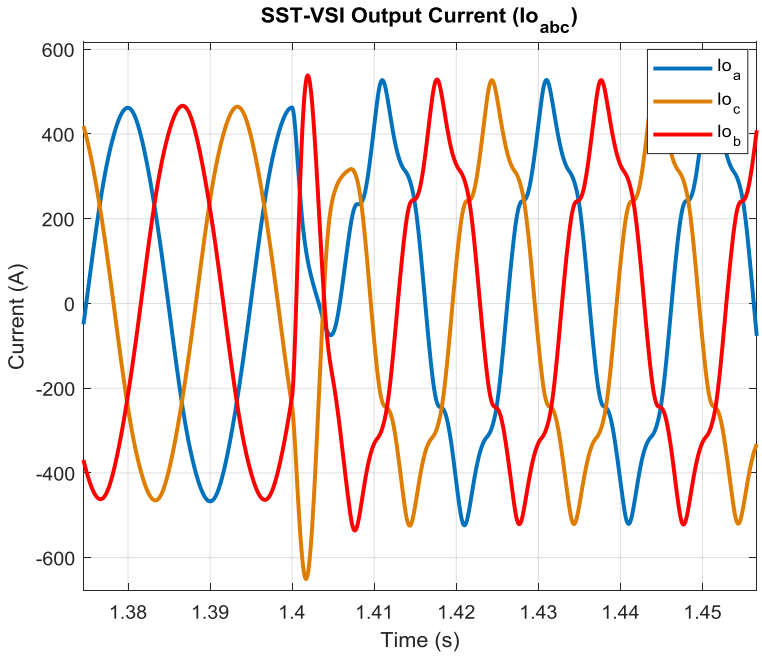


Figure 29. SST output current to the load. The figure is displaying the shift in current from the inductive load to the capacitive load at 1.4 s.

During and after the instant when SST shifted from delivering lagging VARs to the leading VARs, SST maintained its feature of operating at the unity power factor. Only for phase A, in-phase SST input voltage and input current are shown in Figure 30 while the same results were valid for the other phases as well.

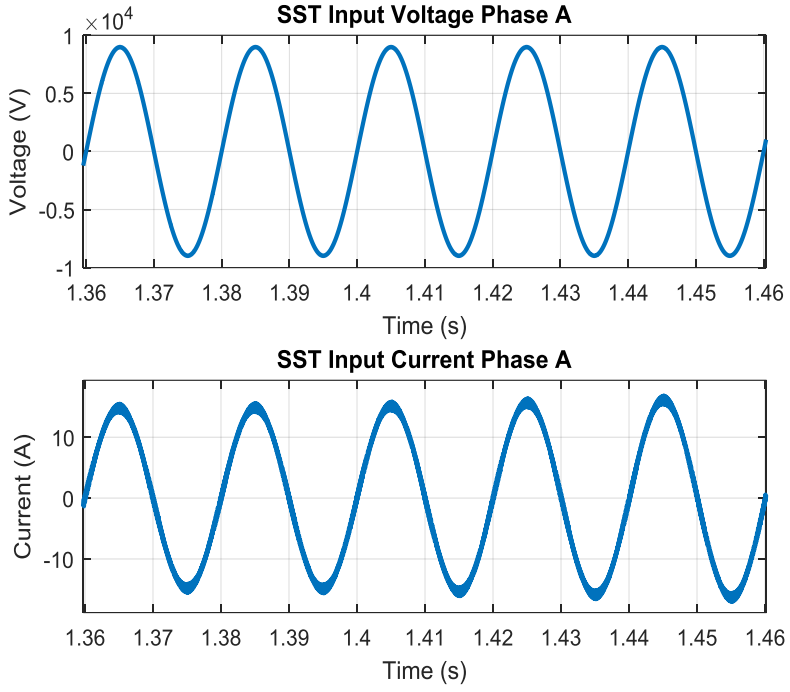


Figure 30. Result displaying that phase A voltage and current are in phase.

SST still maintained the balanced three phase current at the grid side with only 1.89% THD. These results are shown in Figure 31.

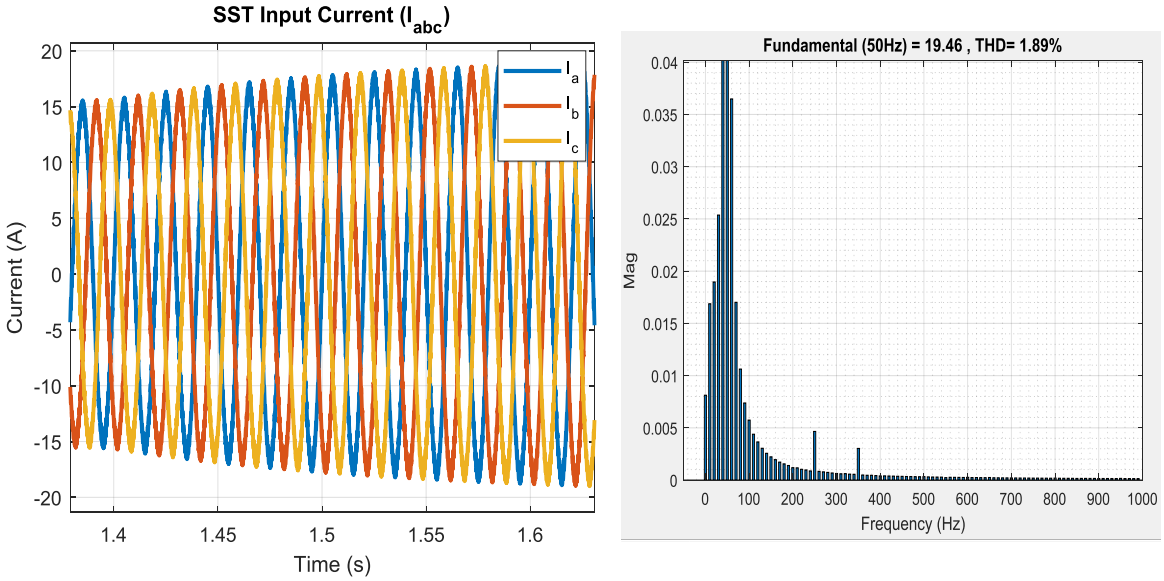


Figure 31. (**a**) SST input current at the grid side. (**b**) THD analysis of the phase A input current.

When the load shifted to capacitive nature, the output current of the SST increased at 1.4 s as shown in Figure 29. Figure 31 displays yet another interesting result. Input current to the SST from the grid side also increased at 1.4 s, but the THD of the balanced input current was further decreased.

4. Conclusions

To replace conventional bulky transformers, a reduced-size 'isolated' SST was proposed in this research. Either the source was single phase, three phase or DC source. The proposed SST model could generate the single phase, three phase or DC voltage for any type of resistive or inductive load. When interfaced with RES, the symmetric configuration of SST made it working as a stand-alone system at the consumer end as well as the grid-tied inverter at the grid side. Simulation results were assessed for scenarios where SST acted as a variable frequency drive and as a power factor improvement device. In addition, when interfaced with RES, SST ensured bidirectional power flow as well. Simulation results validated the performance of the proposed SST for all the scenarios. Working of SST as the VFD and PFI device with a renewable interface makes it ideal for industrial applications where the proposed SST topology may eliminate the requirements of bulky conventional transformer especially for motor drive applications. This justifies the role of SST as VFD. The four-quadrant operation of controlled switches with the DC port within SST enables it to be integrated with the micro/super grids. The proposed SST design has the ability to reject grid side disturbances, and regulate VAR at the grid side and voltage levels for the consumer end. The presented topology of SST can easily support the wide range operation of the distribution system. Future work would be development of the hardware setup for the proposed SST topology, thus to check the validity of the proposed SST model on real time industrial applications. Apart from SST design, optimized integration of SST with hybrid-RES would be a design worth of importance.

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Abbreviations

The following abbreviations are used in this research article:

SST	Solid State Transformer
RESs	Renewable Energy Resources
THD	Total Harmonic Distortion
PI	Proportional Integral
PWM	Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
HVDC	High Voltage Direct Current
FACT	Flexible Alternating Current Transmission
SVC	Static VAR Compensator
STATCOM	Static Synchronous Compensators
UPFC	Unified Power Flow Controllers
IGBT	Insulated Gate Bipolar Junction Transistor
VFD	Variable Frequency Drive
DAB	Dual Active Bridge
VOC	Vector (oriented) Current Control
OCC	Outer Current Control
ICC	Inner Current Control
MIMO	Multi-Input Multi-Output
PCC	Point of Common Coupling
PLL	Phase Locked Loop
IMC	Internal Model Control
PFI	Power Factor Improvement
HFT	High Frequency Transformer
VAR	Volt Ampere Reactive

Notations

The following notations are used in this research article:

Vx	DC voltage at DAB end/input of SST-VSI
$V_{DC,mes}$	DC voltage at SST-VSC end/input of DAB
V_{out}	output voltage of the SST
f_{out}	output frequency of the SST
pc	point of common coupling
v_S	voltage source at converter side
P_{mes}	measured active power
P_{ref}	reference of active power
Q_{mes}	measured reactive power
Q_{ref}	reference of reactive power
$V_{AC,mes}$	measured AC voltage
$V_{AC,ref}$	reference of AC voltage
i_S	current from grid to the SST
i_d	direct component of current
i_q	quadrature component of current
$i_{d,ref}$	reference for d-axis component of current
$i_{q,ref}$	reference for q-axis component of current
e_c	grid voltage
e_d	d-axis component of grid voltage
e_q	q-axis component of grid voltage
$V_{d,ref}$	d-axis component of reference voltage from inner current loop
$V_{q,ref}$	q-axis component of reference voltage from inner current loop
$V_{abc,ref}$	three phase voltage reference signals

k_p	proportional gain of PI controller
k_i	integral gain of PI controller
α_{ICC}	bandwidth of the current controlled system
m	modulation index
f_s	switching frequency
T_1, T_2, T_Z	dwell time of space vector signals in SVPWM
T_S	total time space vector signals in each sub cycle of SVPWM
p.u.	per unit

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