nanomaterials

MDPI

Communication

Generation and Storage of Random Voltage Values via Ring Oscillators Comprising Feedback Field-Effect Transistors

Jaemin Son, Juhee Jeon, Kyoungah Cho * and Sangsig Kim *

Department of Electrical Engineering, Korea University, 145 Anam-ro, Seongbuk-gu, Seoul 02841, Republic of Korea; jaeminson@korea.ac.kr (J.S.); isdf35@korea.ac.kr (J.J.)

* Correspondence: chochem@korea.ac.kr (K.C.); sangsig@korea.ac.kr (S.K.); Tel.: +82-2-3290-3245 (S.K.); Fax: +82-2-3290-3894 (S.K.)

Abstract: In this study, we demonstrate the generation and storage of random voltage values using a ring oscillator consisting of feedback field-effect transistors (FBFETs). This innovative approach utilizes the logic-in-memory function of FBFETs to extract continuous output voltages from oscillatory cycles. The ring oscillator exhibited uniform probability distributions of 51.6% for logic 0 and 48.4% for logic 1. The generation of analog voltages provides binary random variables that are stored for over 5000 s. This demonstrates the potential of the ring oscillator in advanced physical functions and true random number generator technologies.

Keywords: field-effect transistor; positive feedback loop; oscillator; physical unclonable function; random number generator

Citation: Son, J.; Jeon, J.; Cho, K.; Kim, S. Generation and Storage of Random Voltage Values via Ring Oscillators Comprising Feedback Field-Effect Transistors. *Nanomaterials* **2024**, *14*, 562. https://doi.org/10.3390/nano14070562

Academic Editor: Ding Li

Received: 19 February 2024
Revised: 20 March 2024
Accepted: 21 March 2024
Published: 23 March 2024

1. Introduction

Modern computing systems have witnessed rapid development with data-intensive applications, such as artificial intelligence and the Internet of Things [1,2]. However, significant security problems arise, as vast amounts of data are digitally stored in the memory units of computers, where the data are easily accessible and thereby vulnerable to cyberthreats [3]. A practical method to protect data from cyberattacks is to utilize physical unclonable functions (PUFs) or true random number generators (TRNGs), which provide cryptographic keys [4,5]. Unlike data security algorithms, PUFs and TRNGs produce unpredictable cryptographic values because of the inherent randomness of their component devices. This randomness primarily originates from fabrication process variations and stochastic mechanisms that cannot be physically duplicated or cloned [6]. Therefore, PUFs and TRNGs are the key building blocks in the design of security systems.

Recently, nonvolatile random-access memories (RAMs), including ferroelectric RAMs (FRAMs) [7,8], magnetic RAMs (MRAMs) [9–11], and resistive RAMs (ReRAMs) [12–14], have been introduced to generate random variables by exploiting inherent stochastic phenomena. Nonvolatile RAMs utilize various stochastic parameters, such as random telegraph noise, internal latency variations, cycle-to-cycle variations, and device-to-device variations. The unpredictability of the variables and operational stability should be ensured when using their stochastic parameters as sources of random variables. The stochastic nature of nonvolatile RAMs improves the entropy rates of random variables compared with PUFs and TRNGs. However, this deteriorates the device performance and stability during cycling [15]. In particular, FRAMs and ReRAMs suffer from low cycle-to-cycle endurance properties, which leads to a loss of probability distribution for random variables. The thermal instabilities and high energy consumption of MRAMs because of their high current density remain challenging, although they have better cycle-to-cycle endurance than other nonvolatile RAMs.

Feedback field-effect transistors (FBFETs) are emerging as a solution for PUF and TRNG applications because of their exceptional stability under both operational and envi-

ronmental conditions [16–18]. They operate with logic-in-memory (LIM) functions because of their unique positive feedback mechanism, which allows their logic circuits to store logical states [19–21]. In particular, the continuous output voltages of ring oscillators consisting of FBFETs can be extracted using the LIM functions. These LIM functionalities are advantageous for implementing advanced PUF and TRNG applications. Therefore, in this paper, we propose the generation and storage of random voltages using ring oscillators. Random voltages can be derived from oscillatory cycles and can be preserved for several hundreds to thousands of seconds.

2. Simulation Methods

Electrical characteristics of FBFETs, inverters, and ring oscillators were simulated using a commercial two-dimensional device simulator (Synopsys Sentaurus (O_2018.06)) [22]. In these simulations, the physical models for FBFETs included Fermi–Dirac statistics and Slotboom bandgap narrowing models. For a detailed recombination analysis, doping-dependent Shockley–Read–Hall and Auger models were used. Moreover, we analyzed the silicon regions using models for both inversion and accumulation layer mobilities and high-field saturation mobility, with default parameters for all the models. The detailed simulation models and parameters are listed in Table S1, Supporting Information.

3. Results and Discussion

The cross-sectional views of an *n*-channel FBFET (*n*-FBFET) and a *p*-channel FBFET (*p*-FBFET) are shown in Figures 1a and 1b, respectively. Both the FBFETs consisted of a *p*-type doped drain, an *n*-type doped source, and gated/nongated channel regions. Al_2O_3 gate oxide layers and metal gate electrodes (work function = 4.6 eV) were stacked on the top and bottom of the *p*-type doped channel for the *n*-FBFET and the *n*-type doped channel for the *p*-FBFET. These FBFETs had identical dimensional parameters and doping concentrations in each region. The gated channel length (L_{gated}), nongated channel length ($L_{\text{non-gated}}$), silicon channel thickness (T_{Si}), and gate oxide thickness (T_{ox}) were 50, 50, 10, and 3 nm, respectively. The doping concentration of the *p*-type doped drain, *n*-type doped source, and nongated regions (the *n*-type doped channel for the *n*-FBFET and the *p*-type doped channel for the *p*-FBFET) was 1×10^{20} cm^{-3}. The doping concentration of the gated regions (the *p*-type doped channel for the *n*-FBFET and the *n*-type doped channel for the *p*-FBFET) was 8×10^{19} cm^{-3}. The FBFETs were designed to accurately represent a 3D nanosheet gate-all-around structure. The silicon channel width (W_{Si}) was set to be equal to the T_{Si} = 10 nm, and the gate electrodes at the top and bottom of the silicon channel were coupled together. Their *p*–*n*–*p*–*n* doping structures generate a positive feedback mechanism, which is a reciprocal interaction between the channel potential barriers and the charge carriers. The generation and elimination of a positive feedback loop in the channel region enable rapid switching. In the positive feedback loop, charge carriers accumulate in or are removed from the channel potential wells. The presence or absence of charge carriers in the channel regions results in bistable memory states, allowing FBFETs to operate as switchable-memory devices [23]. Furthermore, the FBFET structures are compatible with CMOS top-down fabrication techniques. The nano-scale silicon channels of the FBFETs can be achieved by stacking Si/SiGe multilayers [24]. The selective removal of the sacrificial SiGe layers enables the devices to be formed as a vertical nanosheet gate-all-around structure. Also, the *p*–*n*–*p*–*n* doping structures can be created using conventional photolithography and an ion implantation process, indicating that the fabrication of the silicon-based FBFETs is cost-efficient and straightforward.

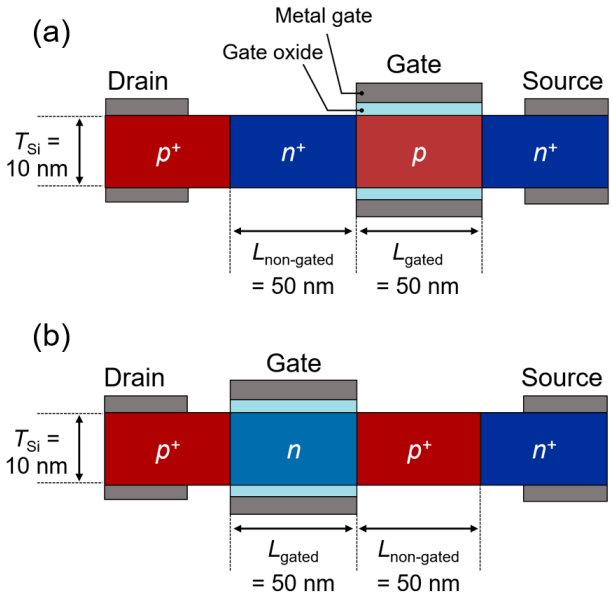

Figure 1. Cross-sectional schematics of (**a**) *n*-FBFET and (**b**) *p*-FBFET.

Figure 2a,b shows the transfer characteristics of the *n*- and *p*-FBFETs, respectively. Negative source voltages (V_S) and positive drain voltages (V_D) were applied to the *n*- and *p*-FBFETs, respectively, based on the configurations of the inverters and ring oscillators. During the forward and reverse gate voltage (V_G) sweeps, latch-up/latch-down phenomena were observed in both the *n*- and *p*-FBFETs, owing to the generation and elimination of the positive feedback loop in their channels. Both the *n*- and *p*-FBFETs exhibited an excellent switching performance, including ON/OFF current ratios (approximately 10^{11}), low OFF currents (approximately 10^{-16} A), and extremely low subthreshold swings (<1 mV/dec). Furthermore, these FBFETs exhibited memory windows defined by the differences between the latch-up and latch-down voltages resulting from the accumulation of charge carriers in the channel potential wells during the positive feedback loop. The positions and widths of the memory windows can be adjusted using the supply voltages (V_D and V_S) or V_G. Considering the experimental fabrication environment, the lateral diffusion effect of the interfaces between the doping regions is investigated in Figure S1, Supporting Information.

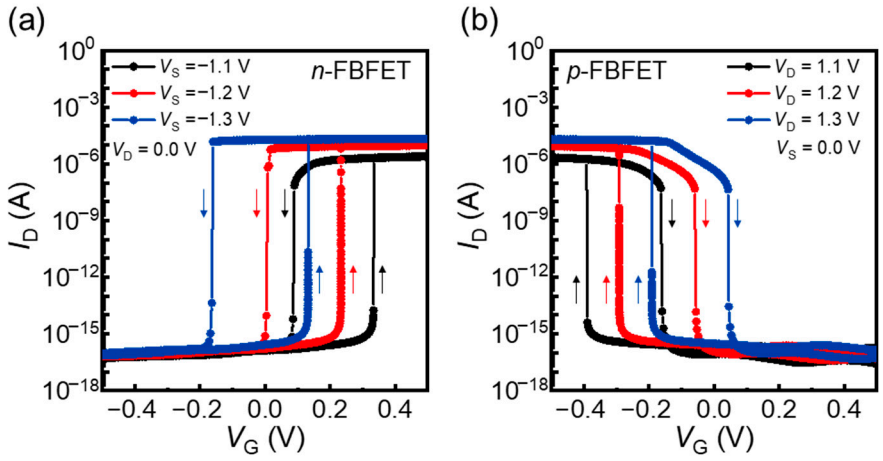

Figure 2. Transfer characteristics of (**a**) *n*-FBFET depending on V_S and (**b**) *p*-FBFET depending on V_D.

On the other hand, the different electrical characteristics between the *n*- and *p*-FBFETs are caused by the different type of the minority charge carriers; the minority charge carriers of the *n*- and *p*-FBFETs are holes and electrons, respectively. These minority charge carriers are key to maintaining the positive feedback loop by continuously accumulating in the po-

tential wells. Generally, electron recombination is much faster than hole recombination [25]. Consequently, the positive feedback loop in the *p*-FBFET exhibits a relatively lower strength compared to that of the *n*-FBFET. However, the rapid electron recombination in the *p*-FBFET can be mitigated by reducing the channel length (L_{ch}) and increasing the T_{Si}. A shorter L_{ch} enhances the charge carrier accumulation, and a thicker T_{Si} increases the amount of charge carriers to flow. Thus, the differences between the *n*- and *p*-FBFETs can be alleviated by adjusting the channel dimension parameters, T_{Si} and L_{ch}.

To evaluate the memory and logic capabilities, we configured the *n*- and *p*-FBFETs into a standard inverter circuit, as depicted in Figure 3a. A parasitic load capacitor (C_L) of 1 fF was connected to the output node to reflect the output capacitances of the inverter and the interconnection line capacitances between the logic gates. Figure 3b shows the static voltage transfer characteristics (VTC) of the inverter. The inverter exhibited a notably high inverter gain with the maximum gain estimated as 3.56×10^5 V/V at V_{DD} = 1.3 V and V_{SS} = −1.3 V. In forward and reverse input voltage (V_{IN}) sweeps, clockwise voltage memory windows were observed owing to the inherent memory characteristics of FBFETs. The inverter can maintain the logic states within the V_{IN} range that corresponds to the memory windows; logic 0 and 1 are held during the forward and reverse V_{IN} sweeps, respectively. For the supply voltages, symmetrical positive V_{DD} and negative V_{SS} values were selected to ensure that the memory window included a V_{IN} of 0.0 V. The voltage condition of V_{IN} = 0.0 V was used for the memory operation of the inverter, enabling the minimization of energy consumption. As for the V_{OUT} values, the voltage values of logic 0 and 1 were negative and positive, respectively, because of the use of positive V_{DD} and negative V_{SS} values.

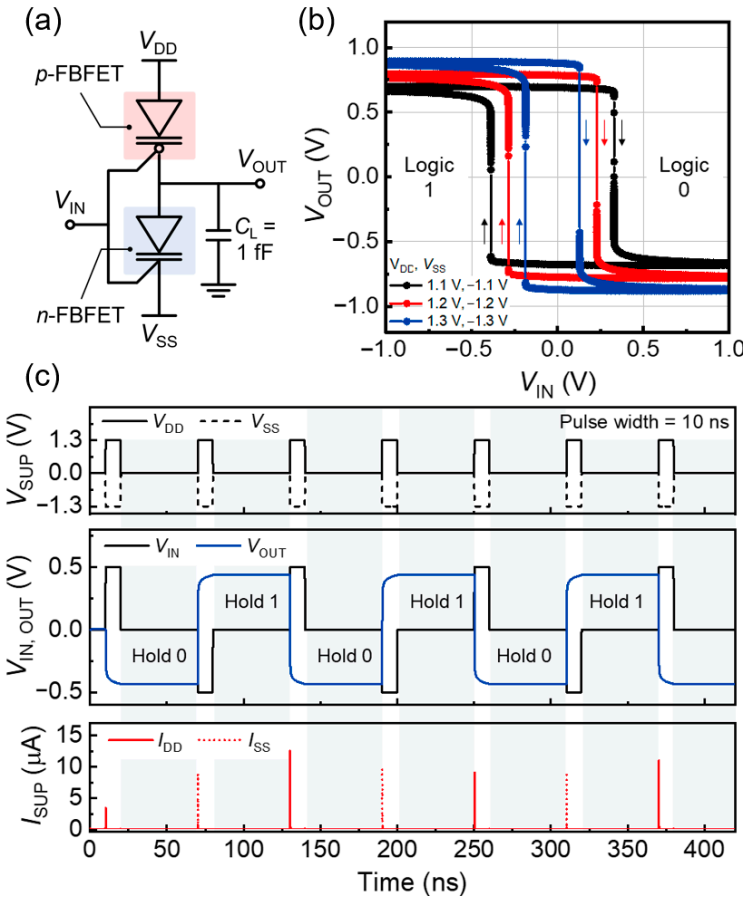

Figure 3. (**a**) Schematic of an inverter consisting of *n*- and *p*-FBFETs. (**b**) VTCs and (**c**) dynamic LIM operation of the inverter.

The inverter performs LIM operations using a memory window within its static VTC. Figure 3c shows the dynamic V_{OUT} responses under a sequence of voltage pulses of logic 0

and 1 with the supply voltages set at V_{DD} = 1.3 V and V_{SS} = −1.3 V. Following each logic pulse of 10 ns, the supply voltages (V_{DD} and V_{SS}) and V_{IN} are reset to 0.0 V for the hold operations. During the hold operations, the inverter maintains its logic state (logic 0 or 1) because of the accumulation of charge carriers in the channels of the component devices. This accumulation causes the component devices to be charged; the *n*- and *p*-FBFETs become charged after the voltage pulses of logic 0 and 1, respectively. Thus, the inverter effectively preserves the logic state without the need for an external bias. Furthermore, FBFETs exhibit quasi-nonvolatile memory characteristics with a duration of hundreds of seconds, surpassing the performance of other charge-based memory transistors [26]. Their superior memory retention capabilities are detailed in our previous work [27,28].

The capability of the FBFETs to maintain the V_{OUT} values offers diverse applications when integrated into logic cascading levels beyond a single-inverter circuit. In particular, in oscillatory operations where the output voltages vary continuously, the LIM functions of the FBFETs can be utilized to generate various V_{OUT} values. To explore the oscillatory behavior of the FBFETs, we configured a three-stage ring oscillator by connecting three inverters, as shown in Figure 4a. Each inverter was connected in sequence, and the output of the final inverter was fed back to the first input to achieve continuous oscillations. The parasitic C_Ls at the output nodes of each inverter were set to 1 fF. Figure 4b shows the transient output characteristics of the three-stage ring oscillator at V_{DD} = 1.3 V and V_{SS} = −1.3 V. Each stage of the output node voltages exhibited self-sustained oscillations that ranged from −0.4 V to 0.4 V with a phase shift of 2π/3 (120°) during oscillation, which is attributed to a π/3 phase shift from each inverter and a π phase shift from static inversion. The ring oscillator frequency (f_{RO}) was obtained using the equation $f_{RO} = (2 \times n \times T_d)^{-1}$, where n is the number of stages, and T_d is the inverter stage delay. For this ring oscillator, T_d and f_{RO} are estimated to be 0.75 ns and 220 MHz, respectively.

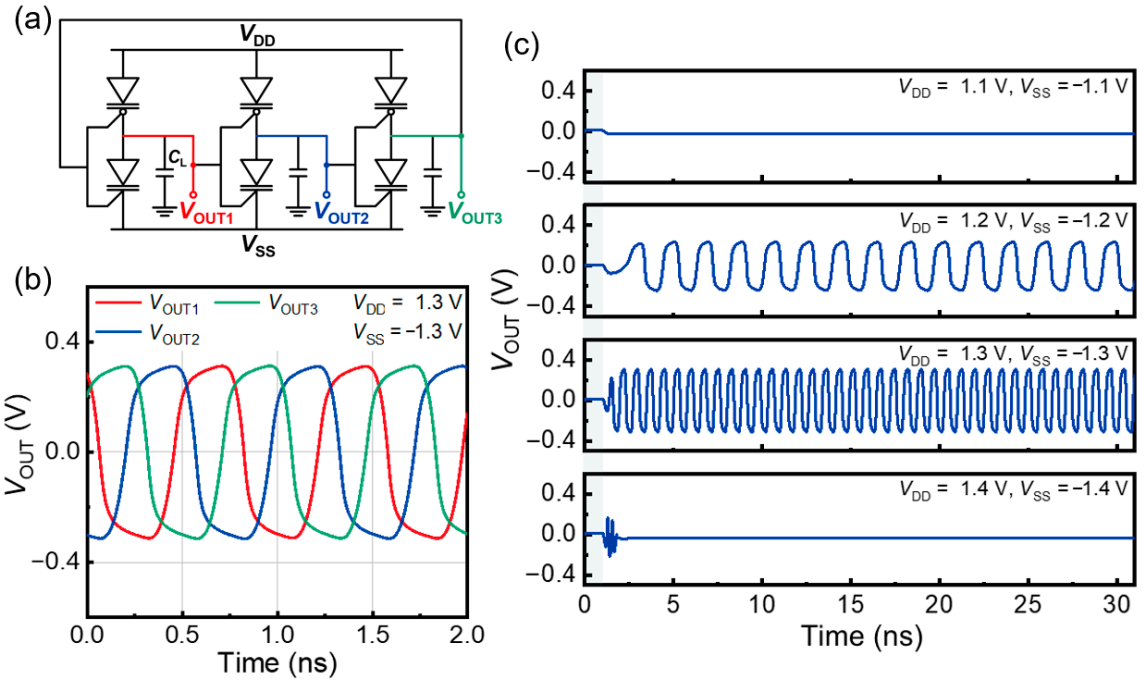

Figure 4. (**a**) Schematic of a three-stage ring oscillator consisting of *n*- and *p*-FBFETs. (**b**) Transient output characteristics of each stage at V_{DD} = 1.3 V and V_{SS} = −1.3 V and (**c**) under various supply voltages.

The transient output characteristics of the ring oscillator at various supply voltages are shown in Figure 4c. When the absolute values of the supply voltages were set at 1.1 V, oscillation did not occur because the V_{OUT} levels of each inverter were insufficient to serve as V_{IN} for the subsequent inverter stages. By contrast, at the absolute supply voltage values of 1.2 V or 1.3 V, the ring oscillator began to oscillate, owing to the adequate V_{OUT} levels of each

inverter. The frequency of these oscillations can be modulated by varying the supply voltage, allowing the system to function as a voltage-controlled oscillator [29]. However, when the absolute values of the supply voltages exceeded 1.4 V, both the *n*- and *p*-FBFETs were turned ON simultaneously, thereby interrupting the oscillation. The excessive accumulation of charge carriers in the channel regions of the FBFETs at high supply voltages interrupts the oscillation.

Analog voltages were randomly generated by the ring oscillator. Figure 5a,b shows the V_{OUT} values of the ring oscillator as a function of time under repetitive power ON (V_{DD} = 1.3 V and V_{SS} = −1.3 V) and power OFF (V_{DD} = V_{SS} = 0.0 V) cycles; in this figure, for the hold operation, the power is OFF. The V_{OUT} values depend on the number of charge carriers accumulated in the channels of the *n*- and *p*-FBFETs, and these values are preserved by the component inverters when the power is switched OFF. When the power was restored, the ring oscillator immediately returned to its oscillatory state without warm-up time. Consequently, the ring oscillator generated and stored random analog voltage values.

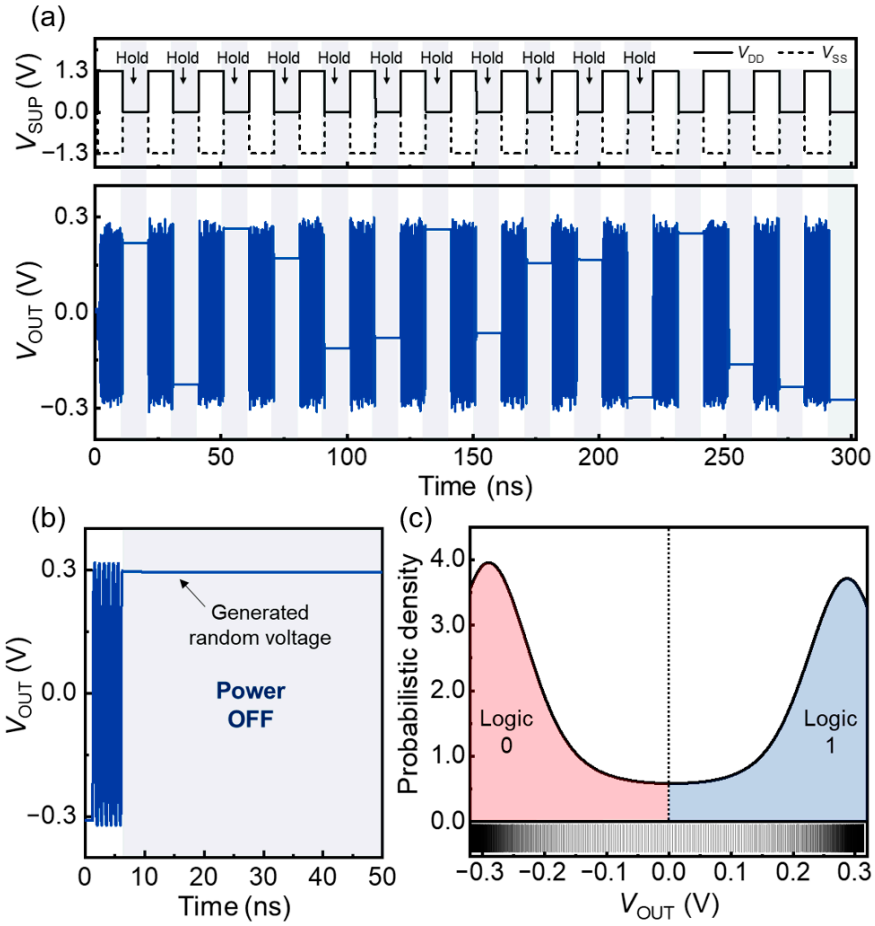

Figure 5. (**a**) Overall and (**b**) detailed memory operations of the ring oscillator under repetitive power ON/OFF cycles. (**c**) Probability density of V_{OUT} values extracted from the oscillatory cycles.

Like other hardware-based TRNG and PUF circuits, the randomness of the FBFET-based ring oscillator comes from the variation in the fabrication and internal latency. Due to the nature of the processes, the speed and amount of the charge carrier accumulation in the FBFET channels differ slightly for every operation, which leads to latency variations. Also, the irregular timing of the power ON/OFF cycles is a random factor for our ring oscillator. Figure 5c illustrates the probability density distribution of the V_{OUT} values extracted from the oscillatory cycles of the ring oscillator. In the distribution, the probability density is congregated at the crest and trough of the oscillation (−0.3 V and 0.3 V) owing to the sine waveform of the oscillation. To use the V_{OUT} of the ring oscillator as a random variable, the probabilities

of the variables should be uniformly distributed and possess a wide bandwidth [15,30]. Therefore, we divided the probability distribution of the V_{OUT} values into two distinct domains: negative and positive V_{OUT} domains, representing logic 0 and 1, respectively. Using this approach, the probabilities of logic 0 and 1 were estimated to be 51.6% and 48.4%, respectively, demonstrating a highly uniform distribution between the two domains. This configuration enabled the ring oscillator to function effectively as a TRNG.

The retention times of the random voltages generated by the oscillations were analyzed to validate the memory stability of the ring oscillator. Figure 6 shows the V_{OUT} retention times of each inverter stage in the three-stage ring oscillator. To generate random voltage signals, supply voltage pulses with durations of 10 ns were applied to the ring oscillator. Following the supply voltage pulses, all the external biases were reset to 0.0 V for 10^5 s to verify the V_{OUT} retention times. During the hold operation, the V_{OUT} values of the ring oscillator decreased toward 0.0 V, owing to the loss of accumulated charge carriers of the component devices. The ring oscillator effectively maintained the V_{OUT} value for an initial holding time of 200 s, and the average degradation of the V_{OUT} value was only 10.6%. The retention time was defined as the time at which the initial V_{OUT} value decreased to 63% of its original value following the standard time constant principle [31]. The average V_{OUT} retention time of the ring oscillator was estimated to be approximately 5500 s, demonstrating robust memory stability. On the other hand, the V_{OUT} retention time of the ring oscillator is affected by the T_{Si} (Figure S2, Supporting Information). As the T_{Si} thickens, the average V_{OUT} retention time decreases. This decrease is due to the bulk recombination, which intensifies with an increase in the channel depth [32]. As a result, thinner T_{Si} is required to provide sufficient V_{OUT} retention time. Nevertheless, the ring oscillator generates analog random voltage signals and stores their values with a significant retention time. These operations are beneficial for security applications, offering a robust method for generating and storing PUF keys in several ring oscillators [33,34].

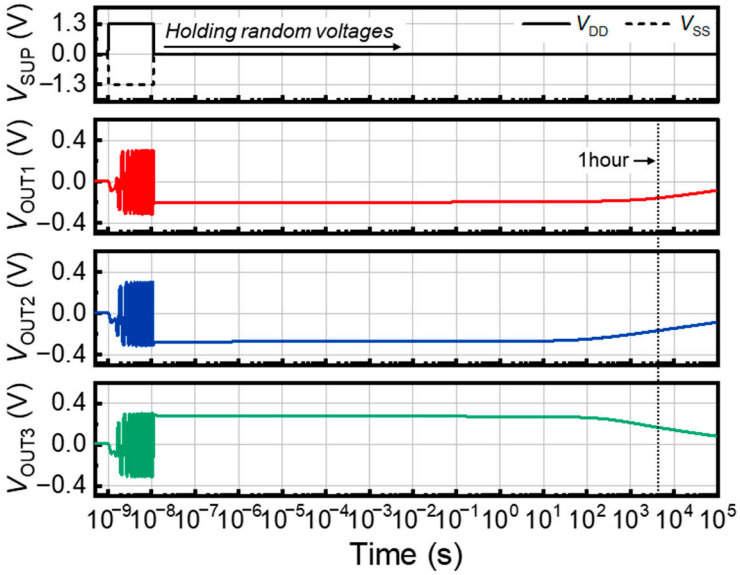

Figure 6. V_{OUT} retention properties of the ring oscillator.

4. Conclusions

This study demonstrated the generation and storage of random voltage values with a ring oscillator consisting of *n*- and *p*-FBFETs using computer-aided design simulations. The ring oscillator exhibited dual capabilities of generating and storing random voltages during power ON/OFF cycles by utilizing the LIM functions of the component devices. The probability distribution of the V_{OUT} values of the ring oscillator can be divided into two distinct domains: logic 0 and 1. The probabilities were close to 50%. Moreover, the ring

oscillator demonstrated the self-storage capability of random variables, with a retention time of approximately 5500 s.

Supplementary Materials: The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/nano14070562/s1, Table S1. Detailed simulation models and parameters; Table S2. Randomness test results of the FBFET-based ring oscillator under NIST SP800-22 test suite; Figure S1. Schematic diagrams and transfer characteristics of (a) n-FBFETs and (b) p-FBFETs with various gaussian doping profiles; Figure S2. Positive and negative VOUT retention properties of ring oscillators with various TSi.

Author Contributions: Conceptualization, J.S. and S.K.; methodology, J.J.; software, J.S. and J.J.; validation, J.S., K.C. and S.K.; formal analysis, J.S. and K.C.; investigation, J.S. and S.K.; data curation, J.J.; writing—original draft preparation, J.S.; writing—review and editing, K.C. and S.K.; visualization, J.S.; supervision, K.C. and S.K.; project administration, S.K.; funding acquisition, S.K. All authors have read and agreed to the published version of the manuscript.

Funding: This study was supported by the National R&D Program through the National Research Foundation of Korea (NRF), funded by the Ministry of Science and ICT (2020R1A2C3004538, 2022M3I7A3046571, and RS-2023-00260876); the Brain Korea 21 Plus Project in 2024 through the NRF, funded by the Ministry of Science, ICT and Future Planning; and a Korea University Grant.

Data Availability Statement: Data are contained within the article and Supplementary Materials.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Abiodun, O.I.; Jantan, A.; Omolara, A.E.; Dada, K.V.; Mohamed, N.A.; Arshad, H. State-of-the-art in artificial neural network applications: A survey. *Heliyon* **2018**, *4*, e00938. [CrossRef] [PubMed]
2. Chen, J.; Ran, X. Deep learning with edge computing: A review. *Proc. IEEE* **2019**, *107*, 1655–1674. [CrossRef]
3. Shamsoshoara, A.; Korenda, A.; Afghah, F.; Zeadally, S. A survey on physical unclonable function (PUF)-based security solutions for Internet of Things. *Comput. Netw.* **2020**, *183*, 107593. [CrossRef]
4. Gao, Y.; Al-Sarawi, S.F.; Abbott, D. Physical unclonable functions. *Nat. Electron.* **2020**, *3*, 81–91. [CrossRef]
5. Lanza, M.; Sebastian, A.; Lu, W.D.; Le Gallo, M.; Chang, M.F.; Akinwande, D.; Puglisi, F.M.; Alshareef, H.N.; Liu, M.; Roldan, J.B. Memristive technologies for data storage, computation, encryption, and radio-frequency communication. *Science* **2022**, *376*, eabj9979. [CrossRef]
6. Al-Meer, A.; Al-Kuwari, S. Physical unclonable functions (PUF) for IoT devices. *ACM Comput. Surv.* **2023**, *55*, 1–31. [CrossRef]
7. Rashid, M.I.; Ferdaus, F.; Talukder, B.M.S.B.; Henny, P.; Beal, A.N.; Rahman, M.T. True random number generation using latency variations of FRAM. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2020**, *29*, 14–23. [CrossRef]
8. Chatterjee, S.; Rangarajan, N.; Patnaik, S.; Rajasekharan, D.; Sinanoglu, O.; Chauhan, Y.S. FerroCoin: Ferroelectric tunnel junction-based true random number generator. *IEEE Trans. Emerg. Top. Comput.* **2022**, *11*, 541–547. [CrossRef]
9. Song, B.; Lim, S.; Kang, S.H.; Jung, S.-O. Environmental-variation-tolerant magnetic tunnel junction-based physical unclonable function cell with auto write-back technique. *IEEE Trans. Inf. Forensics Sec.* **2021**, *16*, 2843–2853. [CrossRef]
10. Finocchio, G.; Moriyama, T.; De Rose, R.; Siracusano, G.; Lanuzza, M.; Puliafito, V.; Chiappini, S.; Crupi, F.; Zeng, Z.; Ono, T.; et al. Spin–orbit torque based physical unclonable function. *J. Appl. Phys.* **2020**, *128*, 033904. [CrossRef]
11. Khan, M.N.I.; Cheng, C.Y.; Lin, S.H.; Ash-Saki, A.; Ghosh, S. A morphable physically unclonable function and true random number generator using a commercial magnetic memory. *J. Low Power Electron. Appl.* **2021**, *11*, 5. [CrossRef]
12. Aziza, H.; Postel-Pellerin, J.; Bazzi, H.; Canet, P.; Moreau, M.; Della Marca, V.D.; Harb, A. True random number generator integration in a resistive RAM memory array using input current limitation. *IEEE Trans. Nanotechnol.* **2020**, *19*, 214–222. [CrossRef]
13. Ielmini, D.; Wong, H.-S.P. In-memory computing with resistive switching devices. *Nat. Electron.* **2018**, *1*, 333–343. [CrossRef]
14. Lin, B.; Pang, Y.; Gao, B.; Tang, J.; Wu, D.; Chang, T.-W.; Lin, W.-E.; Sun, X.; Yu, S.; Chang, M.-F.; et al. A highly reliable RRAM physically unclonable function utilizing post-process randomness source. *IEEE J. Solid-State Circuits* **2021**, *56*, 1641–1650. [CrossRef]
15. Chai, J.; Tong, S.; Li, C.; Manzano, C.; Li, B.; Liu, Y.; Lin, M.; Wong, L.; Cheng, J.; Wu, J.; et al. MoS2/polymer heterostructures enabling stable resistive switching and multistate randomness. *Adv. Mater.* **2020**, *32*, 2002704. [CrossRef] [PubMed]
16. Lee, C.; Ko, E.; Shin, C. Steep slope silicon-on-insulator feedback field-effect transistor: Design and performance analysis. *IEEE Trans. Electron Devices* **2018**, *66*, 286–291. [CrossRef]
17. Navarro, S.; Navarro, C.; Marquez, C.; Salazar, N.; Galy, P.; Cristoloveanu, S.; Gamiz, F. Reliability study of thin-oxide zero-ionization, zero-swing FET 1T-DRAM memory cell. *IEEE Electron Device Lett.* **2019**, *40*, 1084–1087. [CrossRef]
18. Jeon, J.; Cho, K.; Kim, S. Effects of interface states on electrical characteristics of feedback field-effect transistors. *IEEE Access* **2023**, *11*, 54692–54698. [CrossRef]

19. Baek, E.; Son, J.; Cho, K.; Kim, S. Design and Simulation of Logic-in-memory inverter based on a silicon nanowire feedback field-effect transistor. *Micromachines* **2022**, *13*, 590. [CrossRef] [PubMed]
20. Lee, K.; El Dirani, H.; Fonteneau, P.; Bawedin, M.; Sato, S.; Cristoloveanu, S. Sharp switching, hysteresis-free characteristics of Z^2-FET for fast logic applications. In Proceedings of the 2018 48th European Solid-State Device Research Conference (ESSDERC), Dresden, Germany, 3–6 September 2018; pp. 74–77. [CrossRef]
21. Lee, C.; Han, C.; Shin, C. Inverter design with positive feedback field-effect transistors. *Semicond. Sci. Technol.* **2022**, *37*, 035014. [CrossRef]
22. *Sentaurus Device User Guide*; Synopsys: Mountain View, CA, USA, 2018.
23. Lee, C.; Sung, J.; Shin, C. Understanding of feedback field-effect transistor and its applications. *Appl. Sci.* **2020**, *10*, 3070. [CrossRef]
24. Sun, X.; Wang, D.; Qian, L.; Liu, T.; Yang, J.; Chen, K.; Wang, L.; Huang, Z.; Xu, M.; Wang, C. A Novel Si Nanosheet Channel Release Process for the Fabrication of Gate-All-Around Transistors and Its Mechanism Investigation. *Nanomaterials* **2023**, *13*, 504. [CrossRef]
25. Kim, S.; Choi, S.-J.; Moon, D.-I.; Choi, Y.-K. Carrier lifetime engineering for floating-body cell memory. *IEEE Trans. Electron Devices* **2011**, *59*, 367–373. [CrossRef]
26. Lacord, J.; Parihar, M.S.; Navarro, C.; Wakam, F.T.; Bawedin, M.; Cristoloveanu, S.; Gamiz, F.; Barbé, J.-C.; Msdram, A. 2RAM and Z^2-FET performance benchmark for 1T-DRAM applications. In Proceedings of the 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Austin, TX, USA, 24–26 September 2018; pp. 198–201.
27. Lim, D.; Son, J.; Cho, K.; Kim, S. Quasi-nonvolatile silicon memory device. *Adv. Mater. Technol.* **2020**, *5*, 2000915. [CrossRef]
28. Han, S.; Kim, Y.; Son, D.; Baac, H.W.; Won, S.M.; Shin, C. Study on memory characteristics of fin-shaped feedback field effect transistor. *Semicond. Sci. Technol.* **2022**, *37*, 065006. [CrossRef]
29. Mayahinia, M.; Singh, A.; Bengel, C.; Wiefels, S.; Lebdeh, M.A.; Menzel, S.; Wouters, D.J.; Gebregiorgis, A.; Bishnoi, R.; Joshi, R.; et al. A voltage-controlled, oscillation-based adc design for computation-in-memory architectures using emerging rerams. *ACM J. Emerg. Technol. Comput. Syst.* **2022**, *18*, 1–25. [CrossRef]
30. Guerrer, G. RAVA: An open hardware true random number generator based on avalanche noise. *IEEE Access* **2023**, *11*, 119568–119583. [CrossRef]
31. Hertz, M.; Steinken, D. Dynamic in-line analysis of electrostatic discharge resistive-capacitive time constant. In Proceedings of the 2016 International Symposium on Electromagnetic Compatibility-EMC EUROPE, Wroclaw, Poland, 5–9 September 2016; pp. 870–875. [CrossRef]
32. Munteanu, D.; Ionescu, A.-M. Modeling of drain current overshoot and recombination lifetime extraction in floating-body submicron SOI MOSFETs. *IEEE Trans. Electron Devices* **2002**, *49*, 1198–1205. [CrossRef]
33. Ning, H.; Farha, F.; Ullah, A.; Mao, L. Physical unclonable function: Architectures, applications and challenges for dependable security. *IET Circuits Devices Syst.* **2020**, *14*, 407–424. [CrossRef]
34. Mostafa, A.; Lee, S.J.; Peker, Y.K. Physical unclonable function and hashing are all you need to mutually authenticate IoT devices. *Sensors* **2020**, *20*, 4361. [CrossRef]