



# Article Tunnel Oxides Formed by Field-Induced Anodisation for Passivated Contacts of Silicon Solar Cells

# Jingnan Tong <sup>1</sup>,\*, Sean Lim <sup>2</sup> and Alison Lennon <sup>1</sup>

- <sup>1</sup> School of Photovoltaic and Renewable Energy Engineering, UNSW, Sydney, NSW 2052, Australia; a.lennon@unsw.edu.au
- <sup>2</sup> Mark Wainwright Analytical Centre, UNSW, Sydney, NSW 2052, Australia; sean.lim@unsw.edu.au

\* Correspondence: jingnan.tong@unsw.edu.au; Tel.: +61-412-856-392

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**Abstract:** Tunnel silicon oxides form a critical component for passivated contacts for silicon solar cells. They need to be sufficiently thin to allow carriers to tunnel through and to be uniform both in thickness and stoichiometry across the silicon wafer surface, to ensure uniform and low recombination velocities if high conversion efficiencies are to be achieved. This paper reports on the formation of ultra-thin silicon oxide layers by field-induced anodisation (FIA), a process that ensures uniform oxide thickness by passing the anodisation current perpendicularly through the wafer to the silicon surface that is anodised. Spectroscopical analyses show that the FIA oxides contain a lower fraction of Si-rich sub-oxides compared to wet-chemical oxides, resulting in lower recombination velocities at the silicon and oxide interface. This property along with its low temperature formation highlights the potential for FIA to be used to form low-cost tunnel oxide layers for passivated contacts of silicon solar cells.

Keywords: tunnel silicon oxide; passivated contact; silicon solar cell; anodisation

## 1. Introduction

Ultra-thin and uniform silicon oxide  $(SiO_x)$  layers have played a key role as an interfacial layer in a number of high efficiency silicon solar cell designs, including acting as intermediate layers in metal-insulator-semiconductor (MIS) solar cells [1], enhancing passivation at amorphous/crystalline silicon (a-Si:H/c-Si) heterojunction interfaces [2–4] and passivating thin metal-oxide passivated contacts [5,6] and poly-silicon (poly-Si) contacts [7–14]. For full-area poly-Si contacts, the insertion of the SiO<sub>x</sub> layer between poly-Si and c-Si substrate provides effective interface passivation and allows one dimensional carrier flow through the solar cell [8]. These attributes have enabled energy conversion efficiencies exceeding 25% to be achieved [7,8,15,16]. Previous studies have shown that the quality of the tunnel oxide is of great importance to the cell performance [15]. To ensure high open-circuit voltages ( $V_{oc}$ ) and fill factors (*FF*), the SiO<sub>x</sub> layer needs to be homogeneous and as stoichiometric as possible to provide excellent passivation to the c-Si substrate and simultaneously to be sufficiently thin to ensure a low contact resistivity [9]. Moreover, the interface charge density of the tunnel layer has been reported to contribute to the effectiveness of field-effect passivation on silicon surfaces if a high positively-charged tunnel layer is adopted for electron-extracting contacts and high negatively-charged tunnel layer is used for hole-extracting contacts [17].

Oxidation techniques used to form ultra-thin  $SiO_x$  layers for poly-Si contacts include thermal oxidation [18–20], wet-chemical oxidation by HNO<sub>3</sub> [7,21,22] and ozone oxidation [15]. The former method requires critical wafer cleaning and a high thermal budget, which is not typically compatible with reducing manufacturing costs in the photovoltaic industry. Although the latter two techniques can potentially reduce process costs, the  $SiO_x$  layers grown by HNO<sub>3</sub> oxidation contain a high fraction of sub-oxides which are not ideal for interface passivation [15] and the ozone oxidation allows limited

control over oxide properties. Consequently, the development of a room temperature oxidation process that is more compatible with current cell production lines is desirable.

Grant et al. [23,24] reported room temperature anodisation of silicon in HNO<sub>3</sub> with the obtained oxide having a surface recombination velocity comparable to that of thermally-grown oxide after a low temperature anneal. However, the reported method was based on a traditional clipping arrangement where the applied bias generates a potential gradient laterally across the wafer, resulting in non-uniform oxidation. To address this issue, processes have been developed that use illumination or an electric field to induce a current flowing through the wafer in a direction that is perpendicular to the surface that is anodised [25–27]. These methods, which are called light-induced anodisation (LIA) and field-induced anodisation (FIA) respectively, offer the potential to uniformly anodise industrial-sized solar cells using a lower current than would be required by the clipping method.

In this paper, we extend the brief report on the formation of thin  $SiO_x$  layers on *n*-type silicon (*n*-Si) surfaces using FIA [28] with a more systematic study on the oxide stoichiometry and resulting passivation quality. The performance of the  $SiO_x$  layers is then compared to that of the wet-chemically grown oxides and thermally-grown oxides.

#### Overview of the FIA Process

Light-induced anodization can be used to oxidise *p*-type silicon (*p*-Si) surfaces of a solar cell [27,29]. SiO<sub>x</sub> layers of uniform thickness can be grown by placing the *p*-Si surface in contact with the electrolyte and using an external power source bias applied to the *n*-Si surface of the solar cell to offset resistive losses in the electrochemical circuit and enable the *p*-Si surface to be oxidised by the light-induced current of the solar cell. When oxidising *n*-Si surfaces of a solar cell, the FIA process can be employed with *n*-Si surfaces contacting the electrolyte and a positive bias voltage or current applied to the *p*-Si to forward bias the junction so that current can flow through the wafer to oxidise the *n*-Si surfaces.

It should be noted that when forward biasing a *p*-*n* junction in the FIA process, if the surfaces are not sufficiently doped, Schottky diodes can form with the depletion region extending further into the wafer with increasing anodisation bias and rectifying current flow through the wafer [30]. This can be addressed through the use of illumination to generate a photocurrent across the depletion regions at the silicon surfaces so that generated carriers can be swept out of the regions by the applied electric field, allowing current to flow through the wafer. The FIA process can also be used to grow silicon oxides on devices without p-n junctions. Figure 1 shows a schematic diagram of the FIA setup that can be used to anodise an *n*-Si wafer surface. The wafer is made anodic by applying a positive bias via a semi-transparent aluminum contact electrode which is applied uniformly over the wafer surface enabling the entire surface to be anodised. Even though the oxide may start to grow non-uniformly across the wafer surface, the anodization current continues to flow through less resistive paths until the resistance provided by the anodic oxide reaches the same through the entire wafer surface, securing a uniform final oxide thickness. The thickness of the oxide can be controlled by anodisation voltage/current, electrolyte constitution/concentration, and light intensity, suggesting FIA may be a promising alternative when forming a uniform and controllable tunneling  $SiO_x$  at room temperature.



Figure 1. Schematic diagram showing the field-induced anodisation (FIA) process.

## 2. Experimental

The samples used for the thickness and compositional study were phosphorus-doped (*n*-type) double-side polished Czochralski (Cz) (100) silicon wafers (4 cm  $\times$  4 cm) with a thickness of 525 µm and a resistivity of 0.8  $\Omega$ ·cm. The wafers were cleaned via a standard wafer cleaning sequence developed by the Radio Corporation of America (RCA) [31] followed by immersion in 1% (*w*/*v*) hydrofluoric acid (HF) for 2 min prior to the anodisation process. The wafers were then anodised in 0.5 M H<sub>2</sub>SO<sub>4</sub> with the voltage being sensed by a reference electrode. Considering the electrolyte may induce band bending at the silicon surface, an illumination was used to ensure photo-current flow across depletion regions that can form at the electrolyte interface [30].

The thickness of the oxide was evaluated using an ellipsometer from J.A Woollam Co., Inc., Lincoln, NE, USA, (M-2000VI) with a refractive index of 1.46 [32]. Five independent measurements were performed across the surface of the wafers to assess the uniformity of the oxide growth. The FIA  $SiO_x$  sample used for thickness and uniformity check for scanning transmission electron microscopy (STEM) and energy dispersive X-ray spectroscopy (EDS) analyses were anodised using a pulsed voltage source with 50% positive cycle at 1 V and 50% negative cycle at -1 V for the duration of 20 min under an illumination of  $100 \text{ W/m}^2$ . For the following X-ray photoelectron spectroscopy (XPS) analysis and surface passivation assessment, the FIA  $SiO_x$  layers were grown using a constant voltage of 1 V for 20 min with an illumination of  $100 \text{ W/m}^2$ . The thickness and elemental composition of the ultra-thin anodic SiO<sub>x</sub> layers were measured using a JOEL JEM-ARM200F (200kV) aberration-corrected STEM equipped with an EDS system. The STEM sample was prepared by making a lamella from a dual-beam focused ion beam (FIB) system. The XPS from Thermo Scientific UK (ESCALAB250Xi) under ultra-high vacuum (>  $2 \times 10^{-9}$  mbar) was used to characterize the stoichiometry of the FIA oxide. The X-ray source was monochromated Al K $\alpha$  ( $h\nu \times 1486.68$  eV) with the binding energy scale calibrated using a carbon reference (C 1s = 284.8 eV). Photo electrons were collected in the surface-normal direction. The oxide grown by immersion (without an applied bias) in 0.5 M H<sub>2</sub>SO<sub>4</sub> for 20 min under an illumination of  $100 \text{ W/m}^2$  was also analysed by XPS as a reference. In addition, the stoichiometry of the tunnel oxide of a comparable thickness formed by thermal oxidation (in a SEMCO reduced pressure oxidation furnace at 600 °C for 20 min) and wet-chemical oxidation (in 68 wt % HNO<sub>3</sub> acid at 121 °C for 10 min) was also studied for comparison purposes. In order to minimize the ultra-thin oxide from being contaminated by air and/or moisture, oxide samples were kept in a nitrogen environment during transportation for the XPS measurements.

*N*-type (100) double-side polished Cz-Si wafers with a resistivity of  $10-12 \ \Omega \cdot cm$  and a thickness of ~525  $\mu$ m were used for the effective minority carrier lifetime ( $\tau_{eff}$ ) measurements. The wafers were cleaned using the same procedure described above followed by an HF dip before the growth of the ultra-thin SiO<sub>x</sub> layer by FIA, thermal oxidation and HNO<sub>3</sub> oxidation on both sides of the wafers. Note that the same circuit was used when growing FIA  $SiO_x$  on both sides of the wafers. The wafers were rinsed and dried after the first surface was anodised, then turned over to enable the other surface to be in contact with the electrolyte. When anodising the second surface, the semi-transparent aluminum electrode was placed on top of the anodised surface so that current could tunnel through the ultra-thin  $SiO_x$  layer before entering the silicon and allowing the second surface to be anodised. Passivation of the ultra-thin SiO<sub>x</sub> layers was assessed together with a capping layer of ~100 nm amorphous silicon nitride (referred to as SiN<sub>x</sub> in the following). A dual-mode (MW/RF) laboratory scale PECVD system from Roth & Rau (AK400, Hohenstein-Ernstthal, Germany) was used for the SiN<sub>x</sub> deposition. A forming gas anneal (FGA) at 400 °C for 10 min was performed on all lifetime samples after SiN<sub>x</sub> deposition. The  $\tau_{\text{eff}}$  was measured under transient mode using a Sinton WCT-120 bridge from Sinton Instruments after SiN<sub>x</sub> deposition and after FGA. Symmetrical lifetime samples were used to evaluate the passivation quality of the  $SiO_x/SiN_x$  stacks, allowing the upper limit surface recombination velocity ( $S_{eff}$  UL) to be extracted from the following equation:

$$S_{\text{eff\_UL}} = \frac{W}{2} \left( \frac{1}{\tau_{\text{eff}}} - \frac{1}{\tau_{\text{bulk\_intrinsic}}} \right)$$
(1)

where *W* is the Si substrate thickness and  $\tau_{\text{bulk}\_\text{intrinsic}}$  is the Si intrinsic bulk lifetime as parameterized by Richter et al. [33].

#### 3. Results and Discussion

#### 3.1. Ellipsometry Measurements of Oxide Thickness

Figure 2 graphs the thickness of the SiO<sub>x</sub> layer formed by FIA as a function of time. The oxide thickness grown by immersion is compared to the growth profile generated from three different bias voltages with and without illumination. As can be seen, when growing FIA oxide in dark, the thickness over time profile is similar to that of the oxide formed by immersion in the same electrolyte without applying a bias voltage. An illumination of the *n*-Si surfaces with a relatively low intensity of 2 W/cm<sup>2</sup> was able to almost double the growth rate of the oxide when anodising at 1.5 V for less than 8 min. This demonstrates that an illumination is required to secure current flow through depletion regions that can form at the electrolyte interface as a result of the band bending induced by the electrolyte. It is proposed that when forming thin anodic oxides using FIA, the oxide growth is predominately controlled by the supply of positive charge at the electrolyte interface, whereas, for thicker oxides, the diffusion of xidant from the acidic electrolyte through the formed oxide layer to the silicon-oxide interface would dominate the oxide growth. As this study concentrates on the formation of ultra-thin tunneling oxide layers, the thickness of the oxide is primarily governed by the applied potential. When the applied voltage was increased from 1.5 V to 3.0 V, the oxide thickness increased from  $2.34 \pm 0.03$ to  $3.37 \pm 0.07$  nm. It was also found that the uniformity of the oxide across the wafer was improved with longer anodisation times as observed with narrower error bars, which is consistent with the oxide growing until the resistance was the same across the entire exposed silicon area.



**Figure 2.** Thickness of the SiO<sub>x</sub> layer formed by immersion in  $0.5 \text{ M H}_2\text{SO}_4$  and FIA under different anodisation conditions. The thickness was measured using ellipsometry at 5 different points across the wafer and is represented as a mean with the error bars representing the standard deviation [28].

#### 3.2. Microscopic and Spectroscopic Analyses

The thickness and uniformity of the anodic oxide layer were also assessed using high-resolution transmission electron microscopy (HRTEM). Figure 3 shows the cross-sectional images of the  $SiO_x$ layer grown by FIA using a pulsed voltage (varying between 1 V and -1 V) for 20 min under an illumination of  $100 \text{ W/m}^2$ . A capping layer of carbon (C) was deposited for preparation and protection purposes. Oxide thickness was measured at several points across the sample with an average thickness determined to be 1.5 nm, which is lower than the thickness (2.0 nm) measured and fitted from ellipsometry using a refractive index of thermal oxide (i.e., ~1.46). This suggests the refractive index of the anodic oxides may be higher than that of thermally-grown oxide, at least for the oxides grown using longer anodisation time. This could be due to a denser anodic oxide being formed at the silicon interface as revealed by previous reports that the first 1-2 nm anodic oxide has a density of  $2.5 \text{ g/cm}^3$  which is higher than value of  $2.2 \text{ g/cm}^3$  for stoichiometric SiO<sub>2</sub> [34]. The larger density can be attributed to the existence of a layer with accumulated mechanical stress at the anodic oxide and silicon interface [34]. The different SiO<sub>x</sub> layer thickness estimated from ellipsometry measurements and the TEM images could be due to the presence of a transition region containing mostly silicon sub-oxides at the silicon surface which is difficult to differentiate from the SiO<sub>2</sub> in TEM images and contributes to possible errors in estimating the oxide thickness using ellipsometry data. Models chosen to fit ellipsometry data can include additional detail such as an intermixing layer at the silicon and  $SiO_x$  interface which can directly impact the accuracy of the determined  $SiO_x$  thickness, however in this work the SiO<sub>x</sub> layer was modelled as a single layer with a refractive index value of 1.46. The accuracy of the thickness estimate from the TEM images may have been impacted by adsorption of moisture at the surface before capping.



**Figure 3.** (a) High-resolution transmission electron microscopy images of an anodic oxide film formed by FIA using pulsed anodisation (50% positive cycle at 1 V and 50% negative cycle at -1 V) for 20 min under an illumination of 100 W/m<sup>2</sup>, inset shows a higher resolution view. (b) energy dispersive X-ray spectroscopy (EDS) line scan through the oxide layer showing an O peak in the oxide layer.

X-ray photon spectroscopy was used to obtain information on the elemental composition of the anodised oxide films. When growing ultra-thin  $SiO_x$  with low applied bias voltages during the FIA process, the oxide resulting from immersion alone in the wet-chemical solution (0.5 M H<sub>2</sub>SO<sub>4</sub>) may impact the final  $SiO_x$  structure. Therefore, to assess the composition of the ultra-thin anodised oxide film, a wafer that had been immersed in the same electrolyte for a same period of time under the identical light source was used as a reference when performing the XPS measurements. Figure 4a illustrates the Si 2p spectrum obtained for the oxide layer grown by immersion. Both SiO<sub>2</sub> and Si<sub>2</sub>O peaks were detected and the Si<sup>1+</sup> state appears to be the only sub-oxide state, suggesting the oxide grown from immersion alone is highly sub-stoichiometric.

Figure 4b shows the decomposed Si 2p spectrum for the 1.8nm SiO<sub>x</sub> layer grown using FIA. The application of a bias potential of 1.0 V anodises the Si surface towards a structure that is closer to SiO<sub>2</sub> as evidenced by a higher calculated atomic percentage of the Si<sup>4+</sup> state. The sub-oxides contained in the FIA oxide are dominated by Si<sub>2</sub>O followed by SiO and Si<sub>2</sub>O<sub>3</sub>, as can be seen from the detailed look of the sub-oxide states in Figure 4 and the calculated atomic percentage of the sub-oxide peaks presented in Table 1. The sub-oxide ratio defined as the ratio between extremely silicon rich sub-oxide (Si<sup>1+</sup>) and slightly oxygen rich sub-oxide specious (Si<sup>2+</sup>, Si<sup>3+</sup>) is presented in Table 1 and is used to assess the stoichiometry of the oxide formed using different growth methods.

The composition of the ultra-thin  $SiO_x$  layer grown by thermal oxidation (thermal oxide) and nitric acid oxidation (HNO<sub>3</sub> oxide) was also analysed using XPS and compared to that of FIA oxide. Figure 4c,d show the Si 2p spectrums for thermal oxide and HNO<sub>3</sub> oxide respectively. All sub-oxide species exists in the thermal oxide whereas only Si<sub>2</sub>O and Si<sub>2</sub>O<sub>3</sub> peaks are detectable in the HNO<sub>3</sub> oxide. Not surprisingly, thermal oxide consists of the lowest atomic percentage of the Si rich Si<sup>1+</sup> sub-oxide, which yielded the lowest sub-oxide ratio of 0.58, confirming its nearly stoichiometric structure in nature. The highest level of non-stoichiometry is achieved by HNO<sub>3</sub> oxide with a sub-oxide ratio of 2.29 compared to 1.58 of the FIA oxide. It can be assumed that the FIA process drives more oxidant from the acidic electrolyte to the silicon–oxide interface allowing a more stoichiometric oxide to be formed comparing with the oxide grown in nitric acid under elevated temperature. These results show that the sub-stoichiometry of the oxide is dependent on the oxidation mechanism and the kinetics of the occurring reaction. The FIA oxide of a comparable thickness has a moderate level of stoichiometry and can be potentially used as tunnel oxide layers for passivated contacts.



**Figure 4.** X-ray photoelectron spectroscopy (XPS) spectral decomposition of the Si 2p spectrum showing the sub-oxide peaks for: (**a**) oxide grown by immersion alone; (**b**) FIA oxide anodised at constant voltage of 1.0 V for 20 min; (**c**) thermally-grown thin oxide; and (**d**) wet-chemical oxide grown in HNO<sub>3</sub>. A higher resolution view of the sub-oxide region of the spectrum is also shown for each oxide.

Oxide	Thickness (nm)	Si <sup>1+</sup>	Si <sup>2+</sup>	Si <sup>3+</sup>	$Si^{1+}/(Si^{2+} + Si^{3+})$
FIA (1.0 V)	1.8	1.28	0.46	0.35	1.58
Thermal	1.6	0.48	0.47	0.36	0.58
HNO <sub>3</sub>	1.6	1.49	-	0.65	2.29

**Table 1.** Oxide thickness (determined from ellipsometry using a refractive index for thermal oxide of 1.46) for the SiO<sub>x</sub> layer grown using different methods and the atomic percentage of the Si<sup>1+</sup>, Si<sup>2+</sup> and Si<sup>3+</sup> peaks obtained from XPS with the calculated sub-oxide ratio Si<sup>1+</sup>/(Si<sup>2+</sup> + Si<sup>3+</sup>).

#### 3.3. Surface Passivation

Due to the limited passivation solely provided by the ultra-thin  $SiO_x$  films, 100 nm of  $SiN_x$  was deposited on top of the  $SiO_x$  layer on both sides of the wafer to ensure a reasonable  $\tau_{eff}$  to be measured. Amorphous  $SiN_x$  is well-known for its excellent level of field-effect passivation, especially on *n*-Si due to an accumulation layer induced at the silicon surface by high positive charges. However, the insertion of an ultra-thin tunnel  $SiO_x$  layer was expected to have an impact on the chemical passivation of the silicon surfaces, allowing us to compare the passivation of the  $SiO_x$  layers grown using the different oxidation methods.

Figure 5a graphs  $\tau_{eff}$  as a function of excess carrier density ( $\Delta n$ ) for SiO<sub>x</sub> fabricated by FIA, thermal oxidation and HNO<sub>3</sub> oxidation, both before and after FGA. After SiN<sub>x</sub> deposition, the samples anodised by FIA achieved an  $\tau_{eff}$  of ~3.8 ms, which is higher than that of the wet-chemically oxidised wafers in HNO<sub>3</sub> solution (2.8 ms), and lower than the  $\tau_{eff}$  obtained for thermally-oxidised samples (7.0 ms) at  $\Delta n = 1 \times 10^{15}$  cm<sup>-3</sup>. This trend fits in well with the  $S_{eff_UL}$  values extracted and graphed in Figure 6. The average  $S_{eff_UL}$  for the FIA oxide was ~7.2 cm/s compared to 3.7 cm/s for the thermally-grown oxide and 8.6 cm/s for the oxide grown in HNO<sub>3</sub>. To correlate the surface passivation results with the sub-oxide ratios reported in Table 1, a bar chart showing the average  $\tau_{eff}$  at  $\Delta n = 1 \times 10^{15}$  cm<sup>-3</sup> for samples passivated by different SiO<sub>x</sub> and SiN<sub>x</sub> stack is presented in Figure 5b. It was observed that in the as-deposited form, the  $\tau_{eff}$  increased with a decreasing sub-oxide ratio, confirming that the more stoichiometric tunnel oxides more effectively reduce recombination at the *n*-Si surfaces. This finding is consistent with previously-published results [15]. Since the chemical passivation is strongly influenced by the Si and SiO<sub>x</sub> interface, a more stoichiometric oxide at the transition region is expected to result in a lower interface trap density ( $D_{it}$ ) and hence a lower surface recombination velocity.

Very low surface recombination velocities (4.8 cm/s at  $\Delta n = 1 \times 10^{15}$  cm<sup>-3</sup>) were achieved in the absence of a tunnel oxide (i.e., SiN<sub>x</sub> deposition following HF immersion). The  $\tau_{eff}$  of these samples was higher and the  $S_{eff\_UL}$  was lower for all injection levels compared the samples which included a tunnel SiO<sub>x</sub> either grown by FIA or by HNO<sub>3</sub> oxidation. This is most likely due to a Si-rich interface layer which was reported to be unintentionally deposited in the dual-mode plasma reactor used for this study even when using a recipe for a stoichiometric SiN<sub>x</sub> [35]. However, with the insertion of a tunneling thermal oxide layer at the interface, improvement of passivation can be seen, most likely due to the more O saturated Si bonds at the interface.

The effect of FGA on the passivation provided by  $SiO_x/SiN_x$  stack and by  $SiN_x$  alone was also evaluated. It can be seen from Figure 5a,b that the  $\tau_{eff}$  was increased for all samples after annealed in forming gas with reduction in  $S_{eff\_UL}$  also being observed. The improvement in passivation is presumably due to the release of H atoms during the FGA which diffuse into the Si and  $SiO_x$  or  $SiN_x$ interface to passivate the dangling Si atoms. Overall, the ultra-thin tunnel  $SiO_x$  layer prepared by thermal oxidation provided the best passivation, followed by FIA oxide, then the oxide grown in HNO<sub>3</sub>. This result suggests that the FIA process can offer a low-cost alternative for forming ultra-thin tunnel  $SiO_x$  layers for passivated contacts. The through-wafer oxidation can result in oxides of uniform thickness. However, as high temperatures (> 800 °C) are used to form poly-Si, the compositional structure of the FIA oxide and its passivation quality after high temperature annealing will be assessed in future experiments.



**Figure 5.** (a) Values of  $\tau_{\text{eff}}$  measured as a function of  $\Delta n$  for *n*-Si wafers symmetrically passivated by SiO<sub>x</sub> and SiN<sub>x</sub> stack before (solid symbols) and after (open symbols) forming gas anneal (FGA). The  $\Delta n$  dependent  $\tau_{\text{eff}}$  for samples passivated with thin FIA SiO<sub>x</sub> (dark-grey squares) capped with SiN<sub>x</sub> layer is compared to those passivated by thin thermal SiO<sub>x</sub> (red triangles) and HNO<sub>3</sub> SiO<sub>x</sub> (blue circles) when capped with SiN<sub>x</sub>. The  $\tau_{\text{eff}}$  of samples passivated with a single layer SiN<sub>x</sub> after hydrofluoric acid (HF) immersion (green diamonds) is shown for reference. (b) Values of  $\tau_{\text{eff}}$  obtained at  $\Delta n = 1 \times 10^{15}$  cm<sup>-3</sup> for samples passivated with different thin SiO<sub>x</sub> and SiN<sub>x</sub> stacks and with a single layer SiN<sub>x</sub> before and after FGA. Three samples were measured for each group with the solid columns showing the mean and error bars representing the minimum and maximum. The sub-oxide ratio (SOR) is included in the category label with the oxide preparation method.



**Figure 6.** Values of  $S_{\text{eff}\_UL}$  extracted at  $\Delta n = 1 \times 10^{15} \text{ cm}^{-3}$  for *n*-Si samples passivated with ultra-thin SiO<sub>x</sub> formed by FIA, thermal oxidation and wet-chemical HNO<sub>3</sub> oxidation followed by a SiN<sub>x</sub> capping. Data presented includes three samples per oxidation condition. The values of  $S_{\text{eff}\_UL}$  for samples passivated by a single layer SiN<sub>x</sub> after HF immersion are also shown.

## 4. Conclusions

We have demonstrated the potential of using anodic SiO<sub>x</sub> formed by FIA as a tunneling oxide layer for passivated contacts for Si solar cells. The stoichiometry and passivation quality of these SiO<sub>x</sub> tunneling layers were compared to those formed by thermal oxidation and chemical oxidation in HNO<sub>3</sub>. It was shown that the fraction of Si-rich sub-oxides present in the FIA oxide layer was higher than detected in the thermally-oxidised film, but lower than that observed in the wet-chemical oxide, of a comparable thickness. Furthermore, the surface passivation provided by the interfacial SiO<sub>x</sub> correlated with the oxide stoichiometry with the SiO<sub>x</sub> layers containing more O-rich sub-oxides in the transition region resulting in lower recombination velocity at the Si/SiO<sub>x</sub> interface. Given the effective passivation provided by the FIA oxide and its controllability offered from the room-temperature anodisation process, it was concluded that FIA provides a robust way of fabricating uniform tunneling oxide layers for passivated contacts for Si solar cells. Uniformity is assured through the FIA process with the oxide growing to the same thickness because current flows though the wafer until the resistance is uniform across the surface. Future work will investigate the passivation provided by the FIA oxides capped with poly-Si and the effect of high temperature annealing on their properties.

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