

Article

Energy Efficient Supply Boosted Comparator Design

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Abstract: This paper presents a new mixed-signal design technique called supply boosting technique (SBT) and the design of an energy efficient, sub-1 V supply boosted comparator (SBC) in a standard complementary metal oxide semiconductor (CMOS) process. The selected CMOS process does not allow sub-1 V operation with a wide input range due to high threshold voltage (high- V_{TH}) of MOS transistors (+0.8 V/−0.9 V). Despite this, the proposed comparator operates sub-1 V supply voltages with input common mode voltage larger than 60% of supply voltage by utilizing a supply boosting technique. The measured power consumption of the supply boosted comparator for 1 V supply was 90 nW and speed was 6500 conversions per second, resulting in 14 pJ per conversion energy efficiency.

Keywords: supply boosting; mixed-signal design; low-voltage design; comparator

1. Introduction

Comparators are one of the fundamental building blocks affecting key performance parameters of mixed-signal subsystems such as analog-to-digital converters (ADCs). Their energy efficiency, speed, offset, and common-mode input range have to be optimized for sub-1 Volt operation. Input range is especially critical if they are to be used in successive approximation ADCs, which are considered to be one of the optimum topology for low-voltage and energy-limited applications [1]. Satisfying these requirements becomes more challenging when the sum of the threshold voltages of complementary metal oxide semiconductor (CMOS) transistors is larger than the system supply voltage. This becomes more pronounced for sub-100 nm CMOS processes, considering threshold voltages have not been

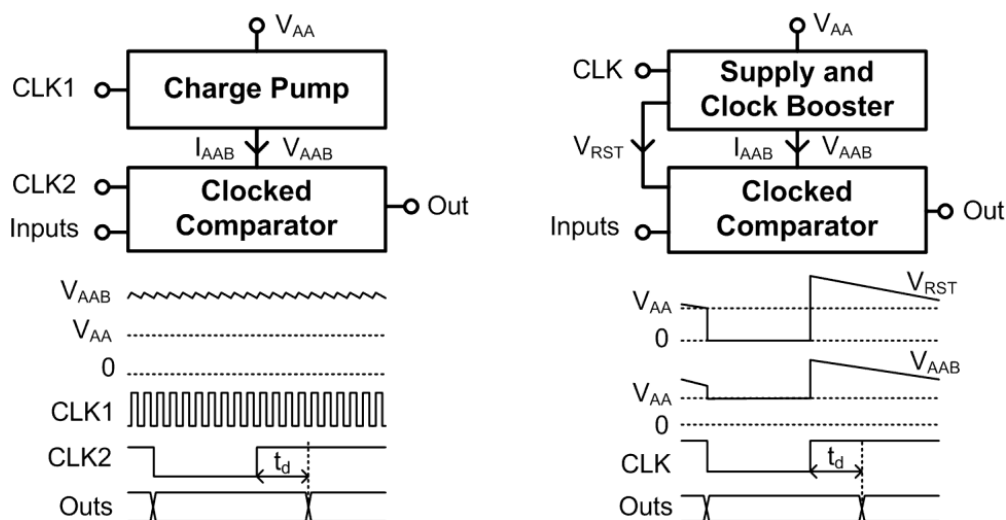
scaled with the same pace as supply voltages [2]. Thus, for sub-1 V designs, CMOS processes that offer native or low threshold devices are preferred even at the expense of increased leakage related power consumption. This becomes a major design concern for battery operated systems used in energy-limited applications where standby power limits operation life-time [3]; making low leakage sub-micron CMOS processes ($L_{min} > 0.15 \mu\text{m}$) attractive. These processes, however, offer high- V_{TH} transistors and process supply voltages of 3.3 V or more, which creates a challenging mixed-signal circuit design especially if system supply voltage is lower than the process supply voltage, *i.e.*, 1 V or lower. Few circuit design techniques have been published addressing these challenges [4–12]. However, these techniques result in increased circuit complexity, higher power consumption, degraded energy efficiency, or slower operation. In addressing some of these drawbacks, a new mixed-signal design technique called supply boosting (SBT) was proposed [13–15]. A new comparator topology has been developed using supply boosting resulting in low-voltage, and energy efficient operations.

This paper is organized as follows. The low-voltage design technique, called supply boosting technique, is introduced in Section 2. Analysis and design considerations of supply boosted comparator (SBC) are given in Section 3. Section 4 is dedicated to measurement results and discussions. Finally, conclusions and future directions are given in Section 5.

2. Supply Boosting Technique (SBT)

Supply boosting has not been investigated and used as extensively as the clock boosting or bootstrapping for designing low-voltage analog and mixed-signal circuits. One involving boosting supply voltage, is called charge-pump technique (CPT) used for designing OPAMPs, comparators, and phase-locked loops (PLLs) [9–12]. In the CPT, supply voltage is pumped continuously to keep circuit supply voltage (V_{AAB}) higher than the system supply voltage (V_{AA}) as shown on Figure 1a. Two clock signals are used in charge pump based circuits. The faster one is used by the charge pump block for maintaining low ripple on boosted supply voltage. The slower one is used by the main circuit which is a clocked comparator in this case.

Figure 1. Characteristic signals and blocks of a clocked comparator using: (a) charge pump technique (CPT); (b) supply boosting technique (SBT).



Main benefits of using boosted supply voltage are extended input range and reduced system supply voltage. Low ripple voltage on the boosted supply voltage is required for CPT based circuits [9]. Otherwise it degrades noise performance of the main circuit. To achieve low ripple, sophisticated charge pump circuits have to be used which increase circuit complexity, size, and power consumption. Another important design requirement is that the boosted supply voltage has to be less than the maximum allowed process supply voltage (V_{AAP}) for reliable device operation due to increased internal electric field. This is one of the main issues using boosting techniques in sub-100 nm processes in which V_{AAP} is already around 1 V.

A modified version of the charge pump circuit design technique is proposed and called supply boosting technique (SBT) [13–15]. In supply boosted circuits, system supply voltage is boosted locally only once allowing boosted voltages such as clock and supply voltages to drop from their boosted level, V_{AAB} , as shown in Figure 1b. Sophisticated charge pump circuit used in CPT is replaced with a simple supply and clock booster (SCB) circuit. The SCB reduces circuit complexity, size, and overall noise performance of the main circuit. For clocked comparator, for example, one clock signal (CLK) is required resulting in a simplified clocking scheme. Also, a lower boosted supply voltage is chosen than the maximum allowed process supply voltage to avoid device reliability issues. Boosting supply voltage once also minimizes overall power consumption increased due to the added charge pump circuits. Thus, supply boosting technique based circuits achieve better energy efficiency than charge pump based circuits.

In the supply boosting circuit, supply voltage drops from the boosted level depending on the total current or power consumption of the main circuit. The higher the power consumption, the faster the supply voltage drops in supply boosted circuits. In this case, a larger supply voltage ripple is observed in charge pump based circuits. Large boosting or pump capacitors or lower current consumption is required for lower supply voltage drop or ripple. Increased capacitor size further increases dynamic power consumption of charge pump based circuits, while having a minimal effect on supply boosted circuits. Thus, a tradeoff among power consumption, speed, noise, and circuit size exists in both design techniques.

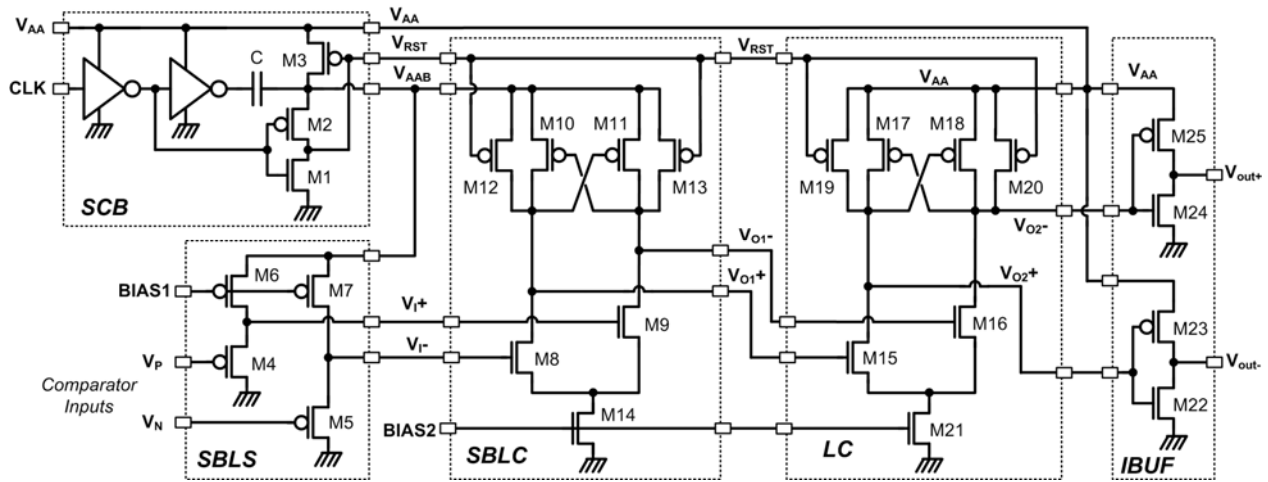
3. Supply Boosted Comparator (SBC) Design

The proposed supply boosted comparator (SBC) can be partitioned into sub blocks shown in Figure 2. It is composed of supply boosted level shifters (SBLs), latched comparator cores, buffers, and supply and clock booster (SCB) circuits. Boosted supply voltage (V_{AAB}) and boosted clock signal (V_{RST}) are generated by the compact supply and clock booster circuit. Boosted supply voltage is used by the p-type level shifter and first latched comparator, while boosted reset signal is used by pre-charge switches in latched comparators.

3.1. Supply and Clock Booster (SCB) Circuit

The supply and clock booster (SCB) circuit is composed of five transistors and a boosting capacitor as shown in Figure 2. It generates boosted supply and reset signal employing a one-shot charge pump circuit [16]. Boosted supply voltage (V_{AAB}) equals the system supply voltage (V_{AA}) when clock input is low (CLK = 0), and is ideally boosted to twice the system supply voltage ($2V_{AA}$) when clock input is high.

Figure 2. Schematic diagram of proposed supply boosted comparator (SBC).



The boosted reset signal (V_{RST}) is 0 when clock input is low and boosted ideally to twice the system supply voltage ($2V_{AA}$) when clock input is high. Bottom plate of the boosting capacitor (C) is connected to inverter side to improve boosting efficiency. Bulk nodes of PMOS devices in SCB (M2, M3) were connected to boosted supply output (V_{AAB}). Boosting capacitor value can be calculated using (1).

$$C = \frac{t_d \times I_{AAB}}{(1 - \alpha) \times V_{AAB}} \quad (1)$$

where t_d is comparator's delay time, α is discharge ratio of boosted supply voltage from its boosted level when clock input is high, and I_{AAB} is total current consumption of the comparator circuits draining current from V_{AAB} bus.

Ideal boosted level of the supply is $2V_{AA}$ for the SCB circuit shown in Figure 2. Considering parasitic and the load capacitance (C_L) on the SCB output, V_{AAB} can be found using (2).

$$V_{AAB} = (1 - \alpha) \times \left(\frac{2C + C_L}{C + C_L} \right) \times V_{AA} = \beta V_{AA} \quad (2)$$

where β is boosting factor. Required capacitor size for 10% drop on the boosted level ($\alpha = 0.1$), 200 K conversions per second comparator speed ($t_d = 5 \mu s$), and 1 μW static power consumption ($I_{AAB} = 1 \mu A$) on 1 V system supply voltage is 25 pF which could be integrated on-chip. Lowering current consumption will further reduce capacitor size. However, lowering current also results in larger comparator delay.

3.2. Supply Boosted Level Shifter (SBLS) Circuit

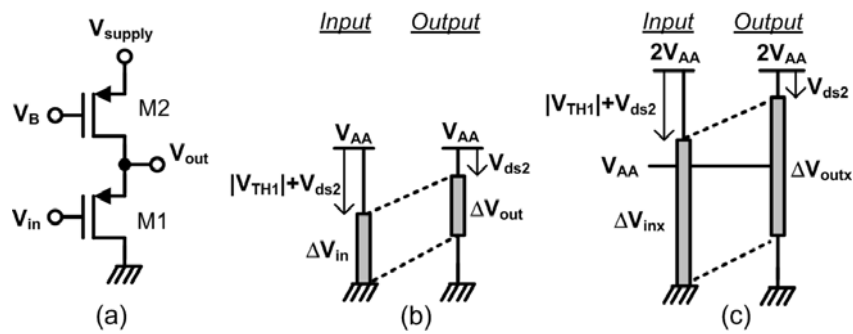
The supply boosted level shifter circuit is composed of p-type source followers driving and isolating input nodes from supply boosted comparator core. It expands common mode input range of comparator beyond the system supply voltage (V_{AA}) as shown in Figure 3. This expansion is achieved by using V_{AAB} as the supply voltage for the level shifter during comparison period. Common mode input and output ranges of SBLS for supply voltage equal to V_{AA} and βV_{AA} are given using (3) and (4).

$$\left. \begin{aligned} \Delta V_{in} &= V_{AA} - |V_{TH1}| - V_{ds2} \\ \Delta V_{out} &= G_{SPLS} \cdot \Delta V_{in} \end{aligned} \right\} \quad \text{for } V_{supply} = V_{AA} \quad (3)$$

$$\left. \begin{aligned} \Delta V_{inx} &= \beta \cdot V_{AA} - |V_{TH1}| - V_{ds2} \\ \Delta V_{outx} &= G_{SPLS} \cdot \Delta V_{inx} \end{aligned} \right\} \quad \text{for } V_{supply} = \beta V_{AA} \quad (4)$$

where G_{SPLS} is small-signal voltage gain of the source follower. Here strong inversion is assumed for all transistors. Equations (3) and (4) are depicted for $\beta = 2$ on Figure 3b,c.

Figure 3. Supply boosted level shifter (SBLS) circuit; (a) schematic; (b) common mode input and output ranges for $V_{supply} = V_{AA}$; (c) for $V_{supply} = 2V_{AA}$.



Common mode input range of the p-type source follower without supply boosting for 1 V system supply voltage is between 0.1 V and 0.6 V for PMOS threshold voltages between -0.9 V and -0.4 V. Supply boosting with $\beta = 1.65$ improves input range from 0.1 V to 0.75 V and from 0.6 V to 1.25 V for same threshold voltages. If the threshold voltage is less than -0.65 V, rail-to-rail input range could be achieved for 1 V supply voltage. Bulk node of input transistor (M1) has to be connected to the output to reduce signal dependent threshold variations and offset. Considering G_{SPLS} of 0.8 and $\beta = 1.65$, output voltage swing can be increased from 0.08 V to 0.6 V for -0.9 V threshold voltage.

3.3. Latched Comparator (LC)

Comparator core composes a biased differential amplifier with regenerative type cross-coupled load functioning as latch. This continuous time latched comparator (LC) [17] provides lower kick-back noise and slower speed than its dynamic counterparts [18]. It works in two phases: pre-charge and compare. In pre-charge phase ($V_{RST} = 0$) output nodes are connected to the boosted supply bus through PMOS switch transistors. In compare phase ($V_{RST} = V_{AAB}$), the switches are turned off and comparison of the input voltages is performed.

Since the differential pair is continuously biased, static power is consumed during both pre-charge and compare phases. Comparator cores are biased with tens of nA so that static power consumption is low. Low bias currents also allow one-shot supply boosting to be used more effectively.

N-type differential pair was used due to the fact that the differential input signals are level shifted by two p-type SBLS. The first latched comparator (SBLC) uses boosted supply voltage, V_{AAB} , instead of the system supply voltage, V_{AA} . Output of SBLC is coupled directly with the second latched comparator (LC). Supply voltage of the second LC is not boosted so that the logic level is restored before being driven by the inverter buffers which have high switching thresholds.

3.4. SBC Design and Simulation

The proposed supply boosted comparator shown in Figure 2 was designed using a 0.5 μm 2P3M CMOS process to achieve 10-bit resolution while attaining wide input common mode range. Threshold voltages of MOSFETs (+0.8 V/−0.9 V) in selected processes resulting in less than 0.1 V common mode input range for 1.0 V supply if a conventional clocked comparator is used. In the proposed comparator, the calculated common mode input range was 0.7 V, for $\beta = 1.6$ and $G_{SPLS} = 0.8$.

Although supply boosting technique improves dynamic range of the comparator, it should be designed carefully according to speed limitations. Regeneration time constant of latched comparator core can be found using (5).

$$t_d = \frac{C_L}{g_{m,p}} = \frac{C_L}{\sqrt{2K'_p \left(\frac{W}{L}\right)_p \cdot I_D}} \quad (5)$$

where $g_{m,p}$ is the transconductance of cross coupled PMOS devices (M10, M11 or M17, M18 in Figure 2) and I_D is their bias current. To reduce the regeneration time constant, $g_{m,p}$ must be increased by increasing its bias current. On the other hand, increasing the bias current causes the boosted supply voltage to drop at a higher rate and may cause failure unless the boosting capacitor is large enough. Since the size of the on-chip boosting capacitor cannot exceed a certain range due to limited area, proposed supply boosted comparator could only be used for low power, medium speed applications. For example, consider the SBC design supplied from a single 1 V power supply. For reliable operation of the comparator, the boosted supply must not fall below a certain level given in (6).

$$V_{AAB} = |V_{THP}| + 3V_{od} \quad (6)$$

where V_{od} is the overdrive voltage of devices and V_{AAB} can be found from (2). In (6), it is assumed that all devices have the same overdrive voltages. Hence the voltage drop (ΔV) across the boosting capacitor during the compare phase must not fall below a certain level that is given in (7)

$$\Delta V < V_{AAB} - |V_{THP}| - 3V_{od} \quad (7)$$

Since the comparison phase takes at least one time constant of the comparator, t_d , during this time we can write,

$$\frac{I_{AAB} \cdot t_d}{C} < V_{AAB} - |V_{TP}| - 3V_{od} \quad (8)$$

Using (5) in (8) and defining γ as the ratio of current in the latched comparator cores to the total comparator current, the maximum current that can be drained from the boosted supply can be found using (9). This gives the upper limit of the total current for a given boosting capacitor.

$$I_{AAB} < 2 \cdot \gamma \cdot \mu_p C_{ox} \left(\frac{W}{L}\right)_p \left(\frac{C}{C_L}\right)^2 (V_{AAB} - |V_{TP}| - 3V_{od})^2 \quad (9)$$

Based on aforementioned considerations, a supply boosted comparator was designed in a 0.5 μm CMOS process. Device sizes used in the design are listed in Table 1. Long channel lengths were used to reduce input referred offset voltage, increase gain, and improve matching. 10 nA and 20 nA bias

currents were used in SBLS and LCs, respectively. A 20 pF booster capacitor was used based on total static current of less than 100 nA and comparator delay of 50 μ s for 1 V supply. Parasitic load capacitance of the SCB was around 4 pF resulting in α of 0.2 and β of 1.6.

Table 1. Device sizes used in SBC design.

| Device | Width (μ m) | Length (μ m) | M |
|------------------|------------------|-------------------|---|
| M1 | 6.0 | 0.6 | 2 |
| M2–3 | 6.0 | 0.6 | 4 |
| M4–5,10–11,17–18 | 6.0 | 1.2 | 8 |
| M6–7,14,21 | 6.0 | 3.0 | 2 |
| M8–9,15–16 | 6.0 | 1.5 | 8 |
| M23,25 | 6.0 | 0.9 | 8 |
| M22,24 | 6.0 | 1.2 | 4 |
| M12–13,19–20 | 6.0 | 0.6 | 1 |

Operation of proposed comparator was verified through HSpice simulation at different process, supply voltage and temperature (PVT) corners. Simulation result for 1.2 V supply, 1.0 V common mode input, and ± 0.25 mV delta input voltage is shown in Figure 4. Comparator delay is mainly determined by second LC and switching threshold of the output buffer. Simulation shows two input cases: $dV_{IN} = +0.25$ mV that force V_{o+} to high between 20 μ s and 30 μ s, and $dV_{IN} = -0.25$ mV forcing output lower, between 35 μ s and 45 μ s. Pre-charge time was 5 μ s for the simulation. The delay introduced by the SBLS and SBLC for the first input is around 2.5 μ s (V_{ol-} and V_{ol+}). Second LC and inverting buffer delay on the other hand is around 6 μ s. Thus, there is room for improvement for a faster operation if a different second LC stage is used. One possible solution is using NMOS type SBLS following SBLC for improving conversion speed.

Layout size of the supply boosted comparator was $240 \mu\text{m} \times 200 \mu\text{m}$ using SCMOS design rules ($L_{min} = 0.6 \mu\text{m}$ for C5) from MOSIS [19]. A 20 pF poly1-poly2 capacitor ($0.8 \text{ fF}/\mu\text{m}^2$) was used in the supply and clock booster block resulting in a boosting capacitor occupying almost 50% of the layout area. Micrograph of the SBC is shown in Figure 5.

4. Measurement Results and Discussion

A test setup shown in Figure 6 was developed for measuring static and dynamic characteristics of the supply boosted comparator (SBC). Two 16-bit digital-to-analog converter (DAC) IC was used to generate SBC inputs. Control and communication signals were generated using a field programmable gate array (FPGA) on test board. Control signals in the design were level shifted from 3.3 V to desired system supply voltage (V_{AA}) level. Analog and digital signals were monitored using mixed-signal oscilloscope (MSO) while current consumption was recorded through a precision multimeter (Tektronix DMM4050) with up to 0.1 nA resolution. Power supply to the SBC was separated from the other parts of the chip. Biases were generated on-chip and controlled digitally through a serial communication link.

Figure 4. Hspice simulation result of the supply boosted comparator for $V_{AA} = 1.2$ V, $V_{IN,DC} = 1.0$ V, $dV_{IN} = \pm 0.25$ mV.

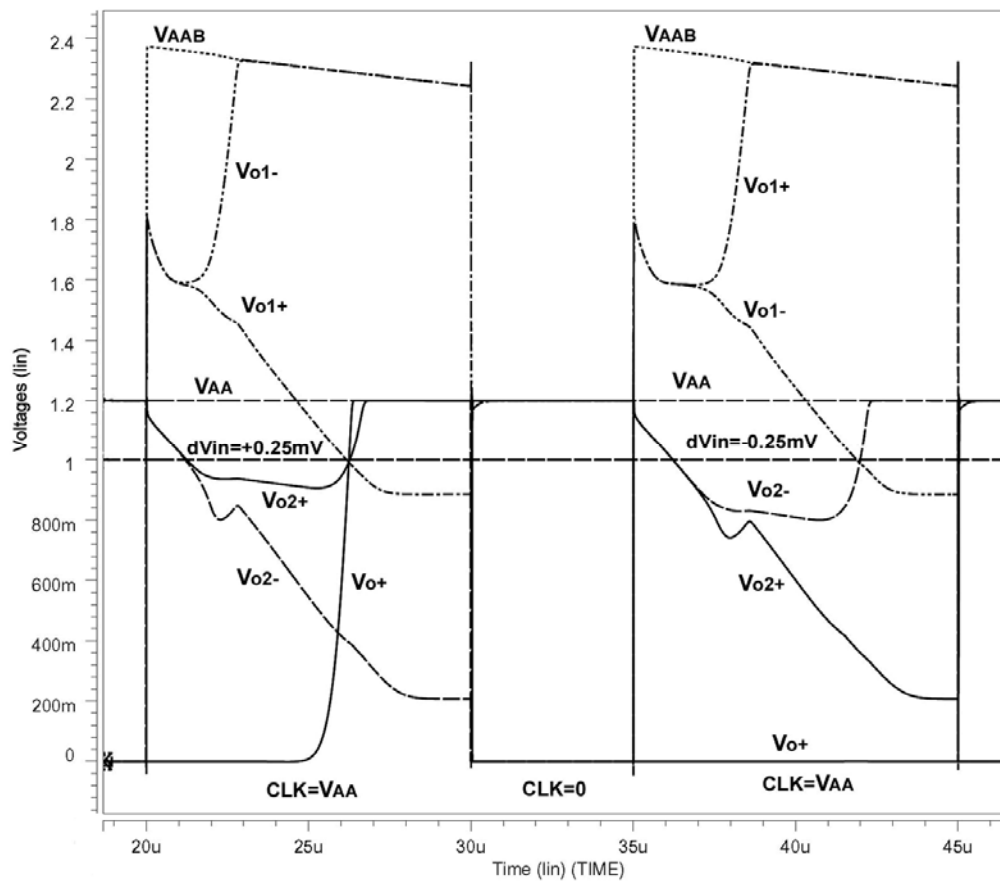


Figure 5. Micrograph of the SBC design.

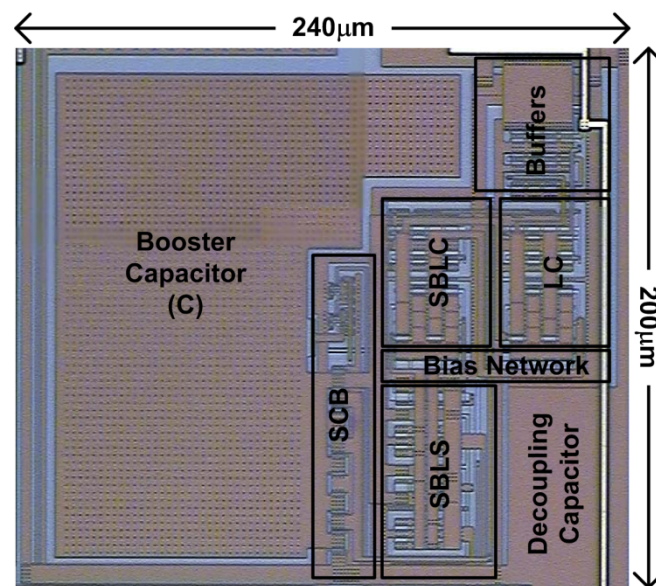
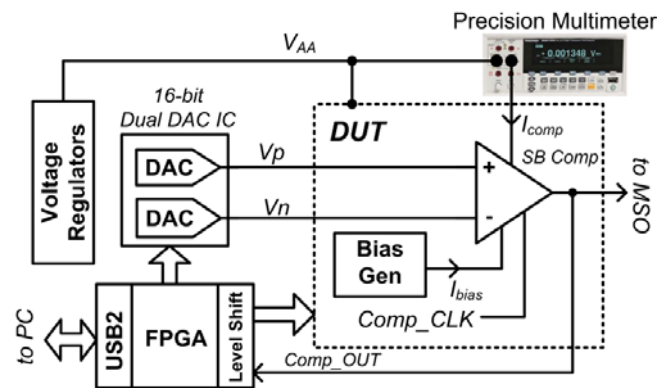


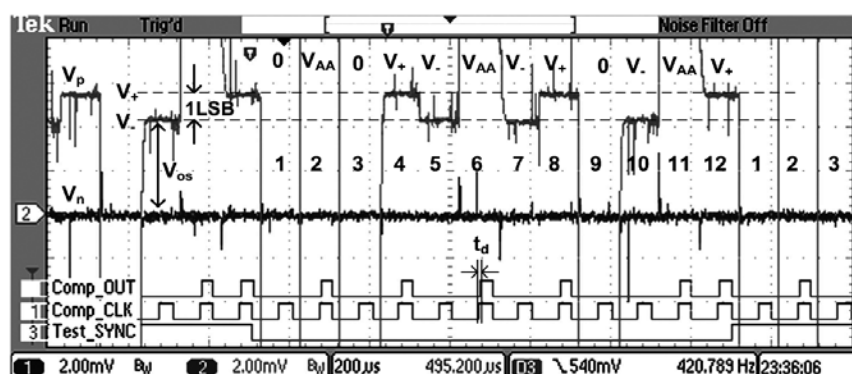
Figure 6. Measurement setup.



Measurement Results

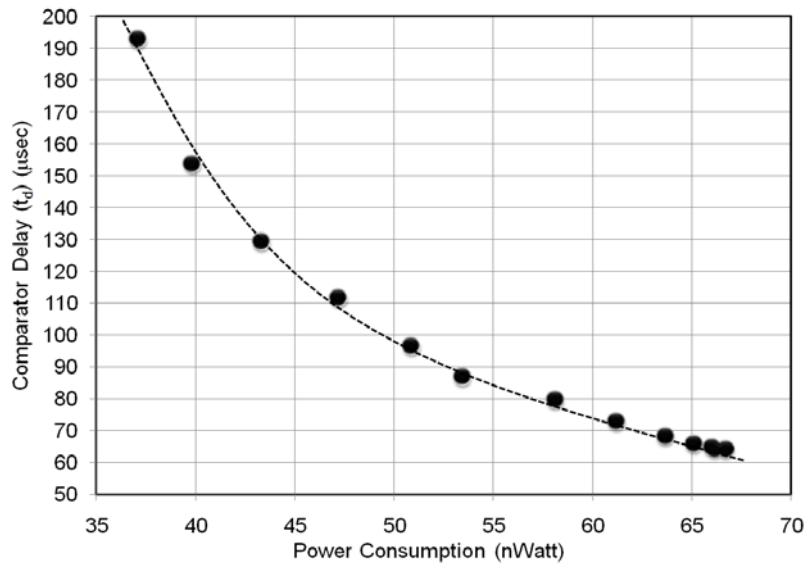
Power consumption and comparator delays were measured under worst-case input conditions described in [20]. A test pattern shown on Figure 7 was generated that is composed of 12 input transitions. They were generated by the 16-bit DACs and applied to positive and negative (V_p and V_n) inputs of the design. Four distinct voltage levels were generated as test patterns: V_{AA} , 0, V_+ and V_- . V_- equals the common mode voltage (V_{CMI}) plus input offset voltage (V_{OS}) of the comparator while V_+ is kept one desired least significant bit (LSB) above the V_- level. Comparator's negative input (V_n) was kept at V_{CMI} level while the test pattern was applied to positive input (V_p). Comparator delay time (t_d) was measured for worst case input transition. Transitions between levels 4 and 5 and levels 7 and 8 shown in Figure 7 are the worst case transitions that force comparator to resolve one LSB equivalent effective voltage difference applied to its inputs. Figure 7 also shows measured characteristics of SBC for $V_{AA} = 1.0$ V and $V_{CMI} = 0.5$ V. Measured 1LSB equivalent effective input voltage was 1.2 mV, and offset voltage was 4.1 mV.

Figure 7. Input and output signals captured during dynamic testing of supply boosted comparator under worst case input conditions.



Delay time (t_d) *versus* average power consumption (P_{avr}) of the comparator was measured at various biasing conditions. Delta input voltage ($dV = V_+ - V_-$) was 1 mV, while clock frequency (f_{CLK}) was set to 4 kHz with duty cycle of 20% during this measurement. Dynamic power consumption was measured by setting comparator's bias currents to zero while running the clock. It was 25 nW. Measurement results are shown in Figure 8. It represents the tradeoff between speed and power consumption of SBC.

Figure 8. Measured power consumption *versus* comparator delay for $V_{AA} = 1.0$ V, $V_n = 0.5$ V, $dV = +1$ mV, $f_{CLK} = 4$ kHz.

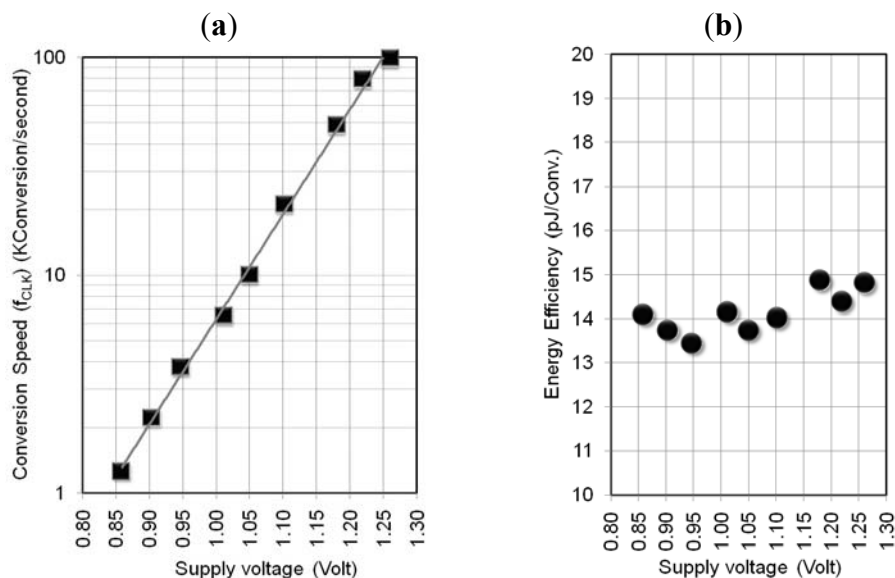


Delay time, maximum clock speed, and power consumption of the SBC were also measured for V_{AA} between 0.85 V and 1.25 V. $dV = 5$ mV and $V_{CMI} = V_{AA}/2$ was used during measurements. Figure 9a shows the measured maximum clock frequency *versus* supply voltage while Figure 9b represents calculated energy efficiency of the SBC. Energy efficiency was calculated using (10) using measured power consumption and maximum conversion speed of the comparator.

$$E_{eff.} [\text{Joule/Conversion}] = \frac{\text{Power [Watt]}}{\text{Speed [Conversion/Second]}} \quad (10)$$

Measured energy efficiency was fairly constant and was between 13 and 15 pJ per conversion. Measured minimum supply voltage of the SBC design was 0.85 V with better than 1000 conversions per second speed.

Figure 9. Measured: (a) conversion speed and (b) energy efficiency of SBC.



Precision of the comparator (V_{PRCS}) was measured for supply voltages between 0.85 V and 1.2 V while sweeping common mode input voltage (V_{CMI}) between 0 and V_{AA} as shown in Figure 10. Bit resolution of the SBC was then calculated using (11) and plotted in Figure 11.

$$n = 3.32 \cdot \log_{10}(V_{CMI}/V_{PRCS}) \quad (11)$$

For 8-bit resolution common mode, input range was measured to be around 60% of the system supply voltage, while it was about 55% and 40% for 9-bit and 10-bit resolutions, respectively. Compared to conventional comparators, this represents six times ($6\times$) improvement of the common mode input range for 8-bit resolution when $V_{AA} = 1$ V.

Figure 10. Measured precision of the SBC for various supply voltages.

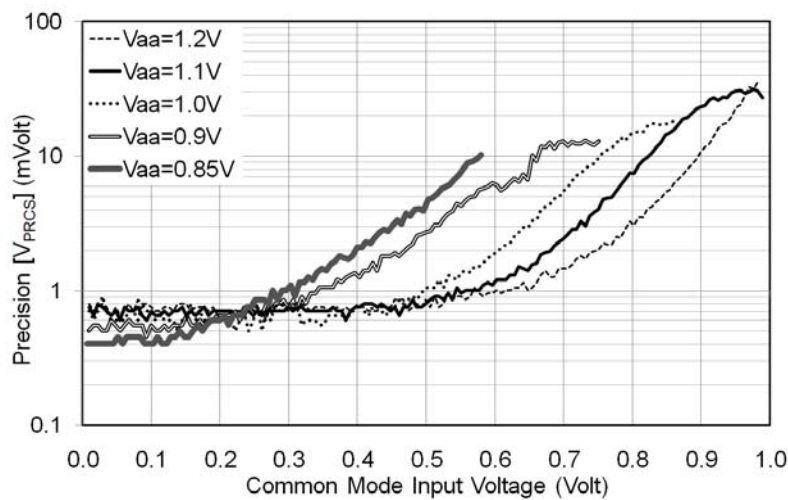
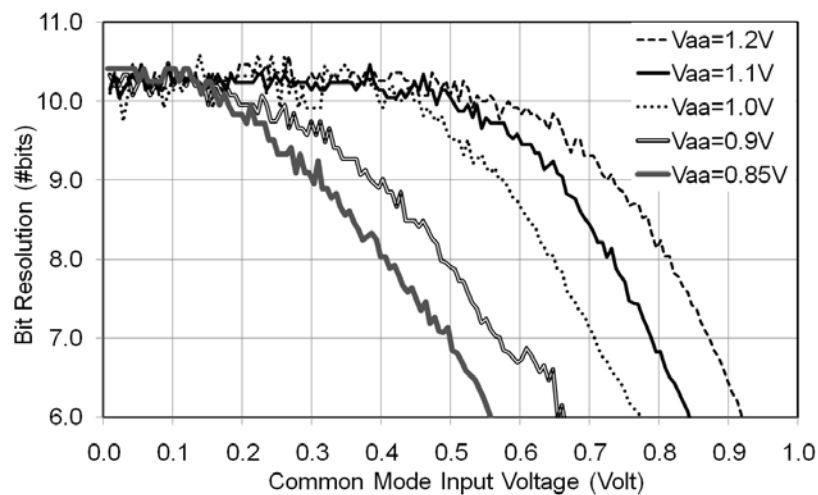


Figure 11. Measured bit resolution of the SBC for various supply voltages.



Measurement results of the supply boosted comparator at 1.0 V supply voltage are summarized and compared in Table-2. The SBC achieves lower supply voltage operation, better power consumption and energy efficiency, without increasing complexity and area of the comparator.

Table 2. Comparison table.

| Parameters | This Work | Ref. [20] | Ref. [5] | Unit |
|------------------------------|----------------------|-------------|-------------------|------------------|
| CMOS Process Technology | 0.50 | 0.50 | 0.25 | μm |
| Threshold voltage (N/P) | +0.8/−0.9 | +0.74/−0.85 | +0.48/−0.6 | Volt |
| Supply Voltage | 1.0 | 1.0 | 1.0 | Volt |
| Supply Voltage Range | >0.85 | >1.0 | >1.0 | Volt |
| Input Range (V_{CM}) | 0.75 | 1.0 | 1.0 | Volt |
| Conversion Speed | 6.5 | 250 | 1000 ^a | KC/s |
| Power Consumption | 0.09 | 5.0 | 21.0 | μWatt |
| Energy Efficiency | 14.0 | 20.0 | 21.0 | pJ/C |
| Layout Area (LA) | 0.048 | 0.037 | 0.024 | mm^2 |
| Normalized Area ^b | 133,300 ^c | 147,200 | 384,000 | - |

^a simulation only; ^b LA/L_{min}^2 ; ^c $L_{min} = 0.6 \mu\text{m}$.

5. Conclusion

A new comparator topology was proposed utilizing the supply boosting technique (SBT) to achieve sub-1V operation. It was shown that SBT improves the common mode input range of the comparator, achieving both high precision and low energy operation. The proposed comparator topology would be especially useful in mixed-signal systems such as implantable biomedical devices that use CMOS process for which only high- V_{TH} MOSFET devices are available.

The proposed comparator was fabricated using a 0.5 μm CMOS process. Measurements showed that the comparator achieved better than 15 pJ/conversion energy efficiency, 0.62 V common mode input range which is six times better than that of conventional comparator topologies with 8-bit resolution on a 1 V supply.

The speed of the supply boosted comparator is mainly determined by the second latched comparator stage. Speed could be improved using an N type source follower following first supply boosted latch comparator (SBLC) circuit. It is expected that this improvement would be between six and ten times the current speed for 8-bit resolution.

Acknowledgments

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