Journal of
Low Power Electronics and Applications

MDPI

Article

Fully Differential Miller Op-Amp with Enhanced Large- and Small-Signal Figures of Merit

Anindita Paul [1], Jaime Ramirez-Angulo [2,*], Héctor Vázquez-Leal [3,4], Jesús Huerta-Chua [2] and Alejandro Diaz-Sanchez [5]

1 Electrical Engineering & Renewable Energy, Oregon Institute of Technology, 3201 Campus Drive, Klamath Falls, OR 97601, USA; anindita.paul@oit.edu or aninditapaul08@gmail.com
2 Instituto Tecnológico Superior de Poza Rica, Tecnológico Nacional de México, Luis Donaldo Colosio Murrieta S/N, Arroyo del Maíz, Poza Rica 93230, Mexico; chua@itspozarica.edu.mx
3 Facultad de Instrumentación Electrónica, Universidad Veracruzana, Cto. Gonzalo Aguirre Beltrán S/N, Xalapa 91000, Mexico; hvazquez@uv.mx
4 Consejo Veracruzano de Investigación Científica y Desarrollo Tecnológico (COVEICYDET), Av Rafael Murillo Vidal No. 1735, Cuauhtémoc, Xalapa 91069, Mexico
5 Department of Electronics, INAOE, Puebla 72840, Mexico; adiazsan@inaoep.mx
* Correspondence: jramirezangulo@gmail.com; Tel.: +52-191-5474-4388

Abstract: A highly power-efficient, fully differential Miller op-amp with accurately controlled output quiescent current is introduced. The op-amp can drive both capacitive and resistive load due to the presence of the auxiliary amplifier. This amplifier helps to achieve class AB operation of the proposed op-amp. The fully differential auxiliary amplifier is compact and uses a resistive local common-mode feedback network. It consumes only 6% of the total current of the op-amp. The proposed op-amp has several innovative features. Incorporating the auxiliary amplifier helps to improve the unity gain frequency, power efficiency, slew-rate, and common-mode rejection ratio of the proposed op-amp. It can drive a wide range of resistive (200 Ω–1 MΩ) and capacitive loads (5 pF–300 pF). The op-amp has a large signal dynamic current efficiency of 8.6 and a large signal static current efficiency of 7.9. The small-signal figure of merit is 8.7 for R_L = 1 MΩ and 7.3 for R_L = 200 Ω.

Keywords: analog integrated circuit; class-AB; fully differential; miller effect; slew-rate

Citation: Paul, A.; Ramirez-Angulo, J.; Vázquez-Leal, H.; Huerta-Chua, J.; Diaz-Sanchez, A. Fully Differential Miller Op-Amp with Enhanced Large- and Small-Signal Figures of Merit. *J. Low Power Electron. Appl.* **2022**, *12*, 9. https://doi.org/10.3390/jlpea12010009

Academic Editor: Andrea Acquaviva

Received: 27 December 2021
Accepted: 5 February 2022
Published: 8 February 2022

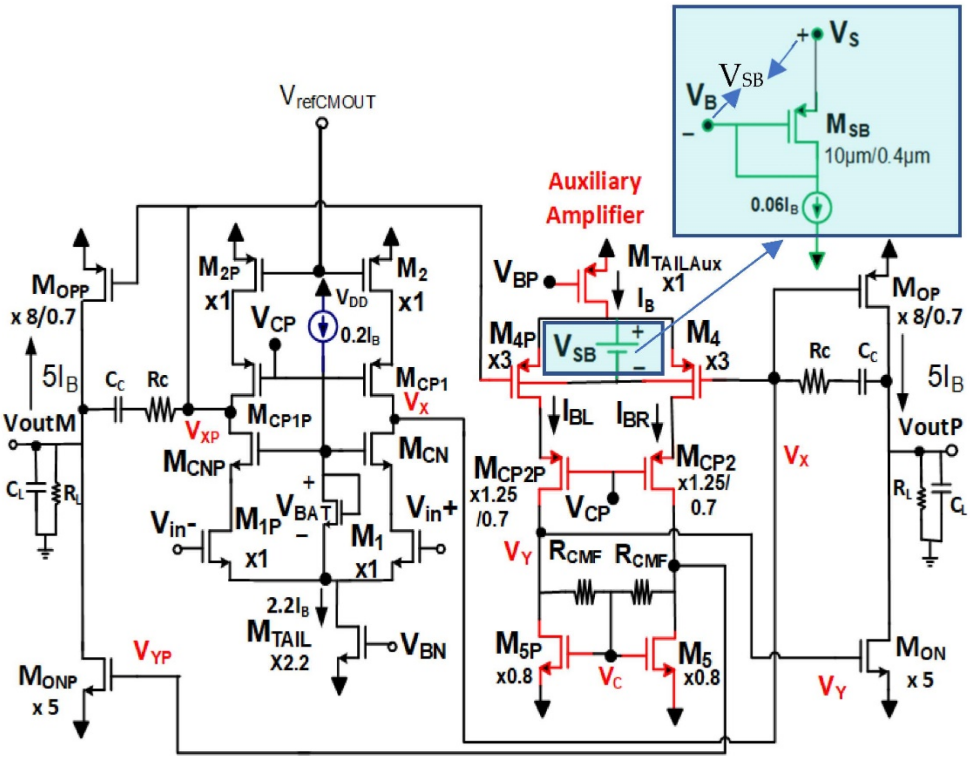
1. Introduction

Fully differential signal processing is a wise choice to maintain signal integrity in high-speed data acquisition systems such as communications, imaging, instrumentation, and video applications. Analog-to-digital converters [1] are essential components in high-speed data acquisition systems [2]. They need a differential amplifier to drive their differential input. The use of an integrated fully differential amplifier for modern mixed-signal [3] processing applications can provide many advantages such as: (a) increased immunity to external noise, (b) suppressed noise from power supply, (c) increased output voltage swing [4,5] for a given voltage rail, which is ideal for low-voltage systems, and (d) reduced even-order harmonics. Thus, designing a power-efficient fully differential amplifier [6] that can drive a wide range of resistive and capacitive loads is very useful for today's battery-operated portable electronic equipment, e.g., for the Internet of Things (IoT) [7] applications. The conventional class-A [8] fully differential Miller op-amp has an asymmetric slew-rate (SR) and a current efficiency CE = I_{outpk}/I_{totQ} < 0.5, where I_{outpk} is the minimum of the positive and negative peak output currents: $I_{outpk} = MIN\{I_{outpk}{}^{+}, I_{outpk}{}^{-}\}$. Most approaches to implement class AB output stages incorporate a floating battery between the gates of the output nMOS and pMOS transistors of a Miller op-amp. The popular class AB op-amps with floating batteries can be seen in [9,10]. A push-pull class AB op-amp [11–13] can be designed to drive both resistive and capacitive loads. However, the practical implementation of the floating battery is challenging in today's sub-micron technology, where the supply voltage is a serious constraint. In order to maintain a well-defined constant output quiescent current, I_{outQ} independent on supply voltage, nominal component values, and technology parameter variations, the floating battery scheme requires an additional I_{outQ} control circuit. The control circuit can be complex and further increase the supply requirements and power dissipation, which can significantly lower the current efficiency.

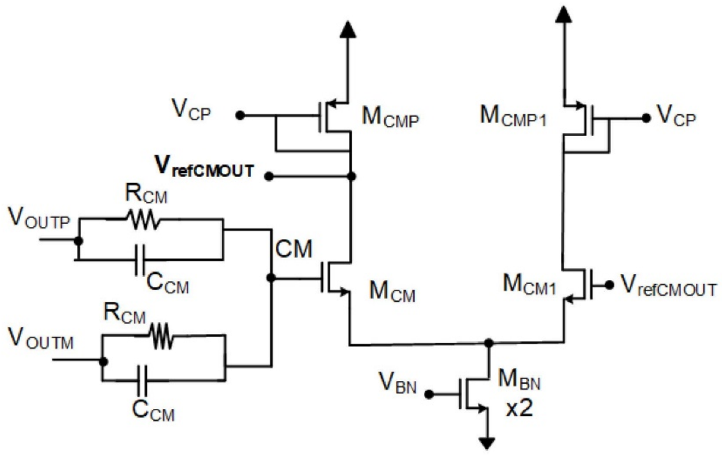
In the proposed approach, an improved class-AB op-amp is implemented by utilizing a compact fully differential auxiliary amplifier instead of two floating batteries. This approach significantly improves the figures of merit of the op-amp over fully differential class AB Miller op-amps based on a floating battery implementation. The following section describes the scheme in detail. The op-amp's performance is measured and compared using conventional: (a) large-signal dynamic current efficiency figures of merit $FoM_{Dyn} = SR.C_L/P_Q$ [14,15], where SR is slew rate, P_Q is the quiescent power dissipation, and C_L is load capacitance; (b) small-signal figures of merit $FoM_{SS} = f_u.C_L/P_Q$ [14,16], where f_u is the unity gain frequency; (c) and authors introduce a new large-signal static current efficiency figures of merit $FoM_{stat} = {I_{outp}}^{RL}/I_{Qtotal}$.

2. Proposed Op-Amp

The proposed class-AB op-amp shown in Figure 1 is a fully differential operational amplifier that can drive a wide range of resistive and capacitive loads. The op-amp uses a high gain telescopic input stage to keep a high DC open-loop gain even for low-valued resistive loads (high resistive loading conditions) that degrade the gain of the output stage and push-pull class AB output stages. Conventional Miller compensation is used to achieve stability over a wide range of loading conditions. The main contribution of this paper is the utilization of a compact, fully differential auxiliary amplifier (AuxAmp) that is used to achieve power-efficient class AB operation and improved unity gain frequency f_u in the proposed op-amp. As discussed in detail below, this approach offers several advantages with respect to conventional class AB schemes: it generates signal voltages V_Y and V_{YP} that are amplified versions and in phase with V_X and V_{XP}. In order to have enough headroom for the auxiliary amplifier's input differential pair (M_4, M_{4P}), a floating battery V_{SB} is used to reduce the threshold voltage of M_4, M_{4P}. This floating battery is implemented using a diode-connected PMOS transistor with a minimal quiescent current, just like V_{BAT} in the input stage is used. In addition, M_4 and M_{4P} are scaled up by a factor of three. This is to reduce their drain-source saturation voltage V_{DSsat}. A resistive local common-mode feedback (RLCMFB) network is used as a load in order to obtain moderate gain A_{Aux} from the AuxAmp. The non-inverting gain of the auxiliary amplifier is given approximately by $A_{Aux} = (V_Y - V_{YP})/V_X = (V_{YP} - V_Y)/V_{XP} = g_{m4,4P}R_{CMF}/2$. The AuxAmp increases the overall open-loop gain, the unity-gain frequency, and significantly the peak negative output currents and slew-rate of the op-amp. This AuxAmp also assists the proposed op-amp in maintaining an accurate output quiescent current I_{OutQ} minimizing the effect of temperature, supply voltage variations, and technology parameter variations on I_{OutQ}. The quiescent gate voltages V_Y, V_{YP} of transistors $M_{ON,ONP}$ control the quiescent output current I_{outQ}. Under quiescent conditions, no current flows in resistors R_{CMF}, and the gate-source voltage of $M_{ON,ONP}$ is $V_Y = V_{YP} = V_{GS5P,5Q}$, independent of the value of R_{CMF} that sets the gain A_{Aux}. The AuxAmp consumes only 6% of the total op-amp quiescent current, which helps to keep the op-amp's current efficiency high.



(a)



(b)

Figure 1. (**a**) Proposed fully differential op-amp. (**b**) Common-mode feedback network.

2.1. Operation

In the presence of positive input differential signals, the voltage at node V_X decreases and at V_{XP} increases, while the voltages at node V_Y decrease and at node V_{YP} increase by a factor A_{Aux}. As a result, M_{OP} will provide a large output positive current and M_{ONP} a large negative output current. The drain currents of M_{ON}, M_{OPP} will decrease and eventually reach zero. Similarly, M_{ON} can provide large negative output currents for negative input signals, and M_{OPP} can provide large positive output currents as the voltage at V_{XP} decreases. In the conventional floating battery scheme where variations V_X, V_{XP} are transferred directly to V_Y, V_{YP}, the maximum negative output current is limited by the relatively small positive excursion of V_X, V_{XP} transferred to V_Y, V_{YP}. In the proposed scheme, the gain A_{Aux} increases significantly the excursion of V_Y, V_{YP} and the peak negative output current. A_{Aux} also increases the open-loop gain, common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and unity gain frequency of the op-amp.

2.2. Frequency Response

The gain of the telescopic input stage A_I is given by (1).

$$A_I = g_{m1} R_X = g_{m1}\left(g_m {r_o}^2/2\right) \tag{1}$$

For simplicity, it is assumed that g_m and r_o are the transconductance gain and output resistance of all unit size NMOS and PMOS transistors, and R_X is resistance at nodes V_X, V_{XP}.

The single-ended gain of the auxiliary amplifier is given by $A_{Aux} = (g_{m4,4P} R_{Y,YP})/2$. $R_{Y,YP}$ is the resistance at nodes V_Y and V_{YP}: where $R_Y = r_{o4P}.g_{mCP2P}.r_{oCP2P}||R_{CMF}||r_{o5P}$. The value of the R_{CMF} is selected in such a way so that $R_{CMF} \ll r_{o4P}, r_{oCP2P}, r_{o5P}$. As a result, R_Y can be approximated as $R_Y \approx R_{CMF}$. Thus, gain of the auxiliary amplifier can be expressed approximately by (2).

$$A_{Aux} \approx (g_{m4,4P} R_{CMF})/2 \tag{2}$$

The gain of the output stage is given by (3).

$$A_{out} = (g_{mOP} + A_{Aux} g_{mON}) R_{out} \tag{3}$$

where R_{out} is $R_{out} = r_{oOP}||r_{oON}||R_L$. g_{mOP} and g_{mON} are transconductance gains of output transistors M_{OP} and M_{ON}.

Thus, the open-loop DC gain A_{OLDC} of the proposed op-amp is expressed by (4).

$$A_{OLDC} = A_I A_{out} = \left((g_m r_o)^2/2\right)\left(g_{mouteff} R_{out}\right) \tag{4}$$

where $g_{mouteff} = g_{mOP} + A_{Aux} g_{mON}$.

The dominant pole is at node $V_{X,\,XP}$, and is given by (5).

$$f_{PDOMX} = 1/(2\pi R_X C_X) \tag{5}$$

Here, C_X is given by $C_X = (1 - (-A_{out}))C_C$.

The gain-bandwidth product (GBW) of the proposed op-amp is given by the expression (6).

$$\begin{aligned} GBW &= (A_I A_{out}) \tfrac{1}{2\pi R_X (1 + A_{out}) C_C} \\ &= (g_{m1} A_{out}) \tfrac{1}{2\pi (1 + A_{out}) C_C} \end{aligned} \tag{6}$$

A_{out} is strongly dependent on R_L. For very low R_L values, it can even take values $|A_{out}| < 1$. Besides the dominant pole, the proposed op-amp has two pairs of high-frequency poles: one at V_Y (V_{YP}) and another at V_{outP} (V_{outM}). The output high-frequency pole f_{Pout} is given in (7).

$$f_{Pout} = (g_{mOP} + A_{Aux} g_{mON} + G_L)/(2\pi C_L) \tag{7}$$

In the proposed op-amp, the auxiliary amplifier causes f_{Pout} to be higher than output pole frequency f_{Pout_conv} of the conventional op-amp shown in Figure 2. The high-frequency output pole of the conventional op-amp of Figure 2 is given in (8).

$$f_{Pout\_conv} = (g_{mOP\_conv} + G_L)/2\pi C_L \tag{8}$$

where g_{mOP_conv} is the transconductance gain of the output PMOS transistor of the conventional op-amp. The value of f_{Pout} of the proposed op-amp for C_L = 300 pF and R_L = 1 MΩ is 6 MHz, whereas the output pole frequency for the conventional-A op-amp f_{Pout_conv} is only 687 kHZ for a similar loading condition.

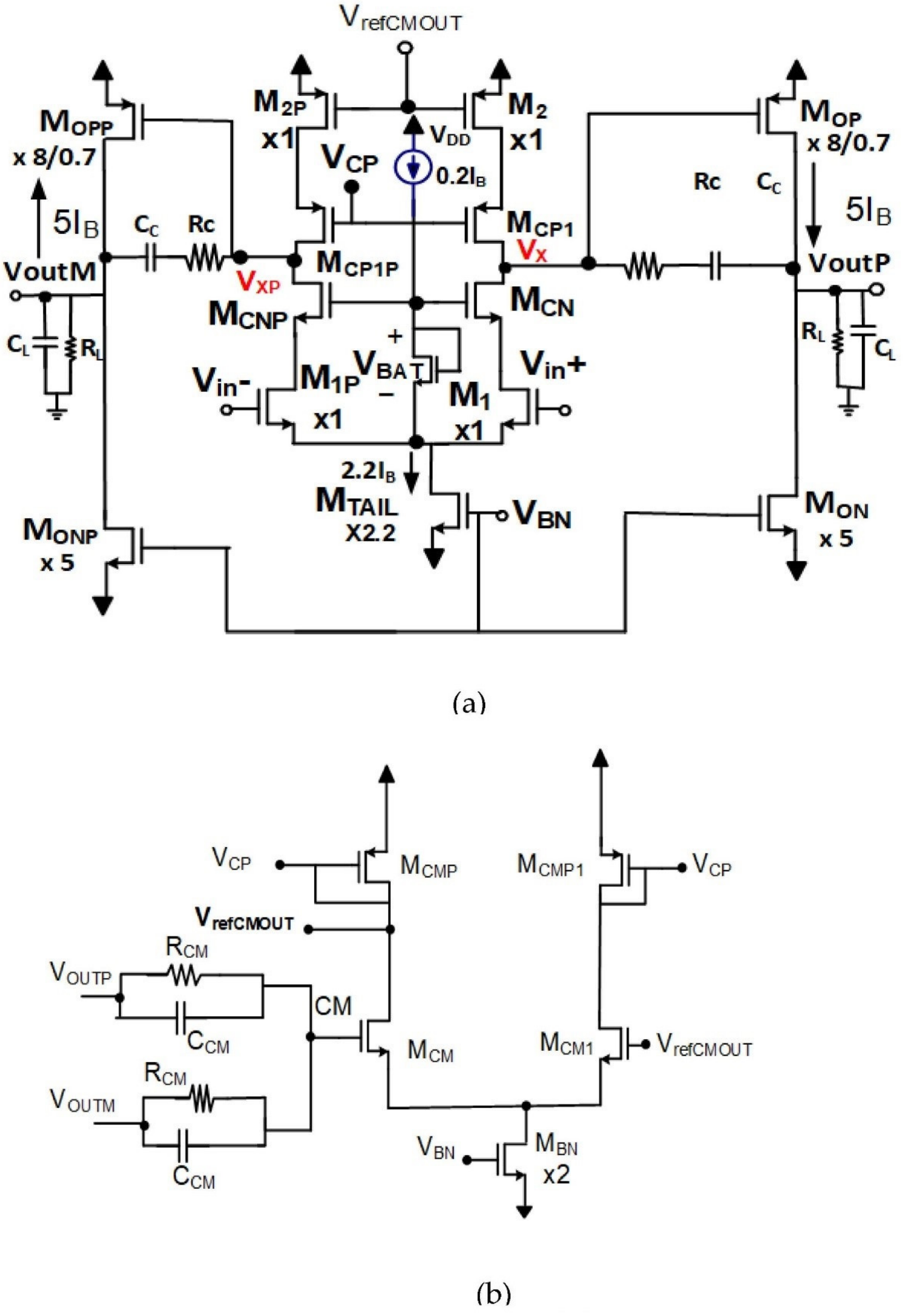


Figure 2. (**a**) Conventional Class-A amplifier. (**b**) Common-mode feedback network.

It can be seen that the auxiliary amplifier in the proposed op-amp shifts the output pole to a higher frequency. Consequently, a higher unity gain frequency can be obtained in the proposed op-amp.

The pole at nodes V_Y, V_{YP} is expressed by (9).

$$f_{PY} = 1/(2\pi R_{CMF} C_Y) \quad (9)$$

Here, C_Y is given by $C_Y \approx C_{gsON} + C_{dBCP2P} + C_{dB5P} + C_{gdON}(1 + (A_{out}/A_{VY})) + C_{gd5P}$. From (9), it can be said that the location of the poles (f_{PY}) at node $V_{Y,YP}$ depends on the value of R_{CMF}. The high-frequency pole f_{PY} is inversely proportional to the value of $R_{CMF,}$ i.e., $f_{PY} \propto 1/R_{CMF}$. Again from (2), it can be seen that the gain of the auxiliary amplifier depends on the value of R_{CMF}, i.e., $A_{Aux} \propto R_{CMF}$. Thus, the selection of R_{CMF} plays an essential role in determining the stability, overall open-loop gain, and slew-rate improvement of the proposed op-amp as the gain of the auxiliary control of the dynamic current of $M_{ON,ONP}$. In the proposed circuit, the value of the R_{CMF} is 60 kΩ. This selection of R_{CMF} helps to place f_{PY} at a higher frequency than the unity gain frequency of the op-amp. The higher value of f_{pY} helps achieve approximately constant gain from the auxiliary amplifier until the proposed op-amp's unity gain frequency. The value of the f_{PY} in the proposed op-amp is 29 MHz, which is twice larger than the unity gain frequency of the proposed op-amp.

The zero is given by (10).

$$f_z = 1/\left(2\pi C_C\left(R_C - (g_{mOP} + A_{Aux} g_{mON})^{-1}\right)\right) \quad (10)$$

3. Results

The proposed and conventional class-A (Conv-A) op-amps are simulated with Cadence using TSMC 180 nm CMOS technology parameters. For a fair comparison, equal unit size pMOS and nMOS transistors with W/L = 10 μm/0.4 μm are used in both op-amps. The output nMOS and pMOS transistors are scaled up by the factors 5/1 and 8/0.7 with respect to unit size transistors. The value of the compensation capacitor is 3 pF for both op-amps. The only difference between the proposed and Conv-A op-amp is that the Conv-A op-amp does not have the auxiliary amplifier, which only increases power dissipation by 6%. The schematic diagram of the Conv-A amplifier is given in Figure 2. The value of the RCMF used in the auxiliary amplifier of the proposed op-amp is 60 kΩ. The values of RC in the proposed op-amp are 200 Ω and 6 kΩ for the capacitive loads CL = 5 pF and 300 pF, respectively. For the fixed CL, the selected compensation network can drive RL values from 1 MΩ to 200 Ω, whereas in the conventional op-amp for a similar capacitive load CL = 300 pF and 5 pF, the values of RC are 18 kΩ and 500 Ω. A bias current IB = 17 μA, dual supply voltages VDD = 900 mV, VSS = −900 mV, and a reference common-mode output voltage VrefCM = 0 V are used for the simulations of both op-amps. Figures 3 and 4 show open-loop frequency responses of the Conv-A and the proposed op-amps. It can be seen from the responses that both op-amps are stable for the wide range of capacitive (5 pF–300 pF) and resistive load (200 Ω–1 MΩ). However, the proposed op-amp's gain is higher and varies from 116.4 dB to 74.5 dB for RL, changing from 1 MΩ to 200 Ω. For similar loading conditions, the Conv-A op-amp has the gain that varies from 96.8 dB to 57.2 dB. The proposed op-amp achieves a higher gain because of the auxiliary amplifier.

The transient response of the proposed op-amp was simulated using the unity gain closed loop inverting amplifier configuration, shown in Figure 5. Equal R_{in} and R_f values of 100 kΩ were used in the simulation. Figure 6 shows the transient response of the proposed and Conv-A op-amps in unity gain inverting configuration for a 1 MHz, ±400 mVpp pulse input, with C_L = 300 pF and two resistive load values R_L = 200 Ω and 1 MΩ. From the pulse response, it can be seen that the Conv-A op-amp cannot follow the input pulse, whereas the proposed op-amp can follow the input for all the considered loading conditions. The proposed op-amp has a slew rate of 13 V/μs, whereas the Conv-A op-amp has a much lower slew rate of 0.9 V/μs. The proposed op-amp can provide ±4.36 mA peak currents to a 300 pF capacitor. On the contrary, the Conv-A op-amp can provide only 58 μA peak negative output currents, which corresponds to the class-A op-amp's output quiescent current (I_{outQ}). Figure 7 shows the single-ended output currents of both op-amps in the 200 Ω resistive load for ±400 mV pulse input. It can be seen that due to the substantial limitation of the negative current in the Conv-A op-amp, the outputs cannot follow the negative excursion of the input pulse. As a result, the op-amp cannot provide differential complementary output signals. It can be seen that the peak negative current is –58 µA. On the other hand, the proposed op-amp can provide complementary output signals with equal positive and negative output currents of ±1 mA in the 200 Ω resistive loads for the ±200 mV pulse input.

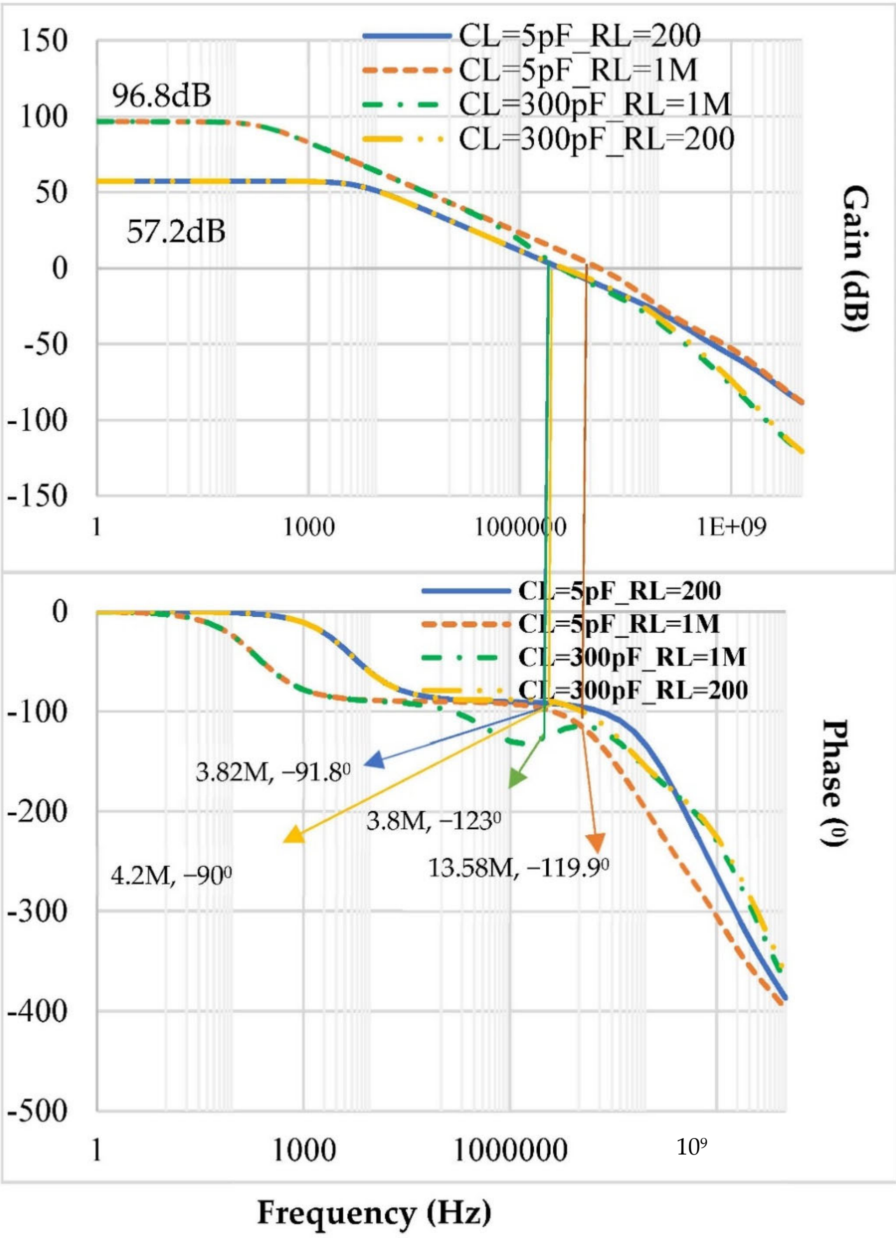


Figure 3. Frequency response of Conv-A op-amp.

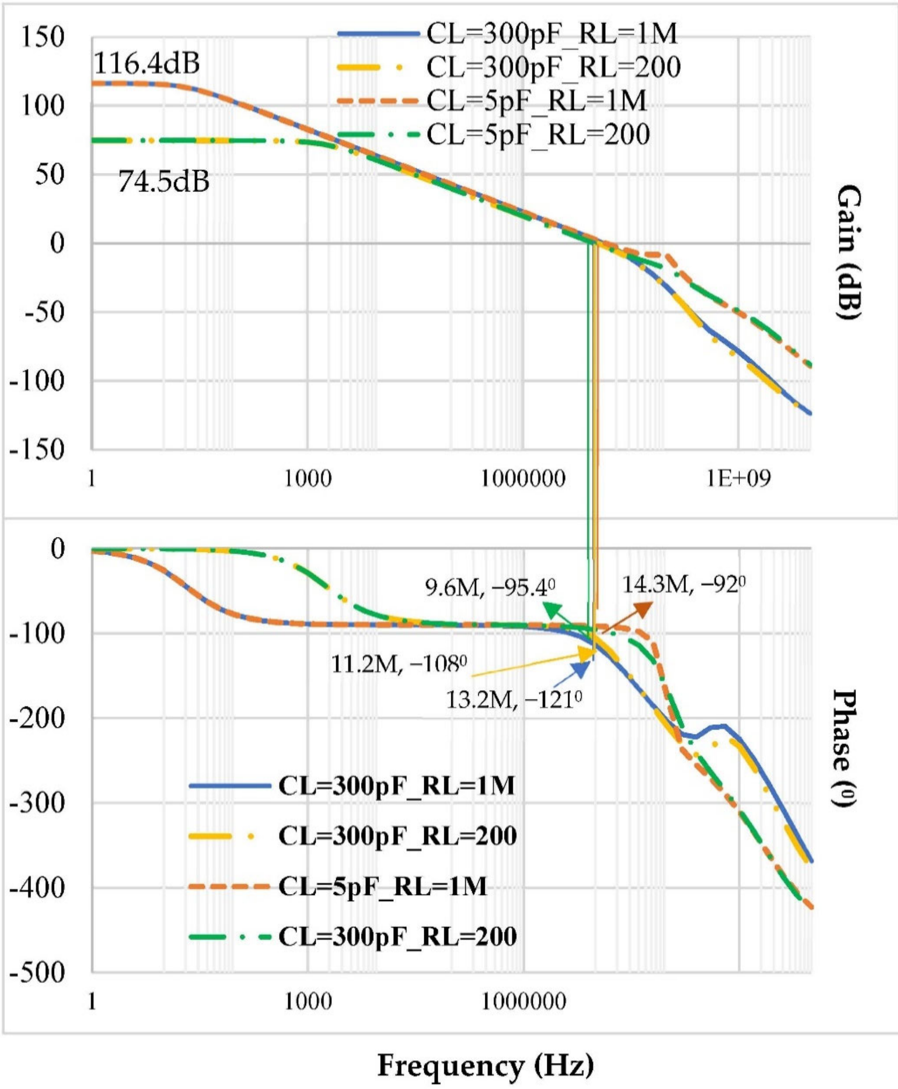


Figure 4. Frequency response of proposed op-amp.

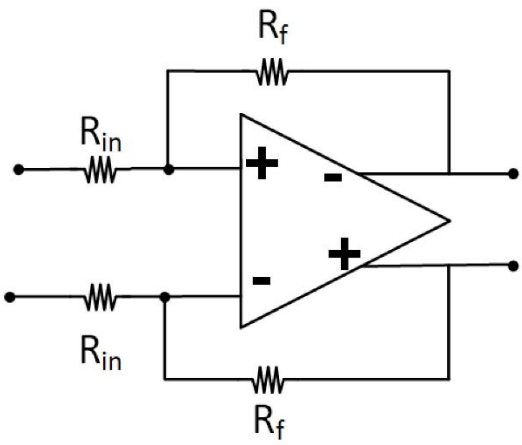


Figure 5. Unity gain inverting fully differential amplifier.

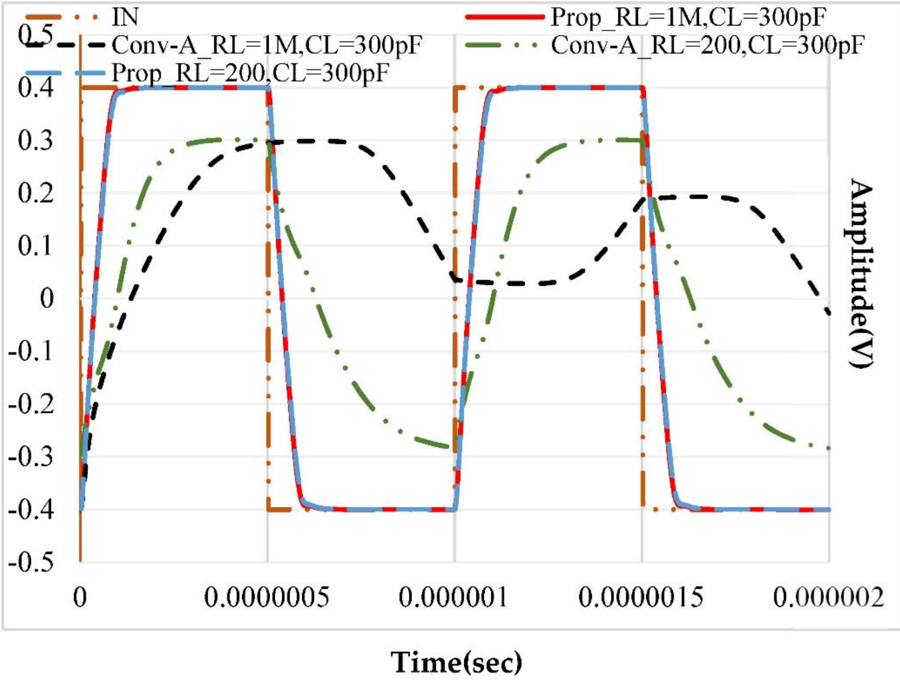


Figure 6. Pulse response of the proposed and conventional op-amp, C_L = 300 pF and R_L = 1 MΩ and 200 Ω.

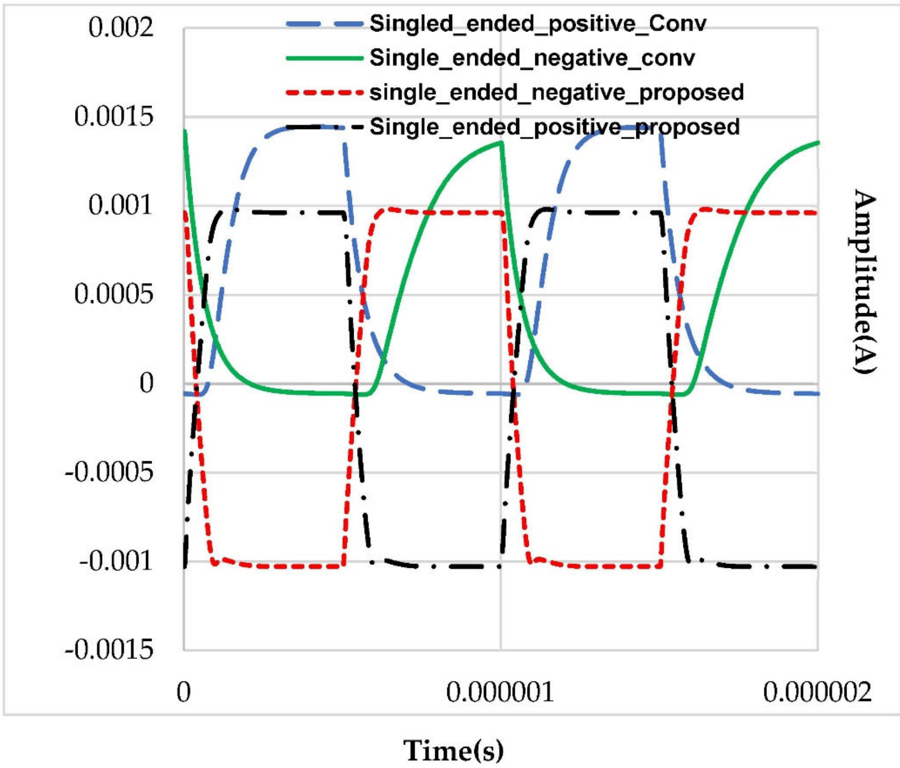


Figure 7. Single-ended transient current in R_L = 200 Ω of the proposed and Conv-A op-amp for ±400 mV pulse input.

Figure 8 shows the output current of the proposed and Conv-A op-amp for C_L = 300 pF, 5 pF, and R_L = 1 MΩ for the ±400 mVpp 1 MHz pulse input. The proposed op-amp can provide ±4.36 mA peak currents to 300 pF load capacitors. On the contrary, the Conv-A op-amp can provide only 58 µA negative output, which corresponds to the class-A op-amp's output quiescent current (I_{outQ}). Figure 9 shows the total harmonic distortion of the proposed and Conv-A op-amp for a 400 mV amplitude sinusoidal signal whose frequency is varied from 1 kHz to 8 MHz. It can be seen that the proposed op-amp has much lower (35 dB) harmonic distortion than the Conv-A op-amp.

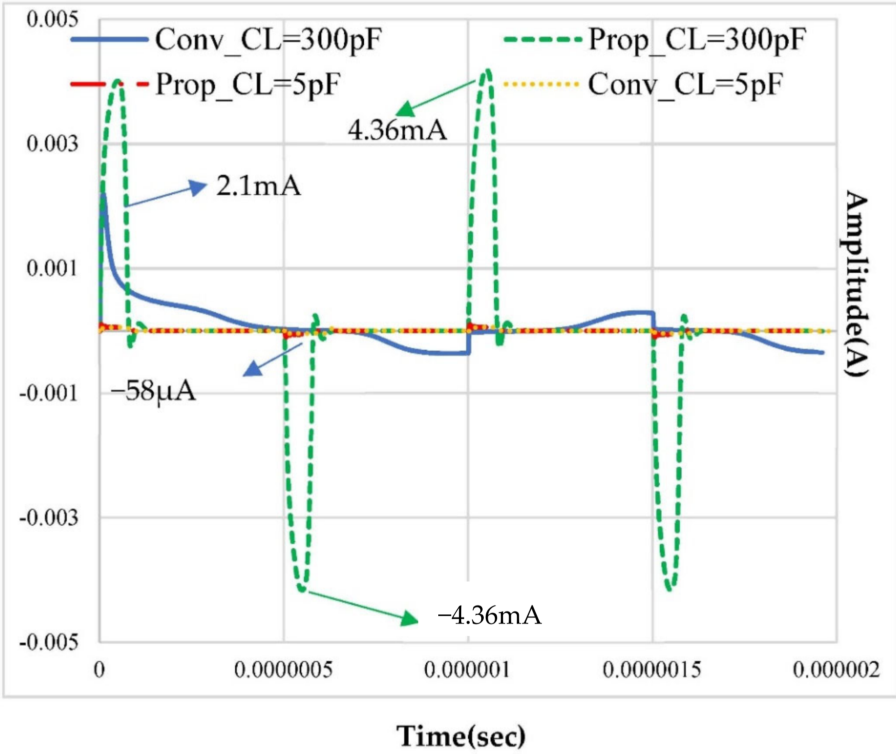


Figure 8. Output current of the proposed and conventional op-amp for C_L = 300 pF, 5 pF and R_L = 1 MΩ for the ±400 mVpp, 1 MHz pulse input.

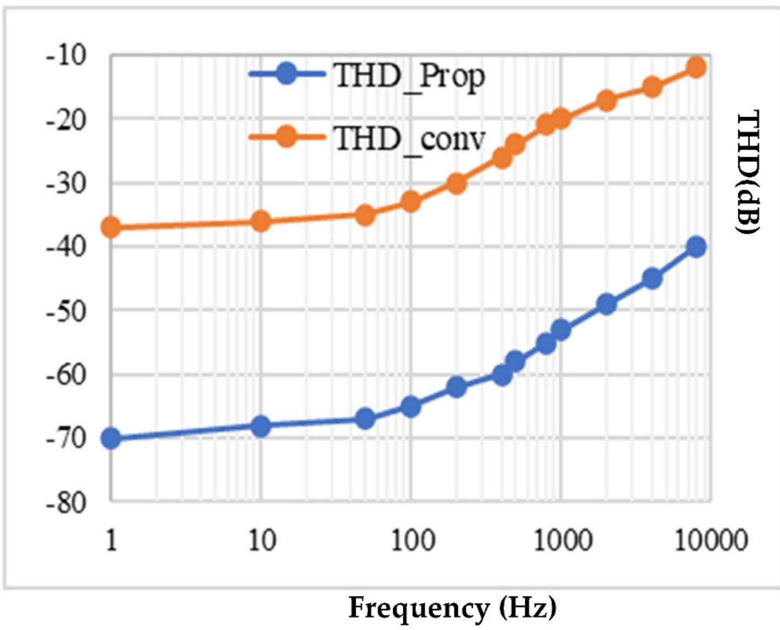


Figure 9. THD of the proposed op-amp at different frequencies for 400 mV amplitude sinusoidal signal and R_L = 200 Ω, C_L = 300 pF.

The proposed op-amp has close to rail-to-rail output swing from −1.69 V to 1.69 V for a ±1.7 V, 0.5 MHz triangular input signal. It can be seen in Figure 10. Tables 1–3 show the corner analysis of the proposed op-amp at different temperatures. It can be asserted that the proposed op-amp is robust against the variation of process technology and temperature. The standard deviation (Std.) for each parameter at different corners is calculated for each considered temperature and given in the table. The common-mode rejection ratios (CMRRs) and power supply rejection ratios (PSRRs) are measured, including 2% typical mismatches between the differential pair transistors in both op-amps. The positive and negative PSRRs are 95 dB and 92 dB. The CMRR of the proposed op-amp is 96 dB. Table 4 shows comprehensive simulation results of the proposed op-amp and comparisons of the performance with state-of-the-art works. The proposed op-amp has the highest static and dynamic current efficiency figures of merit.

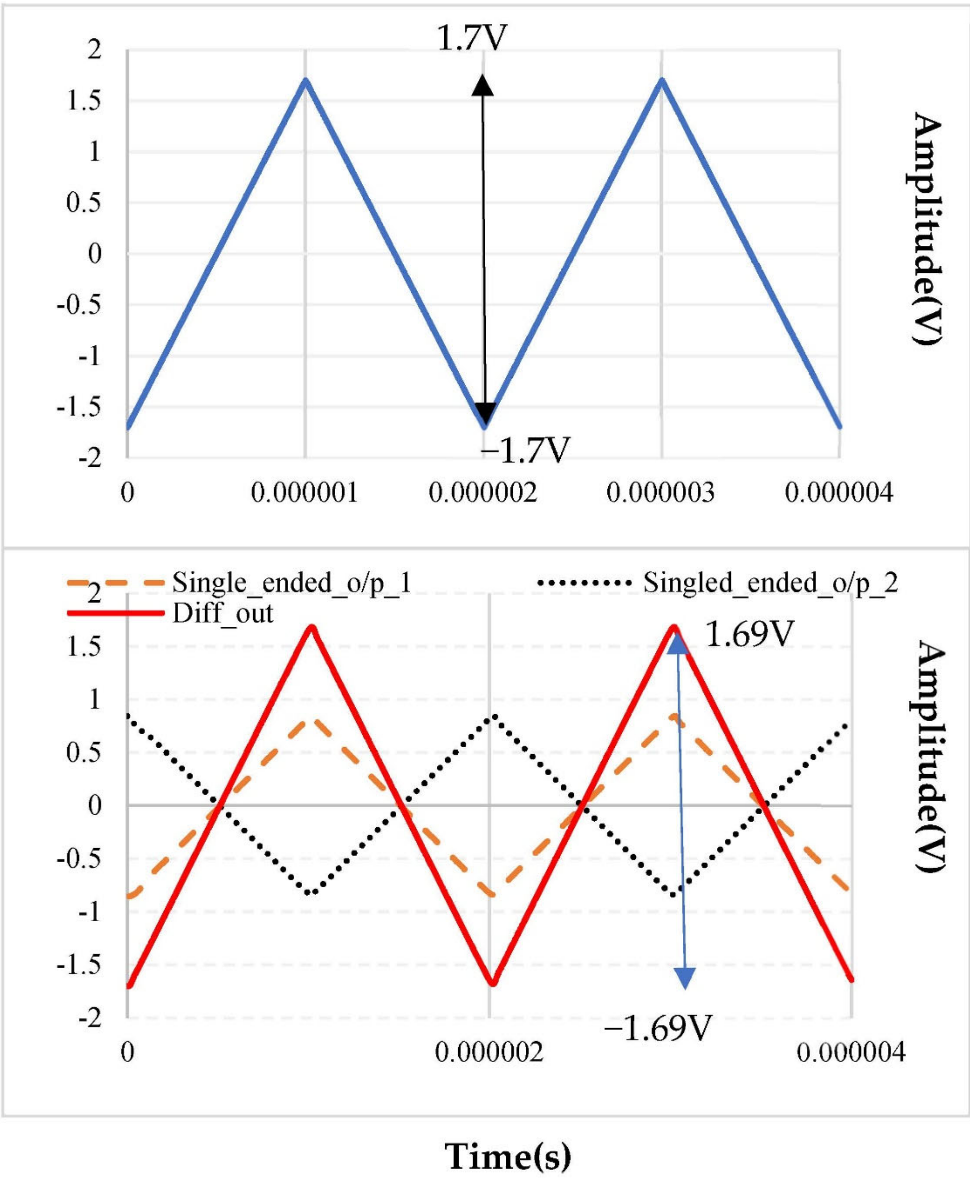


Figure 10. Determination of close to rail-to rail output swing using a ±1.7 V, 0.5 MHz, triangular input signal.

Table 1. Corner analysis of op-amp at T = −20 °C.

Corner	tt	ff	fs	sf	ss	Std.
I_{TotalQ} (μA)	253	251	250	249	247	2
f_u (MHz) @ R_L =1 MΩ	15.5	16.9	15.2	14	13.5	1.19
PM (°) @ R_L =1 MΩ	59	56	56	62	63	2.92
Gain	117.9	114	117.6	118	117	1.5
SR (V/μs)	13	11	10	10	9	1.4
$I_{outpk}{}^{-}$ R_L =200 Ω (mA)	2	1.9	1.9	2	2	0.05

Table 2. Corner analysis of op-amp at T = 27 °C.

Corner	tt	ff	fs	sf	ss	Std.
I_{TotalQ} (μA)	253	252	250	252	255	1.62
f_u (MHz) @ R_L =1 MΩ	13.4	14.5	13	13.2	12	0.8
PM (°) @ R_L =1 MΩ	59	58	61	60	60	1.01
Gain (dB)	116.4	110	113	114.2	120	3.35
SR (V/μs)	13	12	11	12	14	1.01
$I_{outpk}{}^{-}$ R_L =200 Ω (mA)	2	1.9	2	2	2	0.04

Table 3. Corner analysis of op-amp at T = 120 °C.

Corner	tt	ff	fs	sf	ss	Std.
I_{TotalQ} (μA)	251	259	251	252	255	3.07
f_u (MHz) @ R_L = 1 MΩ	9.5	9.4	9.5	10	9.2	0.26
PM (°) @ R_L = 1 MΩ	58	58	58	57	59	0.63
Gain (dB)	100	95	111	110	117	7.9
SR (V/μs)	11	14	11	12	15	1.62
$I_{outpk}{}^{-}$ R_L = 200 Ω (mA)	2	1.8	1.9	2	2	0.08

Table 4. Summary of the simulated results and performance comparison.

Parameter (Units)	Proposed	Conv-A	[17]	[18]	[19]	[20]	[21]
Inversion Level	SI	SI	SI	SI	SI	SI	SB
CMOS Process (μm)	0.18	0.18	0.18	0.18	0.18	0.35	0.18
Supply Voltage (V)	±0.9	±0.9	1.8	1.8	1.8	3.3	±300
Capacitive Load (pF)	5–300	5–300	10	1	100	25	10

Table 4. *Cont.*

Parameter (Units)	Proposed	Conv-A	[17]	[18]	[19]	[20]	[21]
Resistive Load (Ω)	1 M/200	1 M/200	-	-	-	500	-
SR (V/µs)	13	0.9	17.83	650	63	248.6	8.4
DC Gain (dB)	116.4/ 74.5	96.8/57.4	73	85.6	84	69.5	42.2
PM (°)	59/82 @C_L = 300 pF, R_L = 1 MΩ/ @C_L = 300 pF, R_L = 200 Ω	57/90	64	66.7	77	69.65	54
f_u (MHz)	13.32/11.21	3.88/4.2	15	987	91	354	16.1
CMRR @DC (dB)	96	90	80	80	-	45	85.12
PSRR+ @DC (dB)	95	87	78	78	-	27.5	53.25
PSRR-@DC (dB)	92	85	-		-	-	56.89
$I_{outpk}{}^{+}{}_{RL}$ (µA)	2000 @200 Ω	1500 @200 Ω	-	-	-	2000 @500 Ω	-
$I_{outpk}{}^{-}{}_{RL = 200\,\Omega}$ (µA)	2000	1500	-	-	-	0	-
I_{totQ} (µA)	253	182	239	1000	1722	8042	41.3
Power (µW)	455	327.6	429.68	1800	3100	26,540	24.8
Input Referred Noise	317@1 kHz nV/$\sqrt{\text{Hz}}$	330@1 KHz nV/$\sqrt{\text{Hz}}$	84@100 kHz nV/$\sqrt{\text{Hz}}$	118 µV_{rms} (1 Hz–100 MHz)	340@100 kHz nV/$\sqrt{\text{Hz}}$	35.52 @100 kHz	69@1 MHz
FOM_{CEDyn} (V.pF/µs.µW)	8.6	0.82	0.41	0.4	2	0.23	3.39
FOM_{SS} (MHz.pF/µW)	8.7/7.3	3.5/3.8	0.35	0.5	2.9	0.33	6.49
FOM_{CEStat} (µA/µW)	7.9	-	-	-	-	0.08	-

4. Conclusions

The proposed fully differential op-amp can drive a wide range of resistive (200 Ω–1 MΩ) and capacitive (5–300 pF) loads. A compact auxiliary amplifier is used in the op-amp. This sets a well-controlled output quiescent current and increases the op-amp's unity gain frequency, significantly the peak negative output current. The proposed op-amp has high dynamic and static current efficiencies as well as a large and small-signal figure of merit. The auxiliary amplifier consumes only 6% of the total op-amp current, making the proposed op-amp highly power-efficient.

Author Contributions: Investigation, writing, review, and editing were completed by A.P., J.R.-A., H.V.-L., J.H.-C. and A.D.-S. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not Applicable.

Data Availability Statement: Data is contained within the article.

Conflicts of Interest: There is no conflict of interest.

References

1. Walden, R.H. Analog-to-digital converter survey and analysis. *IEEE J. Sel. Areas Commun.* **1999**, *17*, 539–550. [CrossRef]
2. Karki, J. Fully differential amplifier design in high-speed data acquisition systems. *Analog Des. J.* **2002**. Available online: https://www.ti.com.cn/cn/lit/an/slyt034/slyt034.pdf#page=35 (accessed on 26 December 2021).
3. Kobayashi, H.; Kushita, N.; Tran, M.T.; Asami, K.; San, H.; Kuwana, A.; Hatta, A. Analog/Mixed-Signal/RF Circuits for Complex Signal Processing. In Proceedings of the 2019 IEEE 13th International Conference on ASIC (ASICON), Chongqing, China, 29 October–1 November 2019; pp. 1–4.
4. Gray, P.R.; Hurst, P.J.; Lewis, S.H.; Meyer, R.G. *Analysis and Design of Analog Integrated Circuits*, 5th ed.; Wiley: Hoboken, NJ, USA, 2001.
5. Spinelli, E.M.; Haberman, M.A.; Guerrero, F.N.; García, P.A. A High Input Impedance Single-Ended Input to Balanced Differential Output Amplifier. *IEEE Trans. Instrum. Meas.* **2020**, *69*, 1682–1689. [CrossRef]
6. Banu, M.; Khoury, J.M.; Tsividis, Y. Fully differential operational amplifiers with accurate output balancing. *IEEE J. Solid-State Circuits* **1988**, *23*, 1410–1414. [CrossRef]
7. Hassan, A.H.; Mostafa, H.; Salama, K.N.; Soliman, A.M. A Low-Power Time-Domain Comparator for IoT Applications. In Proceedings of the 2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS), Windsor, ON, Canada, 5–8 August 2018; pp. 1142–1145.
8. Razavi, B. *Design of Analog CMOS Integrated Circuits*, 1st ed.; McGraw-Hill: New York, NY, USA, 2001.
9. Monticelli, D.M. A quad CMOS single-supply op amp with rail-to-rail output swing. *IEEE J. Solid-State Circuits* **1986**, *21*, 1026–1034. [CrossRef]
10. Langen, K.D.; Huijsing, J.H. Compact low-voltage power-efficient operational amplifier cells for VLSI. *IEEE J. Solid-State Circuits* **1998**, *33*, 1482–1496. [CrossRef]
11. Pang-Cheng, Y.; Jiin-Chuan, W. A class-B output buffer for flat-panel-display column driver. *IEEE J. Solid-State Circuits* **1999**, *34*, 116–119. [CrossRef]
12. Gregorian, R.; Temes, G.C. *Analog MOS Integrated Circuits for Signal Processing*, 1st ed.; Wiley Series on Filters: Design Manufacturing and Applications; Wiley: Hoboken, NJ, USA, 1986.
13. Aloisi, W.; Giustolisi, G.; Palumbo, G. A 1-V CMOS output stage with high linearity. In Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS' 03., Bangkok, Thailand, 25–28 May 2003; p. I.
14. Grasso, A.D.; Palumbo, G.; Pennisi, S. Advances in Reversed Nested Miller Compensation. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2007**, *54*, 1459–1470. [CrossRef]
15. Sutula, S.; Dei, M.; Terés, L.; Serra-Graells, F. Variable-Mirror Amplifier: A New Family of Process-Independent Class-AB Single-Stage OTAs for Low-Power SC Circuits. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2016**, *63*, 1101–1110. [CrossRef]
16. Kuo, P.Y.; Tsai, S.D. An Enhanced Scheme of Multi-Stage Amplifier With High-Speed High-Gain Blocks and Recycling Frequency Cascode Circuitry to Improve Gain-Bandwidth and Slew Rate. *IEEE Access* **2019**, *7*, 130820–130829. [CrossRef]
17. Basumata, U.; Mondal, A.; Das, S.; Rahaman, H. Design of Two-Stage Fully-Differential Driver in SAR ADC with Indirect Feedback Compensation Technique. In Proceedings of the 2021 International Symposium on Devices, Circuits and Systems (ISDCS), Vellore, India, 3–5 March 2021; pp. 1–5.
18. Ahmed, M.; Shah, I.; Tang, F.; Bermak, A. An improved recycling folded cascode amplifier with gain boosting and phase margin enhancement. In Proceedings of the 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, Portugal, 24–27 May 2015; pp. 2473–2476.
19. Shamsi, H.; Anisheh, S.; Abbasizadeh, H.; Dadkhah, C.; Lee, K.-Y. A 84 dB DC-Gain Two-Stage Class-AB OTA. *IET Circuits Devices Syst.* **2019**, *13*, 614–621. [CrossRef]
20. Neag, M.; Kovács, I.; Oneț, R.; Câmpanu, I. Design options for high-speed OA-based fully differential buffers able to drive large loads. *Microelectron. J.* **2021**, *114*, 105115. [CrossRef]
21. Renteria-Pinon, M.; Ramirez-Angulo, J.; Diaz-Sanchez, A. Simple Scheme for the Implementation of Low Voltage Fully Differential Amplifiers without Output Common-Mode Feedback Network. *J. Low Power Electron. Appl.* **2020**, *10*, 34. [CrossRef]