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Review

Review on the Basic Circuit Elements and Memristor Interpretation: Analysis, Technology and Applications

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Abstract: Circuit or electronic components are useful elements allowing the realization of different circuit functionalities. The resistor, capacitor and inductor represent the three commonly known basic passive circuit elements owing to their fundamental nature relating them to the four circuit variables, namely voltage, magnetic flux, current and electric charge. The memory resistor (or memristor) was claimed to be the fourth basic passive circuit element, complementing the resistor, capacitor and inductor. This paper presents a review on the four basic passive circuit elements. After a brief recall on the first three known basic passive circuit elements, a thorough description of the memristor follows. Memristor sparks interest in the scientific community due to its interesting features, for example nano-scalability, memory capability, conductance modulation, connection flexibility and compatibility with CMOS technology, etc. These features among many others are currently in high demand on an industrial scale. For this reason, thousands of memristor-based applications are reported. Hence, the paper presents an in-depth overview of the philosophical argumentations of memristor, technologies and applications.

Keywords: circuit elements; circuit variables; memristor; argumentation; analysis; technology; modeling; applications

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1. Introduction

Electronic engineering plays a crucial role in modern civilization in both the analogue and digital domains. This was made possible by the contribution of the circuit elements that are commonly called electronic components. Figure 1 shows some examples of electronic components. Depending on their interactions with the other parts of the circuit, electronic components are often placed into two categories, namely, active and passive circuit elements. Active circuit elements are capable of generating electrical energy or power gain to the other parts of the circuit which include for example, transistors, operational amplifiers, integrated circuits, voltage and current sources, etc. Passive circuit elements can only use or dissipate the available power sources, for example resistor, capacitor, inductor, thermistor, light-dependent resistor (LDR), etc. In general, active circuit elements are capable of generating electrical power while passive circuit elements can only store, use or deny the generated power. Additionally, a transistor is an active device owing to its ability to generate power gain. These circuit elements altogether form electronic components (see Figure 1) that have been a major bedrock for modern civilization owing to their tremendous contribution in the advancement of electronic industries. The three branches in Figure 1, illustrate the generalized evolution of the electronic components accordingly. The first, second and third branches give, respectively, the fundamental circuit elements, semiconductor devices and many other components designed to achieve various circuit functionalities.

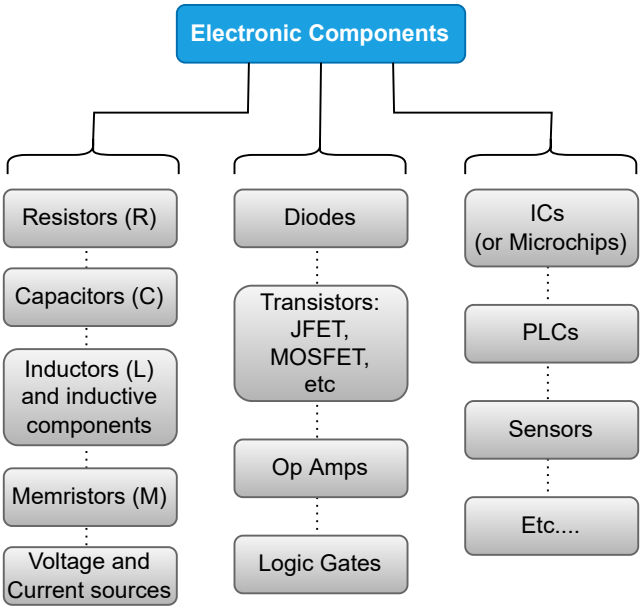

Figure 1. Examples of some electronic components.

The transistor has been the leading component in electronic gadgets due to its reliable capabilities in switching, amplification and micro-scalability. The performances of an electronic device are improved by incorporating smaller and faster circuit components. This approach serves many purposes, for example portability and improved power consumption because fewer components are involved. However, transistor scaling is challenging as they are presently few nano-meters in size, hence the need for an alternative to transistors for future electronic systems design. Scalability of electronic components becomes an important factor in order to meet the increasing demand of reliable digital electronic systems. Currently, nano-scalability is one of the main challenges in the nano-electronics industries [1], especially due to the high demand of faster and more reliable systems (small, medium and large scales). For seven decades, transistors have been the leading component contributing to the exponential advancement in electronic systems and designs [2]. However, modern transistors suffer from nano-scalability issues owing to their infinitesimal dimensions [3]. The performance of devices and systems improves with the reduction in the size of their constitutive circuitries [4] and often brings forth advantages such as reliability, lower power consumption, speed, cheapness, portability, etc., thanks to memristor nano-scalability.

The memristor is a two-terminal nonlinear dynamic electronic device and is typically a passive nano-device whose conductivity is controlled by the time-integral of the applied voltage (also known as flux) across it or the time-integral of the current (also known as charge) flowing through it. This new component was first envisioned by circuit theorist Leon Chua in 1971 and it is proclaimed to be the fourth basic passive circuit element (alongside the resistor, capacitor and inductor) having interesting features that make it suitable for various applications. For example: high-density memory applications, bio-electronics or bio-inspired applications, storage and processing of big data, and image recognition and processing. It is impossible to completely discard the transistor due to the emergence of the memristor because it is an active device while the memristor is a passive one. However, using both of them in a circuit will tremendously improve its performance, because one memristor can replace multiple transistors.

Memristive behaviour has been observed experimentally for two centuries but remained unidentified because no one had ever thought of the contingency of the fourth basic circuit element in electronics. The first human-made memristor dated in 1801 by English chemist Humphry Davy [5], in which the fingerprint of a memristor manifested experimentally with a carbon arc discharge lamp (incandescent light) and was considered as

the first artificial electric light source. Some devices and systems were shown to possess the now well-known signature of a memristive device (pinched hysteresis loop) owing to their inholding inertia [6] which occurs from the movement of mobile ions or oxygen vacancies, the formation and splitting of conductive filaments and phase-change transition of some materials for data storage, e.g., sputtered $Ge_2Sb_2Te_5$ films [7,8]. This inertia causes latency in the system mechanism, resulting in the exhibition of its memory effects. Contemporarily, the memory effect is also seen in nano devices [9] in which the dynamics of electrons and ions depend on the previous history of the device.

Leon Chua [10] observed from symmetrical argument of the circuit elements (shown in Figure 2) that for the sake of completeness there should be a fourth passive circuit element in addition to the conventional resistor, capacitor and inductor. He theorized the existence of the memristor and its electromagnetic interpretation. However, the memristor differs from the three other passive circuit elements in the sense that it is a nonlinear element and capable of storing information. As clearly presented in [10], some theories were established supporting the existence of the fourth basic circuit element, its electromagnetic interpretation and some promising applications. Few years later, Chua and Kang [11] elaborated a broader class of nonlinear systems called the memristive systems, as discussed in Section 3.

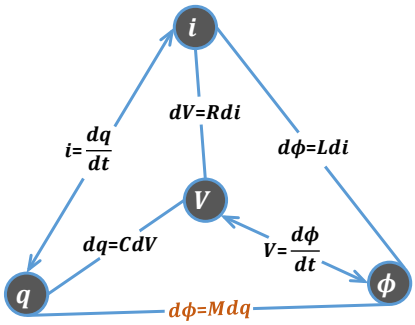

Figure 2. Symmetrical argument of the memristor as the fourth basic passive circuit element.

Although the principle theories of memristor exist [10], its realization remained a mystery for nearly four decades. Then in 2008 [12], a team of researchers from the Hewlett Packard (HP) laboratory led by Stanley Williams published a paper in *Nature Journal* announcing their successful realization of a two-terminal solid-state device bearing the characteristics of the memristor described by L. Chua in 1971 [10]. This discovery, which is described as accidental while working on nano crossbar grid [3], paved the way for more awareness that continued to attract the global attention of many researchers, engineers and scientists, therefore exploring more possible features of the memristor in terms of applications and technologies. Some memristor technologies include the Redox reaction, Ferro-electricity, Organic chemistry, etc., and will be discussed in Section 4. The conventional resistance to the flow of charges through a conducting material or wire is often analogously described to flowing water through a pipe of uniform cross-sectional area. The analogy of memristance with respect to the flowing charge is seen in flowing water through a pipe having a variable diameter [13,14]. The volume of water flowing through the pipe increases with increasing of the pipe's diameter, hence the water encounters a lower resistance path, while it decreases with decreasing of the pipe's diameter, hence encountering a higher resistance path.

The memristor is seen as the most promising element, not only capable of replacing transistors for some applications, but also to revolutionize electronic industries virtually in every facet of electronic systems, design and applications [3]. Hence, memristor becomes a suitable component for nanotechnology. The most common properties that make memristor a good candidate for future technologies are: Nano-scalability, Memory capabilities, Conductance modulation and Nonlinearities whose contemporary demand is at its peak. For example, transistors suffer nano-scalability limitations due to their finite dimensions while

it would be required that they can be of infinitesimal dimensions. Therefore, they cannot effectively undergo any further reduction in size as they are presently a few nano-meters [15]. As stated by Gordon Moore, co-founder of Intel corporation, "The number of transistors incorporated in a chip should approximately double every 24 months"and hence is called Moore's Law. This law holds only if the sizes of chips associated with circuitries keep reducing, otherwise the law will cease to be true. Transistors are tiny electrical switches, forming the fundamental unit that drives all electronic gadgets. As the transistors become smaller, they also become faster and require less electricity to operate. Clearly, there will be a limit when transistors cannot undergo any further reduction in size, which seems to be different with memristor nano-scalability.

However, the memristor discovery in [12] is still under criticism as some researchers are not convinced about the memristor [16,17]. The researchers in [18], tried to prove that the real memristor stated in [10] is not identifiable and even an impossibility. Intuitively, the three known basic passive circuit elements (resistor R, inductor L and capacitor C) are unquestionably independent of one another and they are in existence naturally, hence referred to as the fundamental circuit elements. However, on the other hand, the claim for memristor as the fourth fundamental circuit element is challenging owing to its one-to-one resistor dependencies [19]. Namely, it bears the exact same unit of measurement as the ohm Ω and a deductive-like expression, as:

$$M = \frac{V}{i} = \frac{\frac{d\phi}{dt}}{\frac{dq}{dt}} = \frac{d\phi}{dq} = M(q)\,, \tag{1}$$

it very much resembles a resistor, hence memristor is the portmanteau of memory resistor. Here $M(q)$ is the memristance and it is expressed in ohms (Ω) as is a resistor.

Notwithstanding, the fact that a memristor cannot be realized by any simple combination of the three basic circuit elements (R, L and C) proves that the memristor is actually a fundamental circuit element [3]. Although its position as the fourth fundamental passive circuit element is challenging [18,19], the memristor bears a massive technological impact and it appears to be a good candidate for numerous designs and applications. Moreover, since its inception in 2008, thousands of publications were published on memristor technologies and applications (too many to be cited) and in doing so, they affirmed memristor as the fourth basic circuit element. The number of memristor publications grows exponentially, hence outweighing the few criticisms.

This study is organized as follows. Section 2 presents briefly the three known basic passive circuit elements and is then followed by the memristor argumentation as the fourth basic passive circuit element and its description by mode of excitation. Section 3 presents memristor insights and its strong philosophical criticism, especially when it is referred to as the fourth basic passive circuit element. Section 4 introduces the memristor technologies and a thorough description and analysis of TiO_2 memristor. Section 5 presents analog and SPICE models of the memristor useful for demonstrations and simulation of memristor-based applications. Section 6 presents the modeling of memristor as a function of the flowing charge through it. Section 7 presents some interesting application areas of the memristor. Finally, the results and the contents of this paper are discussed in Section 8.

2. The Basic Passive Circuit Elements and Memristor Argumentation

This section presents briefly the three familiar fundamental passive circuit elements, namely resistor R, inductor L and capacitor C and is then followed by the memristor argumentation as the fourth fundamental passive circuit element. The voltage V and current i sources are the basic active circuit elements in the form of dependent or independent sources. We first recognize the relationship between electric voltage V and magnetic flux ϕ, as typically known from Faraday's law, as:

$$V(t) = \frac{d\phi(t)}{dt} \text{ or equivalently : } \phi(t) = \int_{-\infty}^{t} V(\tau)d(\tau)\,, \tag{2}$$

that is,

$$\phi(t) = \int_0^t V(\tau)d(\tau) + \phi_0 \,,$$

where $\phi_0 = \int_{-\infty}^{0} V(\tau)d\tau$, is the initial flux at time $t = 0$ and may be zero or nonzero. Similarly, the relationship between electric current i and electric charge q is conventionally known as;

$$i(t) = \frac{dq(t)}{dt} \text{ or equivalently : } q(t) = \int_{-\infty}^{t} i(\tau)d(\tau) \tag{3}$$

$\Rightarrow$

$$q(t) = \int_0^t i(\tau)d(\tau) + q_0 \,,$$

where $q_0 = \int_{-\infty}^{0} i(\tau)d\tau$ is the initial charge at time $t = 0$ and may be zero or nonzero. Hence, these four variables, namely voltage V, current i, magnetic flux ϕ and electric charge q are called the fundamental circuit variables. Each pair of these four circuit variables are interrelated by the basic passive circuit elements via a constitutive relationship of the form $\hat{f}(m, n) = 0$ characterizing the port equations of their circuit functionality, where n and m are any of V, i, ϕ or q circuit variables.

Figure 2 illustrates the symmetry argument of the four basic circuit elements with respect to the four circuit variables. In the case of resistor R, it can be seen that m and n are voltage and current, respectively, and is given by the constitutive relationship $dV = Rdi$. Similarly, the constitutive relationships of capacitor C and inductor L are $dq = CdV$ and $d\phi = Ldi$, respectively. However, there is a possible missing relationship between magnetic flux ϕ and electric charge q.

In 1971, Leon Chua proposed that for the sake of completeness there must be a fourth fundamental passive circuit element which gives the missing relationship between ϕ and q, thus having a constitutive relationship: $\hat{f}(\phi, q) = 0$ or equivalently as $d\phi = Mdq$, where M is the Memristor, a portmanteau of 'memory'and 'resistor'. The naming of the fourth basic passive circuit element as memristor (memory resistor) portrays that it has the property of resistance with memory. This fact arises due to the peculiar nature of memristor to remember the history (memory effect) of its previous state (resistance), even after the power is disconnected and restarted from this previous state after the power is reconnected, irrespective of the duration upon which the power is ON or OFF (i.e., it could be a day, a month or years) [3]. This special property suggests the memristor as a promising element in memory applications.

These four circuit variables in conjunction with the four passive circuit elements produced a set of six possible equations, one equation more than the previous five already known equations, due to the presence of memristor. We know details about resistors, capacitors and inductors. Therefore, in the following, these familiar passive circuit elements are introduced briefly, while the memristor is evaluated comprehensively.

2.1. Resistor

The resistor is a passive two-terminal basic electronic component discovered by Georg Simon Ohm in 1827, in which, at a constant temperature, the current flowing through these terminals is directly proportional to the voltage drop across it. Resistance is an inherent property of a material that resists the flow of electric charge (or electric current) through it, dissipating power in the process as heat. It is measured in Ohm (Ω) named after the inventor. Resistors are components designed basically to offer resistance in the circuit, commonly used as a current-limiting device. Virtually every electronic circuit is composed of at least one or more resistors, either a real component or by choosing the type of the material itself (resistivity). Currently, there are many types of resistors suitable for different applications, for example: *Fixed resistor, Rheostat or Variable resistor, Potentiometer (pre-set or post-set), Thermistor, Varistor, Thermocouple, Photo resistor or Light-Dependent Resistor (LDR),*

Voltage-Dependent Resistor (VDR), Barretter, Strain gauge, etc. Some of them are nonlinear such as: Thermistor, Varistor, Photo resistor, etc. Resistors are characterized by: the resistance, the tolerance, the maximum working voltage, the power rating, the temperature coefficient, the noise, and even an inductance effect [20].

2.2. Capacitor

The capacitor is the first passive two-terminal basic electronic component invented by Ewald Georg von Kleist in 1745. It comprises two conductive materials separated by a dielectric. The dielectric could be air or any appropriate insulation material. Condenser is almost synonymous to capacitor, condenser being for the circuit element, capacitance for the electric characteristic, and these terminologies are often used interchangeably. Capacitance characterizes the amount of charge stored in the condensator between two parallel conducting materials subject to potential difference, and is measured in Farad (F) often used with sub-multiple prefixes such as micro (μ), nano (n), pico (p), etc. As with resistors, there are many different types of capacitors used for different applications. For example: Ceramic capacitor, electrolytic, film, Tantalum, Silva Mica, variable, SMD capacitors, etc. Capacitors have been used extensively in areas such as: power conditioning, signal processing, energy storage, coupling, filters, tuning radios and resonance, sensors, output regulation of power supply, etc.

2.3. Inductor

The inductor is a passive two-terminal basic electronic component discovered by Michael Faraday in 1831. It is capable of storing energy in the form of a magnetic field due to the passage of an electric current through it. Any current-carrying conductor is associated with a magnetic field circulating around the conductor. The strength of the field or magnetic flux is directly proportional to the magnitude of the electric current flowing through it. A straight coil wire has one turn and as such, it has less inductance. Moreover, the generated magnetic field becomes more significant if the wire is coiled to a certain number of turns. However, the field is more concentrated if the coil is wound on a ferromagnetic material (or iron core format) and has a higher inductance. Additionally, due to the variation of the formed magnetic flux, a voltage (self-induced voltage source according to Faraday's law) is induced in the coil and acts in such a way to oppose itself to any change in the current that causes it (according to Lenz's law). Similarly, there are various types of inductors made in different sizes and shapes, and some are sorted by the kind of applications and the type of winding and core materials. Power inductors are larger than general purpose inductors. In addition to storage of energy, the inductor is used extensively in numerous applications, such as: transformers, induction motors, relays, radio tuning, television, filters, transmission systems, sensors and many other applications in conjunction with capacitors and resistors.

2.4. Memristor

Memristor is claimed to be the fourth basic circuit element [10] (alongside the resistor, capacitor and inductor). It is a nonlinear passive two-terminal electronic component defined by the relationship between the magnetic flux linkage ϕ and the electric charge q. The definition of a *memristor* is given by its pioneer [21], as: "*any 2-terminals device, exhibiting a pinched hysteresis loop which always passes through the origin in the voltage-current plane when driven by any periodic input current source, or voltage source, with zero DC component. If the input is a current source, it is called a current-controlled memristor. If it is a voltage source, it is called a voltage-controlled memristor* ". The name memristor is the contraction of memory resistor owing to its peculiar nature to resist the flow of electric current (as achieved by a resistor) and at the same time to remember the last amount of charge passed through it at the time when the power was disconnected, hence to memorizing the previous device resistance. Memristor keeps track of its dynamic resistance with respect to the current or electric charge flowing through it.

From the memristor symbol, see Figure 3, the unmarked side (the plus sign terminal) and the marked side (the minus sign terminal) indicate, respectively, the higher and lower potential terminal [22]. Memristor is a non-symmetrical two-port element, the polarity reversal and its effect from the application perspective was demonstrated [23]. This is very important for someone to consider before using a memristor in certain applications, e.g., biomimetic system [24].

Figure 3. Memristor symbol.

Recall that the magnetic flux ϕ represents the time-integral of voltage $V(t)$ and the electric charge q is the time-integral of electric current $i(t)$, hence these quantities are to be determined between two reference points. The fact that memristor is always defined by the integral of its input and output quantities ($V(t)$ and or $i(t)$), explains in essence why memristor remembers its previous resistance or has a memory effect. The constitutive relationship of a memristor is expressed as $d\phi = M(q)dq$, where M is the memristance that is short-form for memory resistance. Memristance is the property of a memristor to remember its previous resistance state. It is defined by the functional relationship between magnetic flux ϕ and electric charge q, and is measured in Ohms (Ω), the same measurement unit as resistance. The instantaneous memristance can be deduced from the dynamic slope of the ϕ-q locus given in the ϕ-q plane as shown in Figure 4. The relationship between the magnetic flux ϕ and the electric charge q could be expressed in two forms depending on the modes of excitation, namely: $\phi = f_M(q)$ for a charge-controlled memristor (i.e., memristor device excited by a current source) or $q = f_G(\phi)$ for a flux-controlled memristor (i.e., memristor device excited by a voltage source), where f_M and f_G are nonlinear functions denoting memristance and memductance, respectively.

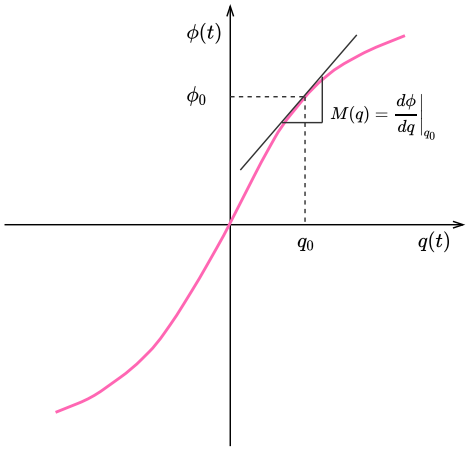

Figure 4. Memristance expression from a ϕ-q curve. Remark that, due to integration constants, this curve can be shifted horizontally and/or vertically.

The resistance of the memristor (or memristance) changes dynamically with the amount and direction of current flowing through it. People often confuse memristance with resistance. However, memristor differs from resistor in the sense that:

- It has entirely different constitutive relationship in comparison to resistor.
- Its resistance changes according to the quantity of charges having previously passed through it.
- Its resistance changes according to the direction of electric current flowing through it because it is not a bilateral device. Therefore, its connection mode matters.

- It preserves the previous history of electricity, according to the charge passed through it previously, at any given time. In other words, it has memory of the previous electricity passed through it (memory effect).
- It is nonlinear in nature.
- It has pinched hysteresis loop in the voltage–current response in a circuit, depending on its initial condition. Moreover, memristor has different circuit response according to its initial condition.
- It cannot be realized by any combination of the three known circuit elements (capacitor, resistor and inductor) and hence it can be considered as "fundamental".
- It has a unique nature for the relationship between magnetic flux and electric charge (which is not directly available by measurement).
- It behaves differently in DC and AC conditions.

Nevertheless, the memristor and resistor share some similarities, for example:

- Both offer resistance to the flow of electric current.
- Their quantities (i.e., memristance and resistance) have the same unit of measurement, i.e., Ohms, symbol: Ω.
- No phase shift in their voltage and current wave-forms, because $V(t) = M(q)i(t) \Rightarrow i(t) = 0$ if $V(t) = 0$ and vice versa.
- They both dissipate energy as heat (Joule effect). They are not loss-less devices, i.e., without preservation of energy. They are always associated with power (P) intake, i.e., $P \geq 0$.

3. The Memristor Insights and Its Philosophical Arguments

A broader class of nonlinear systems is reported [11], called memristive systems in which some nonlinear dynamic systems were found to exhibit memristive behavior. Additionally, systems whose resistance depends on its internal state (e.g., temperature) are believed to be memristive. Examples of these systems are: *Thermistor*, *Discharge tube*, *Hodgkin–Huxley (or Ionic) System* and *Tungsten filament lamps*. The memristive systems are generally described by one-port and state equations:

$$\begin{cases} y = f(x, u, t)u, \\ \dfrac{dx}{dt} = g(x, u, t), \end{cases} \tag{4}$$

where u is the input to the system, y is the output of the system, x is a vector denoting the set of internal state variables of the system, f is a nonlinear vector function and g is a nonlinear scalar function. Equation (4) affirms that memristive systems are nonlinear systems because the function f depends nonlinearly on the dynamic state variable x and both functions (f, g) depend on the input u to the system. Notice that Equation (4) describes a time-variant system, so all the variables are also functions of time. For time-invariant memristive systems, Equation (4) is rewritten as follows:

$$\begin{cases} y = f(x, u)u, \\ \dfrac{dx}{dt} = g(x, u). \end{cases} \tag{5}$$

Moreover, an ideal memristor is considered as a special case of a memristive system which can be expressed as:

$$\begin{cases} y = f(x)u, \\ \dfrac{dx}{dt} = g(u), \end{cases} \tag{6}$$

where the state variable x depends solely on the time-integral of the voltage applied across the device or the time-integral of the current flowing through it, for a flux-controlled and charge-controlled memristor, respectively.

In Figure 5, a two-terminal device under test ($D.U.T$) is subjected to a periodic input source $s(t)$, where $s(t)$ could be voltage or current source as highlighted in the aforementioned definition of memristor. If the current–voltage response of Figure 5 on the left corresponds to that of Figure 5 on the right, for any $s(t)$ source respecting the definition in [21], then the black box is called a *memristor*. More details to check whether a candidate system is indeed a memristive system are given in the following.

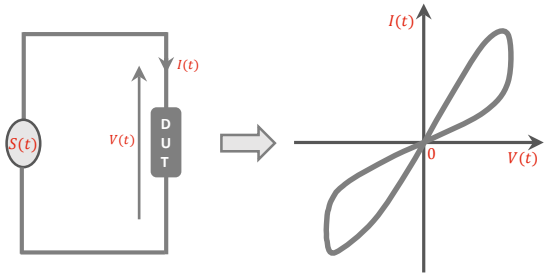

Figure 5. Testing memristor device as a black box (**left**) and current–voltage response of the black box (**right**).

3.1. Fingerprints of a Memristor

Circuit elements such as the resistor, capacitor, inductor, etc., are often characterized by their voltage–current response (V–I characteristics) in any given circuit. Memristor is not an exception, it has a peculiar voltage–current response which is a unique identifier that distinguishes it from any other known circuit element. Hence, it is called the fingerprint of a memristor and is used to characterize a memristive system. The most three well-known memristor fingerprints are enumerated in [25–27], as:

1. The V–I response of a memristor (with positive memristance) is always a pinched hysteresis loop (Lissajous figure) when subjected to a bipolar periodic input signal without offset.
2. The hysteresis lobe area decreases monotonically when the excitation frequency increases.
3. For a fixed-input amplitude, the pinched hysteresis loop shrinks to a single-valued function as the frequency of the input supply tends to infinity.

Figure 6 illustrates the mentioned three figerprints of a memristor. More fingerprints of an ideal memristor are given in [26], including constitutive relationship (CR) between flux and charge and parameter versus state map (PSM) [28]. In fact, nine fingerprints of memristor are given in [26] including the three above mentioned and they give birth to a valid test for assessing a memristor device. In the following, we give the description of a pinched hysteresis loop and pinched hysteresis lobe area.

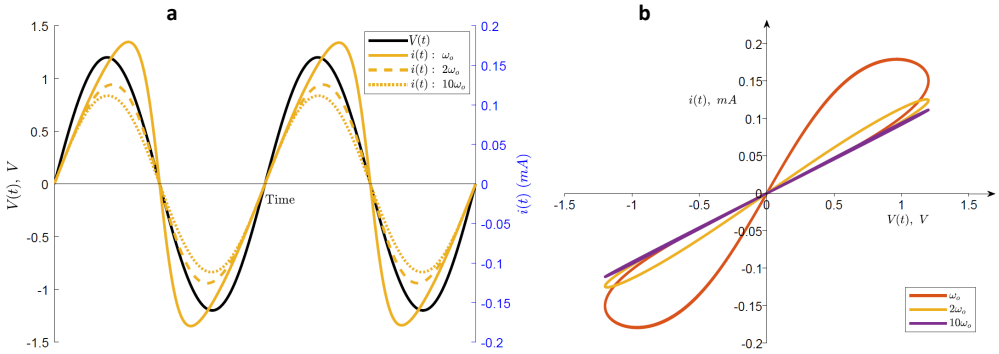

Figure 6. Demonstration of a memristor fingerprint for $f_o = 1$ Hz , $\omega_o = 2\,\pi f_o$ and $V(t) = 1.2\,sin(\omega t)$: $\omega = \omega_o$, $\omega = 2\,\omega_o$ and $\omega = 10\,\omega_o$. (**a**) voltage $V(t)$ and current $i(t)$ in a memristor, (**b**) I–V response of a memristor and effect of frequency variation.

3.1.1. Pinched Hysteresis Loop (PHL)

The voltage–current response of a memristor in a circuit is always a pinched hysteresis loop [27,29]. As seen in Figure 6a, the maxima and minima of the current $i(t)$ and voltage $V(t)$, through and across the memristor, respectively, are not reached simultaneously and this is the cause of the formation of the hysteresis lobe area. The term *pinched hysteresis loop (or PHL) refers to a double-valued Lissajous figure in the voltage–current (V–I) plane which is always pinched at the origin for any given time, for any initial condition, for any input amplitude (voltage or current) and for any input frequency* [28]. The term *pinched* also signifies that $V(t) = 0$ whenever $i(t) = 0$ and vice versa. In other words, for any given value of current $i(t)$, there will be two corresponding values of voltage $V(t)$ except at $i(t) = 0$. The converse is also true, for any given value of voltage $V(t)$, there will be two corresponding values of current $i(t)$ except at $V(t) = 0$. This can be observed from Figure 6a: it shows that current ($i(t)$ in orange) is zero whenever the voltage ($V(t)$ in black) is zero and as a result the hysteresis loop always passes through the origin, see Figure 6b.

It turns out that memristive systems exhibit two different kinds of PHL [25,26] depending upon the system's constituents (i.e., f and g as defined in Equation (4) and the type of excitation (odd-type or even-type) [26]. The two types of PHL are Self-crossing PHL (also known as Transversal or crossing PHL) and Tangential PHL (also known as non-tranversal or non-crossing PHL).

i. **Self-crossing or transversal pinched hysteresis loop (SPHL):** In this type of PHL, the locus cuts across at the origin (or pinched point). Additionally, one can see that the slope of the locus moving toward the origin is different from that of the locus leaving the origin. Figure 7a shows a typical transversal PHL. An example of memristive system with transversal pinched hysteresis loop is the mathematical model of HP memristor (presented in Section 4).

ii. **Tangential or non-transversal pinched hysteresis loop (TPHL):** As the name implies, the locus does not cut across, rather it passes tangentially as confirmed by the arrow directions, see Figure 7b. Notice that it is still pinched at the origin, i.e., $V(t) = 0$ whenever $i(t) = 0$ and vice versa, however, there is always a fixed slope (for both the two slopes, i.e., R_{off} and R_{on}) when the locus moves toward the origin and immediately after leaving the origin. This observation is clear because the separate line slopes coincide together before reaching the origin and remain together even after leaving the origin until a certain amount of voltage or current is reached, then the loci separate and hence the hysteresis lobe area becomes visible, see Figure 7b.

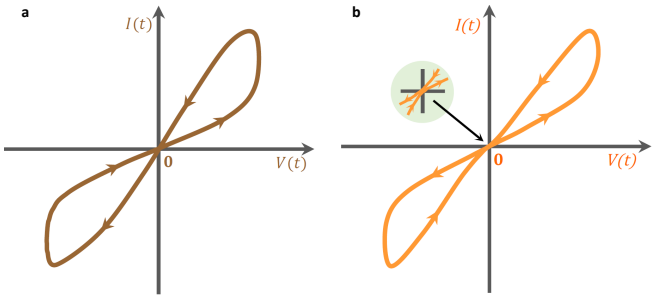

Figure 7. The two types of pinched hysteresis loop (PHL). (**a**) Self-crossing or transversal PHL (e.g., the ones observed in HP and KNOWM memristors) and (**b**) Tangential or non-transversal PHL (e.g., the ones observed in plant and light sources).

There are many memristive systems whose current–voltage response is a tangential PHL, some of these systems being mentioned in [11,25,30]. Moreover, tangential PHL is met in the memristive behavior of plants (Aloe vera and Mimosa pudica) [31]. However, it is reported that the pinched hysteresis loop of an ideal memristor, memcapacitor and meminductor is always a self-crossing PHL [32]. It is even emphasized that self-crossing PHL is another signature or fingerprint of an ideal memristor. Moreover, TiO_2 memristor

(from HP lab [12]) and SDC memristor (from KNOWM [33]) are examples of a memristor with a self-crossing PHL.

3.1.2. Pinched Hysteresis Lobe Area

The hysteresis lobe area decreases when the input frequency increases. Recall that the memristor is a nano device, therefore, a small input signal is enough to generate a large electric field to trigger the device according to: $E = -\frac{dV}{dx}$, when x is the internal state and corresponds to the displacement of charge carriers. Therefore, any small increment in the potential difference V leads to a large magnitude of electric field **E** to be generated. However, the resistance of the memristor depends on its internal state, hence any change in the input signal results in a behavioral change of its internal state as well. Therefore, for example considering an input current $i(t)$ such that:

$$i(t) = I_0 sin(\omega t), \tag{7}$$

the flowing charge is:

$$\begin{aligned} q(t) &= \int_{-\infty}^{t} I_0 sin(\omega\tau) d\tau, \\ &= Q[1 - cos(\omega t)] + q_0 \,, \end{aligned} \tag{8}$$

where $q_0 = \int_{-\infty}^{0} I_0 sin(\omega\tau) d\tau$ is the initial charge just before the current starts to flow and $Q = \frac{I_0}{\omega}$ is the charge delivered by the current source during the first quarter of the period $T = \frac{2\pi}{\omega}$ and the magnitude peak-to-peak of the flowed charge is given by:

$$\frac{2I_0}{\omega} = 2Q. \tag{9}$$

For an ideal charged-controlled memristor, its state variable is rather the charge flowing through the device. It is obvious from Equation (9) that increasing the frequency ω for a fixed amplitude I_0, leads $q(t)$ peak-to-peak amplitude to decrease significantly and hence causes the shrinkage of the pinched hysteresis loop towards a linear graph.

Figure 8a shows the effect of increasing input frequency on the PHL lobe area of the memristor. The input frequency ω is considered in three steps ω_1, ω_2 and ω_3 with the corresponding lobe areas A_1, A_2 and A_3, respectively, such that:

$$\omega_1 < \omega_2 < \omega_3$$

and

$$A_1(\omega_1) > A_2(\omega_2) > A_3(\omega_3)$$

It follows that: as $\omega \to \infty$, $A \to 0$, this behavior is shown in Figure 8b.

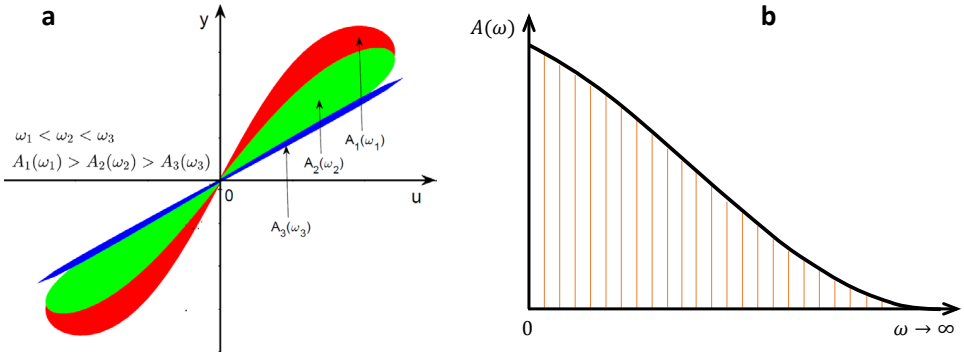

Figure 8. Effect of increasing frequency on the PHL lobe area. (**a**) Hysteresis lobe area shrinkage due to the increase in the input frequency and (**b**) PHL lobe area versus frequency.

The pinched hysteresis lobe area can be calculated. Let us consider a memristor excited by a current source given by $i(t) = I_0 sin(\omega t)$ with $\omega = \frac{2\pi}{T}$, T being the period. By considering a half cycle (i.e., $\frac{T}{2}$) of the input $i(t)$, the hysteresis loop is given in Figure 9, having an enclosed area A and surface boundary S, altogether enclosed in a triangle OCD [34–36].

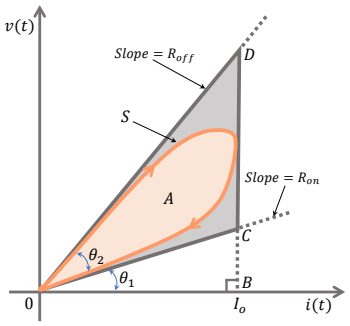

Figure 9. Calculating the area of PHL.

The area A is obtained from the surface integral of the voltage with respect to the current, as:

$$A = \oint_S vs.di. \tag{10}$$

Figure 10 shows the operating point of a memristor in the plane (q, ϕ) starting with an initial charge q_0, corresponding to an initial flux ϕ_0, with the so-called shifted flux $\phi' = \phi - \phi_0$. Let us use a shifted charge $q' = q - q_0$, then:

$$q' = Q[1 - cos(\omega t)]. \tag{11}$$

From Equations (9) and (11), the operating point is within the interval $[q_0, q_0 + 2Q]$, hence the normalized form of the constitutive relationship becomes:

$$\hat{f}(\phi', q') = 0. \tag{12}$$

The corresponding normalized expression of the memristance-versus-state map, becomes:

$$M'(q') = M(q' + q_0) = \frac{d\phi'(q')}{dq'}.$$

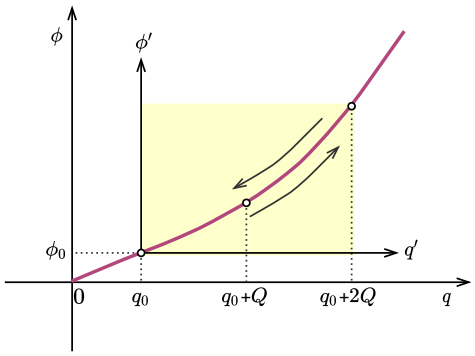

Figure 10. Memristor operating point from the constitutive relationship.

From Equations (7) and (8), the algebraic relation between the charge q' and the current source $i(t)$ is:

$$i^2 = \omega^2(2Q - q')q'. \tag{13}$$

From Equation (10), with $v(t) = M'(q'(t))i(t)$, the area during the first half-cycle can be expressed as:

$$A = \frac{1}{2}\int_0^{\frac{T}{2}} M'(q'(t))\frac{d(i^2)}{dt}dt.$$

The integration by parts gives:

$$A = \frac{1}{2}\Big[M'(q'(t))i^2(t)\Big]_0^{\frac{T}{2}} - \frac{1}{2}\int_0^{\frac{T}{2}} \dot{M}'(q'(t))i^2(t)\,dt, \tag{14}$$

where the dot in M' represents the derivative with respect to time. In [34], the authors consider that the memristance function $M'(q')$ can exhibit step discontinuity points q'_j in the charge interval $[0, 2Q]$, with $j = 1, 2, \cdots, n$, hence, they considered some step changes of the memristance at point q'_j. However, the following excludes the case of any discontinuities for $M'(q')$. In this simplified case, the first term of Equation (14) is zero. Noting that $\frac{dM'}{dt} = \frac{dM'}{dq'}\cdot\frac{dq'}{dt} = \frac{dM'}{dq'}\cdot i(t)$, Equation (14) gives then:

$$A = -\frac{1}{2}\left(\int_0^{\frac{T}{2}} \frac{dM'}{dq'}i^3 dt\right). \tag{15}$$

For example, the pinched hysteresis lobe area of the memristance expression is given in [34] and is described in the following. The given memristance function is rewritten as:

$$M'(q') = R_i - \delta R\frac{q'}{q_d}, \tag{16}$$

where $\delta R = R_{off} - R_{on}$, $R_i = R_{off} - \delta R\frac{q_0}{q_d}$ is the initial memristance at time $t = 0$ and q_d is the charge necessary for the modification of the memristance by the value δR [34]. Since R_i is constant, then $\frac{dM'}{dq'} = -\frac{\delta R}{q_d}$. Using the current source (7), then:

$$A = \frac{1}{2}\frac{\delta R}{q_d}I_0^3\int_0^{\frac{T}{2}} sin^3(\omega t)dt.$$

Using the identity: $sin^3(\alpha) = \frac{3}{4}sin(\alpha) - \frac{1}{4}sin(3\alpha)$, then $\int_0^{\frac{T}{2}} sin^3(\omega t)dt = \frac{4}{3\omega}$ and the area is finally expressed as:

$$A = \frac{2}{3}\frac{\delta R}{\omega}\frac{I_o^3}{q_d}. \tag{17}$$

The area is independent of the initial memristance, however, it is directly proportional to the cubic power of the exciting current and inversely proportional to the input frequency. Note that Equation (17) is determined according to the mathematical model of HP memristor, thus q_d is the charge required to move the tunneling dopant barrier between the doped and undoped region from $x \to 0$ toward $x \to 1$ (see Section 4 for more details).

Moreover, a generalized formulation for computating the hysteresis lobe area of *mem-elements* is reported in [35], taking into account whether the input is a voltage or current. Thus, for a mem-element having input $u(t)$, output $y(t)$, state variable $x(t)$ and a differentiable function $h(x)$, this mem-element can be characterized by:

$$\begin{cases} y(t) = h(x)u(t), \\ \dfrac{dx(t)}{dt} = u(t), \end{cases} \tag{18}$$

where:

$$u(t) = U_{max}sin(\omega t).$$

Thus, the loop area during the first half-cycle is given by:

$$A = -\frac{1}{2}\int_0^{\frac{T}{2}} \frac{dh(x)}{dx}u^3 dt. \tag{19}$$

3.2. Memristor by Mode of Excitation

Depending on the type of excitation, memristor can be characterized as charge-controlled memristor (CCM) or flux-controlled memristor (FCM), see Figure 11.

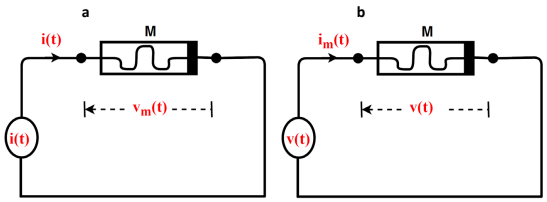

Figure 11. Memristor subjected to current and voltage excitation, respectively. (**a**) Charge-controlled memristor, (**b**) Flux-controlled memristor.

3.2.1. Charge-Controlled Memristor (CCM)

For a charge-controlled memristor, the input applied to the memristor is a current source. The set-up is given in Figure 11a, whereby a current source $i(t)$ is connected to a memristor M. Thus, the current flowing through the memristor will cause a voltage drop $V_m(t)$ across it. From Equation (4), the three variables u, x and y become i, q and v, respectively, q being the time domain integral of the input current i and v the output voltage of the memristor. Hence, the constitutive relation of charge-controlled memristor should always represent the flux (ϕ) dependence on the charge (q), as:

$$\phi = \hat{\phi}(q). \tag{20}$$

Substituting the variables i, q and V into Equation (6), then:

$$\begin{cases} V = M(q)i, \\ \dfrac{dq}{dt} = i. \end{cases} \tag{21}$$

Note that the notation $\hat{\phi}$ in Equation (20) stands for a function definition: it could be any letter, for example f, such that: $\phi = f(q)$, so the ($\hat{}$) will often be removed in the following. Furthermore, notice that Equations (20) and (21) are identical, with $M(q)$ a charge-controlled memristance whose expression can be obtained by differentiating both sides of Equation (20) with respect to t: $\dfrac{d\phi}{dt} = \dfrac{d}{dt}(\hat{\phi}(q))$. As the right hand side is a composite function, it can be seen that:

$$\frac{d\phi}{dt} = \frac{d\phi(q)}{dq} \times \frac{dq}{dt} \Rightarrow \frac{d\phi}{dt} = M(q)\,\frac{dq}{dt} = M(q)i. \tag{22}$$

Therefore, $M(q) = \dfrac{d\phi(q)}{dq} = \dfrac{d\phi}{dq}$. This equation can be rewritten conveniently as:

$$\mathrm{d}\phi = M(q)\,\mathrm{d}q. \tag{23}$$

Moreover, (22) also gives the voltage drop $V_m(t)$ (see Figure 11a) across the charge-controlled memristor $M(q)$: $\dfrac{\mathrm{d}\phi}{\mathrm{d}t} = M(q)\,\dfrac{\mathrm{d}q}{\mathrm{d}t}$, such that:

$$V_m(t) = M(q)\,i(t). \tag{24}$$

Example 1. *Suppose a charge-controlled memristor is characterized by the cubic function as follows:*

$$\phi(t) = \beta q(t) + \frac{\alpha}{3}\,q(t)^3, \tag{25}$$

where the α and β are in $Wb.C^{-3}$ and $Wb.C^{-1}$, respectively, (Wb and C mean Weber and Coulomb, respectively). Equation (25) is a modified version of the one used by Chua [28], by adding parametric coefficients α and β in order for the equation to be homogeneous. It implies that:

$$M(q) = \frac{d\phi}{dq} = \beta + \alpha\,q(t)^2. \tag{26}$$

Let the input current $i(t)$ be: $i(t) = I_o sin(\omega t)$, then the charge is computed as follows:

$$\begin{aligned} q(t) &= \int_{-\infty}^{t} i(\tau)d\tau \\ &= q_0 + \frac{I_o}{\omega}(1 - cos(\omega t)). \end{aligned} \tag{27}$$

Knowing q_0 and $q(t)$, then $M(q)$ and $V_m(t)$ can be calculated from Equations (24) and (26), respectively. Hence, q_0 is the memristor initial charge that determines its previous state. Figure 12 shows some examples for $I_o = 1\ A$, $f = 4\ Hz$, $\alpha = 1\ Wb.C^{-3}$, $\beta = 1\ mWb.C^{-1}$ and two different values of q_0 as 0 C and 0.05 C, respectively, shown by Figure 12a,b.

It is expected that taking different values for q_0, the operating point in Figure 12(a1) will be changed, as will the hysteresis curve of Figure 12(a3), compare Figure 12a,b.

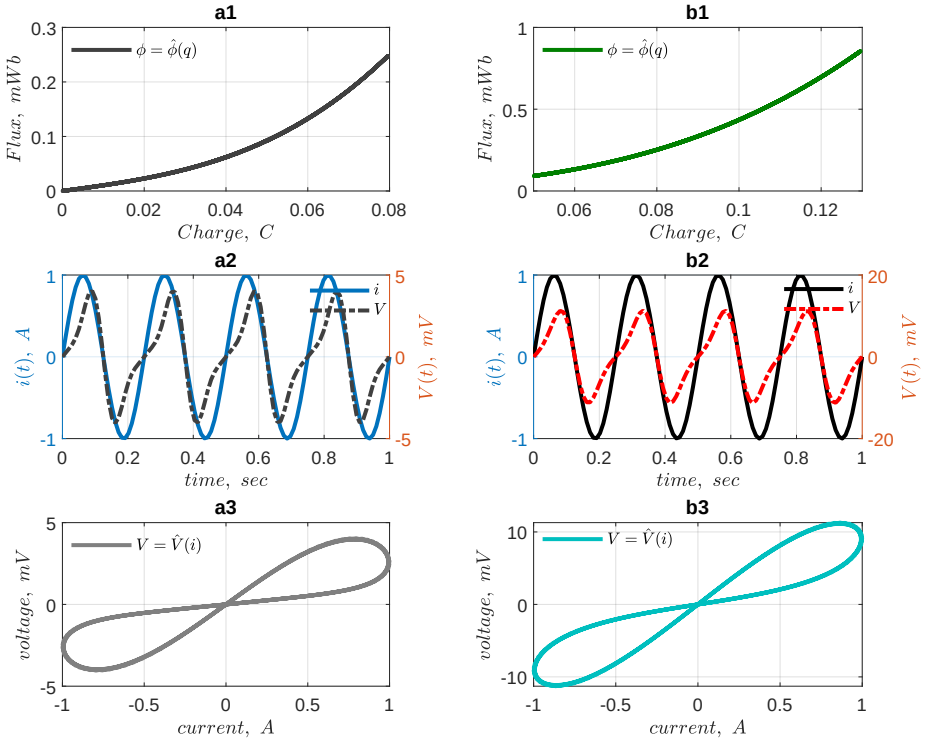

Figure 12. Results of Example 1: $I_o = 1$ A, $f = 4$ Hz, $\alpha = 1$ Wb.C^{-3} and $\beta = 1$ m Wb.C^{-1}. (**a1**–**a3**) $q_0 = 0$ C: (**a1**) ϕ-q curve, (**a2**) $i(t)$ and $v(t)$ waveform and (**a3**) I-V characteristic. (**b1**–**b3**) $q_0 = 0.05$ C: (**b1**) ϕ-q curve, (**b2**) $i(t)$ and $v(t)$ waveform and (**b3**) I–V characteristic.

3.2.2. Flux-Controlled Memristor (FCM)

Memristor is flux-controlled if the input applied to the memristor is a voltage source (see Figure 11b). The applied voltage $V(t)$ causes current $i_m(t)$ to flow through the memristor M. One can see that the triad variables u, x and y in (6) become V, ϕ and i, respectively. Hence, the output of a flux-controlled memristor is current and its constitutive relationship represents the charge dependence on flux. The constitutive relationship of the memristor of this type is given in (28). The state variable is controlled by the flux as the result of time-domain integral of the applied input voltage.

$$q = \hat{q}(\phi). \tag{28}$$

Similarly, substituting the variables V, ϕ and i into (4), it gives:

$$\begin{cases} i = Y(\phi)V, \\ \dfrac{d\phi}{dt} = V, \end{cases} \tag{29}$$

where $Y(\phi)$ is the flux-controlled memductance, measured in Siemens S, the same S.I unit as conductance. Note that $Y(\phi)$ is the inverse of $M(q)$. Thus, ϕ is the time-domain integral of V:

$$\begin{aligned} \phi &= \int_{-\infty}^{t} V(\tau)\, d\tau, \\ &= \phi_0 + \int_{0}^{t} V(\tau)\, d\tau. \end{aligned}$$

Similarly, the expression of $Y(\phi)$ can be deduced by differentiating both sides of Equation (28) with respect to time. Therefore, $\frac{dq}{dt} = \frac{d}{dt}(q(\phi))$, that is:

$$\frac{dq}{dt} = Y(\phi)\,\frac{d\phi}{dt}, \tag{30}$$

with $Y(\phi) = \frac{dq(\phi)}{d\phi} = \frac{dq}{d\phi} \;\Rightarrow$

$$dq = Y(\phi)\,d\phi. \tag{31}$$

The current through the memristor $i_m(t)$ can be expressed from Equation (30), and is finally given by:

$$i_m(t) = Y(\phi)\,V(t). \tag{32}$$

Example 2. *Suppose a flux-controlled memristor described by:*

$$q = \frac{\psi_1}{3}\phi^3 + \psi_2\phi, \tag{33}$$

ψ_1 and ψ_2 are appropriate constants in C.Wb^{-3} and C.Wb^{-1}, respectively. Given a source voltage: $V(t) = V_0 sin(\omega t)$, the equivalent expression of the flux is obtained to be: $\phi = \frac{V_0}{\omega}(1 - cos(\omega t)) + \phi_0$. Using (31), then:

$$Y(\phi) = \psi_1\phi^2 + \psi_2. \tag{34}$$

Hence, knowing $Y(\phi)$, then $i(t)$ is calculated and some examples are given in Figure 13a,b, respectively, for $\phi_0 = 0$ Wb and $\phi_0 = 0.08$ Wb. Similar to Figure 12, here the initial conditions also affect the ϕ-q operating point and hence the I–V curve.

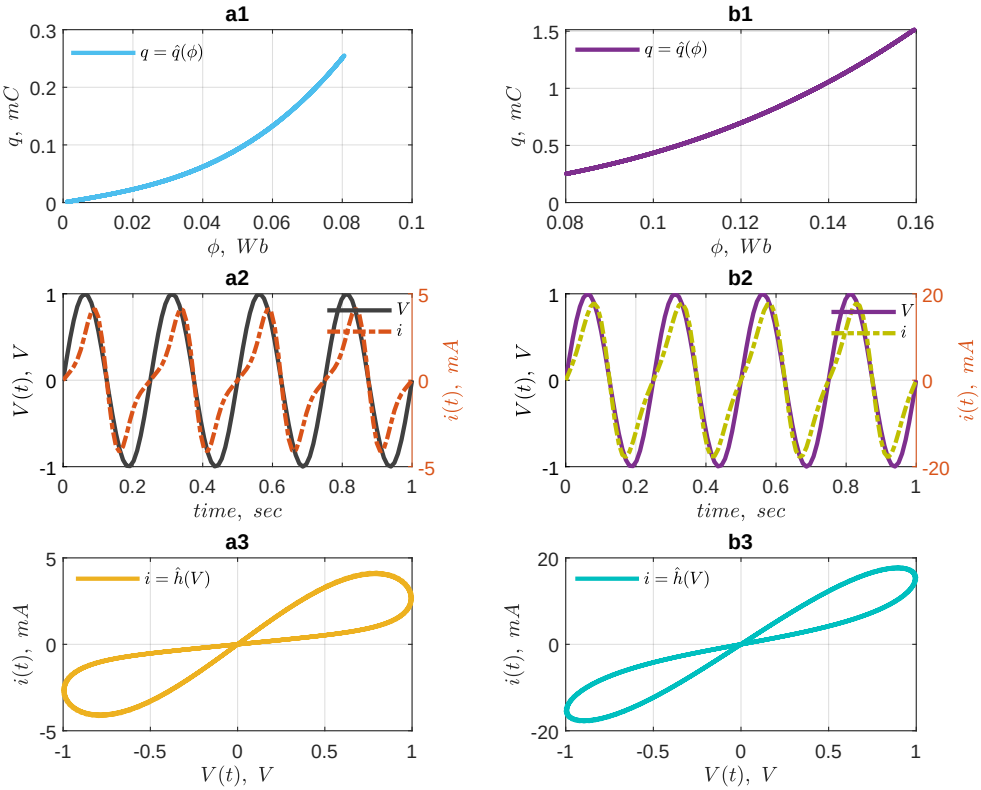

Figure 13. Result obtained for Example 2: $V_0 = 1$ V, $f = 4$ Hz, $\psi_1 = 1$ C.Wb^{-3} and $\psi_2 = 1$ mC.Wb^{-1}. (**a1–a3**) $\phi_0 = 0$ Wb: (**a1**) ϕ-q curve, (**a2**) $i(t)$ and $v(t)$ waveform and (**a3**) I–V characteristic. (**b1–b3**) $\phi_0 = 0.08$ Wb: (**b1**) ϕ-q curve, (**b2**) $i(t)$ and $v(t)$ waveform and (**b3**) I–V characteristic.

3.3. Memory Elements (Mem-Elements)

The emergence of the memristor led to the discovery of two other memory elements [9], namely: *Memcapacitor* and *Meminductor* [37–39]. The memristor M_R is not a loss-less device while the memcapacitor M_C and meminductor M_L are loss-less devices. Their names are derived accordingly from the conventional three circuit elements (resistor, capacitor and inductor, respectively) due to some common features, for example, each having the same unit of measurement as Ohm, Farad and Henry, respectively.

This poses the question of whether the memristor is indeed the fourth circuit element due to its resistance dependency and the appearance of memcapacitor and meminductor. Instead of four circuit elements, why not six altogether? However, the memristor, memcapacitor and meminductor are classified as memory circuit elements or simply mem-elements owing to the ability to remember their previous history, which is a manifestation of their memory effects [40–44].

Due to the relation $i = C\frac{dV}{dt}$ for capacitor and $V = L\frac{di}{dt}$ for inductor, the memory for these elements is already present by the occurrence of the time derivative (of voltage V for capacitor and of current i for inductor). This is not the case for $V = R.i$ through a resistor, and this is the heart of all interests for the new element: the memristor. Notwithstanding, circuit elements can be classified into linear and nonlinear elements. Hence, resistor, capacitor and inductor are rather linear elements, whereas memristor, memcapacitor and meminductor are nonlinear elements.

3.4. Not Every Nonlinear Dynamical System Is an Ideal Memristor

Memristive systems are a class of nonlinear dynamical systems whose current–voltage response resembles the fingerprint of an ideal memristor. However, it is known that not every nonlinear dynamical system is ideally a memristor, even though it exhibits a pinched hysteresis loop in its current–voltage characteristic. Hence, the above outlined criteria of memristor identification are not enough to distinguish a memristor device from some nonlinear dynamical systems that are not associated with a memristor. As recalled earlier, the pinched hysteresis loop is the major criterion used to authenticate a given system as memristor or not [25]. In fact, it states that some memory elements may not exhibit pinched hysteresis loop, and an example of a memcapacitor is even given in [45]. There are concerns in the scientific community regarding what a memristor is and is not [16–19], and further elaborations by Blaise Mouttet and Pershin et al. [46–50] are explained in the following.

Leon Chua generalized the concept of memristor to include all resistance switching memories [28]. However, it is shown experimentally that resistance switching memories are not memristors [46]. Blaise Mouttet reported that L. Chua contradicted himself in [28], against their axiomatic definition of a memristor in 1971 [10]. He further concluded that the HP's memristor lacks scientific merit [17].

It is further clarified that the pinched hysteresis loop as the fingerprint of a memristor, or a memristive device, must hold for all amplitudes, for all frequencies, and for all initial conditions, of any periodic testing waveform, such as sinusoidal or triangular signals, which assume both positive and negative values over each period of the waveform [29]. However, still some dynamical systems fulfilling these conditions are yet not memristor [47,48]. Notwithstanding, a simple testing technique to identify an ideal memristor is reported in [50], which could, together with the concept of pinched hysteresis loop, help to identify a memristor from a non-memristor. However, there is no memristor reported in the literature, adhering to the axiomatic definition that relates charge and flux. Therefore, we may conclude that all the reported memristors are resistive switching devices and they are a special class of memristive systems, hence not an ideal memristor. The fact that an ideal memristor is not yet found and/or simply does not exist, does not discredit the hitherto findings regarding the memristor, as they are still valuable in resistive random access memory (ReRAM) and many other applications, and justify all efforts to better understand this new element.

An ideal memristor is described axiomatically by the constitutive relationship between the charge and the flux, but there is not yet a memristor discovery based on this principle. Contemporarily, all the memristor technologies are based on bipolar resistance-switching mechanisms. This is the main reason used by some scientists to criticize the memristor discovery. In fact, when one considers the existence of an ideal memristor, a possible conclusion is that such a device is likely to be impossible. Optimistically, we believe that one-day such a device will be discovered. However, for the moment, all the memristors are resistance-switching devices with potential applications. Moreover, because they possess the signatures of an ideal memristor, they can be categorized as a special class of memristive system.

4. Memristor Technologies and Models

All memristor technologies follow similar principles of operation—called ***bipolar resistance switching***, which means resistance switching between two limits, namely: R_{on} and R_{off} accomplished by the evolution of the applied signal. R_{on} is the lower resistance limit (higher conducting state) while R_{off} is the higher resistance limit (lower conducting state). Although the principle of operation is the same, each technology differs from one another in terms of resistance-switching mechanism (see Figure 14).

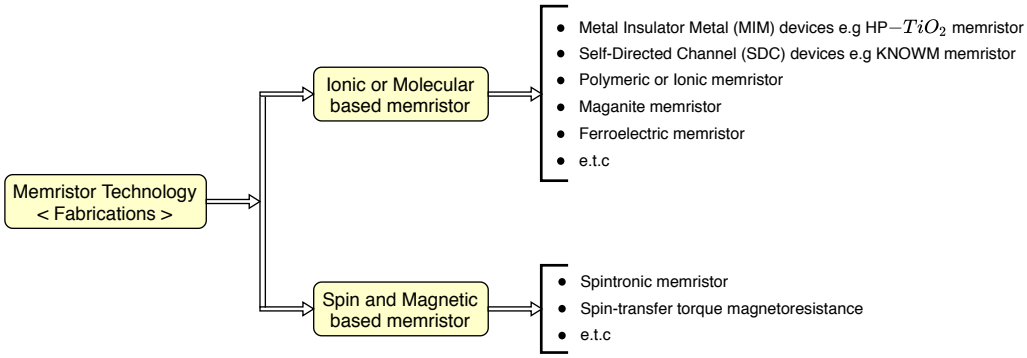

Figure 14. Some memristor fabrications technologies.

The HP memristor also known as TiO_2 memristor uses the principle of a Metal-Insulator-Metal (MIM) device in which a bilayer of titanium oxide (TiO_2) is placed between two platinum metal electrodes, as illustrated in Figure 15b [12]. One layer of the TiO_2 bilayer is doped with positive oxygen vacancies which allow for high conduction and the other layer is pure TiO_2. Therefore, the formation exhibits two limiting resistance states (R_{off} and R_{on}) due to the contraction and the expansion of the doped region. Following the discovery of TiO_2 memristor [12], many memristor technologies are reported using different switching mechanisms. Figure 14 shows the taxonomy of memristor technologies. The memristor technologies are based on ionic or magnetic effects.

For example, the self-directed channel (SDC) device (the KNOWM memristor) uses electropositive metal (e.g., Silver, Ag) for conduction and the resistance-switching transition is due to the formation and dissolution of a high conducting channel filament [13,33]. This is the only memristor chip available yet for purchase, see Figure 16. This is the chip used in the experimental demonstrations in Appendix A.

Other memristor technologies include the following. The ferroelectric memristor is based on a ferroelectric tunnel junction where the tunneling conductance allows for bistable resistance-switching transition and can be tuned according to the duration and amplitude of the applied voltage [51–53]. The memristive behavior was demonstrated experimentally and is attributed to the field-induced charge redistribution at the ferroelectric/electrode interface, which causes the modulation of the interface barrier height. Other memristors named according to fabricating materials, such as, the polymeric (or organic) [54,55], spintronic memristor [56,57], amorphous silicon memristor technology[58] and amorphous

oxide semiconductor zinc–tin-oxide (ZTO) memristor [59]. In the following the TiO_2 memristor is considered due to its simpler modeling equations.

4.1. HP (TiO_2) Memristor: Modeling, Analysis and Interpretation

The TiO_2 memristor is the first discovered two-terminal solid-state memristor observed from a nano crossbar array of wires (see Figure 15a) in which each junction formed a memristor [3,60]. It was demonstrated that the memristor in the crossbar can act as a storage element to give binary output for color images or as a switch to produce different grayscale levels, allowing the processing of images [61]. Figure 15b shows the schematic of TiO_2 memristor [12]. It is made up of a thin film bilayer of Titanium-Oxide TiO_2 of thickness D sandwiched between two platinum (Pt) contacts which serve as electrodes. One portion of TiO_2 is initially doped with oxygen vacancies, and hence becomes TiO_{2-e} and the other portion remains pure TiO_2. These oxygen vacancies allow the layer to become an N-type semiconductor with electrons as charge carriers and thus adopt conductivity, the other undoped side has resistive properties, such that the entire arrangement behaves as a semiconductor material. Notice that in reality the dopants are scattered along the device width, however, its concentration in one edge is negligible compared to that of the other edge, creating two different resistive regions.

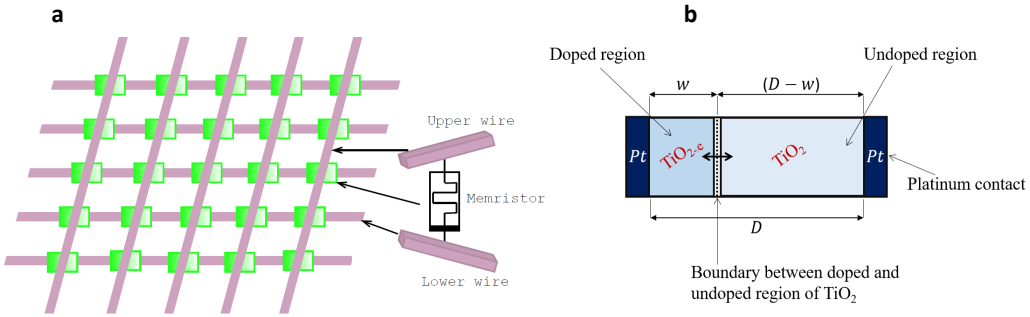

Figure 15. Geometry of HP (TiO_2) memristor. (**a**) Crossbar array of wires with memristor in each junction. (**b**) Structural view of the TiO_2 memristor, i.e., enlargement of the memristor in the junction.

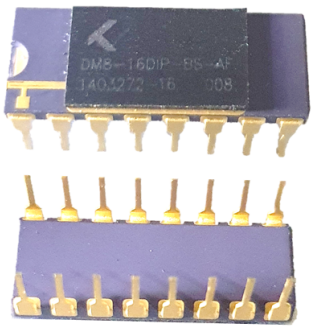

Figure 16. KNOWM memristor chip. The chip contains eight memristors.

The structural arrangement constitutes two resistances R'_{on} and R'_{off} connected in series, as illustrated in Figure 17. R'_{on} resistance corresponds to the doped region (TiO_{2-e}, i.e., higher conducting region) of width (w) while R'_{off} resistance corresponds to the undoped region (TiO_2, i.e., lower conducting region) whose width is $(D - w)$. Note that when $w \to D$, $R'_{on} \to R_{on}$ and if $w \to 0$, $R'_{off} \to R_{off}$. The boundary between doped and undoped regions (shown with two headed arrows) moves back and forth depending upon the direction of the flowing current or the polarity of the applied voltage. If the boundary moves leftward, w decreases and the opposite width $(D - w)$ increases, leading hence to higher resistance. Conversely, if the boundary moves rightward, w increases while $(D - w)$ decreases, leading hence to lower resistance. This further confirms the bipolar

resistance-switching characteristics. Therefore, w acts as the state variable of the device characterizing the instantaneous memristance.

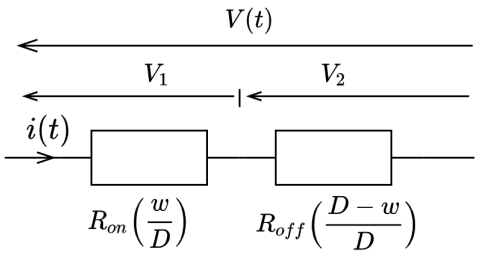

Figure 17. Memristor internal behavioral response. $R'_{on} = R_{on}\frac{w(t)}{D}$, $R'_{off} = R_{off}\left(1 - \frac{w(t)}{D}\right)$, $V_1 = R'_{on}i(t)$, $V_2 = R'_{off}i(t)$ and $V = V_1 + V_2$.

Owing to oxygen vacancies, the electrons, with mass m_e and charge $q = -e$, act as the charge carriers and are accelerated with an electric field:

$$E = \frac{V(t)\ R_{on}}{R_{on}w + R_{off}(D - w)} \tag{35}$$

and eventually stopped as they collide together. Their limiting speed v_l is given by $v_l = \mu_v \vec{E} = \frac{q.E}{m_e}\langle t \rangle$, where μ_v is the mobility of the charge carriers and $\langle t \rangle$ is the average time between two consecutive collisions. The expressions of the voltages V_1 and V_2 across the doped and undoped regions can be expressed, respectively, as:

$$V_1 = \frac{V(t)\ R_{on}w}{R_{on}w + R_{off}(D - w)} \tag{36}$$

and

$$V_2 = \frac{V(t)\ R_{off}(D - w)}{R_{on}w + R_{off}(D - w)}. \tag{37}$$

Note that the electric field in the conductive region can be expressed as $E = \frac{V_1}{w} = \frac{R_{on}}{D}i(t)$. The charge carriers expand then the doped region towards the right corresponding to an increase in the width w with a positive current $i(t)$ such that:

$$\frac{dw}{dt} = \mu_v E = \mu_v \frac{R_{on}}{D} i(t), \tag{38a}$$

$$V(t) = M(w)\ i(t), \tag{38b}$$

$$M(w) = R_{on}\frac{w(t)}{D} + R_{off}\left(1 - \frac{w(t)}{D}\right), \tag{38c}$$

where: $V(t)$ is the voltage across the two-port device, $i(t)$ is the current flowing through it, $M(w)$ is the memristance. Note that $\vec{v_l} = \mu_v \vec{E} \Rightarrow \frac{v_l}{\mu_v} = \frac{1}{\mu_v}\frac{dw}{dt}$ and $v_l = \frac{dw}{dt}$ is the drift speed of the boundary. The dopant mobility (μ_v) determines how quickly the boundary between doped and undoped regions (or the dopants) can move back and forth across the device for any applied signal. The tunneling of the barrier width w is determined by the magnitude and polarity of the applied voltage or current. It can be seen from Equation (38a) that at any given time t, the width $w(t)$ of the doped region depends on the quantity of electric charge having passed through the device.

Finally, with the normalized form $x(t) = \frac{w(t)}{D}$, the modeling Equations (38) become:

$$\frac{dx}{dt} = \mu_v \frac{R_{on}}{D^2}\, i(t), \tag{39a}$$

$$V(t) = M(x)\, i(t), \tag{39b}$$

$$M(x) = R_{off} - \delta R\, x, \tag{39c}$$

where $\delta R = R_{off} - R_{on}$. $M(x) = R_{off}$ if $x(t) = 0$ and R_{on} if $x(t) = 1$. Equation (39c) shows that the HP memristor model remembers the coordinate of the state variable x instead of the charge, however, the coordinate of x is related to the quantity of charge having flowed through the device. Hence x and $q(t)$ are directly proportional to one another. When a signal is applied to the device, the boundary between the doped and undoped regions moves, the direction of this movement depending on the polarity of the applied signal. Recall that the memristance is always positive, therefore it is always expected that: $x \in [0, 1]$ or $0 \leq x \leq 1$. Integrating Equation (39a) for x from 0 to 1, it can be seen that:

$$q_d = \frac{D^2}{\mu_v R_{on}}, \tag{40}$$

where q_d is the charge scaling factor which is required to move completely the doped/undoped boundary from $w = 0$ to $w = D$ [62]. Equation (39a) is rather rewritten as:

$$\frac{dx}{dt} = \frac{1}{q_d}\, i(t), \tag{41}$$

and this model is called the linear dopant drift model.

4.2. Window Function $g(x)$

There exists enriched intrinsic nonlinearity within the memristor device which also manifests in its hysteretic behavior [12], however, when the dopants move toward either of the boundaries, that is, $x = 0$ or $x = 1$, their speed decreases to zero which significantly affects the device dynamics and hence the performance. Due to the nano-nature of memristor devices, a small voltage can result in a huge electric field to be developed across the device, which in turn yields significant nonlinearities in the ionic transport [12]. These nonlinearities become more apparent in the boundaries where the drift speed of the dopant obviously reduces to zero. Hence, this phenomenon is called nonlinear dopant drift. However, the nonlinearity can be more pronounced at the boundary by inclusion of the window function $g(x)$.

Since the state variable x is bounded between 0 and 1, for an applied voltage bias, x is proportional to the quantity of charge q already passed through the device, until it approaches 0 or 1, where it requires higher voltage to switch from OFF resistance state to ON resistance state under positive bias and from ON resistance state to OFF resistance state under negative bias. Hence, the switching transition at these extreme boundaries is described as *hard switching* because these transitions delay until a certain amount of voltage threshold is reached. Thus, hard switching can be specified by considering different boundary conditions, hence the need for a window function. The window function $g(x)$ is basically a dimensionless function multiplied to the right-hand side of Equation (41) for modeling the nonlinear dopant drift when x approaches 0 or 1 and for avoiding x from taking values outside of the limits $[0, 1]$. For example, the SPICE circuit simulation of the linear model often reports computation errors attributed to the values of x. On the other hand, there is no such error even for a hard switching case if a window function (i.e., nonlinear model) is used.

Therefore, a window function $g(x)$ is added as a factor in the right-hand side of Equation (41) in order to maintain x in the interval $[0,1]$ [62]. This is called nonlinear dopant drift modeling and the state Equation (41) now becomes:

$$\frac{dx}{dt} = \frac{1}{q_d} g(x) i(t). \tag{42}$$

The model of TiO_2 memristor is usually characterized by two models, namely: linear and nonlinear dopant drift models, with the state equation given by (41) and (42), respectively. Some authors have tried to define the function $g(x)$ with a more physical description of the device, in modeling the nonlinearity of the charge carriers along the device geometry. Due to the direct dependency of x on $q(t)$, Equation (42) suggests that a higher quantity of charge is needed for w to be closer to 0 or D [12]. Five sufficient and necessary conditions for any efficient window function are outlined by Prodromakis et al. [63].

The proper choice of the window function is of significant importance for predictive modeling of memristors because the system may respond differently with respect to the window function used [64]. There are many suggested window functions essentially to resolve the boundary issues and to impose nonlinearities [65–75]. However, each of them has their own advantages as well as their own disadvantages. Some of the commonly used window functions are described briefly in the following.

- Strukov et al. [12,65] proposed a window function, given by:

$$g(x) = x(1-x). \tag{43}$$

  In the boundary limits, x will remain at 0 or 1 until the device has changed its resistance state.
- Joglekar et al. [62] proposed $g(x)$ to be:

$$g(x) = 1 - (2x-1)^{2p}, \tag{44}$$

  where $p \in \mathbb{Z}^+$ is a positive integer serving as a control parameter. For large p, this window function gives a better nonlinear ionic drift than Strukov et al. However, the model reduces to linear dopant drift if $p \to \infty$. Notice that for $p = 1$, $g(x)$ in Equation (44) becomes: $g(x) = 4x(1-x)$, that is, four times Strukov's function. Hence, the control parameter p gives Joglekar's function more flexibility than Strukov's function.
- Prodromakis et al. [63] proposed $g(x)$ to be:

$$g(x) = 1 - [(x-0.5)^2 + 0.75]^p, \tag{45}$$

  where $p \in \mathbb{R}^+$ is a positive real number. This function has hence more versatility than Joglekar's function. Moreover, here p allows upward scaling of $g(x)$ such that its maximum value, i.e., g_{max}, remains in the interval: $0 \leq g_{max} \leq 1$. One can also see that for $p = 1$, $g(x)$ in Equation (45) becomes: $g(x) = x\,(1-x)$, the same as Strukov's function. Similarly, for $p \to \infty$, the model resembles linear drift model. Moreover, Prodromakis et al. take into account the unusual situation whereby the dopant's drift is such that $g_{max} \gtreqless 1$, by introducing a new scalar j serving as a second control parameter in expression (45), thus becoming:

$$g(x) = j\Big(1 - [(x-0.5)^2 + 0.75]^p\Big). \tag{46}$$

  For a fixed value of parameter p with j varying suitability, $g(x)$ can be scaled up and down in conformity with: $g_{max} \gtreqless 1$.

- Biolek et al. [66] proposed $g(x)$ to be:

$$g(x) = 1 - (x - stp(-i))^{2p}, \tag{47}$$

where $p \in \mathbb{Z}^+$ and i is the current flowing through the memristor, such that:

$$stp(i) = \begin{cases} 1 \ \ for\ i \geq 0, \\ 0 \ \ for\ i < 0. \end{cases} \tag{48}$$

The flowing current i is considered as positive when the device is in saturation mode, i.e., $x \to 1$ corresponding to the expansion of the doped layer, and negative if the device is in depletion mode, i.e., $x \to 0$ which corresponds to the contraction of the doped layer. Notice that there is a discontinuity in the boundaries due to the step function definition of the current i.

- Proposed window function:
In accordance with the role of window function, we propose $g(x)$ as derived from Hann window apodisation function as follows:

$$g(x) = \frac{1}{2}[1 + cos\ 2\pi(\alpha(x))].$$

Moreover, to fulfill the continuity constraints for $x = 0$ and $x = 1$, a sufficient condition stands: $\alpha(x) = x - \frac{1}{2}$, that is:

$$g(x) = \frac{1}{2}[1 + cos\ \pi(2x - 1)]. \tag{49}$$

Figure 18a shows the comparison of the four aforementioned window functions. The window functions by Strukov's team and Biolek's team lacking flexibility, a comparison is drawn between the models by Joglekar on one hand, and Prodromakis on the other, that is, Equations (44) and (45), respectively. The control parameter p is arbitrarily chosen in ascending order in order to observe the corresponding responses of $g(x)$: $p = 1$, 2, 10, and 20, and the results are given in Figure 18b. One can see that for all p, Joglekar's function has $g(0.5) = 1$, unlike Prodromakis's function where $g(0.5)$ is scalable from 0 to 1 with increase in p, with $g(0.5) \equiv g_{max}(x)$. In addition, for $p \to \infty$, both models resemble the linear drift model. Finally, another known window function is the ThrEshold Adaptive Memristor (TEAM) model [67].

Figure 19 shows the comparison of the nonlinear models by Strukov, Joglekar and Prodromakis with respect to the flowing charge. The high- and low-resistance states are $R_{off} = 16$ KΩ and $R_{on} = 100\ \Omega$, respectively. Figure 19 shows the comparison of the memristance transition from its highest resistance state to the lowest state and vice versa. The results show that each model requires a different quantity of charge to fully transition from R_{off} to R_{on} and vice versa.

The effect of choosing a memristor model for a particular application was investigated [76]. It was shown that the amount of charge q_R required for the memristance to fully transit from its high resistance state to the low resistance state and vice versa depends on the model under consideration, see Table 1. Figure 20 shows the comparison of linear and nonlinear models on the memristance transition with respect to the flowing charge. The result is obtained using the nonlinear model by Joglekar and Wolf [62]. The results show that as the parameter p increases, the nonlinear model tends to the linear one.

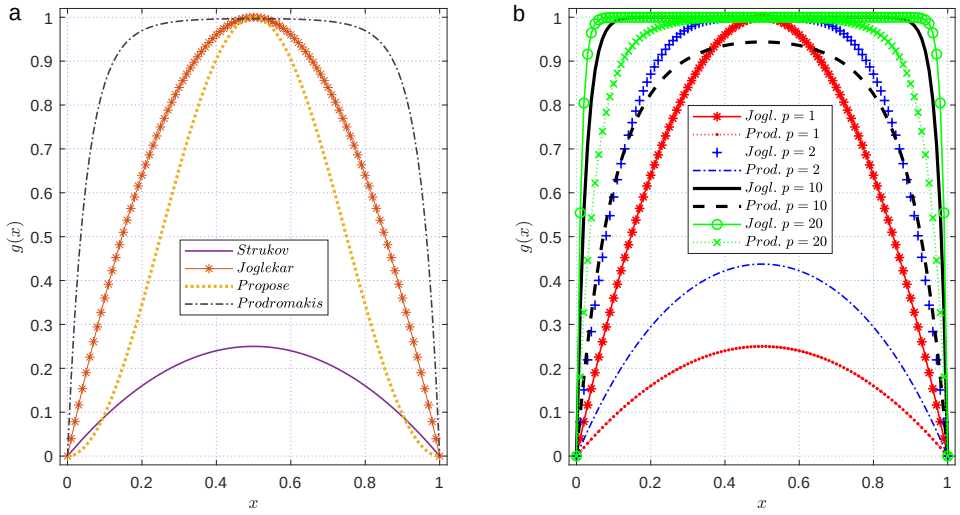

Figure 18. Window functions comparison. (**a**) Proposed window function and its comparison with the discussed functions. Joglekar ($p = 1$) and Prodromakis ($p = 10$), (**b**) Comparison of Joglekar and Prodromakis window functions, showing the effect of varying p.

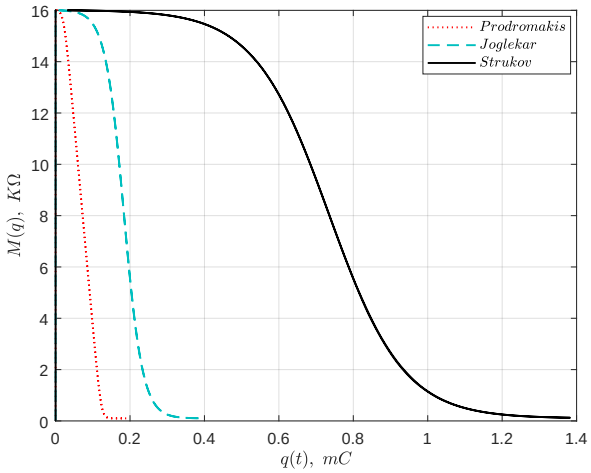

Figure 19. Comparison of the memristance transition with respect to the flowing charge for the models by Strukov, Joglekar and Prodromakis.

Table 1. Comparison of the three nonlinear dopant drift models.

Window Function $g(x)$	**Strukov**	**Joglekar**	**Prodromakis**
Resolve boundary issues	✓	✓	✓
Impose nonlinear drift	✓	✓	✓
Linkage with linear drift	✗	✓	✓
Control parameter	✗	✓	✓
g_{max} scalability	✗	✗	✓
q_R value	1.3 mC	350 µC	150 µC

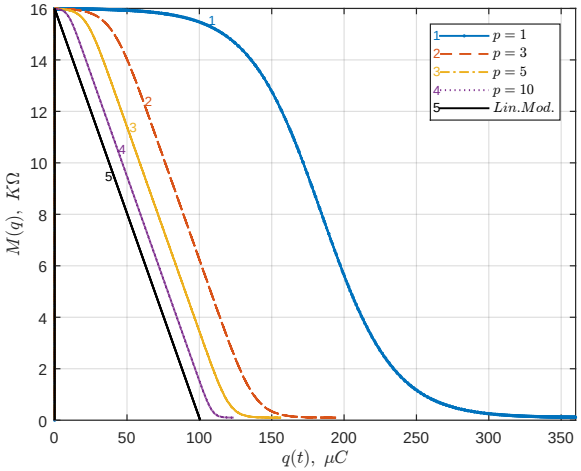

Figure 20. Memristance transition with respect to the flowing charge for linear and nonlinear dopant drift models. The nonlinear model used the window function by Joglekar and Wolf. When the parameter p increases, the nonlinear model tends to the linear one adapt with permission from ref. [76].

The analytical solution of the memristor model is given in the following according to linear and nonlinear models, that is, by observing the effect of window function $g(x)$ in the two possible scenarios: *without any window function Equation (41)* and *with a window function according to Equation (42)*. The analysis also takes into account the mode of excitation, that is, charge-controlled and flux-controlled memristor.

4.3. Linear Dopant Drift Model: Analysis

Here, the state Equation (41) is considered solely, and the state variable x is calculated from this equation to be used in the memristance equation, and subsequently to determine the voltage drop across the memristor and the current flowing through it. Firstly, the case of a current excitation (charge-controlled memristor: CCM) is considered and then followed by the case of a voltage excitation (flux-controlled memristor: FCM). The analytical expressions are derived for each case and the results are given accordingly.

4.3.1. CCM with Linear Dopant Drift Model

In this case, the memristance is driven by a current source. Therefore, for a memristor with memristance $M(q)$ subjected to a time-varying current source $i(t)$, the voltage drop across the memristor will be: $V(t) = M(q)\ i(t)$. The state variable $x(t)$ can be expressed from Equation (41) by integration:

$$x(t) - x_0 = \frac{1}{q_d}\big(q(t) - q_0\big), \tag{50}$$

where $x_0 = \dfrac{w(0)}{D}$ is the state variable at $t = 0$, given the previous history of the device with a charge q_0 having already flowed through the memristor. Actually, for a formed (used) memristor device, x_0 is likely to be non-zero because the dopants are dis-localized, hence the device has some previous information preserved. It is easy to predict x_0 if the initial memristance of $M(x)$ (i.e., $M0$) is known. From Equation (39c): $M_0 = R_{off} - \delta R\ x_0$. Here, x_0 is simply a notation to represent the previous state of the device. Therefore, having $q(t)$ known and $x(t)$ expressed in terms of $q(t)$, from (39c) and (50), thus: $M(q) = R_{off} - \delta R\ x_0 - \delta R\ \dfrac{1}{q_d}(q(t) - q_0)$. With the assumption $x_0 \ll 1$ so that, $M_0 \simeq R_{off}$, thus:

$$M(q) = R_{off} - \delta R \frac{q(t)}{q_d}. \tag{51}$$

Now, from the expression of $M(q)$, $V(t) = M(q)i(t)$ is known for any $i(t)$ and the result is given by Figure 21. The results show the effect of changing frequency on the V–I characteristics.

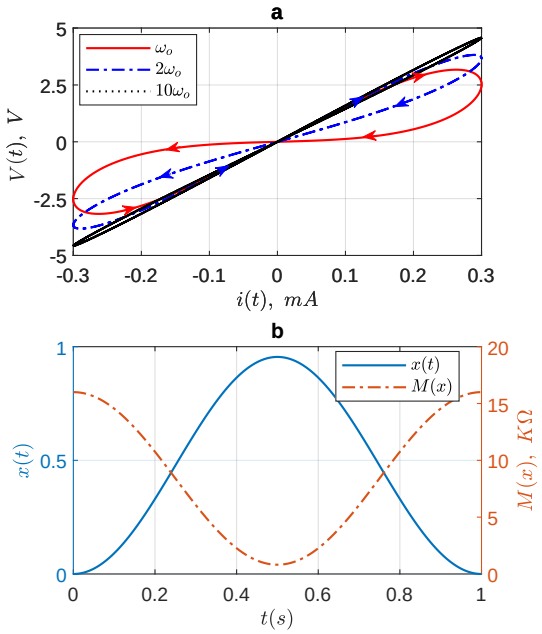

Figure 21. Analytical results of CCM with Linear model, $R_{on} = 100\ \Omega$, $R_{off} = 16\ \mathrm{K}\Omega$, $q_d = 100\ \mu\mathrm{C}$ and three different input frequencies. (**a**) I–V characteristics, (**b**) state variable and memristance transitions for $f = 1$ Hz.

4.3.2. FCM with Linear Dopant Drift Model

Here, the memristor is driven by a voltage source $V(t)$ connected across its two terminals, and the current flowing through the memristor $i(t)$ is given by: $i(t) = Y(\phi)\ V(t)$, where $Y(\phi)$ is the memductance. From the definition of memristor: $d\phi = M(q)\ dq$. Let us substitute an expression of $M(q)$ from (51) in order to obtain the relationship between charge $q(t)$ and the flux $\phi(t)$, thus $d\phi = \left[R_{off} - \delta R\ \frac{q(t)}{q_d}\right] dq$:

$$\phi(t) - \phi_0 = R_{off}\ (q(t) - q_0) - \frac{\delta R}{2q_d}\ (q(t)^2 - q_0^2).$$

This is a quadratic equation in $q(t)$ and is solved to give the feasible value of $q(t)$ compatible with the boundary condition:

$$q = q_d \left(1 - \sqrt{\left(1 - \frac{q_0}{q_d}\right)^2 - \frac{2(\phi - \phi_0)}{q_d R_{off}}}\right). \tag{52}$$

From the Equations (50) and (52):

$$x(t) = x_0 + 1 - \sqrt{\left(1 - \frac{q_0}{q_d}\right)^2 - \frac{2(\phi - \phi_0)}{q_d R_{off}}} - \frac{q_0}{q_d}. \tag{53}$$

With $x(t)$ known, M can easily be determined and $Y = \frac{1}{M}$. Hence, for any input voltage $V(t)$ connected across the memristor, the current $i(t)$ is given by: $i(t) = Y(\phi)\ V(t)$. Figure 22 shows the current–voltage response and the corresponding state variables for three different input frequencies.

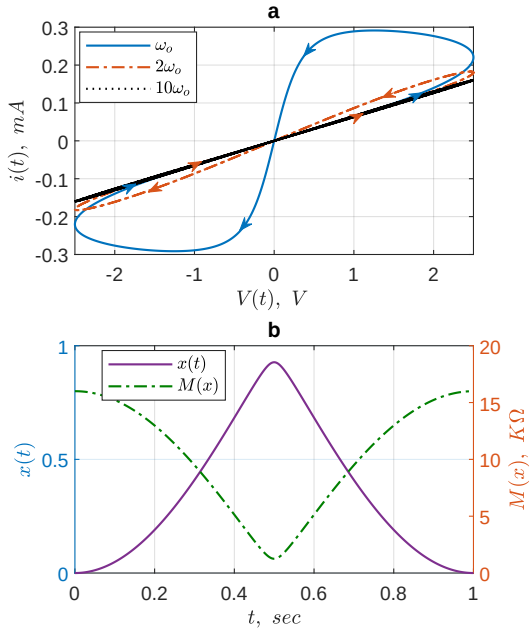

Figure 22. Analytical results of FCM with linear dopant drift model: $R_{on} = 100\ \Omega$, $R_{off} = 16\ \mathrm{K}\Omega$, $q_d = 100\ \mu\mathrm{C}$ and different input frequencies. (**a**) I–V characteristics, (**b**) state variable and memristance transitions for f = 1 Hz.

4.4. Nonlinear Dopant Drift Model: Analysis

Here, we consider the nonlinear dopant drift model which is characterized by Equation (42). Considering $g(x)$ by Joglekar and Wolf [62], for $p = 1$: $g(x) = 4x\ (1 - x)$ corresponding to the $g(x)$ in [12] multiplied by four. The voltage across and current through the memristor can be calculated. This then corresponds rather to Strukov's window function that will be considered as:

$$g(x) = x(1 - x).$$

4.4.1. CCM with Nonlinear Dopant Drift Model

The state Equation (42) becomes: $\dfrac{dx}{dt} = \dfrac{1}{q_d}\ x\ (1 - x)\ i(t) \ \Rightarrow$

$$x(t) = \frac{x_0\ e^{\frac{q - q_0}{q_d}}}{1 - x_0 + x_0\ e^{\frac{q - q_0}{q_d}}}, \tag{54}$$

where $q(t = 0) = q_0$ and $x(t = 0) = x_0$ are the initial conditions at time $t = 0$. Therefore, the charge-controlled memristance $M(q)$ becomes:

$$M(q) = R_{off} - \delta R\ \frac{x_0\ e^{\frac{q - q_0}{q_d}}}{1 - x_0 + x_0\ e^{\frac{q - q_0}{q_d}}}. \tag{55}$$

With an input current $i(t) = I_0\ sin(\omega t)$, the voltage across the memristor is: $V(t) = M(q)\ i(t)$ and the results are shown in Figure 23.

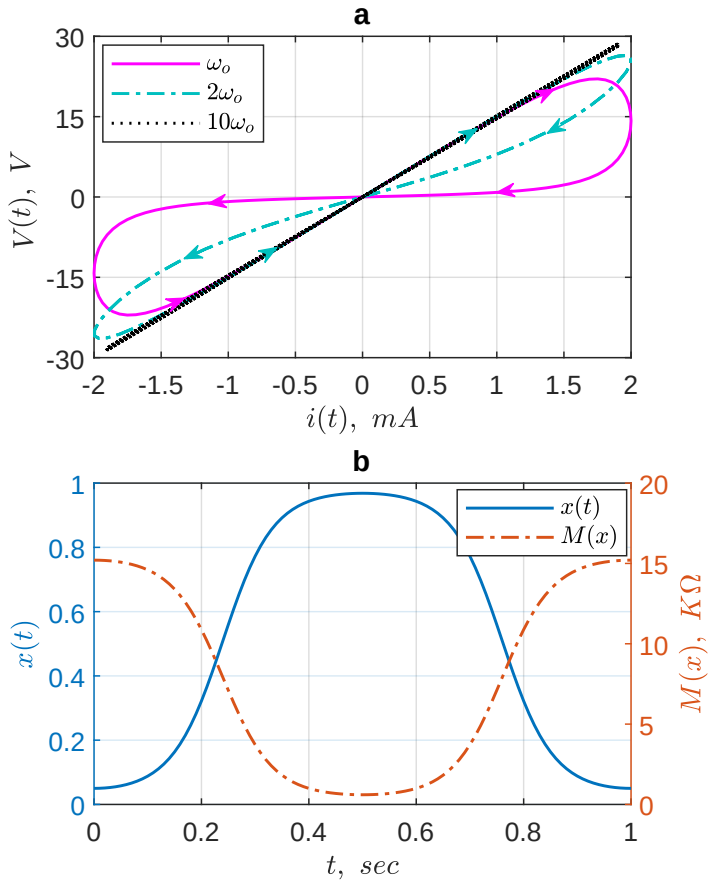

Figure 23. Analytical results of the CCM with nonlinear dopant drift model at different input frequencies. $I_0 = 2$ mA, $x_0 = 0.05$, $q_d = 100$ µC, $R_{off} = 16$ KΩ, $R_{on} = 100$ Ω and $\delta R = 15.9$ KΩ. (**a**) I–V characteristics, (**b**) state variable and memristance transitions for f = 1 Hz.

4.4.2. FCM with Nonlinear Dopant Drift Model

Recall that for any input voltage $V(t) = V_0 sin(\omega t)$ applied to the memristor, the flux is given by $\phi(t) = \frac{V_0}{\omega}\left[1 - cos(\omega t)\right] + \phi_0$ and the dynamic state of the memristor $x(t)$ is driven by flux $\phi(t)$. Therefore, once again by definition $V(t) = M(q)\frac{dq(t)}{dt}$, from Equation (55), it follows that:

$$q(t) = q_0 - q_d \ln\left(\frac{e^{-\frac{V_0[1-cos(\omega t)]}{q_d \delta R\ \omega}} - x_0}{1 - x_0}\right). \tag{56}$$

Similarly, $x(t)$ can be obtained. From Equations (54) and (56), thus: $Y = \frac{1}{M}$ and $i(t) = Y(\phi)V(t)$ and the results are shown in Figure 24.

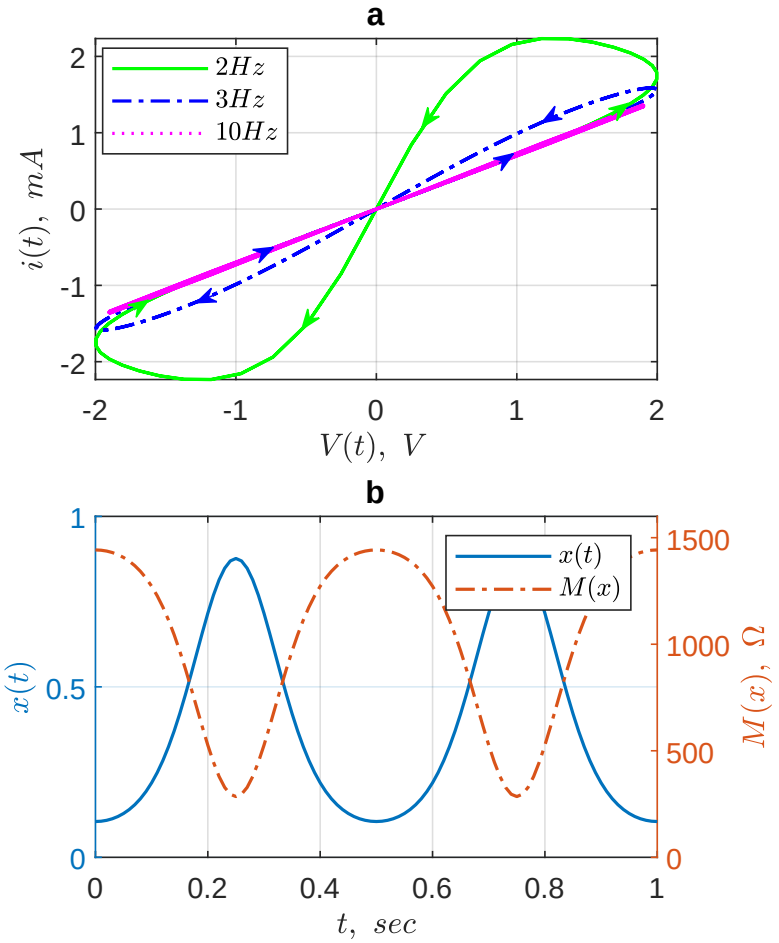

Figure 24. Analytical results of FCM with nonlinear dopant drift modal at different input frequencies. $V(t) = V_0 sin(\omega t)$, $V_0 = 2$ V, $x_0 = 0.1$, $q_d = 100$ µC, $R_{off} = 16$ KΩ, $R_{on} = 100$ Ω and $\delta R = 15.9$ KΩ. (**a**) I–V characteristics, (**b**) state variable and memristance transitions for f = 2 Hz.

4.4.3. In-Memory Computing

In traditional computing (Von Neumann computing architecture), the memory and processing units are separate. Therefore, data processing involves read and write protocols. This process is delayed and energy consuming which is not efficient in high-density data applications such as neural networks and artificial intelligence. These concerns can be avoided by allowing the data to be processed within the memory block, hence referred to as in-memory computing (IMC).

Large networks, such as, neural networks for brain-inspired systems require in-memory computing in order to avoid latency for data accession and processing. This approach improves the processing speed and, hence the overall network performance. In recent years, in-memory computing has become a significant field of study owing to the sizeable data era challenges. Memristor is proved to be a reliable element for achieving efficient memristor-based in-memory computing which is an alternative architecture to Von Neumann computing [77,78]. Many challenges such as stochasticity, CMOS compatibility, memristor integration, etc., for the implementation of memristor-based computing architecture are further discussed in [78,79].

There is significant progress in the development phase of memristor-based in-memory computing, including device architectures, material engineering and challenges to practical implementation [80–91].

5. Spice and Analogue Models of Memristor

SPICE is an acronym of **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis used for simulating and analyzing different circuit functionality. The mathematical description of a given phenomenon can be modeled in SPICE with the aid of its built-in control sources (for example, voltage-controlled voltage source, voltage-controlled current source, behavioral sources, etc.) and other components such as resistors, capacitors, OpAmps. With the discovery of TiO_2 memristor, many SPICE models of memristor were proposed mimicking its behavior. The mathematical description of HP TiO_2 memristor is used to emulate memristor characteristics, as such many models are reported and some are based on particular applications [92–97]. The most commonly used SPICE model is that developed by Biolek et al. [66], whose setup is shown in Figure 25. Figure 25a shows the block diagram representation of the port and state equations of the memristor:

$$V(t) = \left(R_{off} - \delta R x\right) I(t) \text{ and } \frac{dx}{dt} = kI(t)f(x) \text{ with } k = \frac{\mu_v R_{on}}{D^2}. \tag{57}$$

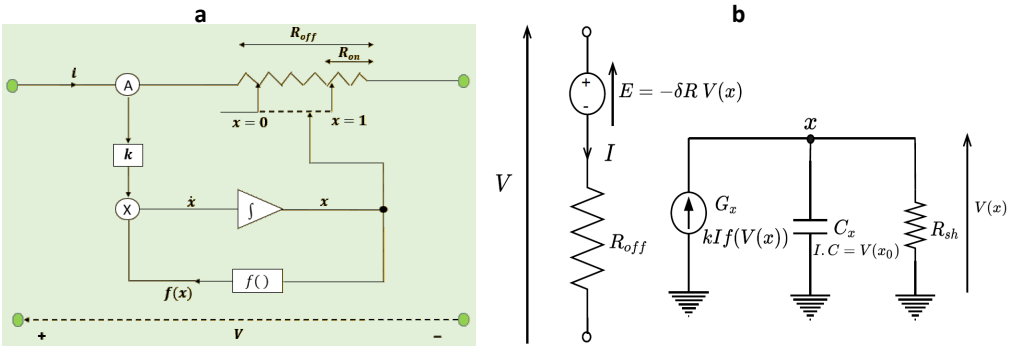

Figure 25. SPICE implementation of TiO_2 memristor model for simulation purposes. (**a**) Block diagram representation of the memristance function: $V = R(x)i$ and $\frac{dx}{dt} = kf(x)i$ where $k = \frac{\mu_v R_{on}}{D^2}$, (**b**) Equivalent SPICE model: E is an E-type voltage source (i.e., voltage-controlled voltage source), G is a G-type current source (voltage-dependent current source) and R_{sh} is the shunt resistance of the integrator.

The ammeter (A) senses the current flowing through the memristor, meanwhile the memory effect is modeled by means of a feedback-controlled integrator. The feedback of the nonlinear window function $f(x)$ models the nonlinear dopant drift and the influence of the boundary conditions. The memristance value between R_{off} and R_{on} is determined by the coordinate of $x \in (0, 1)$.

Figure 25b shows the equivalent SPICE schematic of the Equation (57). The capacitor C_x whose initial voltage models the initial state of the normalized width x_0, is used as the integrator of the differential state equation. The port equation is modeled with the aid of E-type voltage source (voltage-dependent voltage source) whose source is the voltage of capacitor and then multiplied by the gain $-\delta R$, and is connected in series with a resistor R_{off}. $V(x)$ is the voltage of the capacitor C_x and it models the normalized width x of the memristor, while R_{sh} is the shunt resistor grounding the integrator unit. The integrand, that is, the quantity on the right-hand side of the state equation is modeled with the aid of a G-type current source (voltage-dependent current source) that multiplies the memristor current I by the gain $kf(V(x))$. The SPICE netlist file of Figure 25b is given in Figure 26, and is used to create memristor SPICE components for simulation purposes. The integral of the current (or charge) and voltage (or flux), respectively, flowing through and across the memristor can be modeled using the E-type voltage source, hence allowing visualization of the monotonically increasing function of q versus ϕ in the ϕ-q plane.

```
.SUBCKT memristor pl mn PARAMS: Ron=100
+ Roff=16K Ri=11K D=10N uv=10F p=1
* Differential state equation  *
Gx 0 x value={ I(Em)*uv*Ron*f(V(x),p)/D^2}
Cx x 0 1 IC= {(Roff-Ri)/(Roff-Ron)};
Rsh x 0 1T
* Resistive port equation *
Em pl aux value={-I(Em)*(Roff-Ron)*V(x)}
Roff aux mn {Roff}
* Note that I(Em)=I
* flux computation
Eflux flux 0 value={SDT(V(pl,mn))}
* charge computation
Echarge charge 0 value={SDT(I(Em))}
* Nonlinear drift modeling
.func f(x,p)={1-(2*x-1)^(2*p)}
.ENDS memristor
```

Figure 26. Memristor SPICE netlist file.

The initial state of the memristor is given by the initial voltage $V(x_0)$ across the capacitor. The initial memristance R_i is determined as: $R_i = R_{off} - \delta R x_0$. Figure 27 shows the results of the memristor netlist file in Figure 26. The result is obtained using a sine voltage source connected across the port terminals *pl* and *mn* of the memristor. Figure 27a shows the transient results of voltage and current for an input voltage amplitude of 1.2 V and the corresponding I–V characteristic is given in Figure 27b. Furthermore, Figure 27c shows the corresponding monotonically increasing ϕ-q function, thus matching the characteristics of the memristor from its constitutive relationship. Meanwhile, Figure 27d shows the memristance with respect to the transition of the device state variable.

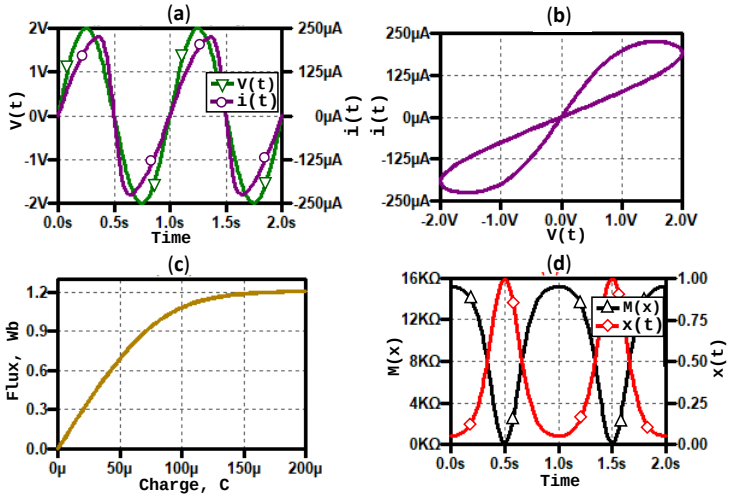

Figure 27. Simulation results of the memristor netlist file given in Figure 26. $V = V_0 sin(\omega t)$, $V_0 = 1$ V, $f = 1$ Hz, $R_{on} = 100\ \Omega$, $R_{off} = 16$ KΩ, $\mu_v = 10$ f m^2/(V.s) and D = 10 nm, which gives $q_d = 100$ µC. (**a**) V and i transients, (**b**) I–V characteristic, (**c**) ϕ-q curve and (**d**) memristance and state variable transitions.

5.1. Analogue Models of Memristor

Analogue memristor models are developed using analog and active components such as operational amplifiers, hence modeling the behavior of memristor for simulation [98–103]. Analog models can be easily implemented in the laboratory for practical and research purposes. For example, Figure 28 shows an analog model of a flux-controlled memristor [98]. The model is analyzed by considering different input signals, for example sinusoidal, triangular input voltage sources, etc., and shows a pinched hysteresis loop, which is the primary signature of a memristor.

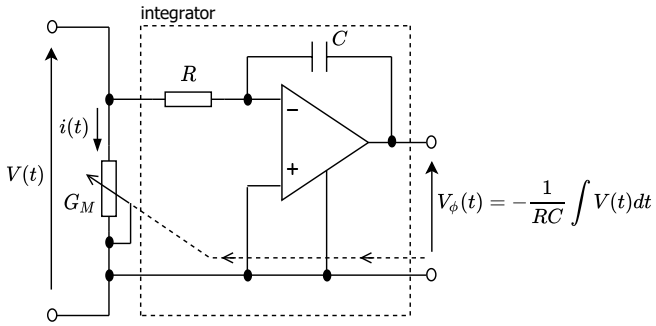

Figure 28. Analogue model of memristor adapt with permission from ref. [98].

Figure 25b is similar to Figure 28 with differences in the integration unit, that is RC and operational amplifier, respectively. Comparing the two figures, one can see that $R_{sh} = R$ and $C_x = C$. As shown in the introduction that for flux-controlled memristors, the state variable is a function of flux and the memristor dynamics depend upon the flux whose magnitude is proportional to the voltage across the memristor. In Figure 28, the operational amplifier block is used as an integrator to generate its output voltage proportional to the flux. The output flux is expressed as:

$$V_\phi(t) = \frac{1}{\tau}\int V(t)dt, \tag{58}$$

where $\tau = RC$ is a time constant. The memductance $G_M(t)$ depends linearly on $V_\phi(t)$, with:

$$G_M(t) = G_0 + K_G V_\phi(t), \tag{59}$$

where G_0 and K_G are constants. Finally, the current $i(t)$ is given by:

$$i(t) = G_M(t).V(t). \tag{60}$$

Equations (58)–(60) are analyzed using a sine voltage $V(t)$ as:

$$V(t) = V_0 sin(\omega t), \tag{61}$$

whose flux $\phi(t)$ is represented by the voltage $V_\phi(t)$ obtained by integrating (61):

$$V_\phi(t) = \frac{V_0}{\tau\omega}(1 - cos(\omega t)) + \frac{\phi_0}{\tau}, \tag{62}$$

where ϕ_0 is the initial flux. Knowing the flux $V_\phi(t)$, the memductance $G_m(t)$ and the current $i(t)$ are to be calculated using Equations (59) and (60), respectively. Figure 29 shows the results of sinusoidal input voltage, observed for different frequencies and Figure 29 shows the results obtained for sine input voltage with values parameters: $R = 1$ KΩ, $C = 1$ μF, $G_0 = 0.5$ S and $K_G = 10$ SV^{-1}. The results are significantly modified with the changes of G_0, K_G and frequency.

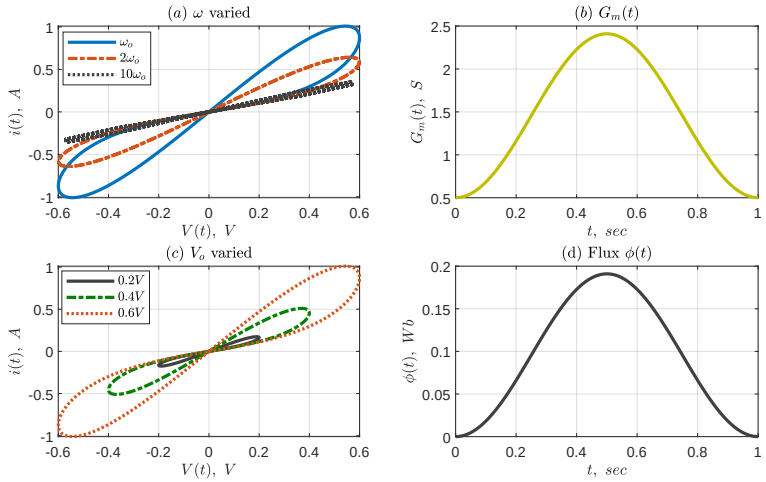

Figure 29. Results of the sinusoidal input voltage. Parameters set: $R = 1$ kΩ, $C = 1$ μF, $G_0 = 0.5$ S and $K_G = 10$ SV^{-1} (**a**) $V_o = 0.6$ V and variation of input frequency, $\omega_o = 2\,\pi f_o$ with f_o = 1 Hz. (**b**) memductance for ω_o and $V_o = 0.6$ V, (**c**) at ω_o frequency and variation of voltage amplitude V_o, (**d**) the flux $\phi(t)$ for ω_o and $V_o = 0.6$ V.

Passive Models of the Memristor Emulator

Figure 30 shows the schematic of a passive memristor emulator [102]. The model is similar to the one in Figure 28 with the exception that junction field effect (JFET) transistor is used instead of the operational amplifier and without any need for internal power to operate. The voltage across the gate (G) terminal with respect to the source (S) terminal corresponds to the voltage V_C across the capacitor C provided that the gate resistance (R_G) is infinite, that is no current flows through R_G. The role of the gate resistance R_G is to avoid leakage of current through the gate, therefore, it separates the gate from the output of the RC cell which acts as a passive lossy integrator having the cutoff frequency $f_c = \dfrac{1}{2\pi RC}$.

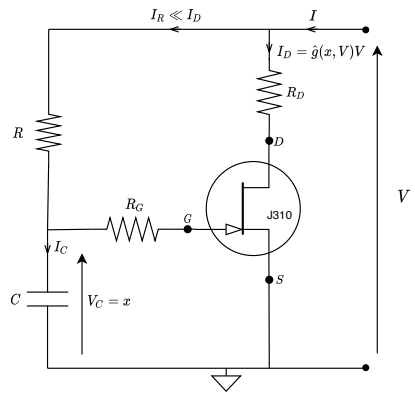

Figure 30. Schematic of a passive memristor emulator adapt with permission from ref. [102].

R_D is a small resistance (optional) connected to the drain terminal in order to measure the current flowing through the drain and then the source terminal. Since no current goes into the gate terminal of the JFET, the current through the resistor R is the same as that through the capacitor, that is: $I_R = I_C$. Therefore, $V_C = V_{GS}$, controls the current through the D-S junction. For frequencies below f_c, the current $I_R = C\dfrac{dV_C}{dt}$ is reflectible with respect to I_D. Taking into account the differential equation of the RC cell and its high impedance level (i.e., $I_R \ll I_D$), the mathematical relationship of Figure 30 can be expressed from Kirchhoff's laws:

$$C\frac{dV_C}{dt} + \frac{V_C - V}{R} = 0 \;\Rightarrow$$

$$\frac{dV_C}{dt} = \frac{1}{RC}(V - V_C). \tag{63}$$

The transconductance of the device is controlled by the voltage V_C across the capacitor and, hence it is equivalent to the state variable x of the system: $V_C = x$. Furthermore, this state variable V_C corresponds to the integral of the port voltage V and $V_{DS} = V$ because R_D is negligible. Therefore, the characteristics of JFET transistor as given in [98], are:

$$I_D = \hat{g}(V_{GS}, V_{DS})V_{DS} = \hat{g}(x, V)V. \tag{64}$$

From Equations (63) and (64) we obtained the following state-dependent Ohm's law relationship:

$$\frac{dx}{dt} = \frac{1}{RC}(V - x), \tag{65}$$

$$I = \hat{g}(x, V)V. \tag{66}$$

This model is used experimentally for the study of chaos in Duffing oscillator [104,105].

6. Modeling

The pinched hysteresis loop gives the circuit response of a memristor and is considered the primary signature for identifying memristive systems. Recall that a memristor is characterized by the constitutive relationship between magnetic flux ϕ and electric charge q, hence the equivalent graphical representation is called ϕ-q curve which in essence gives the characteristics of a memristor. The ϕ-q curve is used to effectively model memristor because it also provides a better representation and analysis of a study dealing with certain initial conditions [21]. The description of the ϕ-q curve of model (39) was illustrated in detail [106]. The memristor model (39) remembers the coordinate of its state variable. However, the dynamics of the state variable x are proportional to the charge $q(t)$ flowing through it. Therefore, from Equation (39a), it gives:

$$x(t) = \frac{q(t)}{q_d} = \frac{1}{q_d}\left(q_0 + \int_0^t i(\tau)d\tau\right),$$

and the expression of the memristance becomes:

$$M(q) = \begin{cases} R_{off}, & \text{if } q(t) \leq 0 \\ R_{off} - \delta R\,\dfrac{q(t)}{q_d}, & \text{if } 0 \leq q(t) \leq q_d \\ R_{on}. & \text{if } q(t) \geq q_d \end{cases} \tag{67}$$

Equation (67) shows the expression of the memristance $M(q)$ as a function of the flowing charge $q(t)$. With $d\phi = M(q)dq$, Equation (67) can be simplified further to observe the ϕ-q curve. Furthermore, it was shown that the model (67) has discontinuities for its first derivative versus q at $q = 0$ and $q = q_d$ which is disadvantageous in the study of memristor dynamics in CNN neighborhood connections between pixel cells because the system requires a continuous $\dfrac{dM}{dq}(q)$ function for all of the flowing charge [106,107]. To avoid such discontinuities, a new model was proposed as follows [106]:

$$M(q) = \begin{cases} R_{off}, & \text{if } q(t) \leq 0 \\ R_{off} - \dfrac{3\,\delta R}{q_d^2}\,q^2 + \dfrac{2\,\delta R}{q_d^3}\,q^3, & \text{if } 0 \leq q(t) \leq q_d \\ R_{on}, & \text{if } q(t) \geq q_d \end{cases} \tag{68}$$

with its first derivative with respect to charge given by:

$$\frac{dM(q)}{dq} = \begin{cases} -\frac{6\,\delta R}{q_d^2} q + \frac{6\,\delta R}{q_d^3}\, q^2, & \text{if } 0 \le q(t) \le q_d \\ 0. & \text{if } q \le 0 \ \text{ or } \ q \ge q_d \end{cases} \tag{69}$$

Furthermore, using $d\phi = M(q)dq$ and Equation (68), the corresponding expression of the relationship between flux ϕ and charge q is given by:

$$\phi = \begin{cases} R_{off}\ q, & \text{if } q(t) \le 0 \\ R_{off}\ q - \frac{\delta R}{q_d^2}\, q^3 + \frac{\delta R}{2q_d^3}\, q^4, & \text{if } 0 \le q(t) \le q_d \\ R_{on}\ q + \frac{\delta R}{2}\, q_d, & \text{if } q(t) \ge q_d. \end{cases} \tag{70}$$

Note that here again, $\phi = \hat{\phi}(q)$ can be shifted vertically or horizontally according to the choice of initial conditions. Figure 31 shows the comparison of the models (67) and (68). The result is obtained for $R_{off} = 16$ KΩ, $R_{on} = 100$ Ω and $q_d = 100$ μC. The black curve is for model (67) and it exhibits angulation due to the discontinuities at $q = 0$ and $q = q_d$. However, the red continuous curve is for the new model (68) which shows a rather better result because it solves the problem of derivative discontinuity at $q(t) = 0$ or q_d. The new model (68) gives a better representation of information in a neuronal scheme. Furthermore, the response of the new model is shown in Figure 32 obtained using a periodic sine input current source.

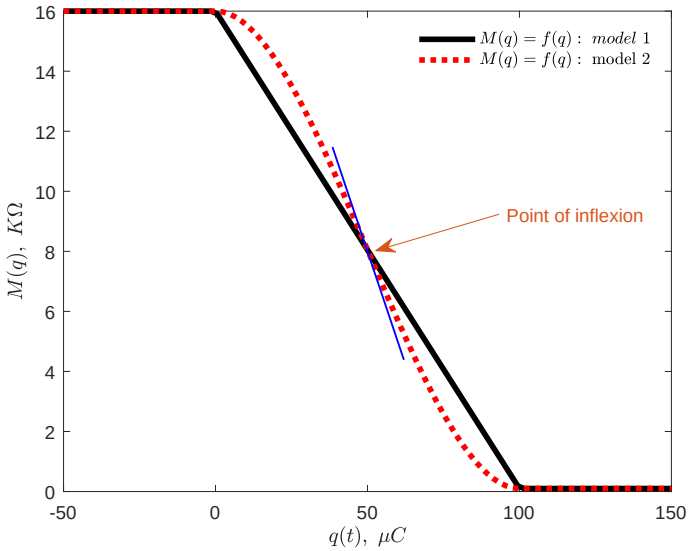

Figure 31. Comparison of the memristance $M(q)$ versus the flowing charge $q(t)$ for models (67) and (68), $R_{off} = 16$ KΩ, $R_{on} = 100$ Ω and $q_d = 100$ μC. The first derivative of $M(q)$ with respect to q $\left(i.e., \frac{dM(q)}{dq}\right)$ for Equation (67) has discontinuity at $q(t) = 0$ and $q(t) = q_d$ while $\frac{dM(q)}{dq}$ for Equation (68) is continuous at these q values.

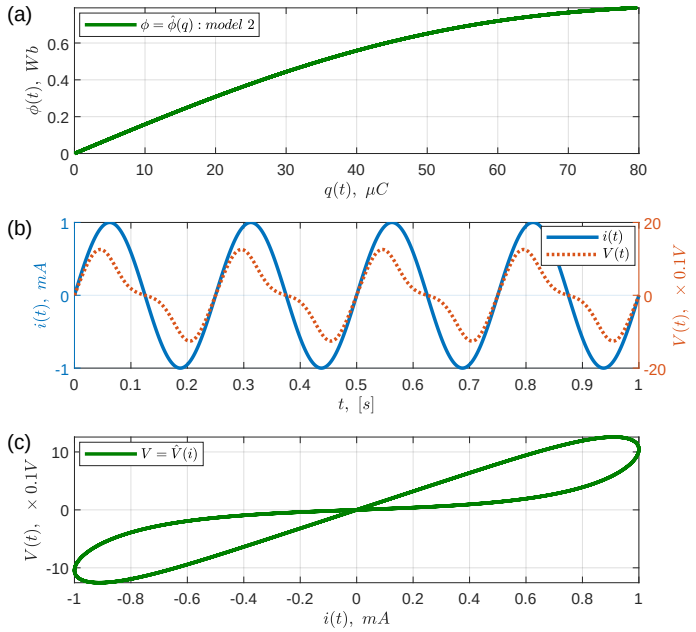

Figure 32. Characteristics of the memristor model given in Equation (68) by using a sine current input $i(t) = I_0\ sin(\omega t)$. The result is obtained for $R_{off} = 16$ KΩ, $R_{on} = 100$ Ω, $I_0 = 1$ mA, $f = 4$ Hz and $q_d = 100$ μC. (**a**) ϕ-q curve, (**b**) current and voltage transients and (**c**) I–V characteristics.

7. Some Potential Applications of Memristor

Memristor has many interesting features useful in electrical and electronic system designs. The following are some features associated with a memristor:

- It stores information, hence reliable for memory applications.
- It undergoes nano-scalability, hence suitable for modern-day nanotechnology.
- Conductance modulation resembling chemical synapse.
- It has connection flexibility, that is, series-parallel connections, and can form a stack of memory cells for high-density storage applications.
- It is compatible with CMOS technology allowing it to have a massively real-time and parallel computation in hybrid systems due to its reliable adaptability with CMOS neurons.
- It is a nonlinear circuit element, by its nature.
- It has low power consumption. As a nano device, it requires little power to operate.
- One memristor can replace multiple transistors in a circuit, thus it will ensure better performance and more reliable systems.

Undoubtedly, the aforementioned features suggest the memristor to be a proper candidate in modern-day electronic industries and for designing very effective neuromorphic systems and memory applications [108–111]. Figure 33 shows the taxonomy of memristor applications in discrete and crossbar array configurations which display the varieties of the memristor possibilities [112]. Since the discovery of HP TiO_2 memristor, the number of published memristive-based applications has increased exponentially. Hence, utilizing memristive devices in existing applications gives numerous advantages, for example: non-volatility, scalability, no leakage current and many more due to its compatibility with CMOS technology in terms of both electrical connections and manufacturing processes.

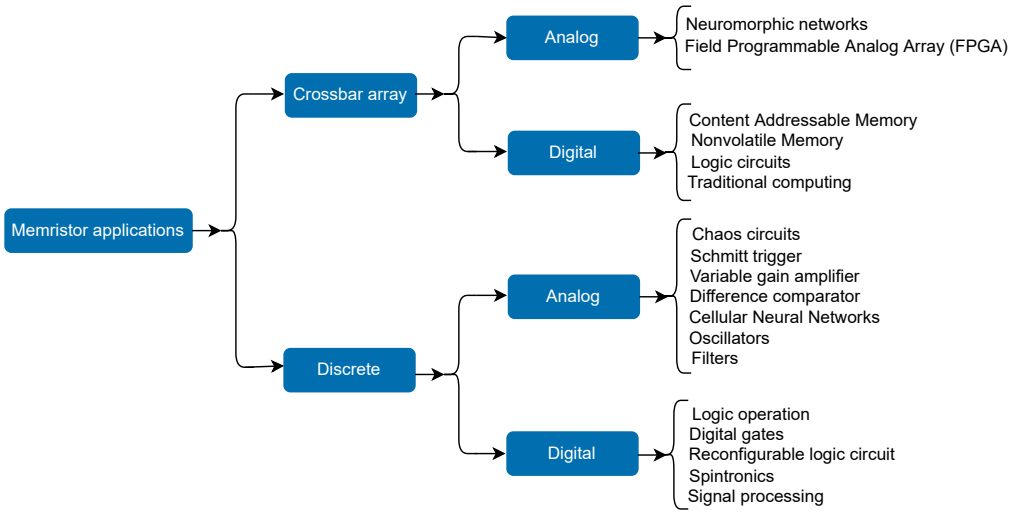

Figure 33. Classification of some memristor applications according to array and discrete configurations in both analog and digital domains.

In the last few years, there have been many proposed memristor-based applications [112–114]. The memristor has non-volatility properties with long retention and fast switching times [115], and is reported to be useful in high-density memory applications, e.g., non-volatile random access memory (NVRAM) and resistive random access memory (ReRAM) [116], storage and processing of big data, image recognition and processing [117,118]. The application of memristor could also be useful in field programmable gate array (FPGA) and implementation of chaotic circuits due to its adaptability to parallel and real-time computations [101,119]. Other applications areas include programmable analogue logic circuits [120–122], frequency and amplitude modulation [123], edge detection [124], neuromorphic system and bio-electronics [125–128] and cellular nonlinear/neural networks (CNN) [129–131].

Another intriguing application area of the memristor is its use as a synapse due to its conductance modulation resembling chemical synapse and very effective high-density connectivity [131,132]. Memristor-based electronic synapses are implemented, applicable to various neuromorphic computing architectures [133–139]. In fact, there is great progress in the phase of using memristor in neural networks and artificial intelligence [140–149].

Although the memristor is useful as a synapse in an artificial neural network, however, being a two-terminal component, it may not be adequate to effectively implement the high-density synaptic connections as each neuron has multiple synaptic connections to other neurons. Therefore, a hybrid multi-terminal memristor component such as memtransistor, with more connection terminals will be more efficient [150–152]. Thus, memtransistor is basically a combination of memristor and transistor and is determined to give a rather more brain-like network than a standalone memristor. Recently, a scalable multi-terminal memtransistor was implemented experimentally using a polycrystalline monolayer of molybdenum disulfide (MoS_2) and the results were very promising. Hence, memtransistor is reported to be useful in neuromorphic computing, for example, as artificial synapse and others such as nonvolatile memory and logic circuits [152–156].

A new function of the memristor as a transducer—called the memosducer—is demonstrated experimentally, and is particularly interesting in the optimization of ultrasonic excitation for Time Reversal-Nonlinear Elastic Wave Spectroscopy (TR-NEWS) dedicated to nonlinear acoustic imaging [157,158]. It was shown that the features of memristor such as hysteretic properties, nonlinearity and memory effect, etc., are promising in TR-NEWS-based ultrasonic imaging.

We are currently working on a memristor-based 2D cellular nonlinear network for signal and image processing as well as electronic prosthesis [76]. Figure 34 shows the schematic of the memristor-based 2D cellular nonlinear network using memristors in the coupling mode. The network is essential for signal and image processing with each cell corresponding to a pixel in an image application purpose. Each cell comprises one linear capacitor C in parallel with nonlinear resistance R_{NL}, and the nonlinear current response through the cell is expressed as:

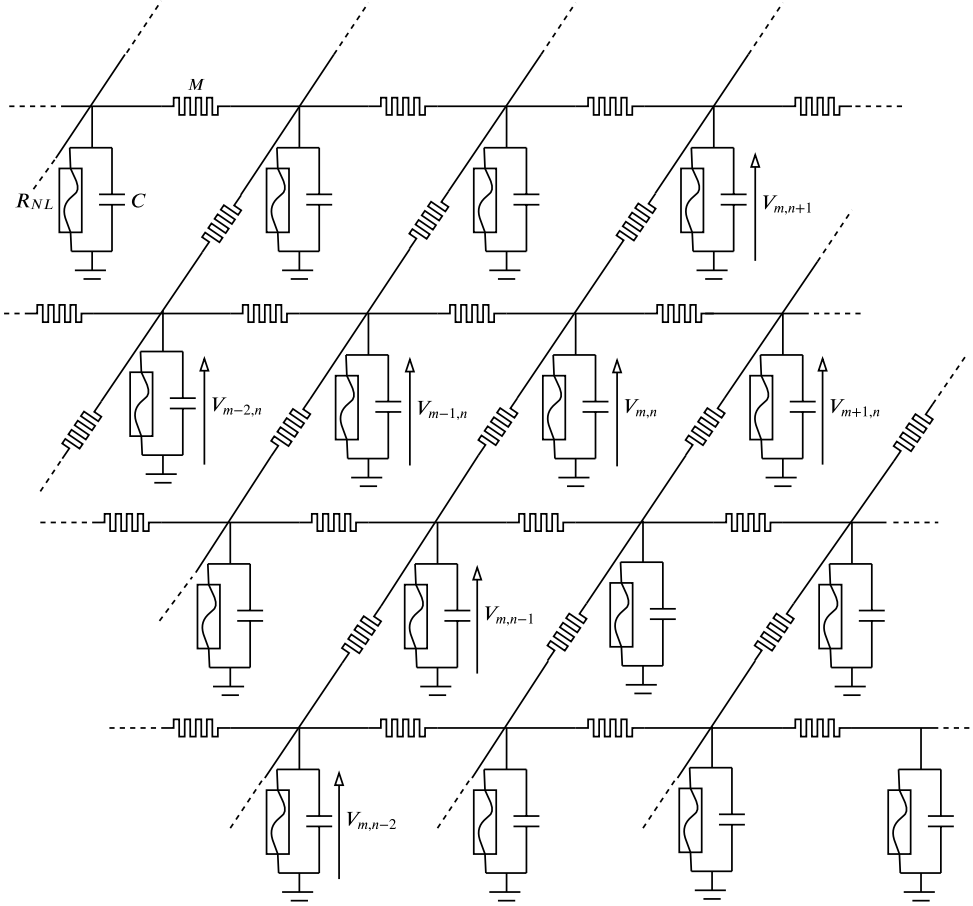

Figure 34. Memristor-based 2D Cellular Nonlinear Network with memristors in the coupling mode.

$$I_{NL_{(m,n)}} = f(V_{m,n}) = \frac{V_{m,n}}{R_o}\frac{(V_{m,n}-V_a)(V_{m,n}-V_b)}{V_aV_b}, \tag{71}$$

meanwhile the nonlinear resistance at this node $R_{NL_{(V_{m,n})}}$ is given by:

$$R_{NL_{(V_{m,n})}} = \frac{V_{m,n}}{I_{NL_{(m,n)}}} = \frac{R_oV_aV_b}{(V_{m,n}-V_a)(V_{m,n}-V_b)}, \tag{72}$$

and the corresponding potential energy $W(V_{m,n})$ becomes:

$$W(V_{m,n}) = \frac{1}{4}V_{m,n}^4 - \frac{V_a+V_b}{3}V_{m,n}^3 + \frac{V_aV_b}{2}V_{m,n}^2 + \mathscr{C}, \tag{73}$$

where $\mathscr{C}$ is a constant of integration. Meanwhile, the parameters V_a and V_b are the characteristic roots of the nonlinear resistance R_{NL}, as used previously in Fitzhugh Nagumo model and R_o is the linear approximation of R_{NL}, see Figure 35a. Unlike RC cells where each cell always stabilizes at 0, here the cell can stabilize at a point of lowest potential energy corresponding to $V_n = 0$ and $V_n = V_b$ (see Figure 35b) and these are the two

possible equilibrium states. Therefore: 0, V_a and V_b are constant voltages corresponding to the characteristic roots of the cubic function $f(V_n)$ at any nodal potential $V_{m,n}$ under consideration, such that: $0 < V_a < V_b$.

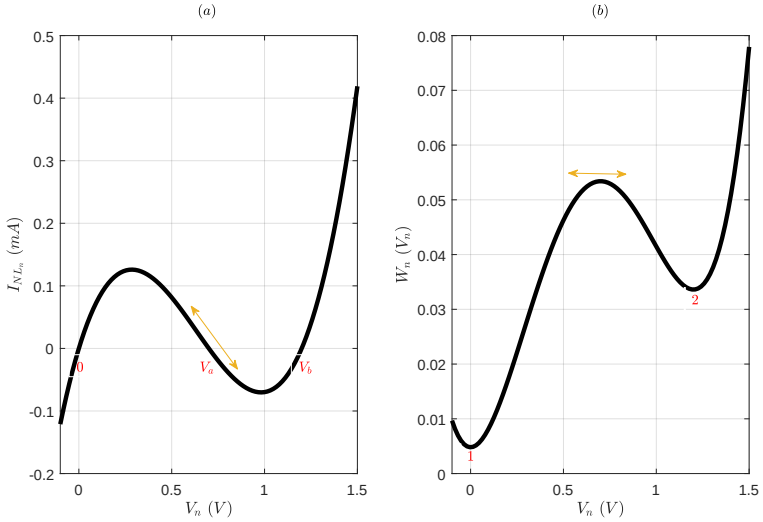

Figure 35. The response of the nonlinear current function and its corresponding potential energy.

Hence, with V_a being unstable potential state, it implies 0 and V_b are the only two stable states. For example, it can be seen from Figure 35b that, for: $V_b - 2V_a > 0$ the cell stabilizes at V_b and for: $V_b - 2V_a < 0$ the cell stabilizes at 0. With respect to the parameters under consideration, different analysis can be performed including the history of the memristor and its effect on image succession.

8. Discussion

The paper presented briefly the three familiar passive circuit elements (R, L and C) and the general description and philosophical argumentation of the fourth passive circuit element - the memristor (M). Memristor technologies are introduced, then followed by the details of the modeling analysis of TiO_2 memristor. According to the mode of excitation, the analytical solutions and results of linear and nonlinear dopant drift models are obtained. The difference between linear and nonlinear models is highly observable as the state variable of the system approaches 0 or 1. For a very small input voltage applied to the memristor, the linear and nonlinear models respond similarly because the state variable operates within the bulk of the device, not toward the edge [76]. The effect of increasing input frequency is shown for each model and the shrinkage of the pinched hysteresis loop area is due to the inverse relationship between the flowing charge $q(t)$ and the input frequency ω (i.e., $q(t) = \frac{I_o}{\omega}$). Furthermore, a new window function is presented, which is derived from the Hann window function. Its response is compared with the ones obtained from the three other functions by Strukov, Joglekar and Prodromakis. From a circuitry perspective, it was shown that the choice of window function is very important for memristor modeling, because each model responds differently due to the different level of imposed nonlinearities [76].

The model of TiO_2 memristor is used to create memristor components in SPICE for circuit simulation purposes. This approach is extended whereby analog components, such as an operational amplifier, are used to mimic the behavior of memristor in SPICE for simulation of memristor-based applications. The passive model of the memristor (Figure 30) operates under some restricted values of parameters in order to meet the conditions $I_R \ll I_D$ and the value of the cutoff frequency f_c. Therefore, we are working to improve this model by avoiding these limitations.

Using the relationship between the state variable x and the charge q, the memristance function is expressed as a function of the flowing charge. Memristor is normally modeled from its constitutive relationship between flux ϕ and charge q because the pinched hysteresis loop only describes its circuit response. A new model of memristor is presented, and due to its desirable continuity for all charges $q(t)$ flowing through the memristor, it is essentially vital in the study of memristor dynamics regarding the neuronal scheme especially when the memristor acts as a synapse.

In general, the advantages of the memristor outweighed its disadvantages and this can be seen in the potentiality of its outlined features in this paper. However, there are some concerns especially in its technology and modeling. For example, the TiO_2 memristor is the first reported two-terminal solid-state memristor, however, it is not yet available for purchase, though it bears a very handy mathematical description used widely to analyze some memristor-based applications. There could be some underlying issues of oxygen in the TiO_2 memristor preventing it from being readily available for purchase. Meanwhile, the SDC (KNOWM) memristor does not have a modeling equation to be used for SPICE circuit simulation of a memristor-based network prior to its implementation. It has been shown that each model responds differently from one another [76]. Therefore, one has to choose carefully the technology or model for use in a given application. Even though there are many in house metal-insulator-metal (MIM) memristors, the technological aspects need to be improved in order to meet the demand of this new and exciting component.

There is good progress in the development phase of a memristor-based networks especially in neuromorphic computing and memory applications. Memristor is able to store and process information at the same time, which in turn reduces power consumption, device circuitries and improve performance. Furthermore, this particular feature suggests the memristor to be a promising element as an alternative to Von Neumann architecture in avoiding the problems of memory-access bottleneck [159]. In fact, memristor brings an era of brain-like computing with some already in the implementation phase for practical realization.

The responses of the four basic passive circuit elements from the perspective of their circuitry are given in Appendix A. Hence, these elements are distinguishable from one another. Memristor may not be the fourth fundamental passive circuit element alongside the resistor, capacitor and inductor [18,19]. A simple test to identify an ideal memristor is presented [50]. According to this test, all the available memristors are resistive switching devices and an ideal memristor remains unlikely to be found [46]. Nevertheless, the contemporary memristor technologies are resistive switching devices, which can be categorized as a special class of memristive system owing to their pinched hysteresis loop characteristics, and they impart a massive technological impact in the twenty first century.

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Appendix A. Experimental Results Showing the Typical Voltage-Current Response of the Four Basic Passive Circuit Elements

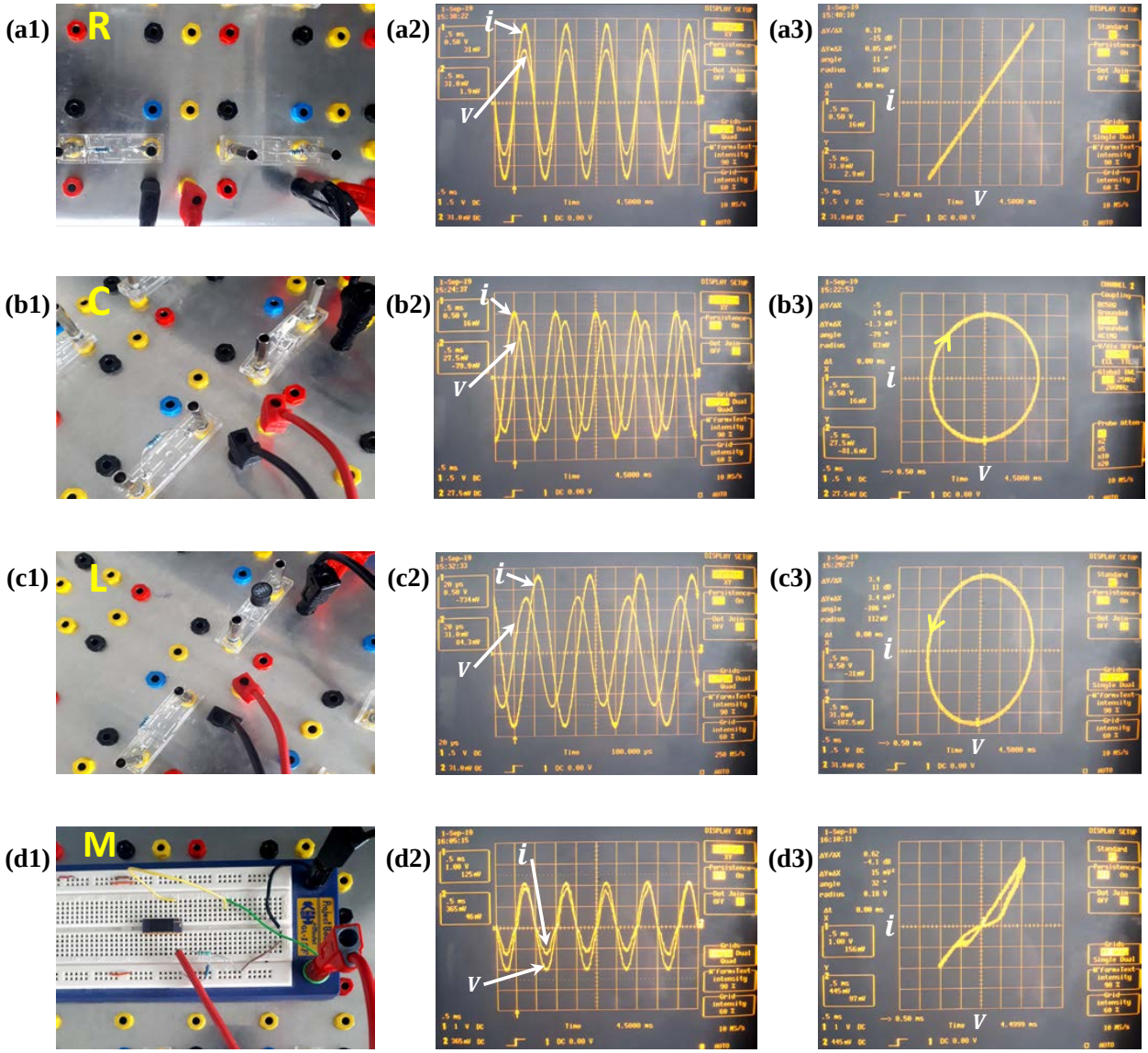

Figure A1. Experimental results of the four fundamental passive circuit elements. (**a1**–**a3**) $R = 1$ KΩ, (**b1**–**b3**) C = 10 nF, (**c1**–**c3**) L = 10 mH and (**d1**–**d3**) KNOWM memristor chip (see Figure 16). The current and voltage waveforms for each component are shown along with the corresponding I–V characteristics. There is no phase difference in $V(t)$ and $I(t)$ waveforms for R and M, while there is a phase difference of $\frac{\pi}{2}$ for C and L. In the capacitor C, $I(t)$ is leading the $V(t)$ by $\frac{\pi}{2}$ and in an inductor L, $V(t)$ is leading $I(t)$ by $\frac{\pi}{2}$. The I-V characteristic of R is a linear graph, for C and L it is a circle (respectively with clockwise and anticlockwise) and for M it is a pinched hysteresis loop. **Scales:** R: time t [0.50 ms/div], current I [0.31 mA/div] and voltage V [0.50 V/div], C: time t [0.50 ms/div], current I [0.28 mA/div] and voltage V [0.50 V/div], L: time t [20 µs/div], current I [0.31 mA/div] and voltage V [0.50 V/div] and M: time t [0.50 ms/div], current I [4.45 µA/div] and voltage V [1.0 V/div].

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