



Article

Tunnel Field-Effect Transistor: Impact of the Asymmetric and Symmetric Ambipolarity on Fault and Performance in Digital Circuits

Chiara Elfi Spano [†], Fabrizio Mo [†], Roberta Antonina Claudino, Yuri Ardesi , Massimo Ruoch ,
Gianluca Piccinini and Marco Vacca ^{*}

Department of Electronics and Telecommunication, Politecnico di Torino, 10129 Torino, Italy

^{*} Correspondence: marco.vacca@polito.it

[†] These authors contributed equally to this work.

Abstract: Tunnel Field-Effect Transistors (TFETs) have been considered one of the most promising technologies to complement or replace CMOS for ultra-low-power applications, thanks to their subthreshold slope below the well-known limit of 60 mV/dec at room temperature holding for the MOSFET technologies. Nevertheless, TFET technology still suffers of ambipolar conduction, limiting its applicability in digital systems. In this work, we analyze through SPICE simulations, the impact of the symmetric and asymmetric ambipolarity in failure and power consumption for TFET-based complementary logic circuits. Our results clarify the circuit-level effects induced by the ambipolarity feature, demonstrating that it affects the correct functioning of logic gates and strongly impacts power consumption. We believe that our outcomes motivate further research towards technological solutions for ambipolarity suppression in TFET technology for near-future ultra-low-power applications.

Keywords: TFET; ambipolarity; digital circuits; power dissipation; fault tolerance; band to band tunneling



Citation: Spano, C.E.; Mo, F.; Claudino, R.A.; Ardesi, Y.; Ruoch, M.; Piccinini, G.; Vacca, M. Tunnel Field-Effect Transistor: Impact of the Asymmetric and Symmetric Ambipolarity on Fault and Performance in Digital Circuits. *J. Low Power Electron. Appl.* **2022**, *12*, 58. <https://doi.org/10.3390/jlpea12040058>

Academic Editors: Costas Psychalinos, Nikos C. Sagias and Ioannis D. Moscholiou

Received: 4 October 2022

Accepted: 28 October 2022

Published: 31 October 2022

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



Copyright: © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

In the last 50 years, Moore's law has boosted the power-performance metrics of integrated circuits. Along with geometrical scaling, the Dennard scaling policy, which consists of scaling the supply and threshold voltage by about the same factor, led to a decrease in the switching power per transistor, such that the power density in a chip remained approximately constant from one technological node to the next. Nowadays, in deep sub-micron technological nodes, the Dennard scaling policy is no more applicable. Indeed, the threshold voltage cannot be further scaled; otherwise it results in an exponential increase in leakage power [1,2]. Consequently, the supply voltage cannot be scaled further without strongly impacting on the system performance. Thus, the power density is no more scaling proportionately, leading to the dark silicon era, characterized by the constraint that all the transistors on a chip cannot be simultaneously powered on at full performance [3].

In this scenario, steep-slope devices such as Tunnel Field-Effect Transistors (TFETs) have emerged as one of the most promising technologies to complement or replace CMOS in ultra-low-power applications [4–6], as several comparisons with CMOS demonstrate [7–12]. The TFETs exploit Band-To-Band Tunnelling (BTBT) as the main conduction mechanism, thus avoiding the Boltzmann-limited subthreshold swing of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). Therefore, TFET technology, thanks to its subthreshold slope below 60 mV/decade, is the key to keep on the scaling down of supply voltage below 0.5 V without affecting the gate over-drive and, thus, the device performance.

Although TFETs present also very low leakage current (I_{OFF}) below pA/ μm and an high ON/OFF current ratio I_{ON}/I_{OFF} [13,14], the low saturation current (I_{ON}) and ambipolarity features still prevent their applicability in low power and high-frequency systems.

The low I_{ON} of the order of hundreds of $\mu\text{A}/\mu\text{m}$ is due to the limited BTBT probability at the source-channel junction [4]. To improve the I_{ON} in these devices, possible solutions relying on bandgap engineering between source and channel, double-gate technology and also on hybrid circuits and increasing the gate-source voltage from a circuit design perspective, were proposed [15–19].

Another disadvantage in TFETs is the presence of ambipolar conduction. Ambipolarity is an intrinsic phenomenon of TFET technology where the conduction occurs for both positive and negative gate voltages. The ambipolar current I_{AMB} flows due to BTBT at the channel-drain junction for negative gate voltage for n -type TFET, and positive for p -type, making TFET technology unsuitable for complementary logic digital systems [19–21]. Even if the ambipolar conduction problem in complementary TFET (CTFET) logic is often mentioned in the literature when dealing with device-level engineering, there are still few studies about the specific circuit-level effects of ambipolar conduction and possible solutions to reduce it [19–24]. In particular, sometimes it is reported that ambipolarity can lead to circuit failure, but nothing is said about the effects in terms of circuit performance, even in the case of partially suppressed ambipolarity (i.e., when it does not produce evident system failure).

In this article, we consider and analyze a vertical AlGaSb/InAs heterojunction TFET demonstrated experimentally in [25]. Then, by employing the Verilog-A circuit model by Hao Lu et al. [26] we perform SPICE simulations in Cadence Virtuoso to analyze the impact of ambipolarity in malfunctions and power consumption in TFET-based logic gates. Indeed, since I_{AMB} is an additive contribution of leakage current, we expect it to cause non-negligible effects on the circuit power dissipation. Our results show that ambipolarity not only affect the correct functioning of logic gates but also strongly impacts on power consumption. These outcomes motivate further research towards technological solutions for ambipolarity suppression in TFET technology for ultra-low-power applications.

2. Theoretical Background and Modeling

2.1. TFET Working Principle

Figure 1 reports the n -type TFET basic structure and the relative band diagrams in its operating regions. The basic n -type TFET device is a p^+i-n^+ junction, with an heavily doped p -type source, an intrinsic or lightly doped channel and an heavily doped n -type drain. The channel is underneath the gate oxide and gate contact, that has the capability of shifting and controlling the channel electron bands to switch ON and OFF the device [4]. The p -type TFET presents complementary doping (n^+ source, intrinsic channel and p^+ drain) with a symmetric voltage device operating mode w.r.t. n -type TFET.

At thermal equilibrium—Figure 1b—the TFET is normally OFF. The Fermi level alignment assures extremely low thermionic leakages of electrons from drain to source and holes from source to drain [4]. The ON state operation is instead represented in Figure 1c. If a sufficiently positive gate voltage V_{GS} is applied (above the threshold), a large amount of electrons can tunnel from the source Valence Band (VB) to the channel Conduction Band (CB), and then by drift they proceed to the drain. Since the tunneling mechanism involves two different bands (VB at source side and CB at channel side) it is referred as Band-To-Band-Tunneling (BTBT). The BTBT phenomenon is indicated in Figure 1c with Φ_{BTBT} (orange arrow). The TFET threshold voltage V_{th} is conventionally defined as the required V_{GS} to have the channel CB edge aligned with the source VB edge, and thus as the onset of the BTBT conduction [4,20,21]. In OFF state (null or slightly negative V_{GS}) an applied drain voltage V_{DS} has the effect of lowering the drain side bands, with no electron flow happening since no available electron states are present in the intrinsic channel band gap for the source electrons to tunnel in—see Figure 1d. Nevertheless, for enough negative V_{GS} values the channel bands are shifted up and the channel VB becomes populated by the source electrons. In addition, BTBT can happen at drain side from the channel VB to the drain CB, resulting in a large and undesired current, referred as ambipolar current I_{AMB} [4,20,21]. The ambipolar state band diagram is depicted in Figure 1e, where Φ_{BTBT}

(orange arrow) indicates again the BTBT phenomenon. The onset of ambipolar conduction occurs when an enough negative V_{GS} aligns the channel VB edge to the drain CB edge. For more negative V_{GS} values the unwanted BTBT exponentially increases with the V_{GS} decrease. Indeed, the tunneling probability can be often calculated within the Wentzel–Kramer–Brillouin (WKB) approximation as [4,20,21]:

$$T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*E_g}}{3q\hbar(E_g + \Delta\zeta)}\right) \quad (1)$$

where: λ is the screening tunneling length, m^* is the electron effective mass, E_g is the channel band-gap, q is the elementary charge, \hbar is the reduced Planck's constant and $\Delta\zeta$ is the overlap of the energy bands, i.e., $E_V|_{source} - E_C|_{channel}$ in ON state and $E_V|_{channel} - E_C|_{drain}$ in ambipolar state. Since $\Delta\zeta$ is directly proportional to V_{GS} (through $-q$) the BTBT probability exponentially increases with the applied V_{GS} above the BTBT phenomenon onset.

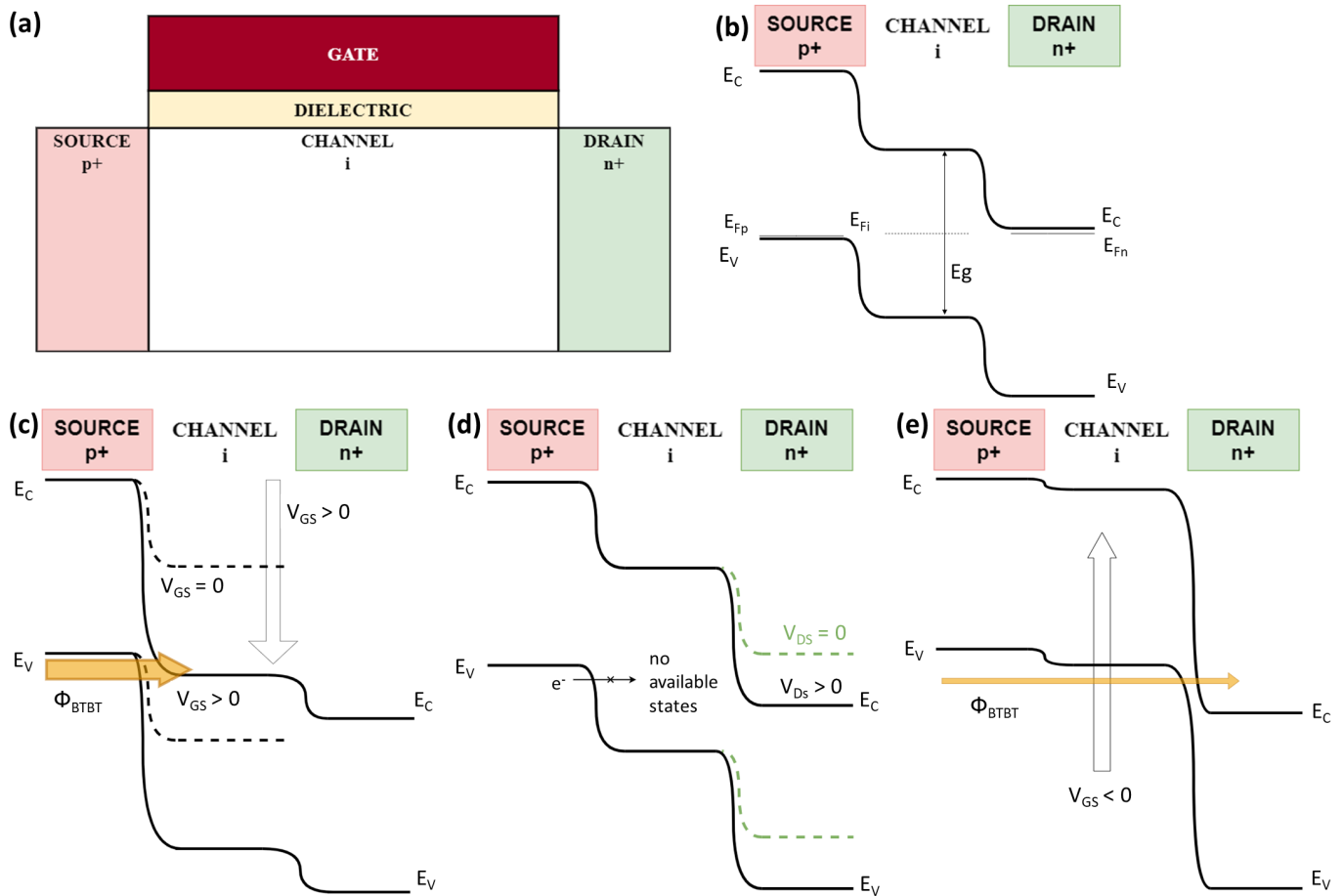


Figure 1. TFET device conceptual structure and operating principle. (a) Basic *n*-type TFET device structure; (b) equilibrium band diagram for the device in (a); (c) ON state band diagram for the device in (a); (d) OFF state band diagram for the device in (a); (e) ambipolar state band diagram for the device in (a).

An interesting peculiarity of TFETs is that it is not possible to have symmetric conduction for positive and negative V_{DS} . Indeed, while in MOSFETs the device structure is completely symmetric and permits to fully exchange source and drain in conduction, in TFETs this is not possible due to the asymmetric p^+-i-n^+ junction and relative longitudinal asymmetric band structure. Considering also the intrinsically dominant drain capacitance in TFETs and the difficulty in lowering the Miller's capacitive coupling in layout, the major resulting drawback is that some circuit nodes can overcome the supply voltage (also more than $2V_{DD}$) or reduce below ground during transients because of the poor capability of discharging capacitances in reversed V_{DS} operating mode [27,28].

2.2. Ambipolarity and Complementary Logic

The great success of digital circuits is established thanks to the principle of design by abstraction levels. Additionally, the usage of abstraction levels is well consolidated for complementary MOSFET (CMOS) logic design and corresponding optimized standard cells. An enormous advantage in TFET-based digital circuits, alongside the compatibility of TFET fabrication processes with CMOS ones, is the possibility of having complementary n -type and p -type devices with fully symmetric transcharacteristics $I_{DS}(V_{GS})$. Indeed, this permits inheriting the design principles and toolchain already developed for CMOS technology. This advantage permits to potentially switch to the novel TFET technology without the burden and the prohibitive cost related to the toolchain re-design, which is otherwise necessary if other kinds of logic are employed or developed for TFETs. Nevertheless, in the case of Complementary TFET (CTFET) logic, the pull-down network (n -type TFETs) and the pull-up network (p -type TFETs) can undergo negative/positive V_{GS} when in OFF states, provoking the undesired ambipolar conduction [20,21].

In this article, we are resolved to clarify the effects of ambipolarity conduction at the circuit level and on complementary digital circuits. In particular, we consider two different kinds of non-ideality effects in TFET transcharacteristics, both leading to an ambipolar conduction for negative/positive V_{GS} values in n -type/ p -type devices:

1. Ambipolar conduction can originate if the n -type (p -type) TFET device undergoes sufficiently negative (positive) V_{GS} , so that the channel VB edge is shifted above the drain CB edge, with drain-side BTBT, as described in Section 2.1. This is the case of Figure 2a in which various n -type TFET transcharacteristics with different ambipolar current values I_{AMB} are reported. In this case, all the transcharacteristics are centered in $V_{GS} = 0$ V, i.e., the minimum I_{DS} value (I_{OFF}) is the one obtained with $V_{GS} = 0$ V. We refer to this case as symmetric ambipolar TFET transcharacteristics, or, to lighten the notation, as the *symmetric ambipolarity* case.
2. In addition, there is the possibility of having non-fully symmetric transcharacteristics. Indeed, it is proved the TFET transcharacteristics to be very sensitive to gate metal workfunction choice, gate stack material engineering, gate fabrication process and variations [27,28]. The main effects is to obtain a shifted TFET transcharacteristic, as depicted in Figure 2b. The detrimental effect is that in normal operating conditions, the slightly negative V_{GS} is already capable of driving the TFET in ambipolar state. We refer to this case as asymmetric ambipolar TFET transcharacteristics, or, to lighten the notation, as the *asymmetric ambipolarity* case.

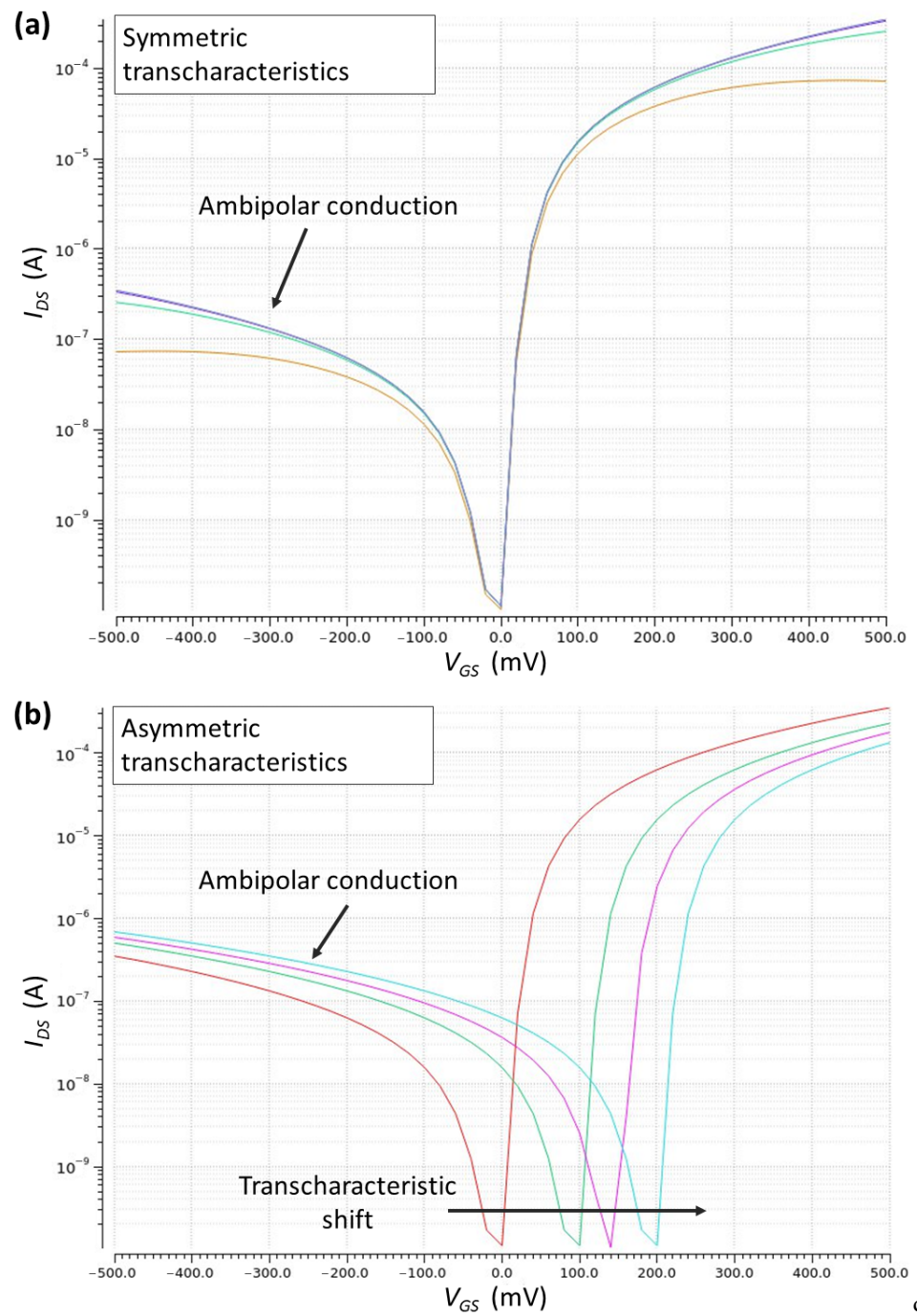


Figure 2. Examples of ambipolar n -type TFET transcharacteristics. (a) Example of TFET suffering of symmetric ambipolarity: symmetric transcharacteristics with different ambipolar currents; (b) Example of TFET suffering of asymmetric ambipolarity: asymmetric transcharacteristics with different shift w.r.t. ideal (red) one.

2.3. TFET Compact Model

In order to understand the effectiveness of an emerging technology, circuit and system-levels figures of merit need to be estimated and compared with current technology. With this purpose, a variety of compact and semi-empirical circuital models have been developed for novel technologies [29–32]. In this work, we employ the TFET compact model developed by Hao Lu et al., at the University of Notre Dame (Notre Dame, ID, USA) [26]. It is an analytical model based on the Kane–Sze formula for calculating the current-voltage characteristics under the WKB approximation. Moreover, the Notre Dame model is proved to represent the

real TFET device behavior well in all its operating conditions, including the ambipolar state. It is a continuous model in which the transition from a TFET operation state to another one happens with no discontinuity, thanks to a suitable mathematical function developed for this purpose. The model is implemented in Verilog-A and includes an empirical capacitive model to permit complete circuit simulations. Moreover, some model parameters should be fitted to experimental data to represent real devices. Of particular interest in this work is the dimensionless parameter s , that enables ambipolar conduction. The ambipolar current I_{AMB} is indeed represented as a scaled and shifted version of the ON current I_{DS} through the parameter s :

$$I_{AMB} = s \cdot I_{DS}(-V_{GS}, V_{DS}) \quad (2)$$

By comparison with the ON state current $I_{ON} = I_{DS}(V_{GS}, V_{DS})$, we notice that the V_{DS} dependence of I_{AMB} is the same as for the ON current. Instead, the V_{GS} dependence is modeled by reversing the sign of the applied V_{GS} . For $s = 0$, the ambipolar current results zero for all the (V_{GS}, V_{DS}) pairs. For increasing s values the ambipolar current increases up to the ON current value I_{ON} , obtained with $s = 1$.

3. Methodology

To investigate the effects of symmetric and asymmetric ambipolarity in realistic complementary logic digital circuits we consider the AlGaSb/InAs heterojunction TFET depicted in Figure 3, and we use Cadence Virtuoso with the Verilog-A Hao Lu model to simulate the CTFET logic circuits with such device.

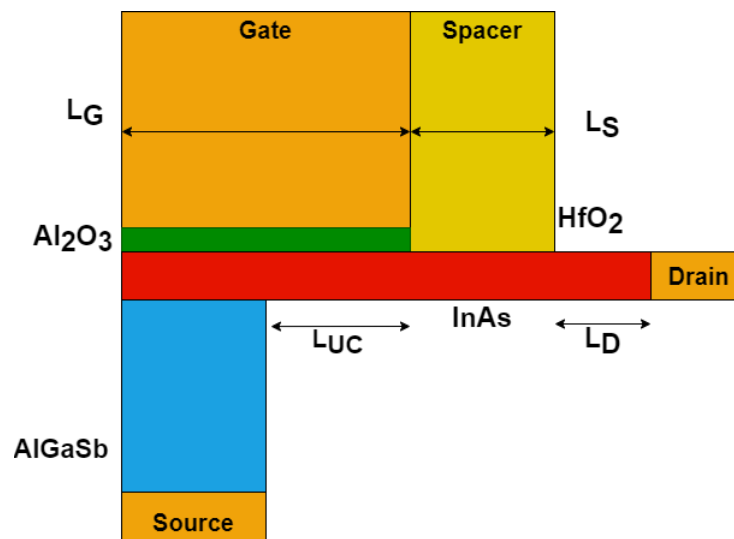


Figure 3. Structure of vertical AlGaSb/InAs heterojunction TFET. L_G is the gate length, L_S the spacer length, L_D the spacer-drain overlapping length, and L_{UC} the undercut length.

The Hao Lu model is proved to well match the experimental data for the considered AlGaSb/InAs TFET [26]. We set the Hao Lu model fitting parameters as indicated in [26] to have a perfect match of the considered AlGaSb/InAs TFET characteristics with the reference device, according to the Hao Lu provided model library [26,33]. The AlGaSb/InAs heterojunction is used to increase the BTBT efficiency from source to channel and thus improving the I_{ON} [4]. The high-k gate oxide is Al_2O_3 and the use of the undercut L_{UC} permits to achieve a steep subthreshold slope. The HfO_2 spacer with the gate-drain underlap is proved to suppress ambipolarity. This is possible through a reduced gate induced band bending at drain side, thanks to the spacer of length L_S , that reduces the gate-drain coupling. To correctly represent the ambipolar conduction resulting from experimental data the s should be set to $s = 10^{-3}$ [26]. Table 1 reports the device parameters that we employ in all our simulations. These parameters refer to the experimental device and to the library component of the Hao Lu model.

Table 1. Physical and geometrical parameters of the considered AlGaSb/InAs heterojunction TFET.

| Parameter Description | Value |
|--|------------------------------------|
| Metal gate workfunction | 4.93 eV |
| Al ₂ O ₃ thickness | 1.4 nm |
| AlGaSb source doping | $4 \times 10^{18} \text{ cm}^{-3}$ |
| Source δ doping plane doping | $6 \times 10^{12} \text{ cm}^{-3}$ |
| InAs channel doping | $5 \times 10^{17} \text{ cm}^{-3}$ |
| Gate length L_G | 20 nm |
| Undercut length L_{UC} | 10 nm |
| Spacer length L_S | 10 nm |
| Spacer-drain overlapping length L_D | 10 nm |

We consider complementary logic CMOS-like digital circuit topologies implemented with n -type and p -type AlGaSb/InAs TFETs. We assume a supply voltage V_{DD} of 0.5 V as predicted by the IRDS [6], and calculate the figures of Merit (FoM) of interest as follows:

- the ON current I_{ON} is calculated as the I_{DS} value with $V_{GS} = V_{DS} = V_{DD}$;
- the OFF current I_{OFF} is calculated as the I_{DS} value for $V_{GS} = 0$ and $V_{DS} = V_{DD}$;
- the threshold voltage V_{th} is calculated starting from its operative definition as the maximum of the second order derivative of the I_{DS} w.r.t. V_{GS} (maximum transconductance method);
- the Subthreshold-Slope (SS) is conventionally calculated as the inverse of the first order derivative I_{DS} w.r.t. V_{GS} in the subthreshold region;
- the Drain-Induced Barrier Lowering (DIBL) is calculated as:

$$DIBL = -\frac{V_{th}^{V_{DD}} - V_{th}^{V_{low}}}{V_{DD} - V_{low}} \quad (3)$$

where $V_{th}^{V_{DD}}$ and $V_{th}^{V_{low}}$ are the threshold voltages for V_{DS} equal to V_{DD} and to a low V_{DS} value V_{low} that we set equal to 0.05 V.

In addition, to evaluate the reliability of the investigated TFET-based logic gates, we quantify the noise margins of the logic gates. The noise margin for logic value ‘1’ (high) is defined as $\Delta V_H = V_{OH} - V_{IH}$, whereas the noise margin for logic value ‘0’ (low) as $\Delta V_L = V_{IL} - V_{OL}$, where:

- V_{OH} is the minimum output voltage for the logic value ‘1’ (high);
- V_{IH} is the minimum input voltage for the logic value ‘1’ (high);
- V_{IL} is the maximum input voltage for the logic value ‘0’ (low);
- V_{OL} is the maximum output voltage for the logic value ‘0’ (low).

These parameters are schematized in Figure 4.

Furthermore, we define and calculate the sensitivity S and the percentage sensitivity $S_{\%}$ of the quantity Q w.r.t. the parameter p as:

$$S = \frac{\partial Q}{\partial p} \approx \frac{\Delta Q}{\Delta p}, \quad S_{\%} = \frac{\partial Q}{\partial p} \cdot \frac{\bar{p}}{\bar{Q}} \cdot 100 \approx \frac{\Delta Q}{\Delta p} \cdot \frac{\bar{p}}{\bar{Q}} \cdot 100, \quad (4)$$

where \bar{p} and \bar{Q} are the nominal/average parameter and quantity, respectively. Finally, we calculate the average dissipated power by the entire logic gate of interest as:

$$P = \frac{1}{T} \int_0^T i_{DD}(t) \cdot V_{DD} dt \quad (5)$$

where $i_{DD}(t)$ is the total current provided by the supply line and T is the considered time interval, set equal to the time required to switch all possible input combinations in sequence with constant clock period of 0.5 ns.

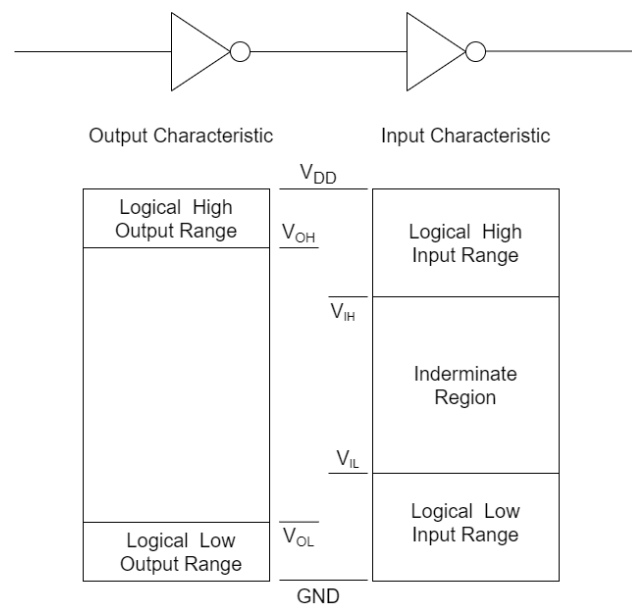


Figure 4. Logical parameters and noise margins definition.

To investigate the effect of symmetric ambipolarity we firstly consider the real ambipolarity present in the considered AlGaSb/InAs TFET, and then we arbitrarily also consider the cases in which $s = 1$ and $s = 0$. The first to understand the effect of an enhanced ambipolarity, leading to an I_{AMB} comparable with the I_{ON} of the device. The latter to understand the effect of a fully suppressed ambipolarity, i.e., $I_{AMB} = 0$. Even if the considered TFET device experimentally presents a partially suppressed ambipolarity ($s = 10^{-3}$), we believe a fair comparison should consider the same reference structure with different ambipolar conduction only ($s = 0$ and $s = 1$). Indeed, by considering different real devices, the structure would be different, making not possible to directly correlate the circuit-level results to the ambipolar conduction only, since many factors would influence it. Whereas, by considering exactly the same reference structure, with enhanced or suppressed ambipolarity leads to fair comparisons, with circuit performance results attributable to ambipolar conduction only.

Furthermore, to investigate the asymmetric ambipolarity effects on circuit functioning and performance, we shift the TFET transcharacteristics by adding a series DC voltage generator V_{shift} on the TFET gates. This has the effect of suitably shifting the TFET transcharacteristics of the desired amount as conceptually described in Figure 2b.

4. Results

Figure 5 shows the n-TFET transcharacteristic $I_{DS}(V_{GS})$ at drain-source voltage $V_{DS} = V_{DD} = 0.5$ V for different values of the symmetric ambipolarity parameter s . Note the suppression of the ambipolarity current I_{AMB} for the transcharacteristic having $s = 0$, and a substantial I_{AMB} comparable with the I_{ON} for the transcharacteristic having $s = 1$. Table 2 reports the main figures of Merit (FoM) for the n -type TFET device. Similar values are obtained with the p -type TFET, thanks to the full symmetry of the device. The TFET FoMs denote a superior device performance compared with commercial 3D MOSFET such as FinFETs and NS-GAAFETs [34–37]. In particular, the obtained subthreshold slope (SS) is well beyond the 60 mV/dec room temperature MOSFET limit, with also a very competitive DIBL [34,35]. As expected from the literature [4], the considered TFET also presents a poor I_{ON} , and a considerably reduced I_{OFF} value, around one order of magnitude less than MOSFET ones [34–37].

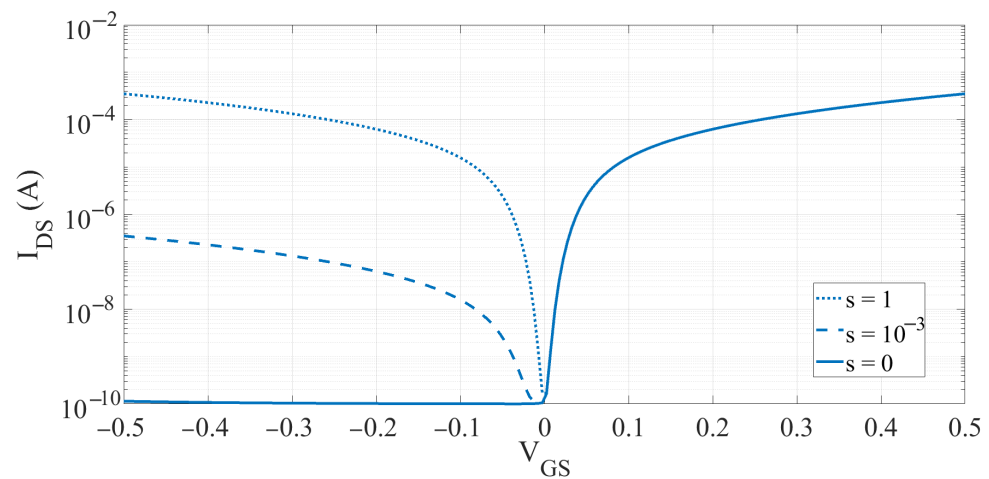


Figure 5. The device transcharacteristic $I_{DS}(V_{GS})$ at $V_{DS} = V_{DD}$ for different values of the s parameter.

Table 2. Calculated FoM for vertical AlGaSb/InAs heterojunction TFET.

| SS (mV/dec) | DIBL (mV/V) | I_{ON} (μ A) | I_{OFF} (pA) | I_{ON}/I_{OFF} |
|-------------|-------------|---------------------|----------------|--------------------|
| 13 | 11 | 351.19 | 111.22 | 3.16×10^6 |

4.1. Functional Verification

We verify the functionality of basic logic gates (NOT, XOR, NAND, NOR) and analyze what is the effect of asymmetric ambipolarity on their logic behavior. For all the logic gates, we perform DC and transient simulations by varying V_{shift} , which corresponds to considering different amount of asymmetric ambipolar conduction due to physical and geometrical parameter variations and to process variations, as mentioned in Section 2.1. In the following, we only show the most significant cases related to the digital inverter and NAND gate, where the ambipolarity strongly impact on their fault tolerances.

Figure 6 reports the Voltage Transfer Characteristic (VTC) $V_{OUT}(V_{IN})$ of the TFET-based inverter for null asymmetric ambipolarity $V_{shift} = 0$ (red line), and finite V_{shift} values (other colors). The V_{shift} value is varied up to 200 mV with a fixed step of 40 mV. All the VTCs present poor performances if compared with typical CMOS ones, with very low slopes, thus requiring a large transition region in which $V_{OUT} < V_{DD}$ (or $V_{OUT} > 0$) before (or after) the flex point at half of the dynamic voltage swing (0.25 V). Such a large transition region is primarily due to the poor driving strengths of the pull-up (p -type TFETs) and pull-down (n -type TFETs) networks. Indeed, because of the extremely low SS value, by sweeping the V_{IN} from ground to V_{DD} , a sharp increment of the sub-threshold currents of the OFF networks occurs, and the typical low TFET saturation current values do not compensate such rapid increase of leakage currents.

For finite values of V_{shift} , the asymmetric ambipolarity gradually affects the output voltage swing of the inverter, by reducing more and more its noise margins with increasing V_{shift} . For low V_{IN} values, the gradual increase of the asymmetric ambipolarity leads to strong increment of the subthreshold current of the pull-down n -type TFET enhancing its driving strength. Because of this, the p -type TFET becomes less effective in pulling up the output line at low values of V_{IN} . Analogous considerations hold for high values of V_{IN} close to V_{DD} : the strong increment of the subthreshold current of the pull-up p -type TFET enhances its driving strength and the n -type TFET becomes less effective in pulling down the output line. A more ideal behavior is instead recovered for greater/lower V_{IN} thanks to a compensation of V_{shift} by V_{IN} itself, causing the V_{OUT} increase/decrease before/after the transition at half of dynamic.

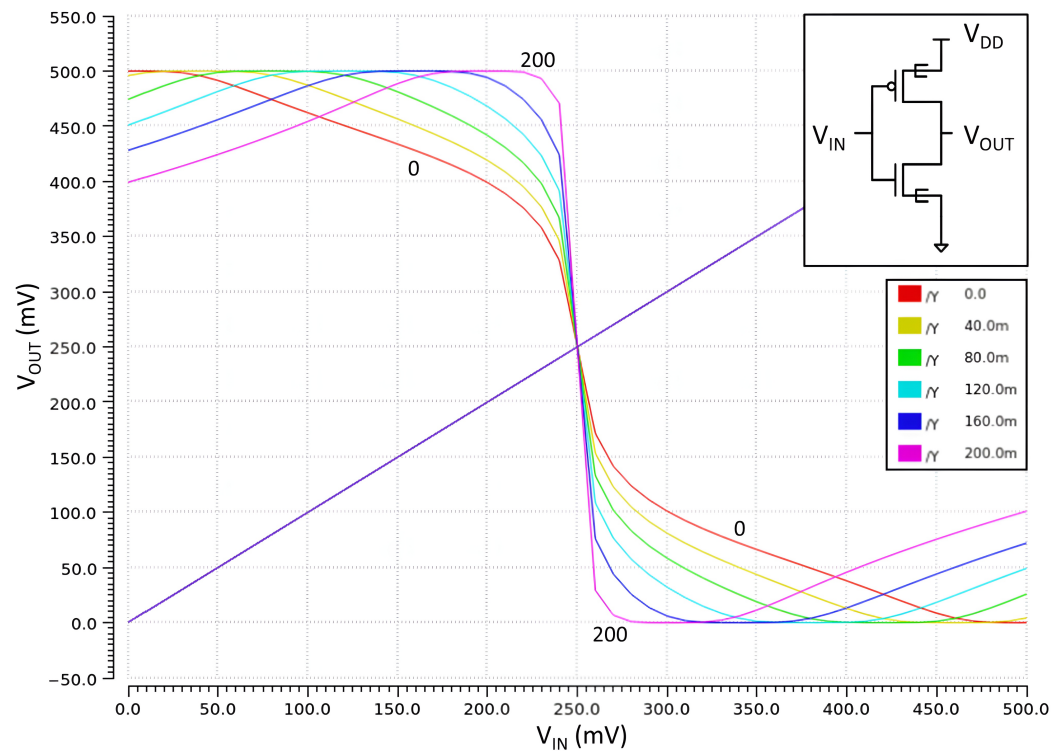


Figure 6. TFET-based inverter transcharacteristics at different V_{shift} values: red (null shift), yellow 40 mV, green 80 mV, light blue 120 mV, dark blue 160 mV, purple 200 mV. The blue straight line corresponds to the $V_{OUT} = V_{IN}$ straight line. The top-right inset shows the CTFET inverter schematic.

Figure 7 reports the transient simulation of the TFET-based digital inverter for different values of V_{shift} . The evident voltage peaks in the output signals are typical of TFET technology [28], and they are due to the asymmetric TFET structure, as mentioned in Section 2.1. Indeed, while in CMOS technology the symmetric conduction of MOSFETs for both positive and negative V_{DS} permits to discharge capacitively coupled lines, for TFETs this does not happen since a reversed V_{DS} leads to poor TFET conduction and thus long time intervals to dissipate the extra charge [28]. In the inverter case, the output voltage transients are short compared with the supposed clock period (i.e., 0.5 ns), nevertheless they are quite marked with maximum peaks that exceed V_{DD} of 200 mV, i.e., 40% of the V_{DD} itself (analogously for ground with -200 mV reached).

From the inspection of the output voltage dynamic evolution we notice that the effect of the asymmetric ambipolarity is to deteriorate the inverter output logic values '1' (V_{OH}) and '0' (V_{OL}). Table 3 report the V_{OH} and V_{OL} values sampled at steady state and the noise margins ΔV_H , ΔV_L of the inverter obtained as described in Section 3 by supposing the input characteristic in Figure 4 not affected by asymmetric ambipolarity ($V_{shift} = 0$) and choosing the input logic values $V_{IH} = 450$ mV and $V_{IL} = 50$ mV, for which an acceptable reduction of the output logic values occurs—Figure 6. The monotonic decrement of V_{OH} and increment of V_{OL} , reported in Table 3 are the causes of the steep reduction of the noise margins for increasing V_{shift} . For suppressed asymmetric ambipolarity the noise margins for low and high logic values results about 50 mV, whereas for $V_{shift} = 80$ mV they are almost halved. This 50% reduction potentially causes metastability and misinterpretation of the logic values when propagating throughout cascaded logic gates. The noise margins obtained for $V_{shift} \geq 120$ mV are almost null and then negative, thus unacceptable for the propagation of the digital information, since the discrimination between the two logic values is no longer possible, and placing cascaded logic gates would cause a failure. This results is better highlighted in Figure 8, in which the percentage noise margins are reported in function of the V_{shift} values.

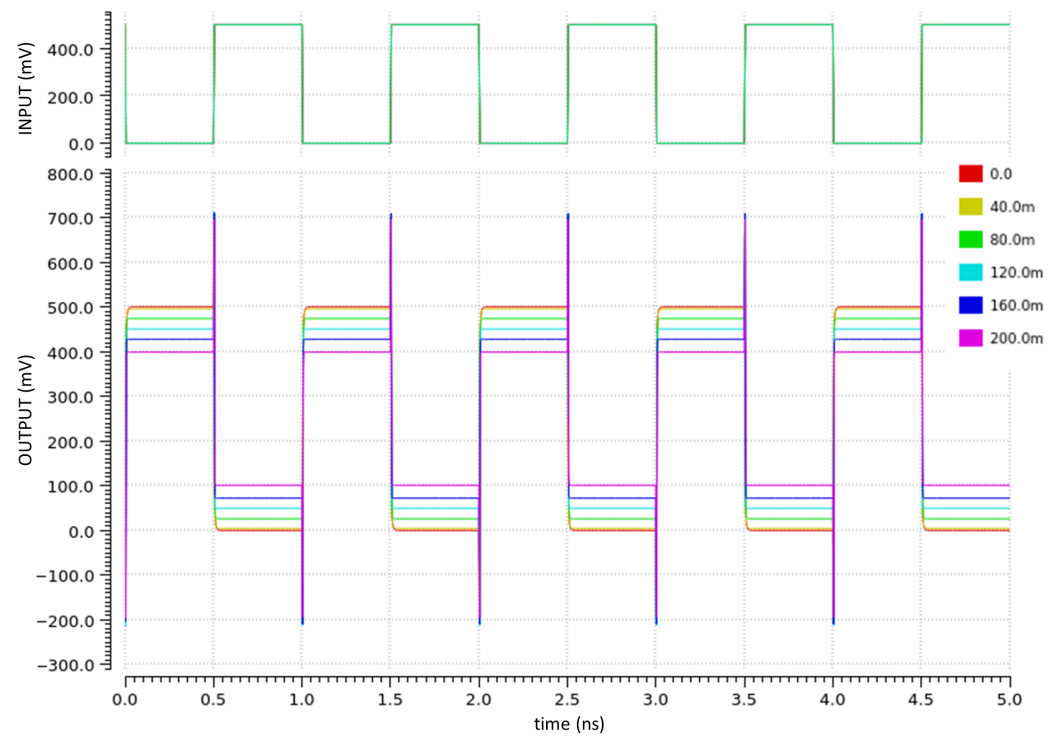


Figure 7. Transient simulation of the TFET-based digital inverter for different values of V_{shift} : red (null shift), yellow 40 mV, green 80 mV, light blue 120 mV, dark blue 160 mV, purple 200 mV. The green signal is the input signal.

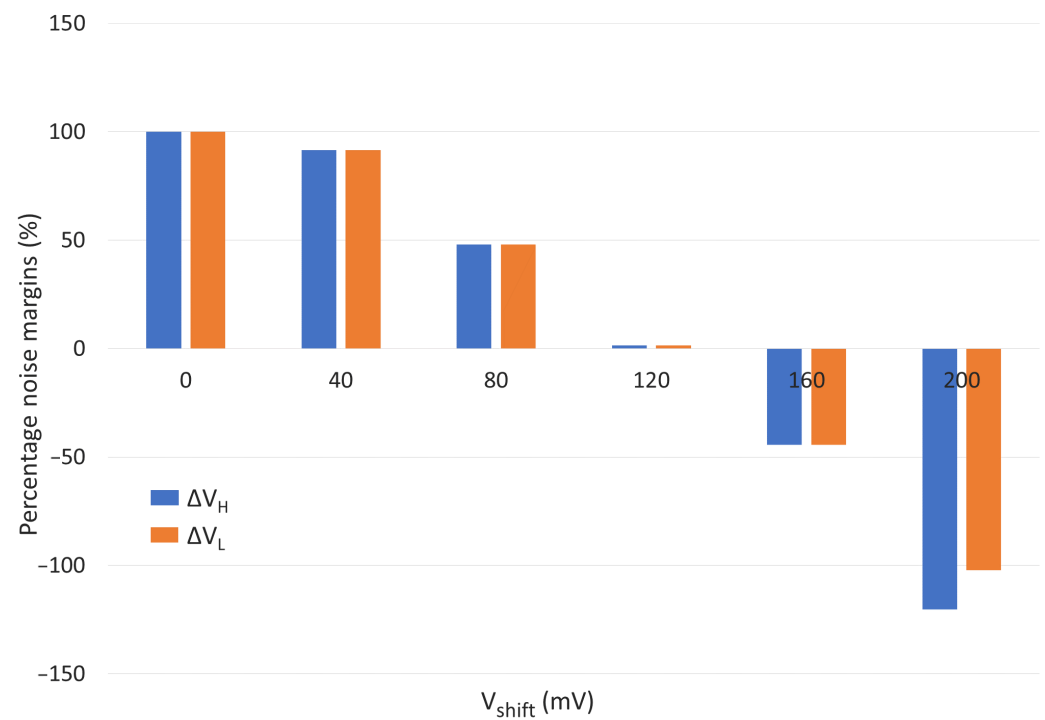
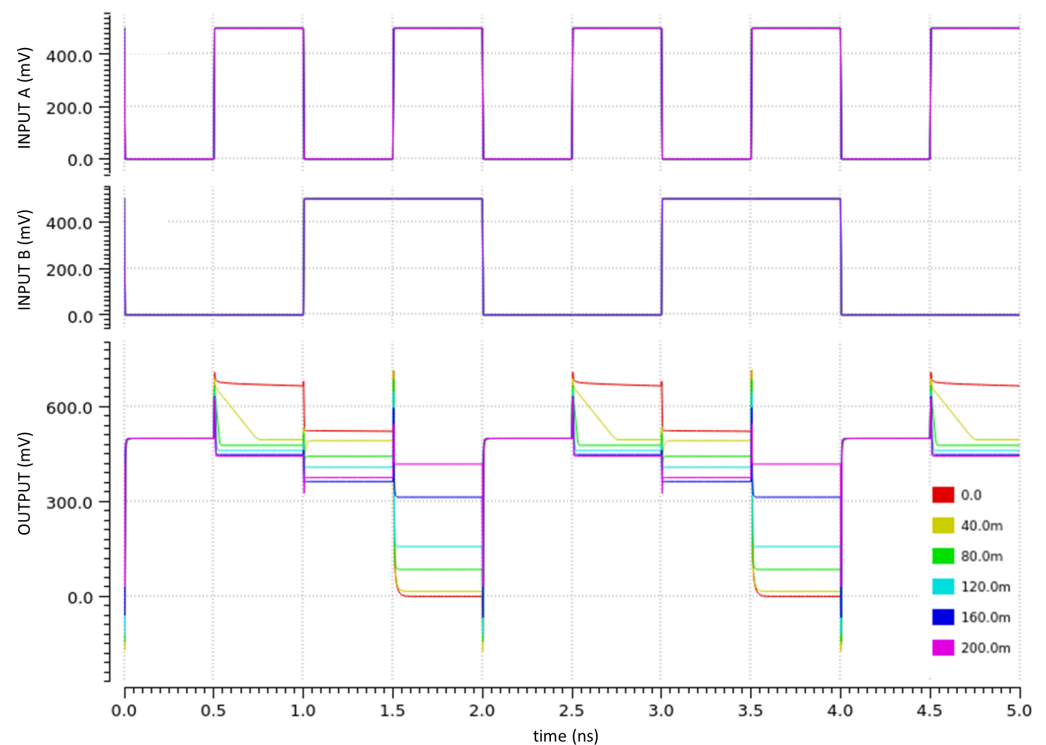


Figure 8. Noise margins percentage of TFET-based inverter as function of different values of V_{shift} . The orange bar represents the percentage noise margin for low logic value, whereas the blue one the reduction of noise margin for high logic value.

Table 3. Output logic values and noise margin of the TFET-based inverter as a function of the asymmetric ambipolarity parameter V_{shift} .

| | Inverter Output Values and Noise Margins (mV) | | | | | |
|--------------|---|---------|---------|---------|---------|---------|
| | $V_{shift} = 0$ mV | 40 mV | 80 mV | 120 mV | 160 mV | 200 mV |
| V_{OH} | 499.992 | 495.742 | 474.057 | 450.711 | 427.853 | 389.934 |
| V_{OL} | 0.008 | 4.258 | 25.942 | 49.289 | 72.146 | 101.066 |
| ΔV_H | 49.992 | 45.742 | 24.057 | 0.711 | −22.147 | −60.066 |
| ΔV_L | 49.992 | 45.742 | 24.058 | 0.711 | −22.146 | 51.066 |

In the following, we also show the effect of asymmetric ambipolarity on NAND gate functioning, and we consider again different values of V_{shift} . The transient simulation of the NAND gate is reported in Figure 9, in which all the possible combinations of inputs are tested. As in the case of the CTFET inverter also the CTFET NAND gate presents output voltage spikes beyond the V_{DD} and below the ground. Nevertheless, for the logic input combination $A = 1$ and $B = 0$ the output node is kept at a voltage value well beyond V_{DD} for all the clock period, showing a slow exponential decay trend. A similar situation, but much less marked, is present also for the $A = 0$ and $B = 1$ case. The reasons are again related to the TFET impossible asymmetric conduction w.r.t. the sign of V_{DS} , that permits extra charge discharging only through the drain to source small leakage paths [28].

**Figure 9.** NAND gate time transient simulation with different TFET transcharacteristic shift values: red (no shift), yellow 40 mV, green 80 mV, light blue 120 mV, dark blue 160 mV, purple 200 mV.

Concerning instead the effect of the asymmetric ambipolarity, in the case of $V_{shift} = 0$ (suppressed asymmetric ambipolarity) no relevant malfunctioning of the NAND gate occurs, meaning that, analogously to the inverter case, the symmetric ambipolarity does not affect the gate functioning. This is true for all the combinations of the input. Instead, for finite V_{shift} values, there is a significant noise margin reduction, with noticeable failures for large V_{shift} values. Therefore, the asymmetric ambipolarity induces behavioral malfunctions in the NAND gate, making it unusable for logical and arithmetic operations. We report some output voltage values of interest in Table 4—low logic level ‘0’ should be

ground (0 V), high logic value ‘1’ should be V_{DD} (500 mV). A significant reduction in noise margins already occur at $V_{shift}=80$ mV, with noise margins preventing cascading stages at $V_{shift} = 120$ mV. The NAND gate does not provide correct logic behavior for V_{shift} larger than 160 mV.

Table 4. Output voltage in mV for the two-input NAND gate for the considered V_{shift} values. A and B are the two inputs of the NAND gate, logic 0 is encoded through a 0 V voltage value while logic 1 is encoded through an 500 mV voltage value. The chosen input combinations highlight the NAND malfunctioning when V_{shift} is increased.

| | NAND Output Voltage (mV) | | | | | |
|-------------|--------------------------|--------|--------|--------|--------|--------|
| | $V_{shift} = 0$ mV | 40 mV | 80 mV | 120 mV | 160 mV | 200 mV |
| A = 0 B = 1 | 523.07 | 492.85 | 443.06 | 409.11 | 362.88 | 376.23 |
| A = 1 B = 1 | 24.28×10^{-3} | 16.22 | 85.34 | 157.51 | 313.86 | 418.44 |

4.2. Power Analysis

We separately investigate the effect of symmetric and asymmetric ambipolarity on dissipated power in the basic CTFET logic cells. Table 5 reports the total average dissipated power, calculated with Equation (5), in function of V_{shift} for the basic two-input logic gates NAND, NOR, XOR and for the Full Adder (FA). The s parameter is fixed at $s = 10^{-3}$ in all cases. As V_{shift} increases the power consumption increases more than linearly. For example, concerning the NAND gate, by passing from $V_{shift} = 0$ to $V_{shift} = 40$ mV the power consumption is doubled, while from $V_{shift} = 40$ mV to $V_{shift} = 80$ mV it increases of more than seven times and from $V_{shift} = 80$ mV to $V_{shift} = 160$ mV it increases of four times. We attribute this trend to the exponential increasing ambipolar current values that replace the OFF current values when the transcharacteristics are shifted with increasing V_{shift} -refer to Equation (1) and the discussion in Section 2.1.

Furthermore, we calculate the percentage sensitivity $S_{V_{shift}}^{\%}$ of the dissipated power w.r.t. V_{shift} starting from the definition of Equation (4) by exploiting the approximation reported in Equation (4). In particular, to extract the $S_{V_{shift}}^{\%}$ values, we interpolate the simulated data sets of Table 5 with straight lines (first order polynomial function) and we assume the angular coefficients of the best fitting straight line (in the least-squares sense) to be equal to $S_{V_{shift}}^{\%}$ (after normalization and multiplication by 100). The interpolations are reported in Figure 10, and the obtained sensitivity values $S_{V_{shift}}^{\%}$ are reported in Table 6. The minimum power consumption sensitivity to the asymmetric ambipolarity is obtained with the NAND gate, with a sensitivity of 17.66%. The sensitivity dramatically increases for more complex logical circuits (XOR and FA), achieving also the 182.52% for the FA case. The greater is the total power consumption of the considered logic gate (from NAND to FA) the larger is also the slope of the interpolating line, i.e., the sensitivity to V_{shift} , and the circuit total power consumption dependence on V_{shift} is dramatically increased if the considered digital architecture dissipates on average more power. In other words, the greater the power consumption, the greater the V_{shift} sensitivity of the dissipated power from the considered digital block.

Table 5. Total power dissipation depending on the asymmetric ambipolarity for parameter V_{shift} .

| | Total Power (μ W) | | | | | |
|------|------------------------|----------------------|-------|--------|--------|--------|
| | $V_{shift} = 0$ mV | 40 mV | 80 mV | 120 mV | 160 mV | 200 mV |
| NAND | 413×10^{-3} | 1.04 | 7.76 | 18.24 | 31.61 | 29.41 |
| NOR | 464×10^{-3} | 957×10^{-3} | 4.91 | 20.92 | 36.53 | 37.02 |
| XOR | 2.32 | 5.42 | 31.29 | 73.56 | 117.40 | 152.46 |
| FA | 11.67 | 18.03 | 95.18 | 203.70 | 277.90 | 345.10 |

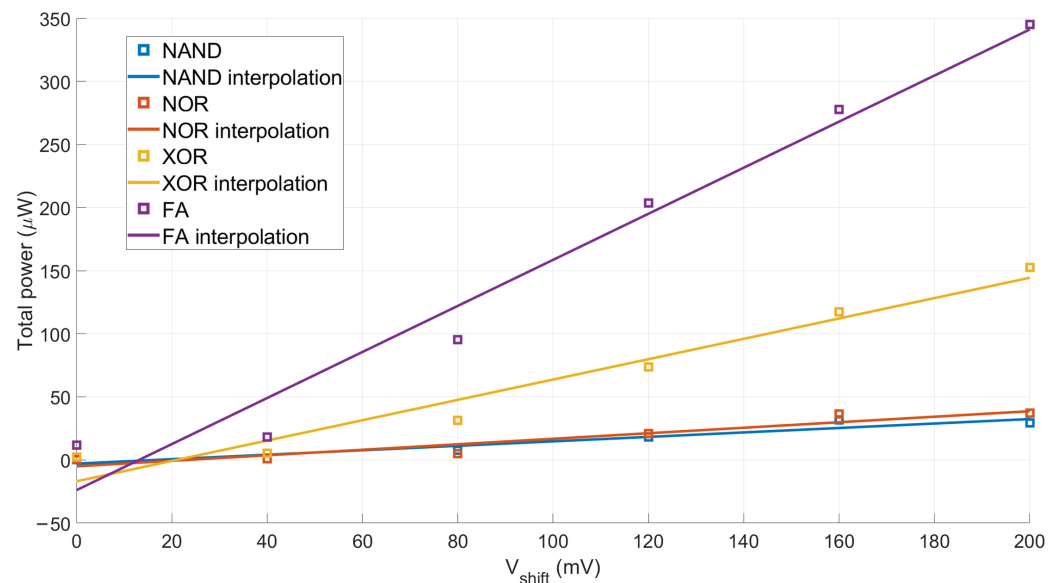


Figure 10. Total dissipated power for the basic logic gates as a function of V_{shift} . The markers are the simulated data, the straight lines are the first order polynomial interpolations (least-squares sense). The negative power values obtained for small V_{shift} values-below 20 mV-are artifacts due to the interpolation through a linear polynomial function.

Table 6. Total dissipated power percentage sensitivity to V_{shift} , indicated with $S_{V_{shift}}^{\%}$.

| | NAND | NOR | XOR | FA |
|----------------------|--------|--------|--------|---------|
| $S_{V_{shift}}^{\%}$ | 17.66% | 21.82% | 80.64% | 182.52% |

We then consider the effect of the symmetric ambipolarity on the total dissipated power. In this case, we consider only symmetric TFET transcharacteristics, i.e., we fix $V_{shift} = 0$, whereas we vary the magnitude of the symmetric ambipolar conduction by changing s from 0 to 10^{-3} to 1. The results are reported in Table 7. For all the considered digital cells the power consumption significantly increases when s is increased. In particular, it dramatically increases of around one order of magnitude when s is increased from 0 (no ambipolarity) to 10^{-3} (suppressed ambipolarity) for the NAND and the NOR gates. Then by further increasing s from 10^{-3} (suppressed ambipolarity) to 1 (full ambipolar device) only a slight increase occurs. This trend is well highlighted in Figure 11, where the increase in dissipated power from the case of $s = 10^{-3}$ to the case of $s = 1$ is not appreciable.

Table 7. Total power dissipation depending on the asymmetric ambipolarity for parameter s .

| | Total Power (μW) | | |
|------|------------------------|-------------------------|-------------------------|
| | $s = 0$ | $s = 0.001$ | $s = 1$ |
| NAND | 41.60×10^{-3} | 412.30×10^{-3} | 413.00×10^{-3} |
| NOR | 32.73×10^{-3} | 463×10^{-3} | 464×10^{-3} |
| XOR | 1.92 | 2.30 | 2.32 |
| FA | 5.46 | 10.27 | 11.67 |

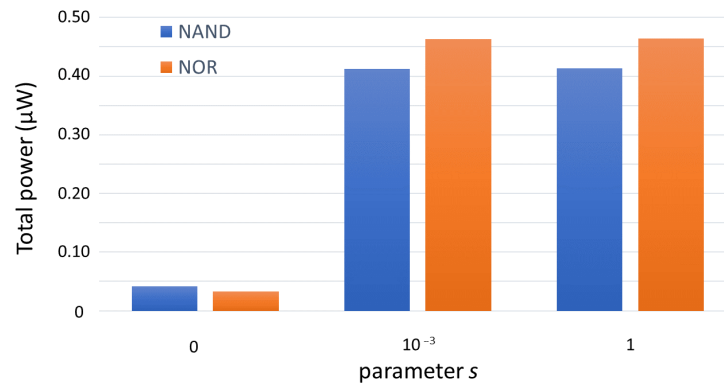


Figure 11. Total power dissipation in function of the amount of symmetric ambipolarity (s value) for the NAND and the NOR gates.

Similar considerations hold for more complex digital cells, namely the XOR and the FA. Nevertheless, we notice that for more complex cells, the increase in power consumption, due to s increase from 0 to 10^{-3} , is much less marked than for the simpler NAND and NOR cells, as reported in Figure 12. Thus, we separately calculate the dissipated power sensitivity through Equation (4) for all the considered gates for the s increase from 0 to 10^{-3} and for the s increase from 10^{-3} and then to 1. We call the first $S_{s:0 \rightarrow 10^{-3}}^{\%}$ and the latter $S_{s:10^{-3} \rightarrow 1}^{\%}$ and we report the result in Table 8. The sensitivity to ambipolar current magnitude is extremely larger for s passing from 0 to 10^{-3} than for s passing from 10^{-3} to 1. Even if more complex digital blocks present reduced sensitivity to s , the trend is confirmed. Because of the direct proportionality of I_{AMB} to s (see Equation (2)) our results reflect in the following: an I_{AMB} three orders of magnitude lower than I_{ON} values is still leading to important non-ideality power consumption and the dissipated power is very sensitive to I_{AMB} , thus also small reductions of I_{AMB} will result in large power consumption reduction.

Table 8. Total dissipated power percentage sensitivity to s parameter.

| | NAND | NOR | XOR | FA |
|------------------------------------|-----------------------|-----------------------|---------------------|---------------------|
| $S_{s:0 \rightarrow 10^{-3}}^{\%}$ | $1.633 \times 10^5\%$ | $1.736 \times 10^5\%$ | $1.8 \times 10^4\%$ | $611 \times 10^4\%$ |
| $S_{s:10^{-3} \rightarrow 1}^{\%}$ | 0.17% | 0.22% | 0.87% | 12.77% |

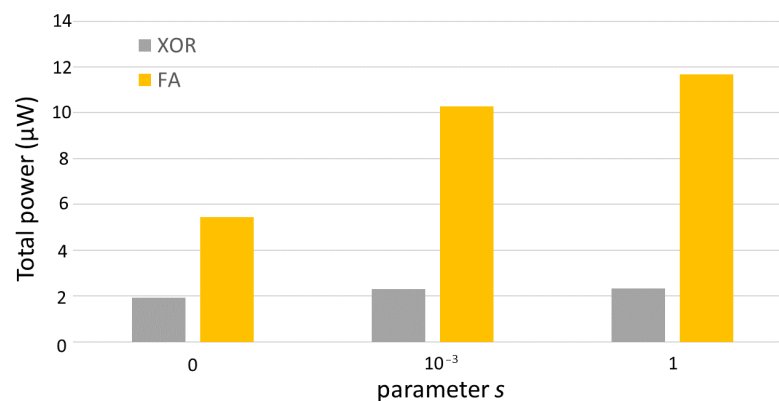


Figure 12. Total power dissipation in function of the amount of symmetric ambipolarity (s value) for the XOR and the FA digital circuits.

5. Conclusions

We investigated through Cadence Virtuoso SPICE simulations the effect of the symmetric and asymmetric ambipolar transcharacteristics in TFET-based complementary logic

circuits. We modeled the asymmetric ambipolarity through a DC voltage generator V_{shift} on the TFET gates, to emulate the transcharacteristics shift, whereas we exploited the s parameter employed in Hao Lu Verilog-A model to account for the effect of the symmetric ambipolarity.

Our results show that symmetric ambipolarity has small effect on complementary logic circuit functioning, while asymmetric ambipolarity, if not kept under control, can lead to strong reduction of noise margins and evident behavioral failure.

Alongside behavioral analysis of circuits we also analyzed the effects of ambipolarity on dissipated power in digital circuits. In this case both the symmetric and asymmetric ambipolarity lead to relevant power performance deterioration. Asymmetric ambipolarity doubles the dissipated power for almost all the considered basic logic circuits, already for few tens of mV of transcharacteristic shift. We verified that the digital circuit dissipated power sensitivity to asymmetric ambipolarity increases with system complexity. In the case of symmetric ambipolarity, the dissipated power sensitivity to I_{AMB} is extremely high for small variations of I_{AMB} when it is order of magnitudes lower than the I_{ON} , whereas the system is less sensible to I_{AMB} variations when I_{AMB} approaches I_{ON} values. Therefore, even small reductions in I_{AMB} can significantly reduce the dissipated power in complementary TFET digital circuits.

We believe our work to clarify the effects of ambipolar conduction on logic failure and power performance of complementary digital circuits based on TFET technology. Moreover, we believe it to motivate future technological efforts to further suppress the ambipolar current in TFETs and to keep under control the TFET transcharacteristic shift due to inaccurate gate engineering and fabrication process variations.

Author Contributions: Conceptualization, G.P., M.V., C.E.S., F.M. and Y.A.; methodology, R.A.C., F.M. and C.E.S.; software/simulations, R.A.C.; formal analysis, C.E.S. and F.M.; investigation, R.A.C., C.E.S. and F.M.; resources, M.R.R. and M.V.; data curation, R.A.C.; writing—original draft preparation, F.M. and C.E.S.; writing—review and editing, Y.A., G.P. and M.V.; visualization, C.E.S. and F.M.; supervision, G.P., M.V., F.M., C.E.S. and Y.A.; project administration, Y.A., G.P., M.V. and M.R.R.; internal funding acquisition, G.P. and M.R.R. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: All the needed data are reported in the article.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Taur, Y.; Ning, T.H. *Fundamentals of Modern VLSI Devices*, 2nd ed.; Cambridge University Press: Cambridge, UK, 2009. [\[CrossRef\]](#)
2. Roy, K.; Prasad, S. *Low-Power Cmos Vlsi Circuit Design*; Wiley India Pvt. Ltd.: New Delhi, India, 2009.
3. Shafique, M.; Garg, S.; Henkel, J.; Marculescu, D. The EDA Challenges in the Dark Silicon Era: Temperature, Reliability, and Variability Perspectives. In Proceedings of the 51st Annual Design Automation Conference, San Francisco, CA, USA, 1–5 June 2014; Association for Computing Machinery: New York, NY, USA, 2014; pp. 1–6. [\[CrossRef\]](#)
4. Ionescu, A.M.; Riel, H. Tunnel field-effect transistors as energy-efficient electronic switches. *Nature* **2011**, *479*, 329–337. [\[CrossRef\]](#) [\[PubMed\]](#)
5. Seabaugh, A.C.; Zhang, Q. Low-Voltage Tunnel Transistors for Beyond CMOS Logic. *Proc. IEEE* **2010**, *98*, 2095–2110. [\[CrossRef\]](#)
6. *International Roadmap for Devices and Systems—Executive Report*; IEEE: Piscataway, NJ, USA, 2021.
7. Aswathy, M.; Biju, N.M.; Komaragiri, R. Comparison of a 30nm Tunnel Field Effect Transistor and CMOS Inverter Characteristics. In Proceedings of the 2013 Third International Conference on Advances in Computing and Communications, Cochin, India, 29–31 August 2013; pp. 149–152.
8. Núñez, J.; Avedillo, M.J. Comparison of TFETs and CMOS Using Optimal Design Points for Power–Speed Tradeoffs. *IEEE Trans. Nanotechnol.* **2017**, *16*, 83–89. [\[CrossRef\]](#)
9. Rendón, M.; Cao, C.; Landázuri, K.; Garzón, E.; Prócel, L.M.; Taco, R. Performance Benchmarking of TFET and FinFET Digital Circuits from a Synthesis-Based Perspective. *Electronics* **2022**, *11*, 632. [\[CrossRef\]](#)

10. Strangio, S.; Settino, F.; Palestri, P.; Lanuzza, M.; Crupi, F.; Esseni, D.; Selmi, L. Digital and analog TFET circuits: Design and benchmark. *Solid-State Electron.* **2018**, *146*, 50–65. [\[CrossRef\]](#)
11. Strangio, S.; Palestri, P.; Lanuzza, M.; Crupi, F.; Esseni, D.; Selmi, L. Assessment of InAs/AlGaSb Tunnel-FET Virtual Technology Platform for Low-Power Digital Circuits. *IEEE Trans. Electron Devices* **2016**, *63*, 2749–2756. [\[CrossRef\]](#)
12. Lu, H.; Paletti, P.; Li, W.; Fay, P.; Ytterdal, T.; Seabaugh, A. Tunnel FET Analog Benchmarking and Circuit Design. *IEEE J. Explor.—Solid-State Comput. Devices Circuits* **2018**, *4*, 19–25. [\[CrossRef\]](#)
13. Knoll, L.; Zhao, Q.T.; Nichau, A.; Trellenkamp, S.; Richter, S.; Schäfer, A.; Esseni, D.; Selmi, L.; Bourdelle, K.; Mantl, S. Inverters With Strained Si Nanowire Complementary Tunnel Field-Effect Transistors. *IEEE Electron Device Lett.* **2013**, *34*, 813–815. [\[CrossRef\]](#)
14. Tomioka, K.; Yoshimura, M.; Fukui, T. Steep-slope tunnel field-effect transistors using III–V nanowire/Si heterojunction. In Proceedings of the 2012 Symposium on VLSI Technology (VLSIT), Honolulu, HI, USA, 12–14 June 2012; pp. 47–48. [\[CrossRef\]](#)
15. Bhuwarka, K.; Schulze, J.; Eisele, I. Scaling the vertical tunnel FET with tunnel bandgap modulation and gate workfunction engineering. *IEEE Trans. Electron Devices* **2005**, *52*, 909–917. [\[CrossRef\]](#)
16. Boucart, K. *Double-Gate Tunnel FET with High- κ Gate Dielectric*; IEEE: Piscataway, NJ, USA, 2008.
17. Toh, E.H.; Wang, G.H.; Samudra, G.; Yeo, Y.C. Device physics and design of double-gate tunneling field-effect transistor by silicon film thickness optimization. *Appl. Phys. Lett.* **2007**, *90*, 263507. [\[CrossRef\]](#)
18. Lu, H.; Seabaugh, A. Tunnel Field-Effect Transistors: State-of-the-Art. *IEEE J. Electron Devices Soc.* **2014**, *2*, 44–49. [\[CrossRef\]](#)
19. Lin, Z.; Chen, P.; Ye, L.; Yan, X.; Dong, L.; Zhang, S.; Yang, Z.; Peng, C.; Wu, X.; Chen, J. Challenges and Solutions of the TFET Circuit Design. *IEEE Trans. Circuits Syst. Regul. Pap.* **2020**, *67*, 4918–4931. [\[CrossRef\]](#)
20. Mamidala, J.; Vishnoi, R.; Pandey, P. *Tunnel Field-Effect Transistors (TFET): Modelling and Simulation*; Wiley: Hoboken, NJ, USA, 2016.
21. Saurabh, S.; Kumar, M. *Fundamentals of Tunnel Field-Effect Transistors*; CRC Press: Boca Raton, FL, USA; Taylor & Francis Group: Abingdon, UK, 2016.
22. Pasupathy, K.R.; Manivannan, T.S.; Lakshminarayanan, G. A Review of Engineering Techniques to Suppress Ambipolarity in Tunnel FET. *Silicon* **2022**, *14*, 1887–1894. [\[CrossRef\]](#)
23. Hraziiu, A.; Vladimirescu, A.; Amara, A.; Anghel, C. An analysis on the ambipolar current in Si double-gate tunnel FETs. *Solid State Electron.* **2012**, *70*, 67–72. [\[CrossRef\]](#)
24. Nigam, K.; Kondekar, P.; Sharma, D. Approach for ambipolar behaviour suppression in tunnel FET by workfunction engineering. *Micro Nano Lett.* **2016**, *11*, 460–464. [\[CrossRef\]](#)
25. Zhou, G.; Lu, Y.; Li, R.; Zhang, Q.; Hwang, W.; Liu, Q.; Vasen, T.; Chen, C.; Zhu, H.; Kuo, J.M.; et al. Vertical InGaAs/InP tunnel FETs with tunneling normal to the gate. *IEEE Electron Device Lett.* **2011**, *32*, 1516–1518. [\[CrossRef\]](#)
26. Lu, H.; Esseni, D.; Seabaugh, A. Universal analytic model for tunnel FET circuit simulation. *Solid-State Electron.* **2015**, *108*, 110–117. [\[CrossRef\]](#)
27. Avci, U.E.; Morris, D.H.; Hasan, S.; Kotlyar, R.; Kim, R.; Rios, R.; Nikonov, D.E.; Young, I.A. Energy efficiency comparison of nanowire heterojunction TFET and Si MOSFET at $L_g = 13\text{nm}$, including P-TFET and variation considerations. In Proceedings of the 2013 IEEE International Electron Devices Meeting, Washington, DC, USA, 9–11 December 2013; pp. 33.4.1–33.4.4. [\[CrossRef\]](#)
28. Morris, D.H.; Avci, U.E.; Rios, R.; Young, I.A. Design of Low Voltage Tunneling-FET Logic Circuits Considering Asymmetric Conduction Characteristics. *IEEE J. Emerg. Sel. Top. Circuits Syst.* **2014**, *4*, 380–388. [\[CrossRef\]](#)
29. Lee, C.S.; Pop, E.; Franklin, A.D.; Haensch, W.; Wong, H.S.P. A Compact Virtual-Source Model for Carbon Nanotube FETs in the Sub-10-nm Regime—Part I: Intrinsic Elements. *IEEE Trans. Electron Devices* **2015**, *62*, 3061–3069. [\[CrossRef\]](#)
30. Liu, H.; Saripalli, V.; Narayanan, V.; Datta, S. *III-V Tunnel FET Model*; nanoHUB: West Lafayette IN, USA, 2015. [\[CrossRef\]](#)
31. Mo, F.; Spano, C.E.; Ardesi, Y.; Piccinini, G.; Graziano, M. Beyond-CMOS Artificial Neuron: A Simulation- Based Exploration of the Molecular-FET. *IEEE Trans. Nanotechnol.* **2021**, *20*, 903–911. [\[CrossRef\]](#)
32. Hussain, I.; Riente, F.; Roch, M.R.; Piccinini, G.; Graziano, M. Performance analysis of transistor-based circuits through TAMAMS Web: From bulk to molecular devices. In Proceedings of the 2016 5th International Conference on Electronic Devices, Systems and Applications (ICEDSA), Ras Al Khaimah, United Arab Emirates, 6–8 December 2016; pp. 1–4. [\[CrossRef\]](#)
33. Lu, Y.; Zhou, G.; Li, R.; Liu, Q.; Zhang, Q.; Vasen, T.; Chae, S.D.; Kosel, T.; Wistey, M.; Xing, H.; et al. Performance of AlGaSb/InAs TFETs with gate electric field and tunneling direction aligned. *IEEE Electron Device Lett.* **2012**, *33*, 655–657. [\[CrossRef\]](#)
34. Choi, Y.K.; Lindert, N.; Xuan, P.; Tang, S.; Ha, D.; Anderson, E.; King, T.J.; Bokor, J.; Hu, C. Sub-20 nm CMOS FinFET technologies. In Proceedings of the International Electron Devices Meeting, Technical Digest (Cat. No.01CH37224), Washington, DC, USA, 2–5 December 2001; pp. 19.1.1–19.1.4. [\[CrossRef\]](#)
35. Agrawal, A.; Chouksey, S.; Rachmady, W.; Vishwanath, S.; Ghose, S.; Mehta, M.; Torres, J.; Oni, A.; Weng, X.; Li, H.; et al. Gate-All-Around Strained Si_{0.4}Ge_{0.6} Nanosheet PMOS on Strain Relaxed Buffer for High Performance Low Power Logic Application. In Proceedings of the 2020 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 12–18 December 2020; pp. 2.2.1–2.2.4. [\[CrossRef\]](#)

36. Zhang, J.; Frougier, J.; Greene, A.; Miao, X.; Yu, L.; Vega, R.; Montanini, P.; Durfee, C.; Gaul, A.; Pancharatnam, S.; et al. Full Bottom Dielectric Isolation to Enable Stacked Nanosheet Transistor for Low Power and High Performance Applications. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019; pp. 11.6.1–11.6.4. [[CrossRef](#)]
37. Loubet, N.; Hook, T.; Montanini, P.; Yeung, C.W.; Kanakasabapathy, S.; Guillom, M.; Yamashita, T.; Zhang, J.; Miao, X.; Wang, J.; et al. Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET. In Proceedings of the 2017 Symposium on VLSI Technology, Kyoto, Japan, 5–8 June 2017; pp. T230–T231. [[CrossRef](#)]