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Article

Power Scalable Radio Receiver Design Based on Signal and Interference Condition

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Abstract: A low power adaptive digital baseband architecture is presented for a low-IF receiver of IEEE 802.15.4-2006. The digital section's sampling frequency and bit width are used as knobs to reduce the power under favorable signal and interference scenarios, thus recovering the design margins introduced to handle the worst case conditions. We show that in a 0.13 μm CMOS technology, for an adaptive digital baseband section of the receiver, power saving can be up to 85% (0.49 mW against 3.3 mW) in favorable interference and signal conditions. The proposed concepts in the design are tested using a receiver test setup where the design is hosted on a FPGA.

Keywords: adaptive receiver; low power; receiver algorithms; packet based communication; sampling clock; word-length

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1. Introduction

In this work we propose minimizing power consumption of digital receiver depending on the quality of signal received. The version of IEEE 802.15.4-2006 at 2450 MHz with DSSS physical layer with OQPSK modulation specifies 65 dB possible variation in the received signal strength. We take advantage of this large variation by designing a power scalable baseband architecture, which adapts itself to the variation in signal and interference levels. The digital section adapts the word length (Q_{dig}) and

sampling frequency (f_s). To make the receiver adaptive and low power, various design techniques are proposed in this paper. The key features of this power scalable receiver are interference detector and SNR estimator (IDSE), variable tap and variable coefficient FIR filter, an adaptivity control unit and an adaptation procedure.

Minimizing power consumption of the receiver has been done by various authors in various ways. Varying f_s of the receiver to minimize power requires varying number of taps in the FIR filter. Authors in [1] have proposed a variable tap FIR filter based on approximate filtering to reduce power. In doing so, authors have demonstrated power reduction by a factor of 10. Besides varying number of taps to save power, we have used minimum resolution coefficients for FIR filters to save power. Author in [2] controls the resolution of analog-to-digital converter (ADC) in receiver and digital-to-analog converter (DAC) in transmitter. The ADC resolution is controlled depending on signal-to-noise and signal-to-interference ratio and resolution of DAC is controlled based on crest factor of modulation scheme. The author has not suggested any way to measure signal-to-noise and signal-to-interference ratio. Authors in [3] have proposed reconfigurable radio for MIMO wireless systems. Authors have emphasized on optimizing number of operations, latency requirements and the architecture of signal processing elements to minimize complexity of the MIMO signal processing. Number of antennas and modulations levels are reconfigurable in the systems proposed in [3]. Adaptive word length control is used to implement an OFDM based low power wireless baseband processing system [4]. OFDM processing essentially consists of filtering, followed by an FFT engine and then an equalization block. The Error Vector Magnitude (EVM) of the received signal is continuously monitored, to adjust the word length. If EVM is above a threshold, the word length is increased to improve precision and conversely, for good EVM (low error rate), the word length is reduced. Our approach for receiver design incorporates controlling the amplitude quantization and sampling frequency depending on the SNR levels and interference presence. Our approach of scaling power by varying Q_{dig} and f_s applies the concepts of adaptive signal processing to minimize power. Traditionally, adaptive signal processing is well known for minimizing error of signal processing structures [5], whereas our objective is to minimize power while keeping the error criteria as a constraint in the optimization formulation. An adaptation procedure is proposed to facilitate adaptation in packetized communication.

Now let us look at power consumption numbers in present day communication receivers on CMOS technologies. In [6] authors have reported IEEE 802.15.4 receiver (CC2420 chip) consuming 20 mA when active with 1.8 V power supply. Low power analog front end design for IEEE 802.15.4 has been proposed in a few papers [7,8] . In [7], authors proposed a front end design in 0.18 μ CMOS technology that consumes 4.32 mW, whereas in a more recent paper the authors in [8] proposed a front end in 90 nm technology that consumes 3.6 mW when active. Authors in [9] have discussed power consumption of various wireless technology for WPAN applications. As mentioned, authors in [9] say that the power consumption of wireless devices scales with the data rate. Typically, IEEE 802.15.4 receiver consumes 20 mA for 0.1 Mbps, 30 mA for Bluetooth at 0.3 Mbps, 100 mA for WLAN at 10 Mbps. Power consumptions in analog and digital portion separately have been reported in some papers. Authors in [10] have reported that baseband of IEEE 802.15.4 consumes 3.2 mA at 1.8 V supply (5.76 mW) in 0.18 μm technology whereas the analog portion consumes 7.0 mA. The authors in [9] have

given break up of analog and digital portion of the receiver for UWB. Here analog portion consumes 20 mA compared with 19.6 mA of digital at 200 MHz.

We start the next section by formulating an optimization problem for minimizing power while varying Q_{dig} and f_s for the digital baseband. Following this we explain our approach to minimize power based on this optimization. Section 3 explains the simulation and interference model used in subsequent sections. Section 4 discusses various blocks of the receiver, which are designed to accommodate variable Q_{dig} and f_s and to be compatible with adaptation procedure. Section 5 discusses the implementation specific details and dynamic power estimation of the design. Section 6 discusses experimental setup and results from the experimental setup to validate the concepts. Section 7 concludes the paper.

2. Power Scalable Digital Baseband

2.1. Optimizing Power

Figure 1. Cartoon of a typical receiver with variable f_s and Q_{dig} of the digital section.

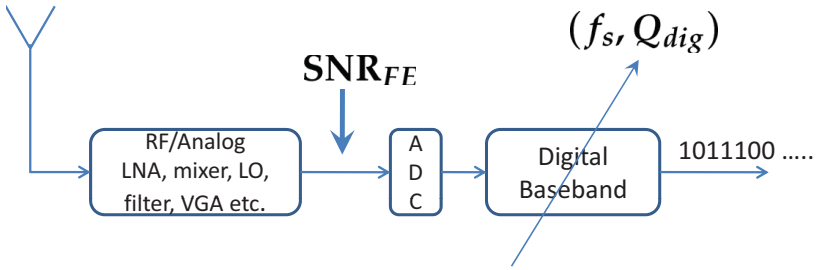


Figure 1 shows a typical receiver. SNR_{FE} is the SNR seen at the input of the ADC. It is the ratio of total signal power to the total noise power. It should not be confused with Eb/No typically used in communication theory literature. Input of the ADC, consists of the signal and the noise. We have assumed a 2nd order Butterworth bandpass filter preceding the ADC. The noise present at the input of ADC also has out of desired signal band components. This makes SNR_{FE} negative when noise is high. The packet error rate (PER) requirement translates to BER of 6.25×10^{-5} [11]. f_s and Q_{dig} are chosen to minimize power while achieving target BER. More formally:

$$\underset{Q_{dig},\, f_s}{\text{minimize}} \quad \text{Power} = f(Q_{dig}, f_s) \tag{1}$$

$$\text{subject to} \quad \text{BER} = h(Q_{dig}, f_s, \text{SNR}_{FE}, \text{interference}) \leq 6.25 \times 10^{-5} \tag{2}$$

BER is independent of Q_{dig} and f_s, if these parameters are chosen very high. In such a case the implementation of digital portion does not alter the SNR calculation of the receiver, *i.e.*, SNR seen at the input of the ADC is almost the same as SNR seen at the input of the demodulator. But in doing so the digital portion is over-designed and hence wastes power. In order to achieve a given BER, there can be different combinations of Q_{dig} and f_s for a given SNR_{FE} and interference levels, each with its own power cost. Values of Q_{dig} and f_s that minimize power as given in Equation (1) will be used. Furthermore, with varying values of SNR_{FE} and interference, the optimal choices for Q_{dig} and f_s can vary, necessitating

an adaptive resolution based digital section. For different levels of SNR_{FE} and interference, the optimal design parameters (Q_{dig}, f_s) will be stored in the LUT and used to configure the receiver. Finding a closed form expression for the function "h" in Equation (2) is hard due to the non-linear relationships. Coarser the ADC quantization (Q_{dig}), harder it becomes to analyze the signal. Hence BER is found through MATLAB simulations, for different (Q_{dig}, f_s) values. The power function in Equation (1) is obtained by Synopsys Prime Power for different Q_{dig} and f_s values. Finally, the optimum Q_{dig} and f_s values are obtained by a simple search over design space.

2.2. Proposed Architecture and Functioning

Figure 2 shows the architecture of the power scalable receiver. It includes synchronization units (acquisition, tracking, phase error estimator, frequency error estimator), CORDIC based NCO (Numerically Controlled Oscillator), FIR matched filters, decimator, demodulator, *etc.* Other than these units, the proposed receiver has units that make it adaptive. As shown in figure, it has an interference detector and an SNR estimator (IDSE), and an adaptivity control unit that decides the Q_{dig} and f_s of different sections of the receiver. For every packet the receiver starts off with the highest resolution and sampling frequency settings during the packet preamble. Synchronization (Timing, Frequency, Phase) is done with the highest settings and simultaneously, the interference and signal levels are estimated. By the end of the preamble, a LUT containing optimal values is consulted and the optimum Q_{dig} and f_s is used for the rest of the packet reception. All sections of the receiver in Figure 2 except the VGA and ADC are implemented in HDL for power estimation.

Figure 2. Proposed Adaptive Receiver. f_s is sampling frequency and Q_{dig} is word length.

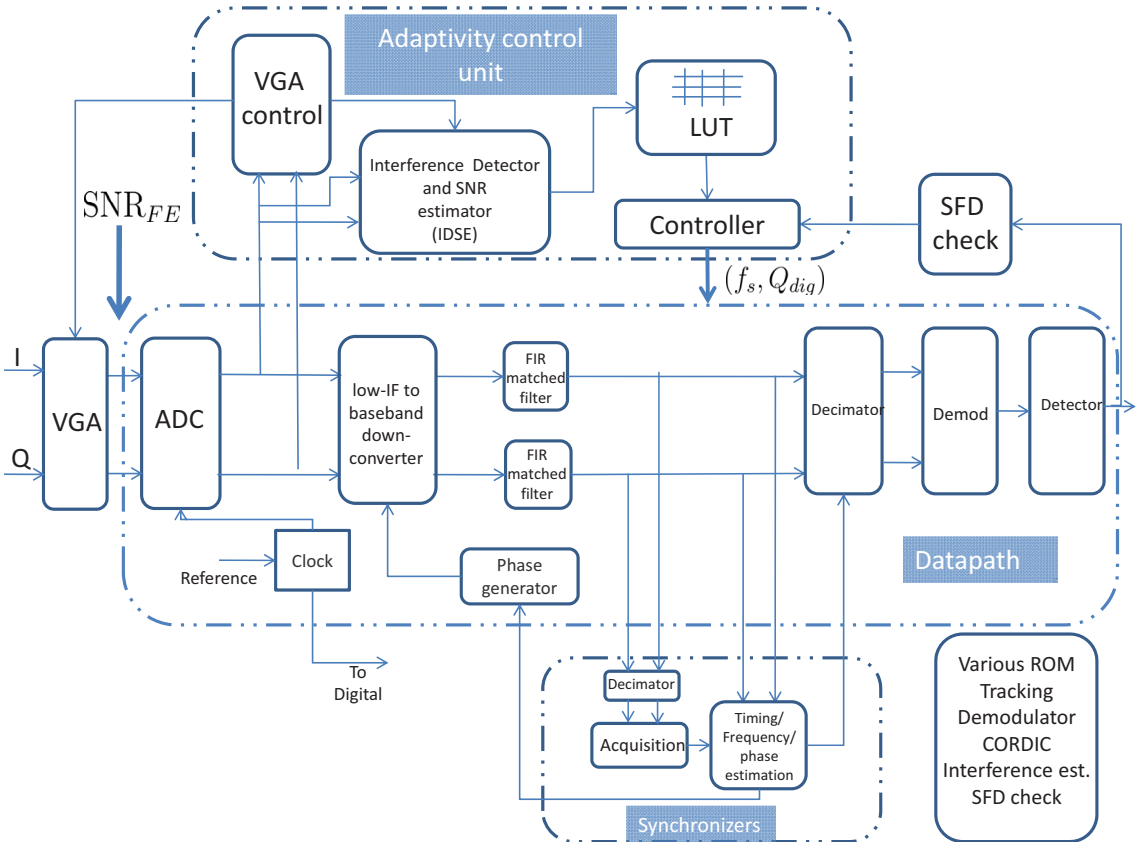
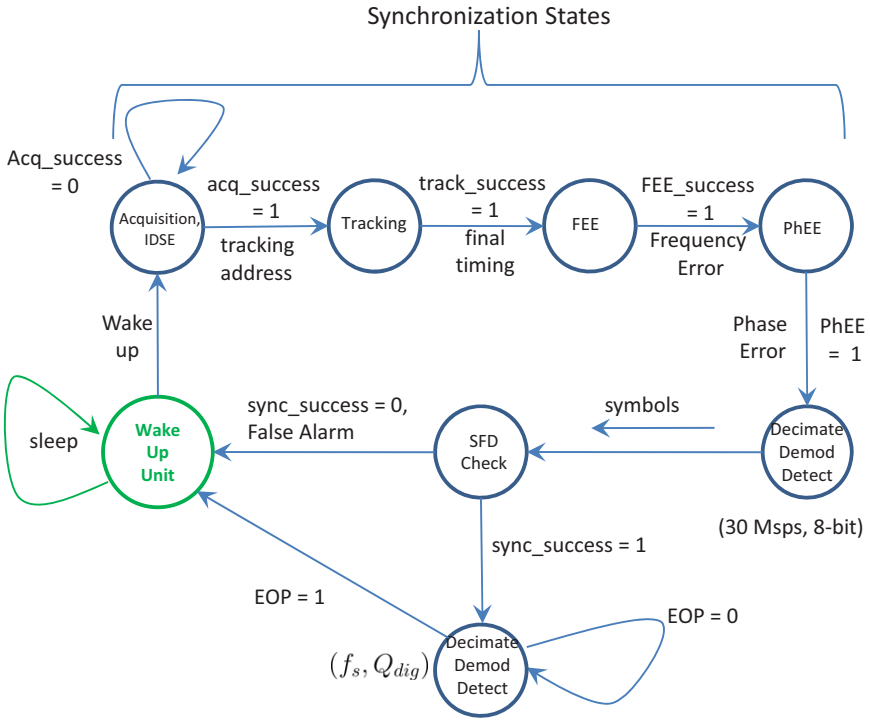


Figure 3 shows the state diagram of the receiver with seven states. Timing synchronization is achieved over Acquisition and Tracking. The Frequency Error Estimator (FEE) estimates the error between carrier frequency of the desired signal and frequency of the local oscillators that down-converts the signal. Similarly, Phase Error Estimator (PhEE) estimates the error in phase of input signal and down-converting signals. These estimates are used to correct the errors in frequency and phase to allow coherent demodulation of the signal. Start-Frame-Delimiter (SFD) check provides a means to check if the synchronization achieved is reliable to further demodulate the data. As shown in the figure, *acq_success*, *track_success*, *FEE_success* and *PhEE* cause transition of states during synchronization. The synchronizing units work in tandem. *sync_succ* signifies completion of synchronization and preamble of the packet. Detailed architecture of these synchronization units can be found in [12–14]. The decimator, demodulator and detector work in two different settings of Q_{dig} and f_s. The first setting as shown in the Figure 3 (30 Msps, 8-bit) is the setting of word length and sampling frequency for the receiver during preamble of the packet. The second setting (Q_{dig},f_s) applies for rest of the packet, *i.e.*, PHY service data unit (PSDU).

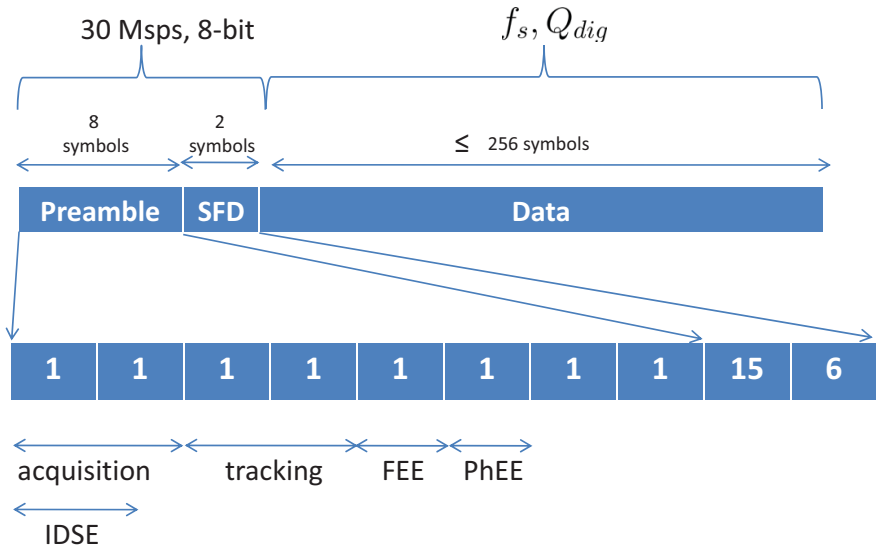
Figure 3. State Diagram of Receiver. STATES: (1) Acquisition; (2) Tracking; (3) Frequency error estimation (FEE); (4) Phase error estimation (PhEE); (5) Decimate, demodulate and detect at Q_{dig1} and f_{s1}; (6) Start-Frame-Delimiter (SFD) check; (7) Decimate, demodulate and detect at Q_{dig2} and f_{s2}.



The preamble is a sequence of symbol "1" followed by two SFD symbols as shown in the Figure 4. The figure shows a typical packet structure and the average time taken by various synchronization steps during the preamble when SNR_{FE} is high. The synchronization designed for this receiver works on the continuous flowing sampled data from ADC. Figure 5(a) shows the typical buffered implementation of a receiver. Here, various signal processing blocks inside the receiver access the data from the buffer. This

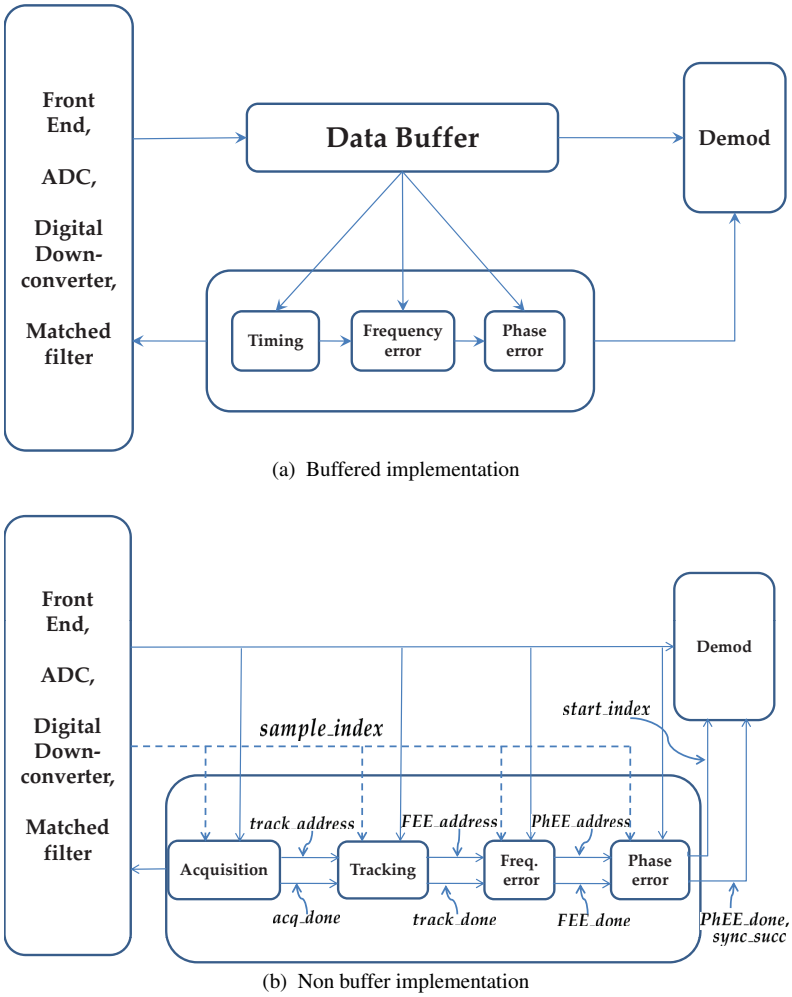
allows the receiver algorithms to reuse the data and gives better convergence performance. However, our approach for the receiver design does not use any buffer to save area and power. Figure 5(b) shows the non-buffered approach. Here, besides passing information regarding completion of its functioning as discussed above, every module passes a sample index to the subsequent module. For, e.g., acquisition unit passes *acq_success* and a count *track_address* to the tracking block once acquisition is done. The tracking unit initiates a counter when *acq_success* is received. The counter counts number of samples and the tracking begins when the counter reaches the count *track_address*. Once the synchronization is done (*sync_success*) is raised, all synchronization blocks turn off and receiver data-path (NCO, Matched filters, decimator, demodulator and detector) adjusts itself to new settings of Q_{dig} and f_s.

Figure 4. Preamble and timing for various synchronization units. Figure shows how various synchronization blocks work in tandem. clk_1 = 30 MHz, Q_{dig1} = 8-bit. clk_2—1 to 30 MHz. Q_{dig2}—1 to 8 bits.



Changing sampling frequency requires the estimates for synchronization computed during preamble to be preserved. Values of the estimate depend on the sampling frequency [13]. The frequency estimate needs to be scaled and the phase continuity has to be preserved. The path from ADC output to the input of the demodulator has a latency of a number of clock cycles due to FIR, CORDIC pipelines, decimator, *etc.*, as shown in Figure 6. When the sampling frequency of the receiver is changed after the packet preamble, the delay elements in these contain samples sampled at the highest sampling frequency used during preamble. The receiver is very sensitive to timing error when the sampling frequency is very low. For, e.g., for sampling frequency of 2 Msps, every pulse is sampled twice. In such a case, an error of one sample results in offset by half a pulse. Hence the delay across the data-path needs to be carefully accounted, particularly, when the sampling frequency is low. While changing Q_{dig} and f_s, it is proposed to discard all samples in delay elements across the receiver. This is due to the fact that the samples in delay elements across the receiver is sampled at higher sampling frequency than the new assigned Q_{dig} and f_s for the data duration. Delay elements are reset when the *adap_ctrl* goes high. As shown in Figure 6, once the *sync_succ* goes high, demodulator waits until the *sample_index* reaches *start_index*. Value of *start_index* is equal to number of clock cycle delay from output of ADC to demodulator.

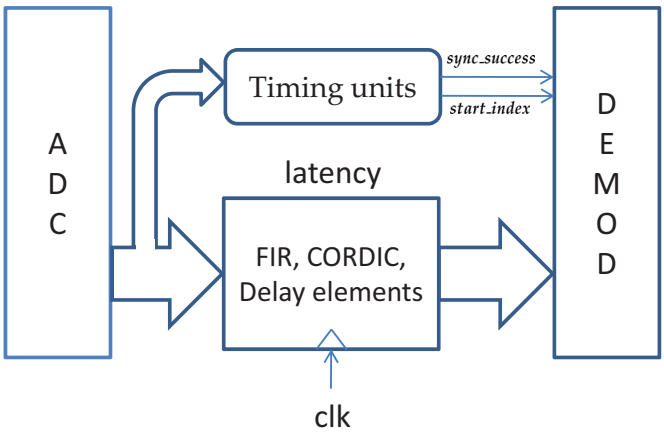
Figure 5. Buffered and non-buffered implementation of the receiver.



(a) Buffered implementation

(b) Non buffer implementation

Figure 6. Latency in data-path and preserving timing.



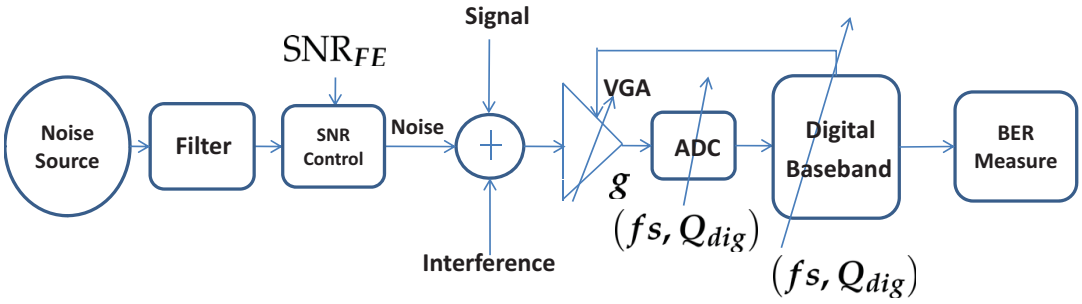
3. Determining Optimal LUT

As discussed in previous section, we use simulations to determine the combinations of quantization parameters that guarantee the BER for Equation (2). Thus for each input SNR_{FE} and interference, we evaluate BER of the receiver for several different settings of Q_{dig} and f_s.

3.1. Simulation Model

We use the fixed point toolbox of Matlab for quantization simulations. The simulation model used is shown in Figure 7. As we see in the simulation model signal, noise and interference pass through the channel select filter. The variable gain amplifier (VGA), upon getting feedback from digital portion of the receiver, re-sizes signal levels to full scale of ADC. Noise levels are controlled by the SNR control to maintain a SNR_{FE} at the input of ADC. Amplitude and time resolutions of ADC and digital baseband sections are variable.

Figure 7. Simulation Model, g is the variable gain of VGA, Q_{dig} and f_s are sampling frequency and bitwidth respectively.



3.2. Interference Modeling

The standard specifies four interfering channels [15]. Channels adjacent to the desired channel transmit at same power level as the desired, -82 dBm, whereas alternate channels should be considered transmitting -52 dBm. Adjacent channels are 5 MHz apart from the desired channel on either side. Similarly, alternate channels are 10 MHz apart. For an IF of 3 MHz [16], input to the ADC can be given as

$$x(t) = \text{Re}\left\{\begin{array}{l} x_0(t)e^{j(2\pi\, 3\times 10^6 t+\theta_0)} + x_1(t)e^{-j(2\pi\, 2\times 10^6 t+\theta_1)} \\ +x_2(t)e^{j(2\pi\, 8\times 10^6 t+\theta_2)} + x_3(t)e^{-j(2\pi\, 7\times 10^6 t+\theta_3)} \\ +x_4(t)e^{j(2\pi\, 13\times 10^6 t+\theta_4)} \end{array}\right\} \tag{3}$$

$x_0(t)$ is the desired baseband signal. $x_1(t)$ and $x_2(t)$ are adjacent baseband signals. $x_3(t)$ and $x_4(t)$ are alternate baseband signals.

BER simulation to find all combination of Q_{dig} and f_s can be very time consuming [17]. Instead we have developed a technique to reduce the computation time. Initially we find the variance of correlations at the output of correlation demodulator. We use the same variance measure in our subsequent simulations with different receiver settings. We found that this technique reduces the simulation complexity lot in comparison with doing BER simulations with bandpass signals.

4. Implementation Details

4.1. Interference Detector and SNR$_{FE}$ Estimator (IDSE)

As mentioned in previous sections, central to the adaptive receiver is the Interference detector and SNR estimator. IDSE is active during the preamble. Power in adjacent, alternate and desired signal bands is measured non-coherently. $\hat{P}_{adj}$ is the power measured in adjacent channels, $\hat{P}_{alt}$ is the total power in alternate channels and $\hat{P}_{sig}$ is the power in the desired signal's channel.

4.1.1. Interference Detector

Proximity of the adjacent channel to the desired channel makes it more harmful to the signal than the alternate channels.

As can be seen from Figure 8, IDSE has three inputs: I and Q inputs from ADC and a signal that indicates if detection or estimation should be done. This input signal has three states: detect alternate, detect adjacent and estimate SNR$_{FE}$. For all three states, setting of NCO is changed to down-convert adjacent or alternate or desired signal. IDSE consists of two arms, one each for one adjacent or alternate channel. Only one arm is active during SNR$_{FE}$ estimation. Both arms have a CORDIC NCO unit to down-convert the interference or signal. Output of detectors/estimator goes to a comparator that compares it with threshold. For interference detection, output of comparators is 1-bit to indicate presence of interferences. In estimator mode, comparator finds the range in which the measured SNR$_{FE}$ falls. LUT has SNR steps with difference of 1 dB. Since SNR variation can be up-to 60 dB so it has 60 SNR steps, requiring 6-bit index. There are four possible combinations from interference detection: Alternate present/absent and Adjacent present/absent, it is indicated by 2 bits. So, LUT is indexed by 8-bits.

Figure 8. Non-coherent interference detection procedure.

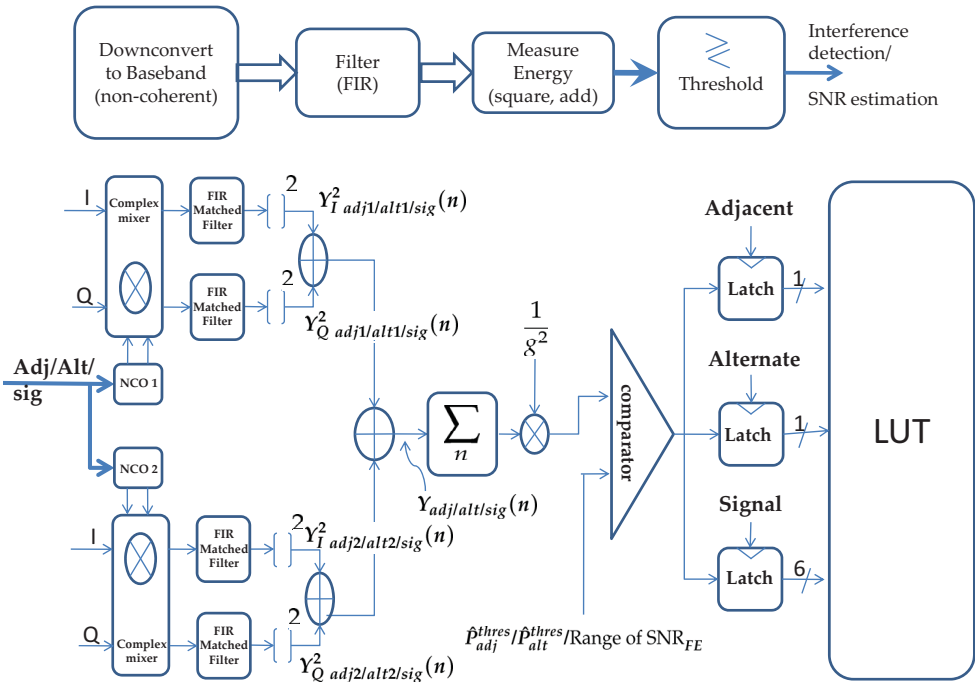
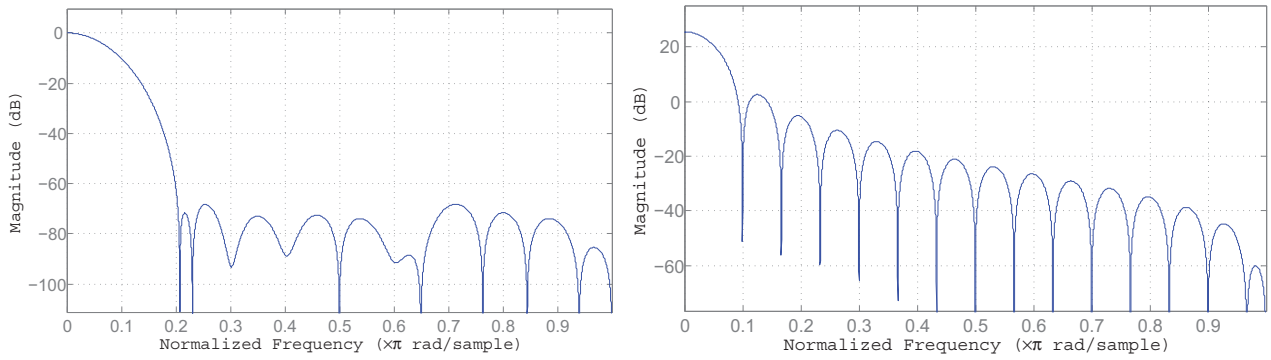


Figure 9(a) and 9(b) are frequency responses of FIR filters used in IDSE and data-path of the receiver. The filter used for IDSE has a sharper roll-off. Interference from each interfering channel is down-converted to baseband and filtered by this filter. It can be seen from the filter's frequency response that the attenuation at 5 MHz and 10 MHz distance is approximately 80 dB. When measuring the desired signal power, due to attenuation by the matched filter, adjacent signal level falls to -162 dB and alternate signal level falls to -132 dB. These levels of interference are quite low and do not corrupt the signal power estimation. Whereas, while measuring interference power, signal power from desired band can affect the interference power measurement. This is due to the fact that the maximum possible signal power is -20 dBm and it can spill to neighboring bands. At such high signal level even after the attenuation by the matched filter, its strength in neighboring channels is high enough to affect interference power measurement.

Figure 9. Frequency Response of FIR Filters.



(a) Frequency Response of FIR Filter in Interference detector

(b) Frequency Response of FIR Matched Filter in the data-path

Let Y_{Iadj1} and Y_{Iadj2} be the in-phase and Y_{Qadj1} and Y_{Qadj2} are the quadrature phase adjacent channels. These terms are analogously defined for alternate channels too. g is the gain of VGA [18,19]. Measured power in adjacent and alternate channels ($\hat{P}_{adj}$, $\hat{P}_{alt}$) can be defined as:

$$\hat{P}_{adj} = \frac{1}{g^2}\sum_{n}^{N} Y_{adj}(n), \tag{4}$$

$$\hat{P}_{alt} = \frac{1}{g^2}\sum_{n}^{N} Y_{alt}(n) \tag{5}$$

where,

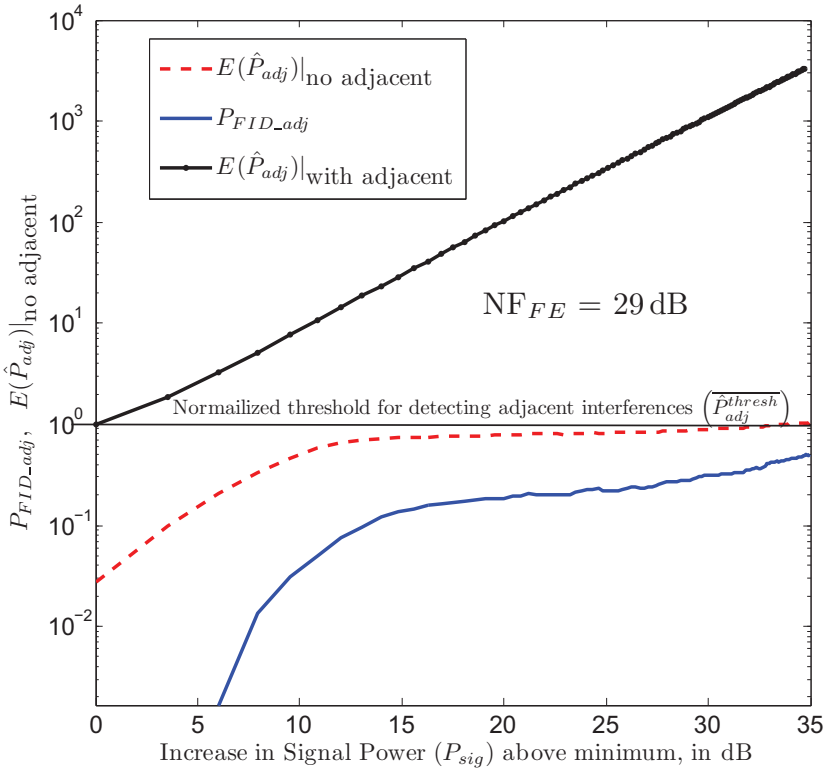
$$Y_{alt}(n)=Y^2_{Ialt1}(n)+Y^2_{Qalt1}(n)+Y^2_{Ialt2}(n)+Y^2_{Qalt2}(n) \tag{6}$$

$$Y_{adj}(n)=Y^2_{Iadj1}(n)+Y^2_{Qadj1}(n)+Y^2_{Iadj2}(n)+Y^2_{Qadj2}(n) \tag{7}$$

If $\hat{P}_{adj}$ exceeds a-priori calculated threshold, $\hat{P}^{thresh}_{adj}$, then adjacent interference is detected. Similarly, $\hat{P}^{thresh}_{alt}$ is the threshold what is compared with $\hat{P}_{alt}$. Figure 10 shows the effect of desired signal power on adjacent channel interference detection. The figure is obtained for front end noise figure (NF_{FE}) of 29 dB [20]. $\overline{\hat{P}^{thresh}_{adj}}$ is the normalized threshold for detecting presence of adjacent interference. When

signal power is large, then even in absence of adjacent interference, $\hat{P}_{adj}$ can exceed $\overline{\hat{P}_{adj}^{thresh}}$. P_{FID_adj} in figure is probability of false adjacent interference detection. P_{FID_adj} increases with increase in desired signal strength. When signal power is more than 30 dBm, then even in absence of adjacent interference $E(\hat{P}_{adj})$ exceeds $\overline{\hat{P}_{adj}^{thresh}}$. As shown later, when P_{sig} is high ($\text{SNR}_{FE} > 15$ dB), Q_{dig} and f_s settings of receiver is a minimum irrespective of outcome of interference detection. Effect of P_{sig} is less severe on detecting alternate interference as alternate channels are farther in frequency domain. Variance of interference detector reduces with increase in number of pulses utilized for detection. Interference detection is done over four half sine pulses, as the variance does not change much for further increase in duration of detection.

Figure 10. Performance of Interference detector for $\text{NF}_{FE} = 29$ dB. Minimum $P_{sig} = -85$ dBm. NF is calculated for minimum P_{sig}. As figure shows, large desired signal power hinders accurate interference detection. But as evident from Table 1, accurate interference detection is needed until P_{sig} is 20 dB above minimum. P_{sig} of 0 dB corresponds to -6 dB SNR_{FE}.



4.1.2. SNR Estimation

Similar to power measurement of interferences, power measured in desired signal channel is

$$\hat{P}_{sig} = \frac{1}{g^2}\sum_{n}^{N} Y_{sig}(n) \tag{8}$$

$$\text{where, } Y_{sig}(n) = Y_{Isig}^2(n) + Y_{Qsig}^2(n) \tag{9}$$

If Y_{Isig} and Y_{Qsig} are given by $x[n] + w[n]$, where $w[n]$ is AWGN, then

$$\hat{P}_{sig} = \frac{2}{g^2}\sum_{n}^{N} g^2(x[n] + w[n])^2 = 2\sum_{n}^{N}(x^2[n] + w^2[n]) \tag{10}$$

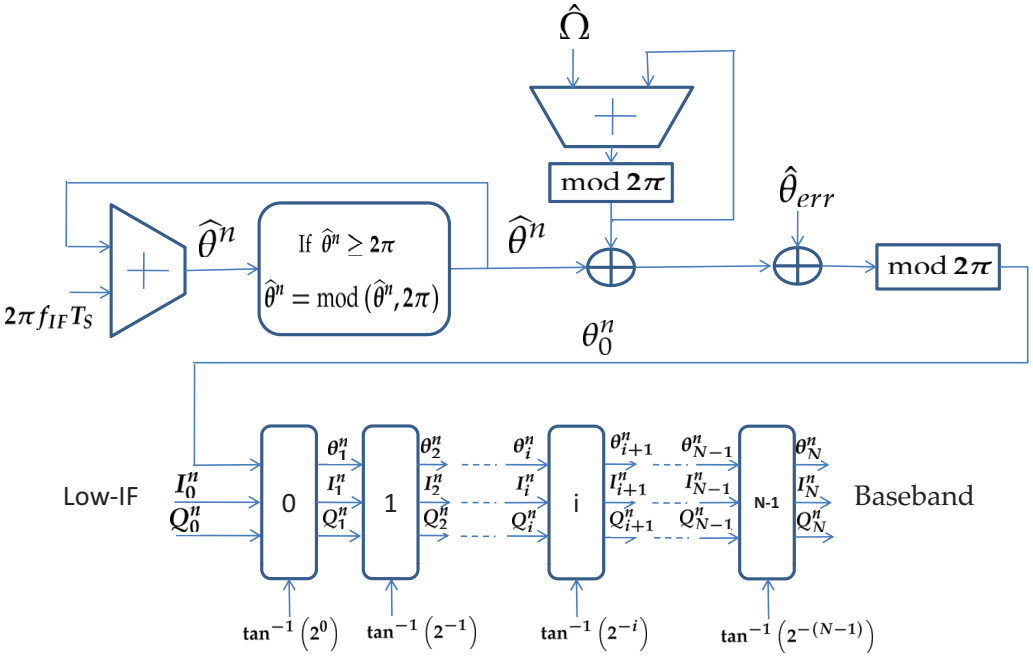
Since signal and noise are uncorrelated, $E(x\,w) = 0$,

$$\widehat{\text{SNR}}_{FE} = \frac{\sum_{n}^{N} x^2[n]}{\sum_{n}^{N} w^2[n]} = \frac{\hat{P}_{sig}}{2N\sigma^2} - 1 \tag{11}$$

Thus to measure $\hat{P}_{sig}$, Equations (8) and (9) can be used. Front end of the receiver is designed for a constant noise figure. Thus the worst case variance of noise (σ^2) contributed by the front end is known. Hence, SNR can be estimated using Equation (11). SNR_{FE} estimator is ON for one symbol duration.

4.2. CORDIC Down-Converter and Phase Generation for CORDIC Blocks

Figure 11. Variable phase generation for CORDIC units. Such units are used in NCO to downconvert the IF signal to baseband, In interference estimators to down-convert interferences to baseband and in adaptive FIR unit to generate sinusoid coefficients. Input to this unit is only T_s, which is fed from LUT.



CORDIC Pipelines

CORDIC is used in rotation mode to down-convert the signal from IF to baseband [21]. Change in sampling frequency requires variable phase generation for CORDIC unit. Figure 11 shows the variable phase generator for various CORDIC/NCO units mentioned above. Input to this block is sampling

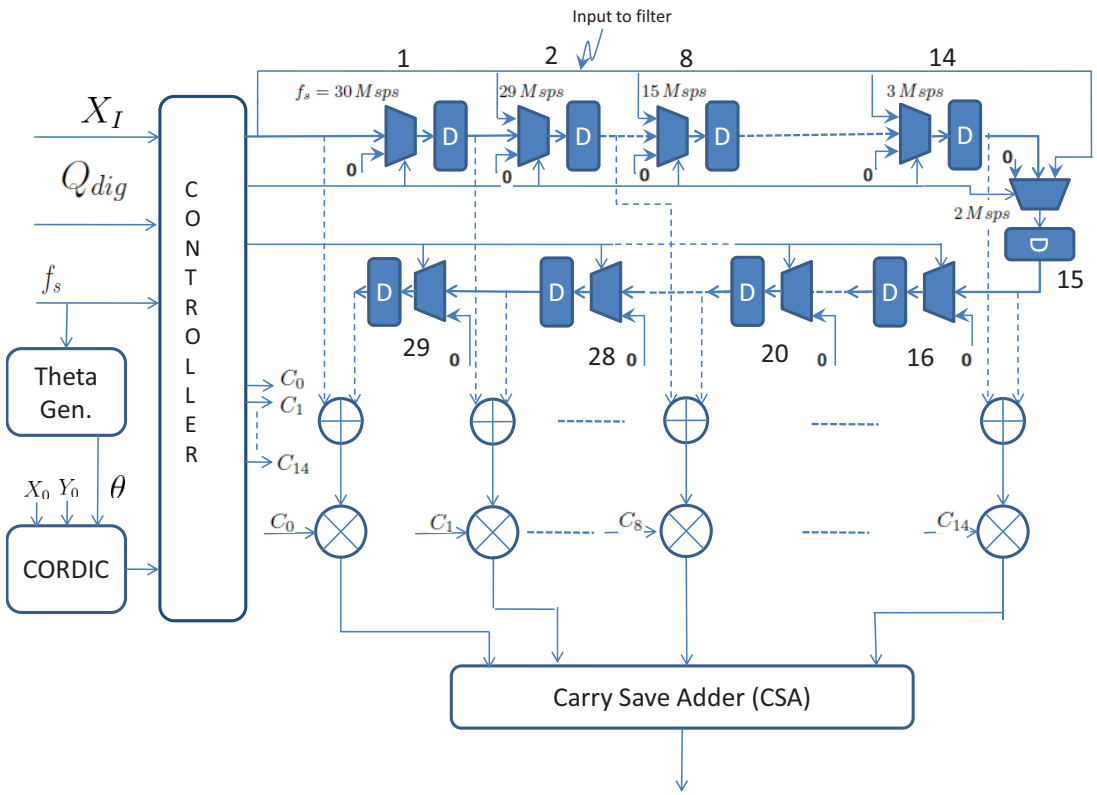
frequency provided by LUT. We have used 11 pipelined stage of CORDIC for IF to baseband conversion. The phase is represented by 32 bits. Number of pipeline stages and word length for phase representation are optimized based on analysis in [22], with the constraint that errors introduced by quantization in above two parameters should not corrupt a full length packet. $\hat{\Omega}$ is the estimated frequency error generated by FEE. $\hat{\theta}$ is the phase error estimated by PhEE.

4.3. FIR Filter, Decimator and Demodulator

4.3.1. Adaptive FIR Filter

FIR filter in the receiver chain is a matched filter to the baseband half-sine pulse. Frequency response of the filter is shown in Figure 9(b). Figure 12 shows the structure of the adaptive FIR filter. As shown, the adaptive FIR structure has one CORDIC unit for coefficient generation, a theta generator for CORDIC unit, one central controller, and 30 taps (corresponding to maximum sampling frequency). The CORDIC unit generates FIR coefficients that are input to multipliers. The theta generator supplies phase values to CORDIC unit to generate coefficients. Generating FIR coefficients with CORDIC makes it more amenable to adaptive architecture. The phase values depend on f_s. Resolution of coefficients are controlled based on Q_{dig}.

Figure 12. Adaptive FIR Filter. Controller controls the multiplexer to select which input to pass on to next delay element. A filter tap is deactivated by feeding a zero to its delay elements. Based on Q_{dig} controller controls the word length of FIR coefficients. Multipliers are Baugh–Wooley multipliers.



Tap coefficients are sampled half sinusoid. Frequency response of filter is shown in Figure 9(b). Since the tap coefficients are symmetric, the filter has folded architecture with number of taps equal to half of number of coefficients. Number of taps need to be adjusted with change in sampling frequency to keep it matched. Each tap in the filter consists of a multiplexed delay element, an adder and a multiplier. The multiplexer is a 3×1 multiplexer. Depending on the sampling frequency, either a zero or output of the preceding delay element or input to the FIR filter is multiplexed to the input of delay element. As shown in the figure, when the sampling frequency is 3 Msps, delay elements numbered 14 and 15 are active and all other delay elements have zero inputs. Multipliers corresponding to inactive taps get zeros at its input and hence have no dynamic power. The carry save adder adds outputs of the multipliers.

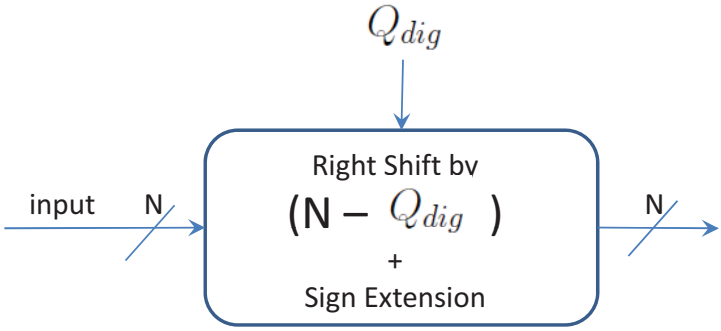
4.3.2. Decimator, Demodulator and Detector

Decimator in the data-path is an adaptive decimator. It decimates incoming samples depending on the sampling frequency. The demodulator is the 16-ary quasi orthogonal correlation demodulator. It correlates the incoming samples with the stored modulation symbols. Output of demodulator is 16 correlation values. The detector finds the maximum of these correlation values and declares it as the symbol arrived.

5. Implementation and Power Estimation

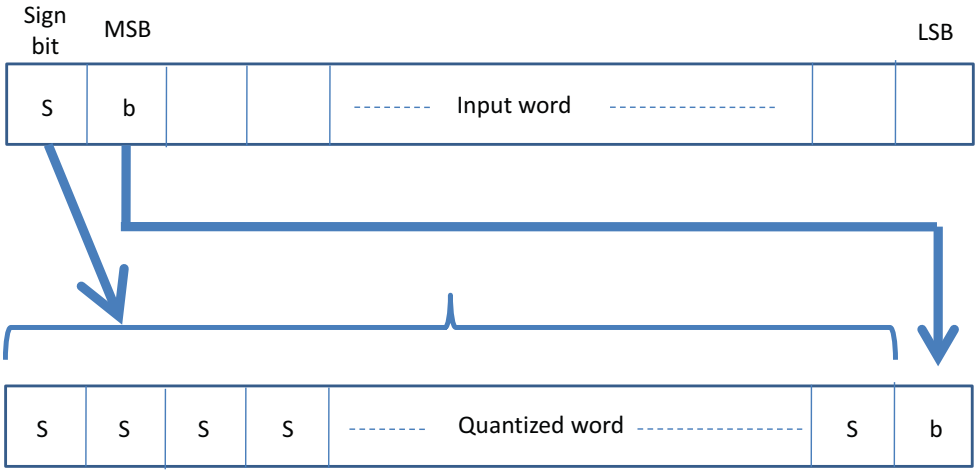
The design is coded in verilog HDL. Once pre-synthesis simulations are successful, RTL is synthesized for ASIC and FPGA implementation. The power estimation and comparison is done for ASIC implementation and design validation is done on FPGA platform. For power estimation, it is synthesized in 130-nm UMC CMOS process for maximum sampling frequency of 30 Msps using Synopsys Design Compiler. The power estimation is done once post synthesis simulation is successful. Synopsys Prime Power is used for estimating dynamic power. Input to Prime Power is the VCD (Value Change Dump) file generated from verilog simulation and the synthesized netlist. The VCD file contains all signal transition that occurred during the simulation. For generating VCD file, input to the simulator are the synthesized netlist, test vectors generated in MATLAB and SDF (Standard Delay Format) file used for synthesis.

Figure 13. Word length (Q_{dig}) control, multi-bit to 1-bit control, on signal level and word level.



(a) Quantization, input/output word length is N

Figure 13. *Cont.*



(b) Multi-bit to 1-bit word

Figure 13 shows a quantizer in hardware. For an input with word length N, quantizer shifts the input to right by $N - Q_{dig}$ with sign of the word preserved as shown in Figure 13 for Q_{dig} equal to one. By doing this, higher order bits do not see lot of switching when they are processed further in the receiver. There will be activity in the lower order bits of the word. Hence with smaller Q_{dig}, there is saving in dynamic power.

Table 1 shows the estimated power for various Q_{dig} and f_s combinations for a given $\widehat{\text{SNR}}_{FE}$ under different conditions of interference. Case-I corresponds to the case when there is no interference and only noise is present in the system. Case-II corresponds to the case when there is no interference on the alternate channels and only adjacent interference is present with noise. Case-III is the case where adjacent channels are absent, whereas, alternate channels and noise are present in the channel. In case-IV all interferences are present along with noise. Every Q_{dig} and f_s combination in the table satisfies the required BER. The estimated power is also shown for all combinations. The combination of Q_{dig} and f_s that consumes lowest power for a particular interference and $\widehat{\text{SNR}}_{FE}$ condition is put into the LUT. Such entries are listed under gray shading. The power is estimated for maximum length packet. Average power (P_{avg}) is calculated as follows:

$$P_{avg} = \frac{P_{synch} \times T_{synch} + P_{data} \times T_{data}}{T_{total}} \quad (12)$$

$$\text{where, } T_{total} = T_{synch} + T_{data} \quad (13)$$

P_{synch} is the average power consumption during preamble and SFD. P_{data} is the average power during data. As shown in Figure 4, T_{synch} is preamble and SFD duration. It is 10 symbol long and data is 256 symbols long. The power spent during synchronization is fixed (P_{synch} = 10 mW) and depends on Q_{dig} and f_s settings for the data duration. In order to have a simple clock generator, the operating sampling frequency (f_{opr}) for the design are integer division of 30 Msps. They are 30, 15, 10, 6, 5, 3, 2, and 1 Msps respectively. As shown in Table 1, the sampling frequencies are quantized to the next higher operating sampling frequency. For, e.g., sampling frequency of 13 Msps is raised to 15 Msps. We can see from the table, maximum power consumed by the design is 3.3 mW. The lowest power consumed by the design as can be seen from the table is 0.49 mW, when f_s is 2 Msps and Q_{dig} is 1-bit. At this sampling

frequency, there is only one multiplier active in the FIR filter. f_s of 2 Msps means the signal with IF of 3 MHz is under-sampled. In spite of under-sampling and coarsely quantizing (1-bit) the signal, specified BER is achieved when $\widehat{\text{SNR}}_{FE}$ is high. Thus we see that saving in power can be approximately seven times when SNR_{FE} is high and interferences are absent.

Table 1. Sampling frequency (Msps) and power (mW) for different interference and $\widehat{\text{SNR}}_{FE}$ values for the receiver.

Interference attenuation	No. of bits	Sampling Frequency (f_s/f_{opr}) in Msps , Power in mW						
	Q_{dig}	$\widehat{\text{SNR}}_{FE} = -6$ dB	$\widehat{\text{SNR}}_{FE} = -4$ dB	$\widehat{\text{SNR}}_{FE} = -2$ dB	$\widehat{\text{SNR}}_{FE} = 0$ dB	$\widehat{\text{SNR}}_{FE} = 5$ dB	$\widehat{\text{SNR}}_{FE} = 15$ dB	$\widehat{\text{SNR}}_{FE} \geq 20$ dB
Case-I	1	*	10/10, 1.48	7/10, 1.48	4/5, 0.85	1/1 0.49	1/1, 0.49	1/1 0.49
No interference	2	13/15, 2.49	7/10, 1.76	4/5, 0.96	1/1, 0.49	1/1, 0.49	1/1, 0.49	1/1, 0.49
Only noise	4	13/15, 2.92	8/10, 2.11	1/1, 0.50	1/1, 0.50	1/1, 0.50	1/1, 0.50	1/1, 0.50
	8	13/15, 3.30	3/3, 0.75	1/1, 0.52	1/1, 0.52	1/1, 0.52	1/1, 0.52	1/1, 0.52
Case-II	1	*	*	*	*	11/15, 2.5	1/1, 0.49	1/1, 0.49
No Alternate	2	*	*	*	*	9/10, 1.76	1/1, 0.49	1/1, 0.49
Adjacent - Standard	4	22/30, 6	8/10, 2.11	8/10, 2.11	7/10, 2.11	7/10, 2.11	1/1, 0.50	1/1, 0.50
Specific	8	12/15, 3.3	8/10, 2.7	8/10, 2.7	7/10, 2.7	5/5, 1.23	1/1, 0.52	1/1, 0.52
Case-III	1	*	*	*	23/30, 4.18	9/10, 1.47	1/1, 0.49	1/1, 0.49
No Adjacent	2	*	*	25/30, 5.0	19/30, 5.0	6/6, 1.5	1/1, 0.49	1/1, 0.49
Alternate - Standard	4	13/15, 2.92	12/15, 2.92	4/5, 1.07	4/5, 1.07	3/3, 0.71	1/1, 0.50	1/1, 0.50
Specific	8	14/15, 3.3	7/10, 2.7	4/5, 1.19	4/5, 1.23	3/3, 0.75	1/1, 0.52	1/1, 0.52
Case-IV	1	*	*	*	*	15/15, 2.15	5/5, 0.85	1/1, 0.49
Standard	2	*	*	*	*	14/15, 2.49	3/3, 0.66	1/1, 0.49
Specific	4	23/30, 6.0	13/15, 2.92	13/15, 2.92	7/10, 2.11	6/6, 1.19	1/1, 0.50	1/1, 0.50
	8	14/15, 3.3	13/15, 3.3	7/10, 2.7	7/10, 2.7	6/6, 1.38	1/1, 0.52	1/1, 0.52

* indicate that the corresponding word length at particular $\widehat{\text{SNR}}_{FE}$ will not result in acceptable BER; Cells in gray shade are the ones fed to the LUT in the receiver.

Looking into Table 1, when there is no interference (Case-I), the variation in power is from 2.49 mW to 0.49 mW. It suggests that even with a high-order interference reject filter in RF chain of the receiver, just by $\widehat{\text{SNR}}_{FE}$ estimation power saving of the order of 5 times is possible. It is evident from the Table 1 that when $\widehat{\text{SNR}}_{FE}$ is very high (>20 dB), f_s of 2 Msps and Q_{dig} of 1-bit works for all interference condition. Thus inaccuracy in interference detection is tolerable at very high $\widehat{\text{SNR}}_{FE}$ as mentioned in a previous section on IDSE. Since this is the power averaged over the maximum packet length possible, the lowest power values is a function of packet length. The average packet length depends on the application and usage. The power numbers for different packet length can be obtained from Equation (12). One more point to consider while looking at the power numbers is, the numbers do not include the possible power savings that can be obtained from a variable resolution ADC. A variable resolution and variable sampling rate ADC can take advantage of different possible Q_{dig} and f_s settings to lower the power consumption.

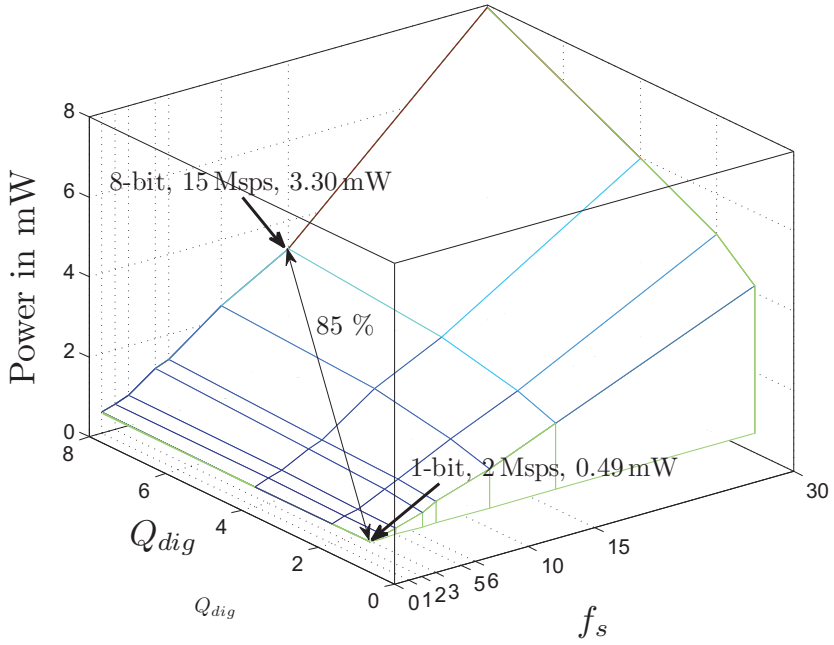
Table 2 shows break-up of gate count of the design in percentage. Total gate count of the design is approximately 606 K gates. We see that tracking unit has largest gate count. We see that expense of adaptivity and lowering power is 16% additional gate count of IDSE unit. The design contains approximately 4.5% memory elements (ROM). The design has many Baugh–Wooley 2's complement signed multipliers in it, it is by virtue of many FIR filters in IDSE unit and in data-path. Though synchronization units consume more area as shown in Table 2, average power consumed by synchronization units is very less. Considering this, we realize that adding any component to data-path requires more attention than adding a component to synchronization unit. Finally, Figure 14 shows the power consumption as a function of Q_{dig} and f_s, as was discussed while formulating the design problem in Equation (1).

Table 2. Estimated gate count and design summary from ASIC simulation.

Blocks and Gate count in %			
IDSE	16	Tracking	36
Match Filters	19.8	Acquisition	5.7
PhEE	4.95	Demod	4.83
ROM	4.1	FEE	4
NCO	2.4	Detector	1.2
Theta gen.	0.86		

Designed for	IEEE 802.15.4-2006
Technology	UMC 130 nm CMOS
Gate count	∼606 K gates
Area	∼2.42 mm^2
Power	variable, 0.49–3.3 mW
Frequency	variable, 1–30 Msps

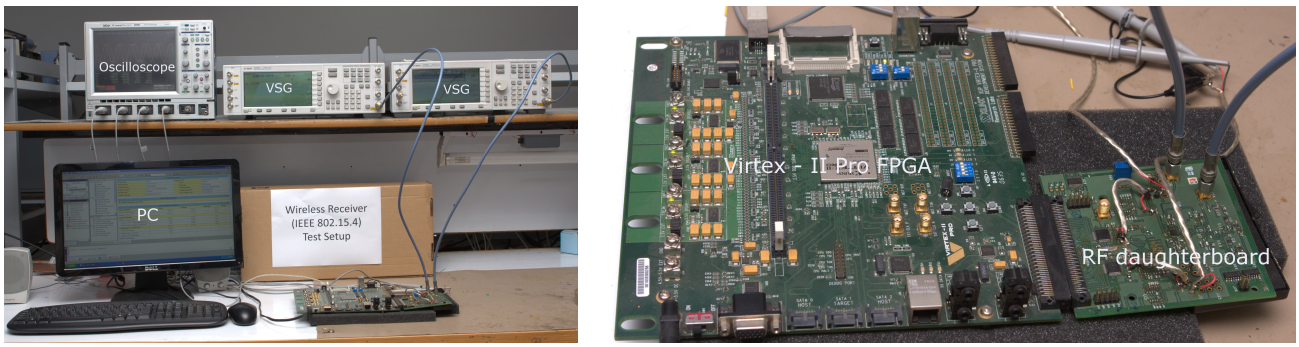
Figure 14. Power as a function of f_s and Q_{dig}, Equation (1). Variation in power consumption of the design in seen to be 85%.



6. Experimental Results and Discussions

The design is implemented on a Xilinx Virtex-II pro FPGA [23] and is tested with a receiver test setup. The test setup includes Vector Signal Generators (VSG), Oscilloscope, FPGA board, spectrum analyzer and a PC with software as shown in Figure 15(a). Figure 15(b) shows the FPGA board with RF daughterboard. RF daughterboard is made using discrete components and works at center frequency of 2.4 GHz. Inputs are modulated RF and local oscillator signals. The RF input from signal generator is downconverted to IF and digitized before presenting it to the FPGA board. The FPGA does the further processing in the digital to extract the packet. Packet error and packet loss are measured inside the FPGA. This is done by transmitting a packet with 20 known symbols by triggering the VSG repeatedly. Demodulated symbols are compared with the stored sequence of symbols in the FPGA. The packet error counter (*packet_err_count*) is incremented with every packet error. For packet loss measurement, number of packet transmitted is counted and compared with the number of *sync_succ* occurred, *i.e.*, number of time synchronization is achieved.

Figure 15. Experimental setup and RF board with FPGA.



(a) Experimental setup

(b) RF board (2.4 GHz) with FPGA

Figure 16 shows snapshot of the baseband signal after the low-IF to baseband downconverter from the experimental setup. The snapshot is taken from within FPGA using Chipscope [23]. Characteristic of the signal changes midway. First half of the snapshot shows the preamble duration. The signal has high dynamic range during this period, when synchronization and IDSE units are active. Second half of the signal has lesser dynamic range. It is the duration of the packet that contains the data. The data duration shown here is captured when the input to the receiver is 1-bit and sampled at 2 Msps.

Figure 16. Baseband signal in the receiver during a packet reception from experimental setup.

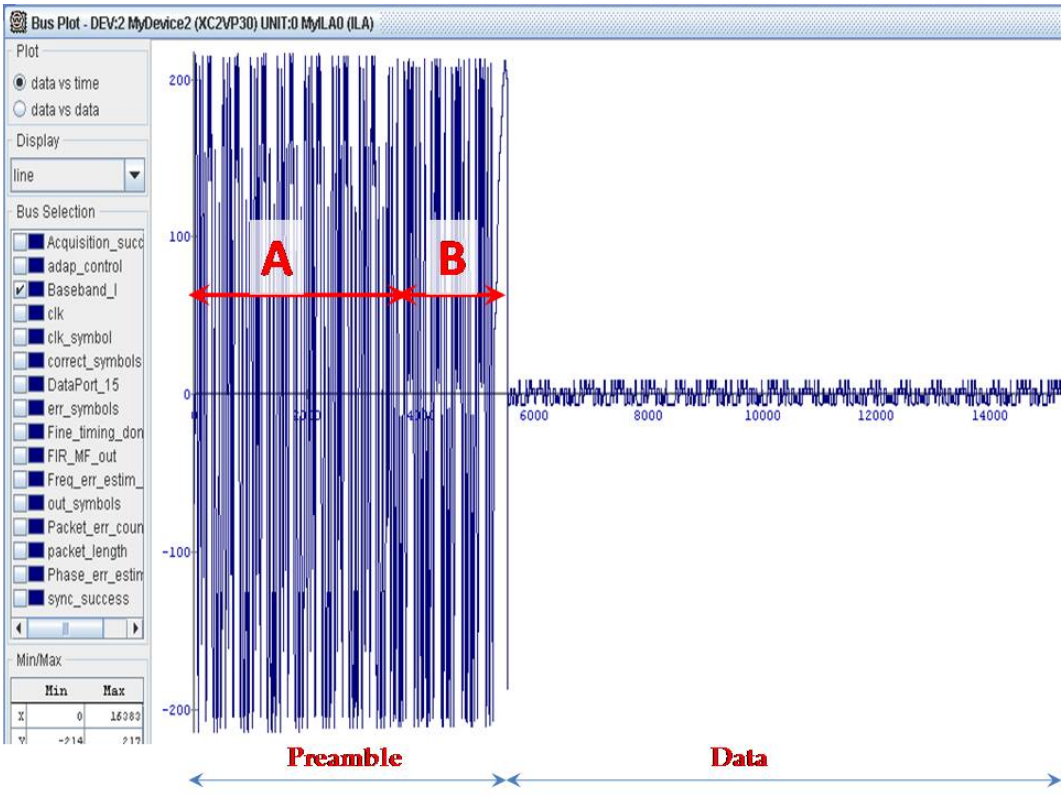
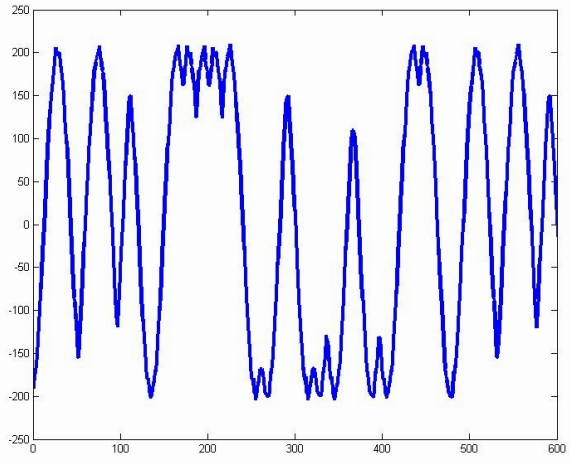
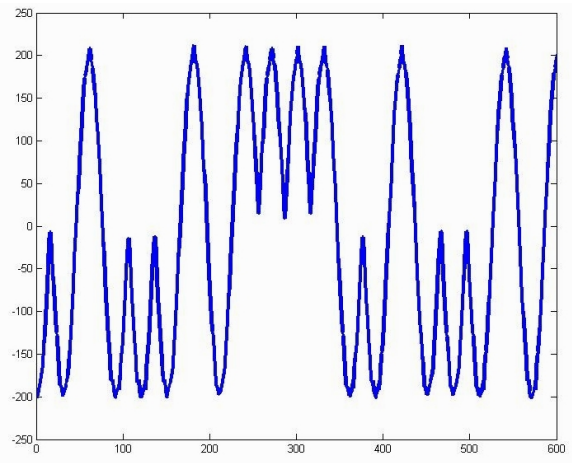


Figure 17 shows the amplitude *vs.* time of the signal during various instances of packet reception. Time is in micro seconds and amplitude is the digitally quantized signal. Figure 17(a) shows the baseband signal with frequency and phase error, corresponding to section labeled "**A**" in Figure 16. Figure 17(b) shows the baseband signal after frequency and phase error correction, corresponding to section "**B**" labeled in Figure 16. The signal shown here is very close to the ideal baseband signal inside the receiver, since input noise is low. The signal has very high resolution, as is evident from the smoothness of the sinusoid pulses. Smoother high resolution signals cause more switching and hence consume more power. Baseband signal during sampling frequency and bitwidth transition is shown in Figure 17(c). As can be seen, the smooth sinusoids transform to less dynamic low resolution signal. Content of registers in the datapath is discarded during this period. Figure 17(d) shows the baseband signal during data period of the packet. As evident from the figure, signal has low amplitude resolution and is not as smooth as signals captured in Figure 17(b). Signal shown in figure is captured when input to the digital receiver is 1-bit and the clock frequency is 2 Msps. The power consumption of the receiver is less when the receiver processes such low resolution (time and amplitude) signal.

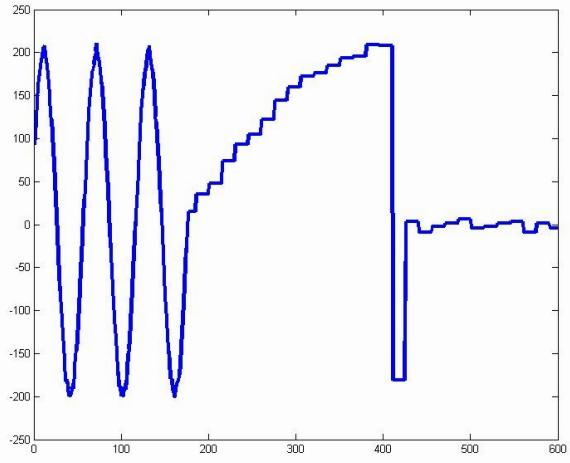
Figure 17. Baseband signals from experimental setup, at various instances of a packet, obtained at the output of low-IF to baseband downconverter.



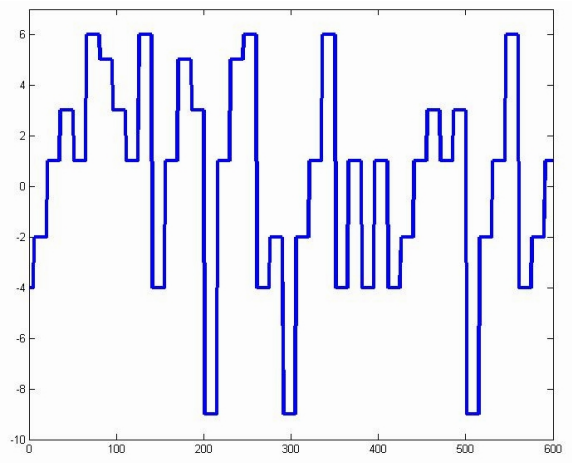
(a) Section A of Figure 16 with frequency/phase errors



(b) Section B of Figure 16, frequency/phase errors corrected



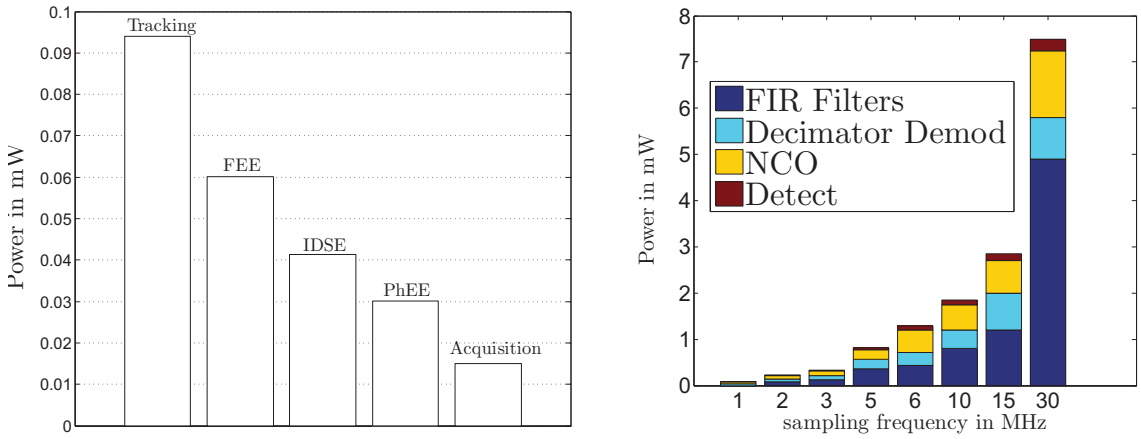
(c) Between preamble and data



(d) During data, input to digital section is 1-bit at 2Msps

Figure 18(a) and 18(b) shows the power break-up of the synchronization and data-path sections. The power is averaged over the maximum packet length. The power break up shown is obtained for Q_{dig} equal to 8-bit. As can be seen that power consumption by the synchronization unit is much smaller than the units in the data path as they are "**ON**" for much shorter duration. Among the synchronization units, the fine time tracking unit consumes the most power as it contains many correlators for estimating the fine timing. In data path FIR filters consume the largest power due to many multiply and accumulate units in it.

Figure 18. Power consumption of synchronization and data-path units, averaged over maximum length packet, for Q_{dig} = 8 bit.



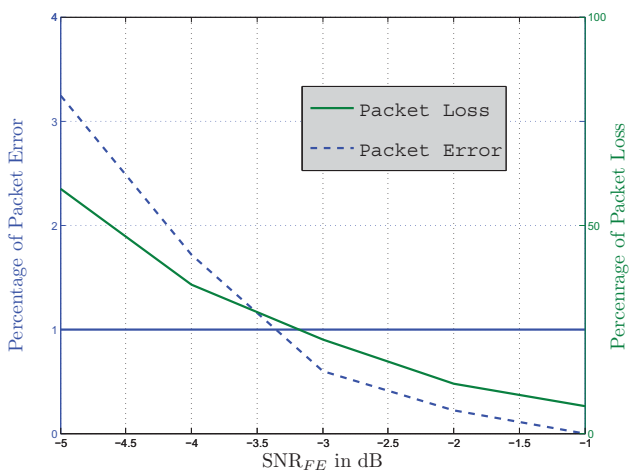
(a) Synchronization units

(b) Data-path units

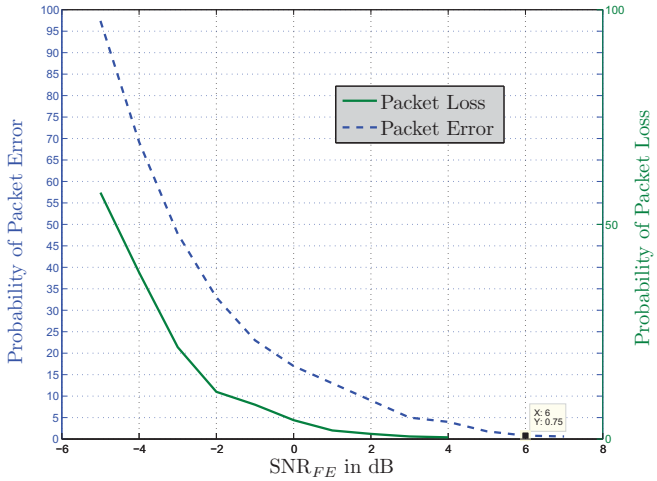
Figure 19(a) shows the measured PER *vs.* SNR_{FE} for the receiver working at 8-bit and 30 Msps. From the figure it is seen that the SNR_{FE} required to meet 1% packet error is around -3.25 dB. Whereas, from Table 1 it is seen that the minimum SNR_{FE} required is around -6 dB. As discussed earlier, non-idealities of the RF front end and the experimental setup might be the reason for this difference.

The Figure 19(b) shows the PER *vs.* SNR_{FE} when receiver works on its lowest configuration, 1-bit and 2 Msps. It is seen from this figure that the lowest SNR_{FE} meeting the error criteria is around 6 dB. Table 1 suggests that it requires around 5 dB of SNR_{FE} for 1-bit 2 Msps setting to meet the error specification. The difference can be attributed to the factors discussed above. The packet loss is nearly same in both Figure 19(a) and 19(b). This is because the synchronization section in both cases runs at same settings of Q_{dig} and f_s. Though the experimental SNR_{FE} values differ from the values obtained through simulation, the difference is not very significant from the point of verifying the idea of the power scalable receiver. The experimental results verify the claim that for different signal conditions different setting (Q_{dig}, f_s) of the receiver can be used to minimize power while meeting the error criteria. The design of the receiver proves to be working well to receive the packets with different Q_{dig} and f_s settings.

Figure 19. Experimentally obtained packet error and packet loss *vs.* SNR_{FE} for two different cases.



(a) Receiver runs at 8-bit 30 Msps



(b) Receiver runs at 1-bit, 2 Msps

7. Conclusions

We have proposed a baseband digital receiver design that changes its sampling frequency (f_s) and word length (Q_{dig}) based on interference detection and signal quality (SNR_{FE}) estimation. The approach is based on a LUT in the digital section of the receiver. Interference detector and SNR_{FE} estimator that suit this approach have been proposed. Settings of different sections of digital receiver changes as f_s and Q_{dig} vary. But, this change in settings ensures that the desired BER is achieved. Overall, the receiver reduces amount of processing when conditions are benign and does more processing when conditions are not favorable. A hardware protocol is proposed for packet based communication that facilitates power scalable design. It is shown that the power consumption by the digital baseband can be reduced by 85% (7 times) when there is no interference and P_{sig} (SNR_{FE}) is high. Design is experimentally verified and the proposed fact is established that energy condition of the hardware can be minimized when the signal condition is better.

Acknowledgement

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