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Article

Comparative Study of Charge Trapping Type SOI-FinFET Flash Memories with Different Blocking Layer Materials †

Yongxun Liu [1,*], Toshihide Nabatame [2], Takashi Matsukawa [1], Kazuhiko Endo [1], Shinichi O'uchi [1], Junichi Tsukada [1], Hiromi Yamauchi [1], Yuki Ishikawa [1], Wataru Mizubayashi [1], Yukinori Morita [1], Shinji Migita [1], Hiroyuki Ota [1], Toyohiro Chikyow [2] and Meishoku Masahara [1]

[1] National Institute of Advanced Industrial Science and Technology (AIST), 1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, Japan; E-Mails: t-matsu@aist.go.jp (T.M.); endo.k@aist.go.jp (K.E.); shinichi.ouchi@aist.go.jp (S.O.); junichi-tsukada@aist.go.jp (J.T.); hiro-yamauchi@aist.go.jp (H.Y.); yuki.ishikawa@aist.go.jp (Y.I.); w.mizubayashi@aist.go.jp (W.M.); y.morita@aist.go.jp (Y.M.); s-migita@aist.go.jp (S.M.); hi-ota@aist.go.jp (H.O.); m.masahara@aist.go.jp (M.M.)

[2] National Institute for Materials Science (NIMS), 1-1 Namiki, Tsukuba, Ibaraki 305-0044, Japan; E-Mails: NABATAME.Toshihide@nims.go.jp (T.N.); CHIKYO.toyohiro@nims.go.jp (T.C.)

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* Author to whom correspondence should be addressed; E-Mail: yx-liu@aist.go.jp; Tel.: +81-29-861-3417; Fax: +81-29-861-5170.

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Abstract: The scaled charge trapping (CT) type silicon on insulator (SOI) FinFET flash memories with different blocking layer materials of Al_2O_3 and SiO_2 have successfully been fabricated, and their electrical characteristics including short-channel effect (SCE) immunity, threshold voltage (V_t) variability, and the memory characteristics have been comparatively investigated. It was experimentally found that the better SCE immunity and a larger memory window are obtained by introducing a high-k Al_2O_3 blocking layer instead of a SiO_2 blocking layer. It was also confirmed that the variability of V_t before and after one program/erase (P/E) cycle is almost independent of the blocking layer materials.

Keywords: charge trapping (CT); flash memory; silicon on insulator (SOI); FinFET; blocking layer; high-k metal gate; variability

1. Introduction

Device scaling is very effective for the fabrication of high-density and low-cost flash memories. However, further scaling of conventional bulk planar MOSFET type flash memories becomes very difficult because of the increased short-channel effect (SCE) and the lowered source-drain (SD) breakdown voltage (BV_{DS}) with scaling down device size [1–3]. Especially, in the NOR-type flash memory, further scaling of device size faces the theoretical limit of BV_{DS} which corresponds to the silicon (Si) and silicon dioxide (SiO_2) conduction band difference (3.2 eV). This indicates that channel hot electron (CHE) programming cannot be guaranteed in the scaled NOR-type flash memories with gate length (L_g) smaller than 100 nm [2,3]. On the other hand, three-dimensional (3D) channel devices, such as fin-type double-gate (DG) MOSFET (FinFET) and fin-channel tri-gate (TG) device, provide excellent SCE immunity owing to the strong controllability of channel potential by the multiple gates [4–13]. Moreover, threshold voltage (V_t) variability in the FinFETs and TG devices is much smaller than that in the conventional bulk planar MOSFETs because the random dopant fluctuation (RDF) induced V_t variation is negligible in the FinFETs and TG devices due to the undoped fin-channels [14–22]. Therefore, the scaled charge trapping (CT) type fin-channel flash memories using silicon on insulator (SOI)-based fin-channels and body-tied bulk Si fin-channels have actively been developed [23–32]. However, a high-k blocking layer is strongly required in the ultimately scaled CT type flash memory fabrication to overcome the gate coupling area decrease with scaling down the device size [33]. As a high-k blocking layer, an Al_2O_3 layer has been used in the planar MOSFET type and body-tied bulk FinFET type flash memories [28,34]. By introducing such a high-k blocking layer, the gate injection current is effectively suppressed during program/erase (P/E) operations because the electric field across the blocking layer is proportionally reduced owing to its high dielectric constant, which is useful for the enlarging of memory window. However, the blocking layer material effect on the electrical characteristics of SOI-FinFET flash memories has not been studied sufficiently. Very recently, we have demonstrated floating gate (FG) type split-gate fin-channel flash memories with a highly suppressed over erase, and experimentally confirmed that nanosize triangular cross-section tunnel areas are useful for the fabrication of the low operating voltage flash memories owing to the enhanced local electric field at the tips of triangular tunnel areas [35–38]. We have also fabricated and investigated FG type crystalline and polycrystalline Si fin-channel flash memories with DG and TG structures, and confirmed that TG structured flash memory shows the better SCE immunity and a larger memory window than the DG structured one owing to the additional top gate and recessed buried oxide (BOX) region [39–41]. Moreover, we have also investigated the gate material effect on the electrical characteristics of the CT type SOI-FinFET flash memories by introducing different gate materials of physical vapor deposited (PVD) titanium nitride (TiN) and n^+-poly-Si [42]. It was experimentally found that a larger memory window is obtained in the PVD-TiN metal gate flash memories

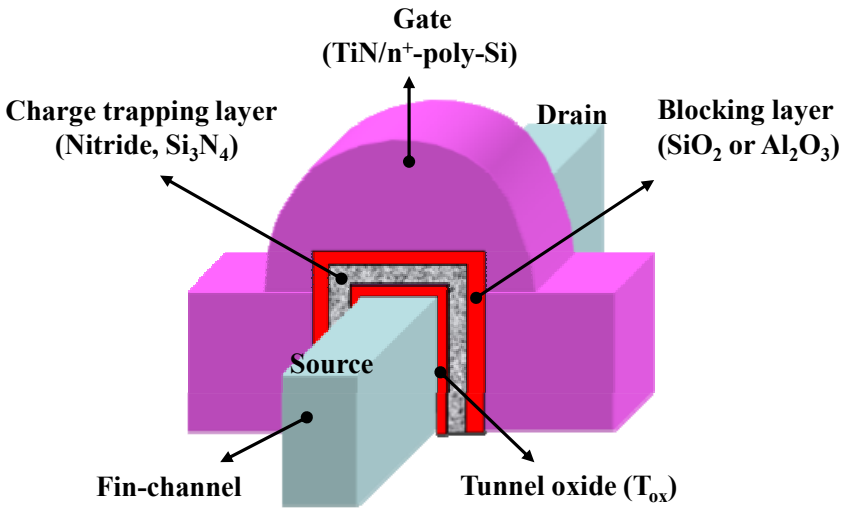
than the n^+-poly-Si gate ones owing to the higher work function of PVD-TiN metal gate, which is efficient to suppress electron back tunneling during erase operation [28,34].

As a further study, in this work, we fabricate CT type SOI-FinFET flash memories with different blocking layer materials of atomic layer deposited (ALD) Al_2O_3 and chemical vapor deposited (CVD) SiO_2, and comparatively investigate their electrical characteristics including SCE immunity, V_t variability and memory characteristics [43].

2. Device Fabrication

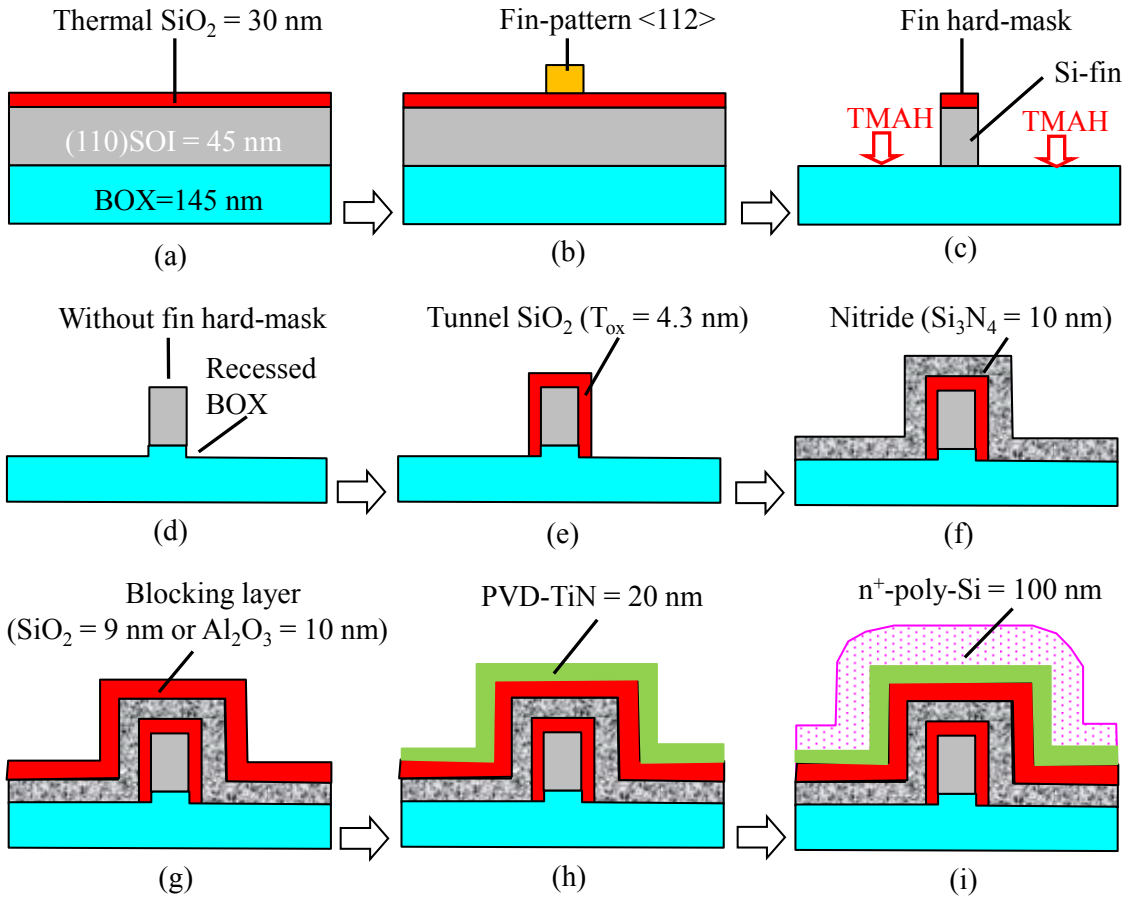
In order to investigate the blocking layer material effect on the electrical characteristics and memory properties of the CT type SOI-FinFET flash memories, we fabricated MANOS (PVD-TiN Metal-Al_2O_3-Nitride-Oxide-Silicon) type and MONOS (PVD-TiN Metal-Oxide-Nitride-Oxide-Silicon) type TG structured SOI-FinFET flash memories. Figure 1 shows the schematic three-dimensional (3D) device structure for the CT type SOI-FinFET flash memory. Except for the deposition of blocking layer materials, the same process was used in the fabrication for both types of devices. To fabricate an ideal rectangular cross-section Si-fin-channel by using the orientation-dependent wet etching, we used lightly doped p-type (110)-oriented SOI wafers as the starting material [7,8]. The initial thicknesses of the top silicon and BOX layers were 70 and 145 nm, respectively.

Figure 1. Schematic three-dimensional (3D) device structure for the CT type SOI-FinFET flash memory with different blocking layer materials of Al_2O_3 and SiO_2.



The schematic device fabrication process flow for the CT type SOI-FinFET flash memory is shown in Figure 2. First, the lightly doped p-type (110)-SOI wafers were thermally oxidized to form a 30-nm-thick SiO_2 layer as shown in Figure 2a, and fin-patterns were delineated in parallel to the <112> direction by using electron-beam (EB) lithography as shown in Figure 2b. The trimming of EB-resist was performed using oxygen plasma to reduce the fin width. The fin-patterns were then transferred to the SiO_2 layer on the (110)-SOI wafers by reactive ion etching (RIE). After removing the EB-resist, further narrowing of the width of SiO_2 hard-mask was carried out with dilute hydrofluoric acid (DHF) solution. By using these techniques, the width of SiO_2 hard-mask was controlled to around 20 nm.

Figure 2. Schematic device fabrication process flow for the CT type SOI-FinFET flash memory. (**a**) Thermal oxidation; (**b**) fin-pattern formation by electron-beam (EB) lithography; (**c**) fin-channel formation by the orientation-dependent wet etching; (**d**) SiO_2 hard-mask removing by RIE; (**e**) tunnel oxide (T_{ox}) formation by thermal oxidation; (**f**) nitride (Si_3N_4) layer deposition by LPCVD; (**g**) blocking layer (Al_2O_3 for MANOS and SiO_2 for MONOS) deposition; (**h**) PVD-TiN deposition; (**i**) n^+-poly-Si deposition.



Through the SiO_2 hard-masks, fin-channels were fabricated by the orientation-dependent wet etching with a 2.38% tetramethylammonium hydroxide (TMAH) solution at 50 °C for 30 s, as shown in Figure 2c. Since the sidewalls of the fin-channels have a (111)-oriented plane with an extremely low etching rate in TMAH compared with other planes, very narrow and straight fin-channels can easily be fabricated. It was experimentally confirmed that the etching rates for (100)-, (110)-, and (111)-oriented Si wafers were 214, 359, and 9 nm/min, respectively [44]. This indicates that the (111) plane is successfully retained in the etching process. To fabricate TG structure, the SiO_2 hard-mask layer was removed by RIE as show in Figure 2d, which results in a slight reduction of fin-height. A recessed BOX region was also formed in this RIE process, which is useful for the suppression of SCE [39–41].

After the fin-channel formation, a 4.3-nm-thick tunnel oxide (T_{ox}) layer was formed by thermal oxidation at 850 °C as shown in Figure 2e, followed by the deposition of a 10-nm-thick Si_3N_4 layer as the charge trapping layer by low-pressure chemical vapor deposition (LPCVD) at 790 °C as shown in Figure 2f. As the blocking layer, a 9-nm-thick tetraethylorthosilicate (TEOS)-SiO_2 layer was deposited for MONOS type devices by plasma CVD at 350 °C, and a 10-nm-thick Al_2O_3 layer was deposited for

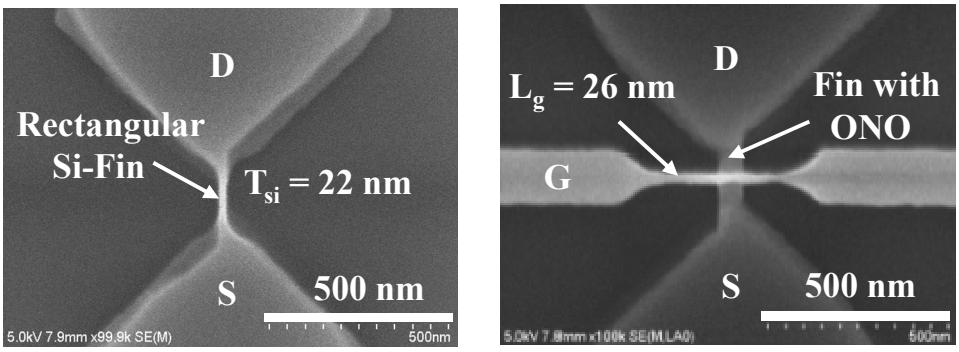
MANOS type device by atomic layer deposition (ALD) at 300 °C as shown in Figure 2g. In the ALD deposition, we used trimetylaluminum (TMA) and water gas at pressure of 14 hPa. As the same gate material, a combination of a 20-nm-thick PVD-TiN layer and a 100-nm-thick n^+-poly-Si layer, was deposited on all wafers as shown in Figure 2h,i. The gate electrodes were also patterned by EB lithography and fabricated by using combination of inductively coupled plasma (ICP) RIE for n^+-poly-Si and wet etching for PVD-TiN. In the PVD-TiN wet etching, we used an ammonium hydroxide (NH_4OH):hydrogen peroxide (H_2O_2):deionized water (H_2O) = 1:2:5 (APM) solution at 60 °C, which provides a high etching selectivity of PVD-TiN to SiO_2 [45,46].

After etching the top ONA and ONO layers on the fin extension and SD electrode regions by RIE, arsenic (As) ion implantation (I/I) was performed for SD-extension with a dose (D) of 4×10^{14} cm^{-2} and a tilting angle (θ) of 60° at a fixed implant energy of 5 keV [47]. Then, an 80-nm-thick gate sidewall spacer was formed by deposition of TEOS-SiO_2 and RIE. For the SD-region I/I, phosphorus ion (P^+) was used with $D = 1.5 \times 10^{15}$ cm^{-2} and θ = 7°, which was followed by the deposition of a 100-nm-thick TEOS-SiO_2 layer on all wafers. To activate the implanted impurities, rapid thermal annealing (RTA) was performed at 830 °C for 2 s. Finally, contact holes and aluminum electrodes were formed, and all wafers were sintered in forming gas ambient at 450 °C for 30 min.

3. Results and Discussion

The scanning electron microscopy (SEM) images of the fabricated MANOS type SOI-FinFET flash memory after fin-channel formation and gate formation are shown in Figure 3a,b, respectively. Note that a straight 22-nm-thick Si-fin channel is successfully fabricated thanks to the orientation-dependent wet etching. Moreover, a scaled 26-nm gate is also clearly confirmed.

Figure 3. SEM images of the fabricated CT type SOI-FinFET flash memory (**a**) after fin-channel formation by the orientation-dependent wet etching and (**b**) after gate formation.

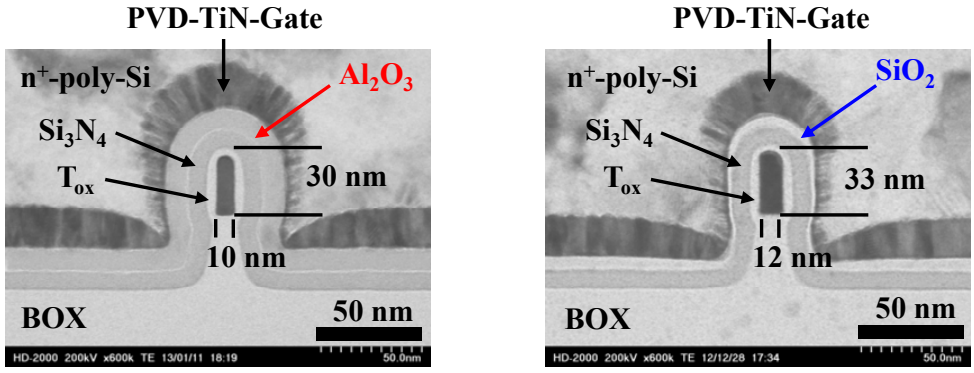


(**a**) (**b**)

Figure 4a,b show the cross-sectional scanning transmission electron microscopy (STEM) images of the fabricated MANOS and MONOS type SOI-FinFET flash memories, respectively. Note that ultrathin and ideal rectangular cross-sectional Si fin-channels are fabricated uniformly. It should be mentioned that the fin-width and fin-height were slightly narrowed and lowered during wafer cleaning and tunnel oxide formation. Moreover, it is clearly confirmed that a uniform tunnel oxide layer is formed on top and sidewalls of the fin-channels without a thick SiO_2 hard-mask on top of Si

fin-channel. This indicates that TG structure is fabricated successfully. Furthermore, it can be seen from STEM images that the charge trapping ONA and ONO layers are not only formed around the top and sidewalls of the fin-channels but also extended to the recessed BOX region. Such a gate all around (GAA) like structure is useful to the suppression of SCE as mentioned before. The observed a thin SiO_2 blocking layer (<9 nm) in Figure 4b probably depends on the pick-up position of STEM sample owing to the poor uniformity of TEOS-SiO_2 layer thickness on a wafer although a 9-nm-thick TEOS-SiO_2 layer was confirmed on a dummy wafer as mentioned before.

Figure 4. Cross-sectional STEM images of the fabricated (**a**) MANOS type SOI-FinFET flash memory with an Al_2O_3 blocking layer; and (**b**) MONOS type SOI-FinFET flash memory with a SiO_2 blocking layer.



(**a**) (**b**)

At first, we evaluated the V_t variability and SCE immunity for the fabricated MANOS and MONOS type SOI-FinFET flash memories with different gate length (L_g) values from 26 to 103 nm. Figure 5a,b show the measured initial I_d-V_g characteristics of the fabricated MANOS type flash memories with different L_g values of 26 and 38 nm, respectively. In this measurement, we used 40 cell transistors for each type to investigate statistical V_t variations. Note that an excellent S-slope of 105-mV/decade is obtained even L_g is scaled down to 26 nm due to the GAA like structure. However, the uniformity of I_d-V_g curve is slightly deteriorated with scaling down L_g from 38 to 26 nm.

To evaluate V_t variations quantitatively, we measured the initial V_t values at a constant drain current of I_d = 1 μA for all devices with different L_g values from 26 to 103 nm. Figure 6 shows the measured standard deviations of V_t (σV_t) and S-slope (σS) as a function of L_g for the fabricated MANOS and MONOS type SOI-FinFET flash memories. It is clear that almost the same σV_t and σS are obtained for both types of devices although they increase slightly with scaling down L_g. This result indicates that the variations of V_t and S-slope are almost independent of the blocking layer materials. The measured average V_t ($<V_t>$) and S-slope ($<S>$) values are summarized as a function of L_g as shown in Figure 7. Note that the smaller V_t roll-off and the better S-slope are obtained in the MANOS devices than the MONOS ones at whole range of L_g due to the high-k effect of Al_2O_3 in MANOS type devices.

Figure 5. Initial I_d-V_g characteristics of the fabricated MANOS type SOI-FinFET flash memories with different L_g values of (**a**) L_g = 26 nm and (**b**) L_g = 38 nm.

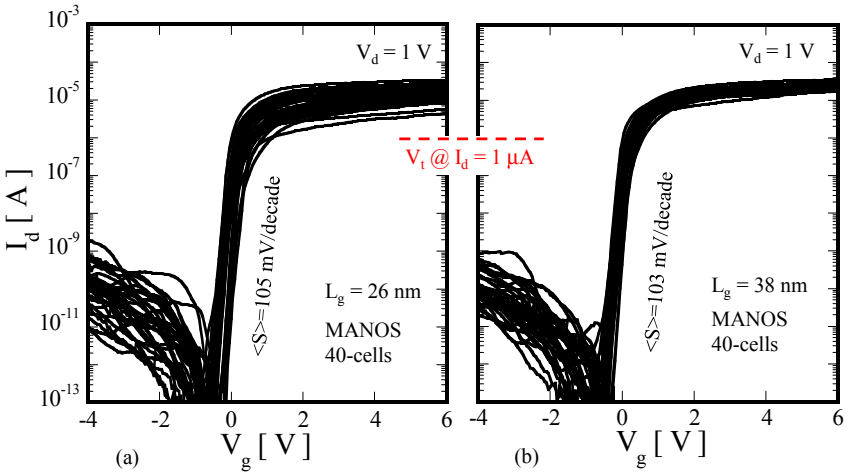


Figure 6. σV_t and σS as a function of L_g for the fabricated MANOS and MONOS type SOI-FinFET flash memories.

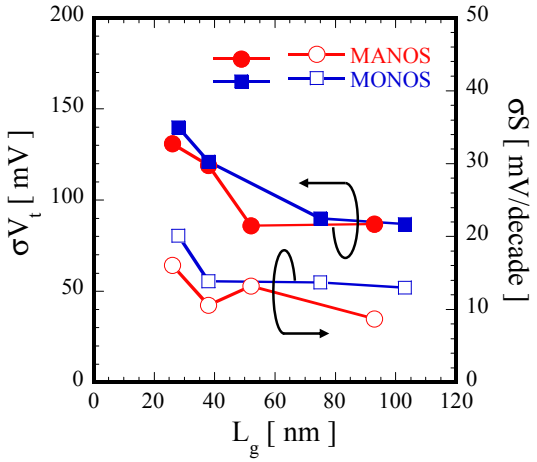
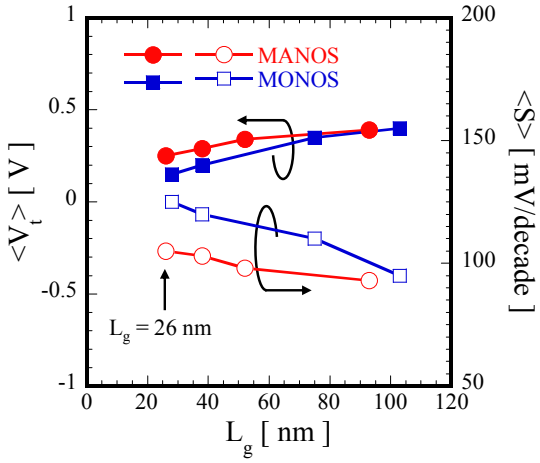


Figure 7. Average V_t (<V_t>) and S-slope (<S>) values as a function of L_g for the fabricated MANOS and MONOS type SOI-FinFET flash memories.



Before evaluation of memory characteristics, gate breakdown voltage was measured for the fabricated MANOS and MONOS type SOI-FinFET flash memory cell transistors. It was found that the gate breakdown voltage is around 17 V. According to this experimental result, P/E bias conditions were determined as V_g = 16 V, pulse-time (t) = 50 μs for programming, V_g = −16 V, t = 20 ms for erasing. In order to evaluate the dependence of the memory characteristics on the blocking layer materials, including V_t variability and memory window, the I_d-V_g characteristics of the fabricated MANOS and MONOS type devices with different L_g values were systematically investigated after one P/E cycle. Figure 8a,b show the measured I_d-V_g characteristics of the fabricated MANOS type flash memory cell transistors with different L_g values of 26 and 38 nm after one P/E cycle, respectively. In this measurement, we used 40 cell transistors for each type. It is clear that a larger memory window is reasonably obtained in the long channel devices as compared to the short channel devices. A similar behavior was also observed in the MONOS type devices.

To compare the V_t variations between MANOS and MONOS type devices, V_t values for all fabricated devices were also evaluated at a constant drain current of I_d = 1 μA. As an example, Figure 9 shows the measured cumulative probability of V_t and σV_t values for the MANOS and MONOS type devices with the same L_g of 38 nm after one P/E cycle. Note that a larger memory window is obtained in the MANOS type devices than the MONOS type ones due to the high-k effect of Al_2O_3 blocking layer in MANOS type devices. However, it is clear that σV_t values for both devices are almost the same although slightly smaller σV_t values are observed in the MONOS type device than MANOS type one. Such comparison was also carried out for all fabricated MANOS and MONOS type devices with different L_g values, and it was confirmed that actually a larger memory window is obtained in the MANOS type devices than the MONOS type ones at whole range of L_g as shown in Figure 10. The deep erase in MANOS type devices should be resulted from the high-k effect of an Al_2O_3 (k ~ 9) blocking layer, which is efficient to enhance the electric field across the tunnel oxide and to reduce the electric field across the layer its self. Therefore, the electron back tunneling is effectively suppressed during erase operation which contributes to the deep erase in MANOS type devices [28,34].

Figure 8. I_d-V_g characteristics of the fabricated MANOS type SOI-FinFET flash memory cell transistors (40 cells) with different L_g values of (**a**) L_g = 26 nm and (**b**) L_g = 38 nm. P/E conditions: V_g = 16 V, t = 50 μs for program, and V_g = −16 V, t = 20 ms for erase.

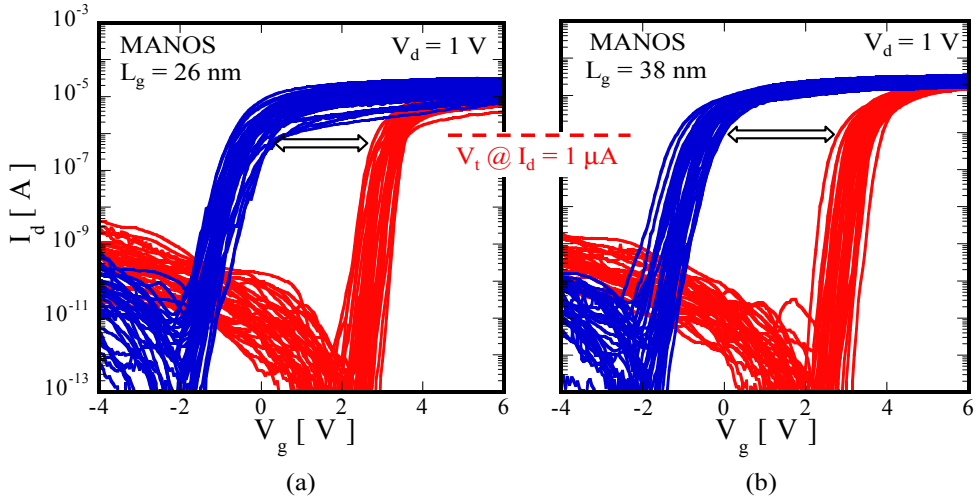


Figure 9. (**a**) Cumulative probability of V_t and (**b**) σV_t of the fabricated MANOS and MONOS type SOI-FinFET flash memories with the same L_g of 38 nm after one P/E cycle. P/E conditions: V_g = 16 V, t = 50 μs for program, and V_g = −16 V, t = 20 ms for erase.

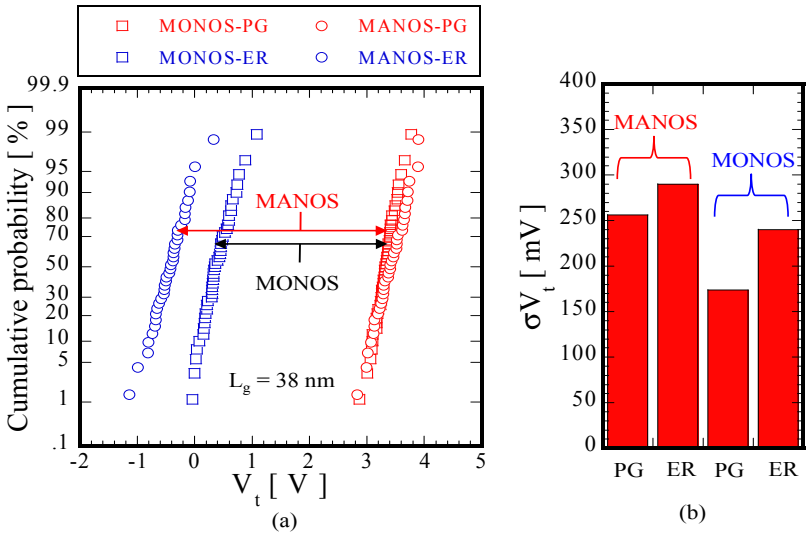


Figure 10. Average V_t (<V_t>) values as a function of L_g for the fabricated MANOS and MONOS type SOI-FinFET flash memory cell transistors after one P/E cycle. P/E conditions: V_g = 16 V, t = 50 μs for program, and V_g = −16 V, t = 20 ms for erase.

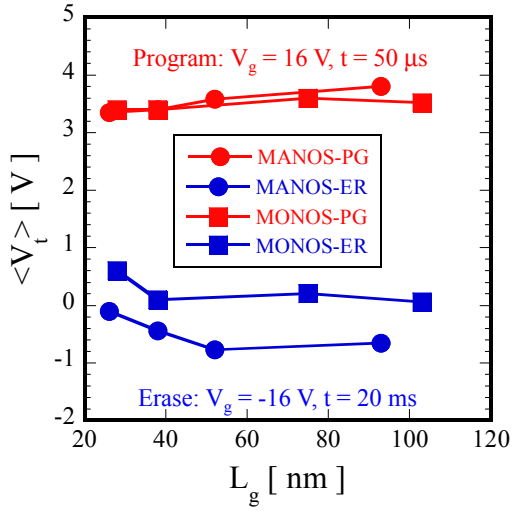


Figure 11a shows the measured P/E characteristics of the fabricated MANOS type device with L_g of 93 nm at different $|V_g|$ values, and the program-time dependence of the I_d-V_g characteristics at V_g of 14 V is shown in Figure 11b. It is clear that a large memory window of 5.6 V is obtained keeping an excellent S-slope of 100-mV/decade due to the GAA like structure. Figure 12a,b show the measured endurance characteristics of the fabricated MANOS and MONOS type devices, respectively. Note that these two kinds of device can operate over 100 k cycles although somewhat remarkable degradation is observed in the MONOS type device after 10 k cycles probably due to the insufficient uniformity of CVD-SiO_2 blocking layer. Moreover, the better data retention is obtained in the MANOS type device than MONOS type one due to the uniform ALD-Al_2O_3 blocking layer as shown in Figure 13.

Figure 11. (**a**) P/E characteristics and (**b**) program-time dependence of the I_d-V_g characteristics of the fabricated MANOS type SOI-FinFET flash memory with L_g = 93 nm.

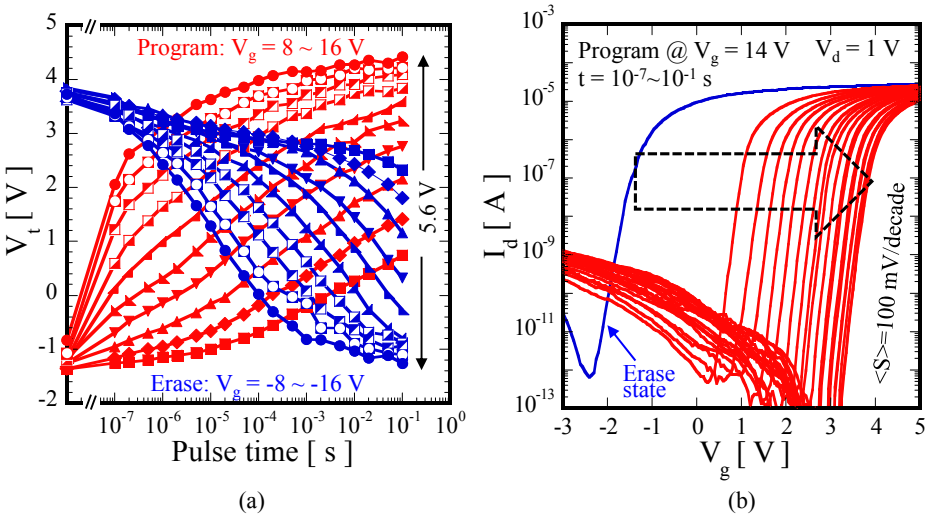


Figure 12. Endurance characteristics of the fabricated (**a**) MANOS type SOI-FinFET flash memory with L_g = 93 nm; and (**b**) MONOS type SOI-FinFET flash memory with L_g = 103 nm.

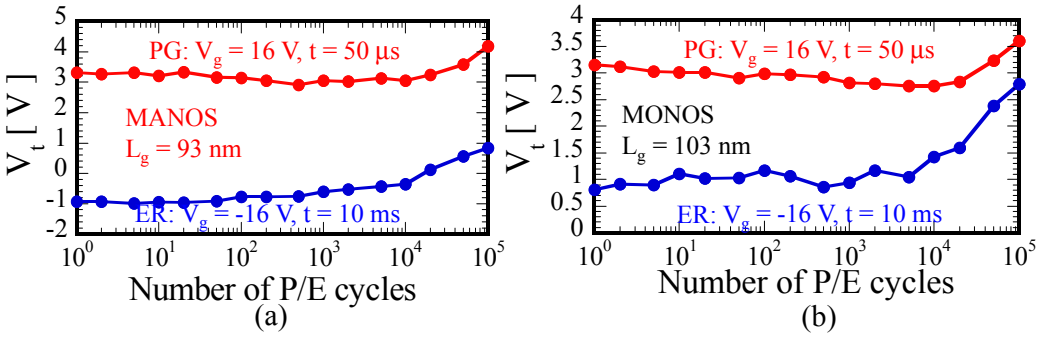
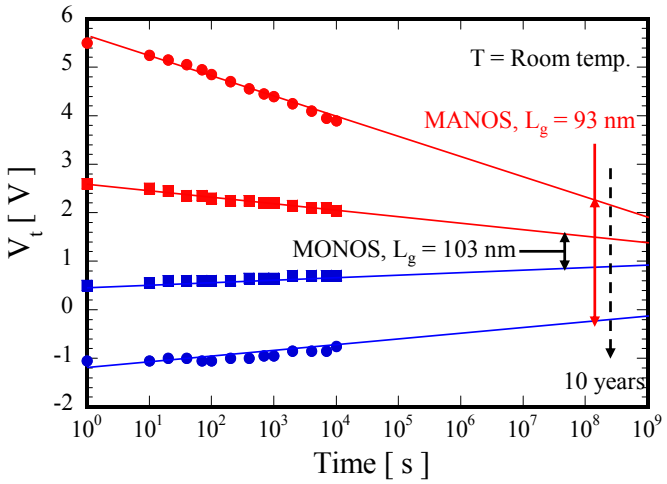


Figure 13. Retention characteristics of the fabricated MANOS type SOI-FinFET flash memory with L_g = 93 nm and MONOS type SOI-FinFET flash memory with L_g = 103 nm at room temperature.



4. Conclusions

We have comparatively investigated the electrical characteristics and memory properties of the fabricated charge trapping type SOI-FinFET flash memories with different blocking layer materials of Al_2O_3 and SiO_2. It was experimentally found that introducing a high-k Al_2O_3 blocking layer instead of a SiO_2 one is very efficient for the enlarging of memory window owing to the high-k effect of Al_2O_3. It was also confirmed that V_t variability before and after one P/E cycle is almost independent of blocking layer materials.

Acknowledgments

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Conflicts of Interest

The authors declare no conflict of interest.

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