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Review

Mastering the Art of High Mobility Material Integration on Si: A Path towards Power-Efficient CMOS and Functional Scaling

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Abstract: In this work, we will review the current progress in integration and device design of high mobility devices. With main focus on (Si)Ge for PMOS and In(Ga)As for NMOS, the benefits and challenges of integrating these materials on a Si platform will be discussed for both density scaling ("more Moore") and functional scaling to enhance on-chip functionality ("more than Moore").

Keywords: high mobility materials; III-V; (Si)Ge; CMOS

1. Introduction

Over the last years, new trends and applications have emerged which will have large economical and societal impact: new computing paradigms like neuromorphic [1] and quantum computing [2], big data and internet-of-things (IoT) [3]. New functionalities will be needed and the key enabling circuits and systems will require a variety of different devices and technologies co-integrated on the same platform. At the core of the hardware innovations will be new process technologies that not only allow for more power-efficient CMOS transistors but also specialized devices to enable new on-chip functionality, e.g., RF/analog, near-threshold Logic, high-speed I/O, optoelectronics, *etc.* At the most detailed level, co-integration of different beyond-Si materials like Ge, III-V, SiGe, *etc.*, with Si will require significant innovations in defect, stress, and process thermal budget management. In this paper, we will address these challenges and the progress made to overcome them. Moreover, we will elaborate on the advantages of using these materials for both extending density scaling and increasing on-chip functionality.

2. High Mobility Materials

(Si)Ge and III-V materials can intrinsically deliver higher hole and electron mobilities than Si: a bulk hole mobility of 1900 cm^2/Vs [4] has been reported for Ge (*versus* 500 cm^2/Vs in Si) and electron mobilities in InGaAs and InAs can be as high as 70,000 cm^2/Vs [5]. This is especially important when scaling down the supply voltage and thus reducing the power density in advanced technologies while still being able to increase the performance at these reduced voltages [6]. The replacement of Si by high mobility materials is not without challenges: to be economically viable and since co-integration with Si devices will be necessary, these materials need to be integrated on a Si platform. The mismatch between Si and Ge is about 4%, and for III-V this can go up to 12% in the case of InAs. As such, achieving material with low defectivity is one of the key concerns. Next to that, finding a gate stack with low interface and high-k dielectric defects could be one of the show stoppers. Finally, the trade-off between performance, leakage and as such scalability will also need to be addressed for the high mobility devices.

In the next sections, we will discuss the challenges related to gate stack, material integration and device scalability. In the last technical section, we will demonstrate that beyond the typical CMOS

scaling these materials could also play a very important role in enhancing the system functionality by providing very specific key components.

3. Ge and III-V Integration on Si Substrates

The lattice mismatch between Si and Ge is 4%. As such growing Ge directly on Si will give rise to the formation of defects which can impact both the leakage and the performance of the devices [7]. The lattice mismatch between InP and In(Ga)As with Si is even higher than for Ge, about 8% and up to 12% for InAs. Specifically, for III-V, the presence of anti-phase boundaries (APB), which occur at the interface between the non-polar (group IV) and polar (group III-V) semiconductors, can pose an even higher challenge for hetero-epitaxy of III-V on Si.

Virtual SiGe [8], Ge and III-V [9] buffer layers on bulk Si wafers have been demonstrated. Typically, 1–2 μm thick layers need to be grown and post-deposition TDD (threading dislocation density) anneals are required to lower the defect density. To date, defect densities as low as 10^6 cm^{-2} have been reported for SiGe [8]. Reported defect levels for III-V on 300 mm Si are, however, significantly higher: 1–2 × 10^9 cm^{-2} [9]. The latter substrates also require a more complex stack consisting of combinations of GaAs, InP and InAlAs to fabricate the required top InGaAs channels.

Starting from these virtual $Si_{1-x}Ge_x$ buffers, either a Ge or $Si_{1-y}Ge_y$ (y > x) top layer can be grown for the PMOS, thereby introducing compressive strain in the channel, while for NMOS, using the same buffer layer (common buffer), a tensile strained Si layer can be grown, thereby allowing integration of both NMOS and PMOS on the same substrate. In [10], Kian-Hui *et al.* demonstrated the co-integration of InAs NMOS and GaSb PMOS using an ultra-thin III-V buffer on Si. As the channel layers are introduced from the very beginning in the process flow, the thermal budget needs to be well controlled, thereby necessitating a lowering of the temperature for the Shallow Trench Isolation (STI) when planar or bulk FinFET devices are considered. In [11], 15 nm wide strained Ge FinFET devices on $Si_{0.25}Ge_{0.75}$ substrates were demonstrated using a novel low temperature STI process.

However, the high substrate cost and potential concerns with self-heating make the virtual buffer approach a lesser viable option for large scale integration. Reports [12] have shown that strained Ge FinFET devices fabricated on SiGe buffers can show up to 115% increase in temperature as compared to Si at scaled dimensions and realistic operating conditions.

An alternative way of introducing these materials is by GeOI/IIIVOI (Germanium-on-Insulator/III-V-on-Insulator) substrates [13,14]. In the case of Ge, these substrates can be fabricated either by bonding of a Ge donor wafer to an oxidized Si handle wafer or by the Ge condensation method, where a SiGe layer grown on a standard SOI (Silicon-On-Insulator) wafer is oxidized thereby turning the SiGe layer into a Ge-rich layer. Recent work by P. Hashemi *et al.* shows that highly performing SiGe-on-Insulator FinFET devices with fin widths below 10 nm and hole mobility around 300 cm^2/Vs can be achieved for a Ge content of 71% [15]. Co-integration of III-V NMOS and Ge PMOS [16] has been demonstrated, starting from a Ge wafer and using wafer bonding to transfer the III-V layer on the common Ge substrate. Specifically, for III-V, L. Czornomaz *et al.* have demonstrated the Confined Epitaxial Lateral Overgrowth (CELO) technique as an alternative way to fabricate III-V on insulator substrates [17].

The latter technique is partially based on the fin replacement technique which is a more elegant solution to grow the different materials selectively in specific areas where needed. This integration scheme can be used for both (Si)Ge and III-V devices. A typical process flow, in this case for III-V, is shown in Figure 1 [18]. The process flow starts from 300 mm Si substrates. In a next step, a standard STI is fabricated, which as such makes this overall integration scheme also compatible with more advanced Self-Aligned Double (SADP) and Quadruple (SAQP) patterning schemes. The Si is then recessed using TMAH and the InP buffer layer is grown using Metal Organic Vapor Phase Epitaxy (MOVPE). The function of this layer is two-fold: firstly, all defects need to be confined in this layer in order to allow the growth of a low defective InGaAs channel layer and secondly it can be used to improve the electrostatic control because the band-offset between InP and InGaAs allows us to

confine the carriers more effectively in the channel. When the InP is grown on a {111} plane after the TMAH etch, a 10 nm thick complex network of twins is formed at the interface with Si. Above this twinned region, the InP lattice is already aligned with that of the underlying Si and the generation of misfit dislocations along the channel are also avoided by initiating the growth on these Si {111} planes of the V-groove. Next to that, no vertical defects such as anti-phase boundaries are observed despite the starting substrates being on-axis Si (001) substrates. This is again attributed to the use of the V-groove [19]. Apart from the introduction of V-grooves, optimization of the nucleation layer is key to grow lowly defective InP in trenches smaller than 50 nm [18]. In a next step, Chemical Mechanical Polishing (CMP) is used to reduce the thickness and planarize the structures. A wet HCl-based etch is then used to recess the InP and subsequently the InGaAs channel is grown. When keeping the indium content to 53%, the channel is lattice-matched to the underlying InP layer and the amount of defects in the channel can be significantly reduced. A second CMP step is used to planarize the channel. The STI is recessed prior to gate patterning to form the fin. Using a modified version of this fin, replacement flow has been used for Ge-based devices and strained Ge FinFETs with fin widths down to 13 nm and a fin pitch of 45 nm have been demonstrated using this technique [20].

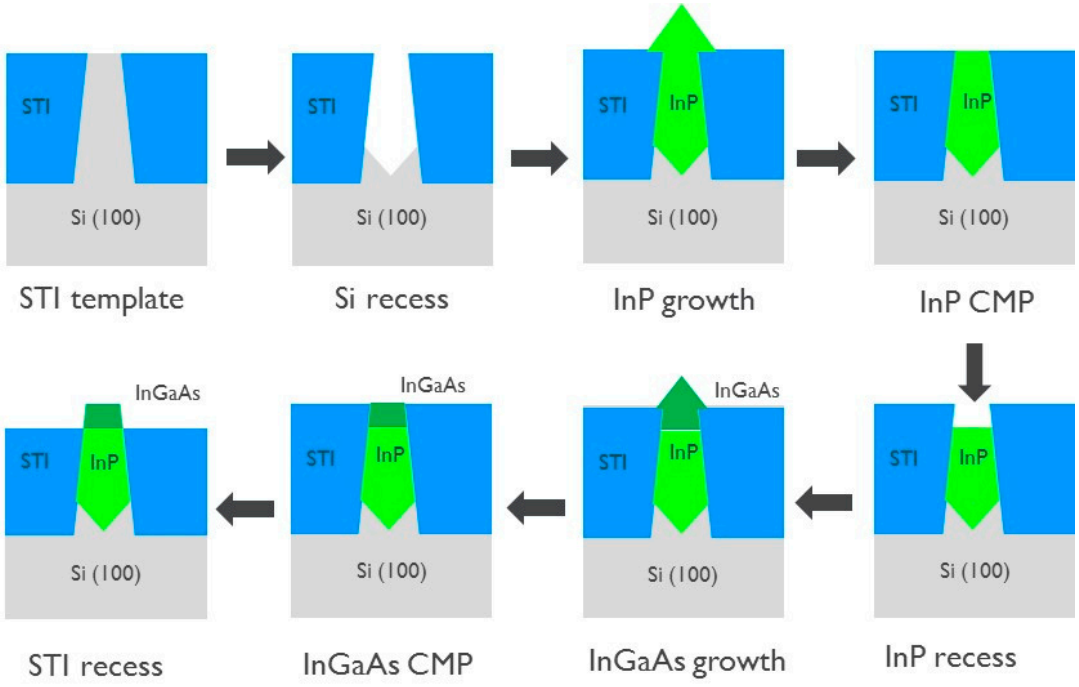

Figure 1. Schematic presentation of the fin replacement process; in this case demonstrated for the channel formation of InGaAs FinFETs.

4. Innovations in Gate Stack

Whereas Si has a stable oxide, the passivation of (Si)Ge and III-V is much more complex and the formation of a gate stack with low interface and gate dielectric defects is one of the major challenges for high mobility materials. Reduction of the defects at the interface and in the dielectric is key to improve performance and electrostatic behavior, next to achieving the required reliability performance.

In the case of Ge, the GeO_2 interface layer is thermodynamically unstable and the layer decomposes in sub-oxides Ge_yO_x at temperatures higher than 400 °C [21]. Dangling bonds at the interface cannot be H-passivated by typical Si-based forming gas anneals. Although a lot of research has been spent on trying to find a reliable and scalable gate stack, only a few routes are being pursued at this moment for Ge and SiGe channels. The first approach uses the growth of a thin Si cap layer on top of the high mobility material, which is then subsequently partially or fully oxidized [22].

This can be combined with standard high-k materials like HfO_2 and the approach is compatible with FinFET topography and can be used on both Ge and SiGe. For SiGe, the pre-clean before Si cap growth is more challenging [15] than in the Ge case. Using this approach, extremely good Bias Temperature Instability (BTI) has been shown [23] for Ge PMOS devices (Figure 2). BTI is responsible for a significant shift in device parameters and as such limits the overall device lifetime, represented by the maximum overdrive voltage. This improvement can be attributed to the fact that only a part or small amount of the oxide traps in the high-κ layer is accessible by the carriers in the channel. The main concern remaining for this gate stack is its scalability: the depleted Si layer contributes to the inversion capacitance, making the Capacitance Equivalent Thickness (CET) or T_{inv} larger.

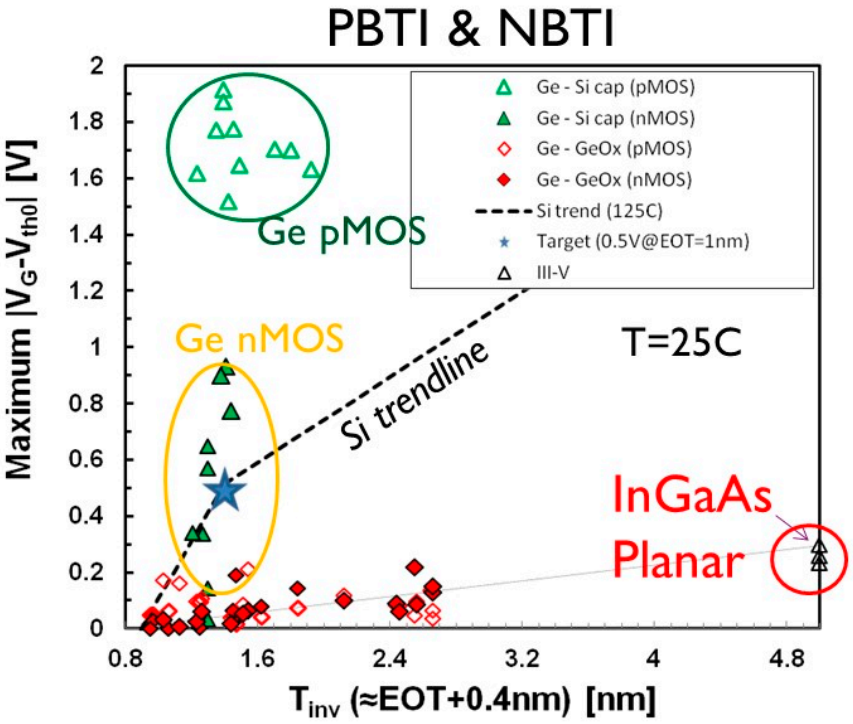

Figure 2. Benchmark plot of maximum overdrive for advanced CMOS technologies. This maximum overdrive represents the maximum overdrive voltage $|V_{GS}-V_T|$, which is allowed to ensure 10 years of reliable continuous operation. Si-passivation of Ge channels yields extremely good reliability for PMOS and is also beneficial for NMOS. GeOx-based gate stacks, however, show much degraded reliability performance, similar to the InGaAs case using Al_2O_3 as gate dielectric, directly on the III-V channel.

The second approach uses plasma oxidation through a thin Al_2O_3 layer, using Atomic Layer Deposition (ALD). This has been demonstrated for both Ge PMOS and NMOS [24]. The idea behind the approach is that the Al_2O_3 acts a protecting layer to prevent subsequent damage to the GeO_x interface layer and also acts as an oxygen barrier to form ultrathin GeO_x layers with high thickness controllability. However, while this seems to be a more scalable approach, the reliability performance of this gate stack has so far not been shown to outperform the Si-cap based gate stack (Figure 2).

The latter approach has also been tried on III-V [25]. While reduction in interface traps and hysteresis has been shown, significant improvements in gate stack performance are needed to show the real potential of III-V [26]. In general, the passivation of the III-V/high-k interface is even more challenging than (Si)Ge as several defect states can be found in the band gap, related to Ga-O, As-O, Ga- or As-dangling bonds. Ga-O and Ga-dangling bonds are responsible for defect states close to the conduction band while As-O and As-dangling bonds are responsible for the states close to the valence band [27]. The midgap states originate from the As and Ga vacancies coming from the surface oxidation itself [28] and are different from the former defects, which cannot be removed by wet

chemical treatment or the self-cleaning effect of the ALD deposition of the high-k layer [29]. For InGaAs, a large defect peak is observed close to the valence band edge and a smaller peak exists at mid gap [27]. Both peaks are donor peaks and are uncharged when the Fermi level is close to the conduction band edge. As such, this is beneficial for the on-state but can lead to degradation of the subthreshold swing and higher off-state leakage. Fermi-level pinning by acceptor-like traps in the conduction band, however, severely degrades the on-state performance of the devices.

Next to that, the interaction of the carriers with traps in the gate dielectric can lead to frequency dispersion in both the CV and the MOSFET transconductance curves, leading to hysteresis. The charging of slow traps leads to stress-time dependent threshold voltage shifts and can impact the overall device reliability significantly (Figure 2). J. Franco *et al.* showed that larger median shifts and aging-induced variance are seen in InGaAs FinFETs w.r.t. their Si counterparts. The latter can be attributed to a larger stochastic impact of single defects on the device characteristics [30], showing that suppressing the defectivity in the channel, at the interface, and in the gate oxide is crucial for the successful introduction of III-V devices.

5. Performance of Scaled High Mobility Devices

The overall concern with high mobility materials is their lower bandgap as compared to Si. This reduced bandgap can give rise to an increased off-state leakage, even at lower supply voltage. Next to that, the reduced scalability as compared to Si, gives rise to higher subthreshold leakage for a given gate length and fin width. The main concern is, however, the higher junction leakage and especially the extension leakage. It was already shown that this extension leakage is dominated by the band-to-band tunneling (BTBT) at the extension/channel side, which is intrinsic to the low bandgap of these materials and cannot be impacted by, e.g., reducing the amount of defects [31,32]. Junction engineering and reduction of the supply voltage can help to reduce the electric field at the drain junction. In [31], it is also shown that for supply voltages below 0.7 V, extension leakage currents below 100 nA/μm can be obtained, thereby fulfilling the high performance (HP) targets. LOP (low operating power) and LSTP (low standby power) specifications will require much higher reduction of the electric fields and as a consequence this will limit the drive current significantly. In that respect, SiGe is an interesting material for PMOS [33]: while the hole mobility is not as high as for Ge, up to 85% Ge its bandgap is very Si-like, thereby allowing us to control the BTBT leakage more effectively.

While for future technology nodes the fin width or the nanowire diameter will need to be scaled down well below 10 nm, the increased quantization effects will give rise to an increase of the bandgap which might be beneficial to reduce this BTBT leakage [34,35]. However, this will go at a cost of decreased mobility as was already shown in [36] for III-V channels and trade-off between leakage and performance will be needed.

Finally, Figures 3 and 4 show the maximum saturation transconductance, a measure for mobility, as function of subthreshold swing, measure for short channel behavior, for different (Si)Ge and III-V devices reported in the literature.

Scaled Ge and SiGe PMOS devices with high performance have been shown at reduced supply voltage, demonstrating the clear potential of these alternative materials. In the case of III-V, the highest Q-factors ($Q = G_{m,sat}/SS_{sat}$) are found for devices with higher In-content channels showing the benefit of the higher electron mobility, and fabricated on small size InP or Si substrates, using either thick buffer layers or III-V on insulator substrates, indicating the importance of defect control. The subthreshold swing can be kept under control by using either a Quantum Well (QW), FinFET or nanowire structure. However, over the last years, also significant improvement in performance has been shown for the InGaAs/InP FinFET [18] and nanowire devices [26,37], monolithically integrated on 300 mm Si substrates.

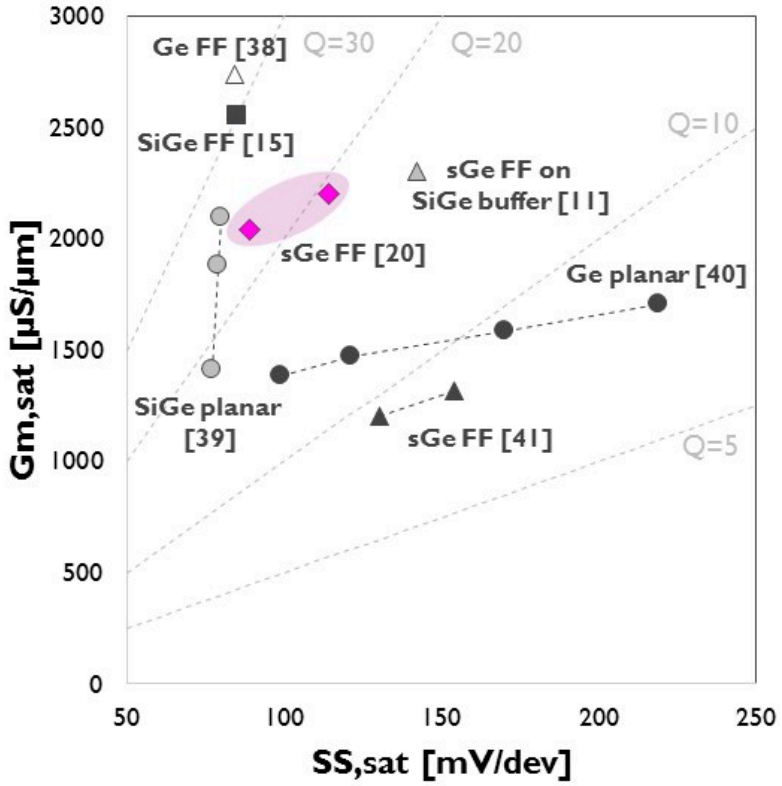

Figure 3. Peak extrinsic transconductance as a function of subthreshold swing measured at V_{DS} = −0.5 V comparing different (Si)Ge devices, both planar and FinFET (FF), reported in the literature [11,15,20,38–41].

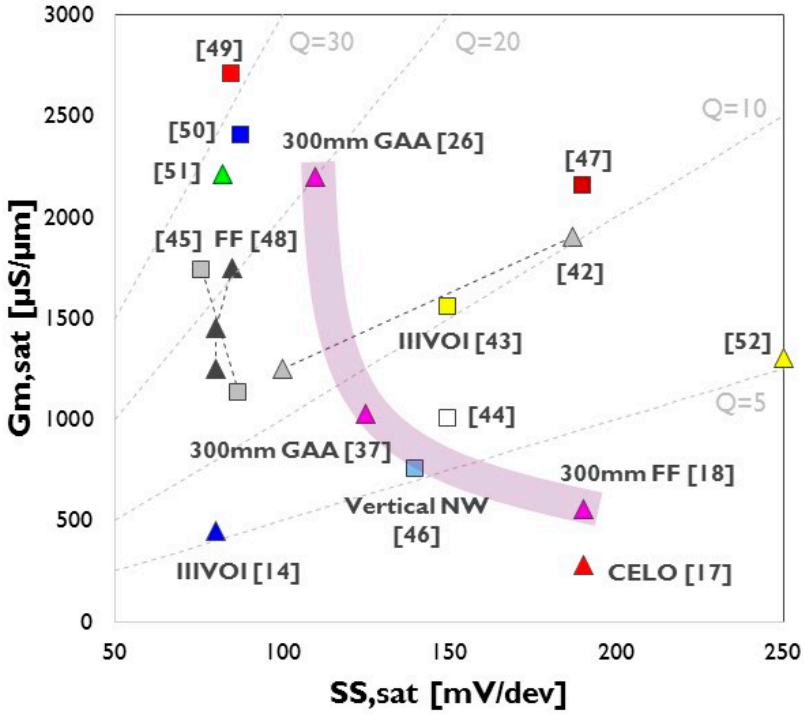

Figure 4. Peak extrinsic transconductance as function of subthreshold swing measured at V_{DS} = 0.5 V comparing different InGaAs (triangles) and InAs (rectangles) devices reported in the literature; FF = FinFET, GAA = Gate-All-Around and NW = nanowire [14,17,18,42–52].

6. Towards Functional Scaling

Standard density scaling is going through rough times with increasing difficulties of reducing the metal and gate pitch. Instead of scaling the gates and devices, there is increasing interest in adding more functionalities to the system rather than reducing the overall footprint of the devices. In particular, applications like IoT, new computing technologies and 5G will require the combination of analog/RF, mixed signal, memory, sensors and digital technologies. While this brings along new challenges, novel power-efficient circuits and systems can be designed in this way. Especially in the context of high mobility materials, one can think of the co-integration of III-V and (Si)Ge photonics for off-chip/on-chip optical interconnections and sensors [53] with high mobility CMOS. Arrays of InP lasers monolithically integrated on 300 mm Si have recently been demonstrated [54], essentially using the fin replacement technique to grow the InP layer in V-grooved Si trenches.

Even more interesting is the use of III-V for RF. III-V High Electron Mobility Transistors (HEMT) are already in standard use for high frequency applications where cutoff frequencies exceeding 1THz [55] have been demonstrated. The RF performance of these devices significantly outperforms that of standard CMOS devices, especially when considering FinFET which suffers from intrinsically higher parasitics. Next to that, III-V and (Si)Ge heterojunction bipolar transistors (HBT) have also shown great potential when high speed requirements need to be fulfilled [56].

So far, Si and III-V circuits have always been fabricated and packaged separately, and then later assembled on the same carrier substrate, which does not really allow the optimization of performance, reduction of power, cost and form factor, and increase in the complexity of the circuit [57]. Circuits that could benefit from a Si/III-V hybrid approach are power amplifiers (PA) [58], low noise amplifiers (LNA) and voltage controlled oscillators (VCO).

Different integration schemes can be considered: apart from the co-integration in the same plane, 3D monolithic integration is being considered where the III-V devices are built on top of the Si CMOS [59]. As the III-V processing requires much reduced temperatures, these are perfect materials to process on top of Si CMOS.

7. Conclusions

For the 7 nm technology node and beyond, high mobility materials like (Si)Ge and III-V are being considered for high performance devices at reduced supply voltage. While high electron and hole mobilities can be achieved using these materials, surface passivation, the design of a reliable and scalable gate stack and the fabrication of substrates with low defectivity are still the major challenges for this technology where both wide bandgap materials and low bandgap high mobility materials need to be co-integrated on the same wafer.

Beyond the standard density scaling, these materials will play a key role in enhancing the functionality of future electronic systems, allowing the co-integration of Si CMOS with specialized components like III-V HEMT or HBT.

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