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Design of a Wideband Antenna for Wireless Network-On-Chip in Multimedia Applications

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Abstract: To allow fast communication—at several Gb/s—of multimedia content among processors and memories in a multi-processor system-on-chip, a new approach is emerging in literature: Wireless Network-on-Chip (WiNoC). With reference to this scenario, this paper presents the design of the key element of the WiNoC: the antenna. Specifically, a bow-tie antenna is proposed, which operates at mm-waves and can be implemented on-chip using the top metal layer of a conventional silicon CMOS (Complementary Metal Oxide Semiconductor) technology. The antenna performance is discussed in the paper and is compared to the state-of-the-art, including the zig-zag antenna topology that is typically used in literature as a reference for WiNoC. The proposed bow-tie antenna design for WiNoC stands out for its good trade-off among bandwidth, gain, size and beamwidth vs. the state-of-the-art.

Keywords: new trends in Network-on-Chip (NoC) architectures; on-chip antenna; networks-on-chip; wireless on-chip communications; multimedia communications

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1. Introduction

The complexity of multi-processor systems-on-chip (MPSoC) computing systems is continuously increasing [1–3]. Implementing multiple on-chip processing cores, and relevant memories, the bottleneck of the computing system becomes the inter-processor communication. To solve the inter-tile communication issue, the state-of-the-art has been characterized by the evolution from standard circuit-switched bus communications, e.g., SoC based on AMBA (Advanced Microcontroller Bus Architecture) bus as in [4], to packet-switched Network-on-Chip (NoC). This is the case of both homogeneous and heterogeneous MPSoCs [5,6]. In Homogeneous MPSoCs [7–10], all the interconnected tiles are of the same type; for example, eight MagicDSP tiles, each integrating an ARM^{TM} core plus a VLIW (Very Long Instruction Word) processor, are interconnected through a NoC in [8]. Instead, multiple ARM Cortex cores are integrated on-chip in [10] to implement cloud sever-on-chip solutions. Other examples of homogeneous NoCs are in Ref. [7,9]. In heterogeneous MPSoCs, the tiles are different, see examples in [11–16]. Particularly in multimedia applications, programmable general-purpose cores can be integrated with memories and with co-processors for computing intensive applications. The co-processors are usually integrated as synthetizable IP (Intellectual Property) macrocells for computing intensive tasks such as video coding, motion estimation/compensation, noise removal or image enhancement, and multi-dimensional transforms [17–22].

The NoC is organized as a conventional ISO/OSI (International Standard Organization/Open Systems Interconnection) stack of layers. Indeed, a NoC aims at bringing on-chip the technologies already developed for computer and telecommunication networks [2,23–36]. The key building blocks of a NoC are routers [23–27], network interfaces (NI) [28], and links [29–33]. This paper will focus on links. Particularly, at the bottom of the stack, in the physical layer, conventional metal-wired links are characterized by the following limits:

- poor scalability;
- increased delay when transferring high data rates—at several Gb/s—among cores and/or memories placed at distances greater than 1 cm;
- increased power consumption to switch—at continuously increasing frequencies—the large capacitance offered by long metal wires.

In the recent literature, optical [31,34,35] or wireless [25,27,31,37–44] links are investigated as an alternative solution to classic metal wires to reduce latency and power consumption issues. Wireless NoC (WiNoC) links are easier to integrate on-chip with respect to silicon photonic solutions that, instead, are not yet mature enough to represent a reliable on-chip networking technology.

One of the main technology bottlenecks for WiNoC is printing the antenna on-chip, e.g., using top metal layers. As a matter of fact, using scaled CMOS (Complementary Metal Oxide Semiconductor) technologies, there are several works published in literature, operating from a few GHz to mm-waves, which already integrate on-chip the transmitter and the receiver, see Ref. [45–55]. Also, for the Analog–Digital converter [45,55] and for the building blocks of a NoC (e.g., NI, Router, Link in [23–33]) there are many works proposing on-chip integrated solutions. Instead, for the antenna, there are still open issues on optimizing the trade-off between area, gain and bandwidth. For example, the survey work [56] also declares that the on-chip antenna is still one of the most difficult components to integrate on-chip. Moreover, [56] declares that, although implementations of on-chip antennas have been proposed and studied in literature, there are still many challenges in manufacturing and integrating them in terms of area, performance, and energy overheads, especially as the number of on-chip cores will be scaling up in the future.

Within the above scenario, this work presents the design of a mm-wave antenna, with bow-tie topology, which ensures a compact size implementation and a high bandwidth, suited for WiNoC applications. The large bandwidth of the WiNoC antenna is important to achieve high data-rate connections also in the case of simple modulation schemes with low spectrum efficiency.

After this introduction, the rest of the paper is organized as follows. Section 2 presents the antenna architecture design, whereas Section 3 discusses the design of the layout and the performance characterization of the antenna. A comparison of the proposed antenna vs. the state-of-the-art is addressed in Section 4. Section 5 discusses the impact of the proposed antenna on the performance of the NoC infrastructure. Conclusions are drawn in Section 6.

2. Design of the On-Chip High-Bandwidth Antenna

For the antenna operating frequency, the spectrum range of mm-waves (literally 30 GHz–300 GHz; in this work, restricted to 50 GHz–100 GHz) has been selected. As it has been demonstrated in Ref. [57–67], transceivers operating at such high frequencies can be designed using low-cost and low-power CMOS technologies. Above 50 GHz, the wavelength amounts to a few millimeters. This aspect is useful to reduce the size of the transceiver and of the antenna with respect to other designs operating at frequencies in the X Band (10 GHz) or below (at sub-GHz frequencies), see as an example Ref. [39,68–71].

In literature, a widely used mm-wave frequency range is the spectrum around 60 GHz. Indeed, this spectrum range is already used in high bandwidth communications due to the availability of a large unlicensed spectrum from 57 GHz to 66 GHz. Industrial alliances such as WiGiG or Wireless HD already use the 60 GHz spectrum.

It is worth noting that cm-range communications in WiNoC applications do not suffer from licensing issues since they are spatially limited and self-contained. Therefore, for WiNoC applications, a large spectrum can be addressed, from 50 GHz to 100 GHz in this work. Indeed, new CMOS SOI (Silicon on Insulator) technologies, characterized by a transition frequency Ft of 300 GHz, or higher, allow operating up to 100 GHz.

To meet this high bandwidth value, a wide band antenna design is proposed in this paper. To this aim, a bow-tie antenna topology, see Figure 1, is proposed. In classic antenna design, such as the zig-zag antenna proposed for WiNoC in [31,37], the size of the antenna depends on the wavelength. Therefore, a conventional antenna is frequency-specific. Instead, the proposed bow-tie antenna is specified by angles and hence the bow-tie antenna is inherently a wideband antenna. With respect to an ideal bow-tie design, the antenna in Figure 1 has the following innovations:

- custom circuitry for antenna–driver matching
- rounded corners to reduce charge accumulation phenomena

Figure 1 shows the layout of the antenna with reference to implementation in a 65 nm SOI CMOS technology. Table 1 shows the values of the design parameters of the bow-tie antenna (L1, L2, L3, W1, W2, W3 and angle α in Figure 1) and of the length and width (L4 and W4 in Figure 1) of the Co-planar Stripline (CPS), which connects the bow-tie antenna to the single-ended port of the transceiver (antenna feed in Figure 1). It is to be noted that the bow-tie antenna is characterized by both horizontal and vertical symmetry, and hence the values of the parameters in Table 1 are valid for both the right and left parts, and for both the top and bottom parts of the bow-tie antenna. Table 1 also shows the area of the rectangle that includes the proposed antenna. The SOI technology has been selected for this work, since it has been proven to be well suited for on-chip antenna integration and for mm-waves operations, see [57,60,61]. Indeed, due to the presence of a high resistive substrate in the SOI technology, it is possible to separate the integrated RF (Radio Frequency) part from the noise coupling due to other circuits (e.g., switching noise of the digital circuits). Moreover, in CMOS SOI technology, passive components can be designed with a higher good-quality factor than in bulk CMOS.

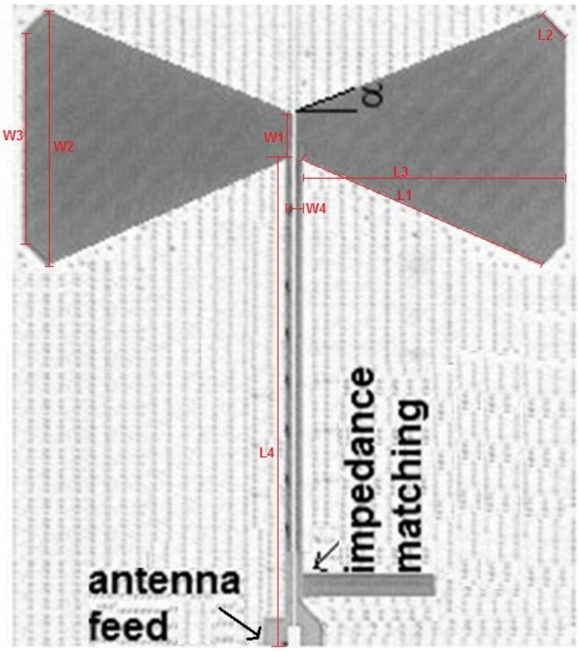

Figure 1. Bow-tie wideband antenna design, 65 nm CMOS SOI.

Table 1. Values of the antenna parameters in Figure 1.

Parameter	L1	L2	L3	L4	W1	W2	W3	W4	α
Value	350 μm	50 μm	350 μm	637 μm	60 μm	330 μm	275 μm	20 μm	25°
Area of the rectangle including the antenna	[L4 + 0.5 × (W1 + W2)] × (2 × L3 + W4) = 832 μm × 720 μm = 0.6 mm^2								

In the proposed on-chip realization, a conductive copper layer with a thickness of about 1 μm is printed on a multi-layer substrate that includes:

(1) a dielectric layer with a thickness of about 3 μm and a relative dielectric permittivity εr of about 3.5;
(2) a buried oxide layer with a thickness of 150 nm (a value typical for SOI manufacturing technology, see p. 11 of [72]) and a relative dielectric permittivity εr of about 4;
(3) a high-resistivity (HR) layer with a thickness of 350 μm (a value typical for wafers used in RF applications, see [73]) and the following electrical parameters: ρ = 5 kΩ·cm and εr = 11.7.

Figure 2 shows a side view of the multi-layer structure in the example case of the CPS implementation. For the sake of space, the figure is not to scale, since the height of the high resistivity layer is two orders of magnitude higher than the height of the conductive and dielectric layers, and three orders of magnitude higher than the height of the buried oxide layer. Moreover, on top of the layers in Figure 2, a passivation layer may be needed due to packaging issues. The effect of a passivation layer and of the packaging on the proposed on-chip antenna is out of the scope of this paper.

The antenna-feeding network is also included in Figure 1. It is represented by the CPS circuit of length L4 and total width W4, whose values are reported in Table 1. The gap between the two strip-lines of the CPS is about 1 μm. To design the antenna, and to properly size all parameters reported in Table 1, electromagnetic simulations have been carried out using the CAD (Computer Aided Design) environment CST (Computer Simulation Technology) Microwave Studio. It is to be noted that there is no equation that is able to size the antenna, but the antenna sizing is the result of an iterative process, supported by simulations in the CAD environment. After several simulations and design trials in the CST Microwave Studio tool, the values in Table 1 have been achieved. The area of the rectangle including the antenna is about 0.6 mm^2, which is much lower than the area of some cm^2 for the antennas proposed by [67,70]. This sizing is not valid for only a specific frequency, but the same antenna has been characterized in a wide frequency range.

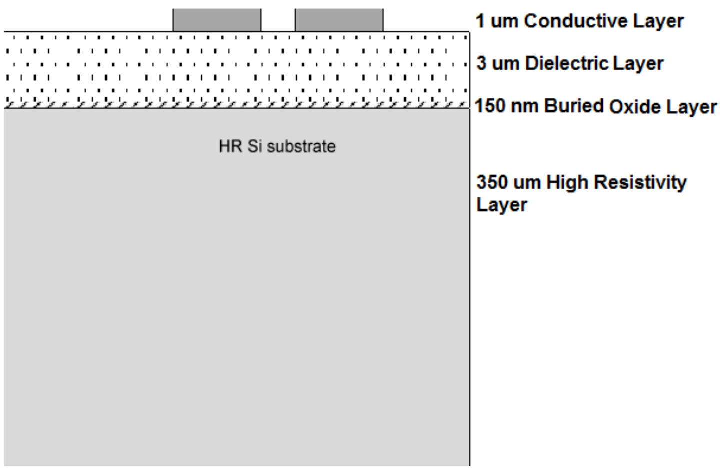

Figure 2. Side view (in the case of a Co-planar Stripline (CPS) implementation) of the adopted single-chip multi-layer structure.

3. Antenna Characterization

With reference to the antenna whose layout is depicted in Figure 1, Figure 3 shows the performance achieved in terms of radiation pattern along the X–Y plane. The relevant half-power beamwidth (HPBW) angle is also shown: the HPBW along the X–Y plane is 110 degrees. Instead, the HPBW along the X–Z plane is 65 degrees.

It is to be noted that for WiNoC applications, where a processing core has to be connected with other processor cores or memory tiles, placed on the same plane, the radiated power of interest is that along the X–Y plane. The power radiated along the Z-axis would be just wasted. This is why the antenna is designed to be directional in its X–Y radiation pattern, featuring a large HPBW of 110 degrees in both directions of positive and negative values of the X axis. The only application where radiation along the Z axis would be useful is in the case of a WiNoC communication in a multi-core system-on-chip fabricated using 3D assembly technology. In such a case, the wireless link is also between cores aligned in the vertical direction, and not only between cores placed in the same plane. However, the use of WiNoC technology in the framework of 3D integration technology is out of the scope of this paper.

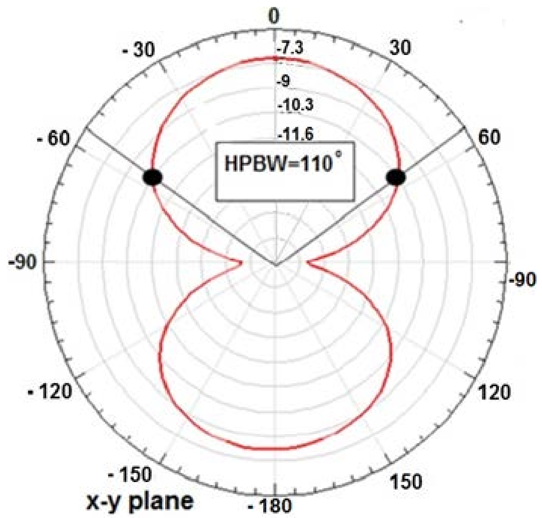

Figure 3. Antenna radiation pattern at 60 GHz along the X–Y plane.

At 60 GHz, the performance in terms of S-parameters has a maximum gain (from CST simulations) of about −7 dBi and a return loss of −39.5 dB. The percentage radiation efficiency η is about 20%. In the state-of-the-art, the antenna bandwidth capability is calculated as the frequency range where the return loss parameter is below −10 dB [74]. Figure 4 shows the S11 antenna performance vs. frequency. From the results in Figure 4, the return loss is always below −10 dB in the range of 51 GHz to 100 GHz, hence an antenna bandwidth capability from 51 GHz to 100 GHz is determined. Frequency values above 100 GHz are not taken into account in this work, since above 100 GHz the CMOS technology is not a suited technology for the integration of the transceivers. Indeed, above 100 GHz, the gain values of the low noise amplifier (LNA) and of the power amplifier (PA) will be too low, and the receiver noise figure (NF) will be too high. Figure 5 shows the 3D radiation pattern and the antenna gain as a function of frequency, at 50 GHz, 60 GHz and 100 GHz, considering a direction of 0 degrees in the X–Y plane in Figure 3.

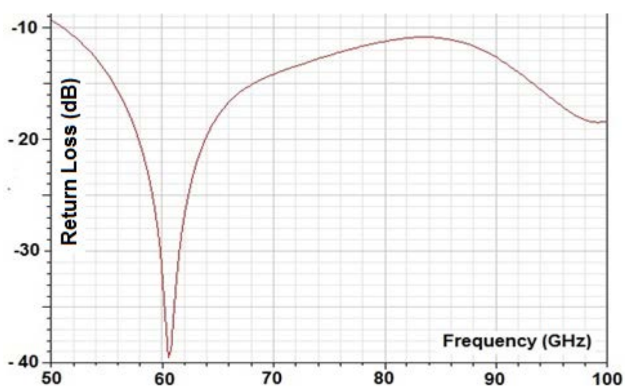

Figure 4. Return loss of the antenna as a function of frequency.

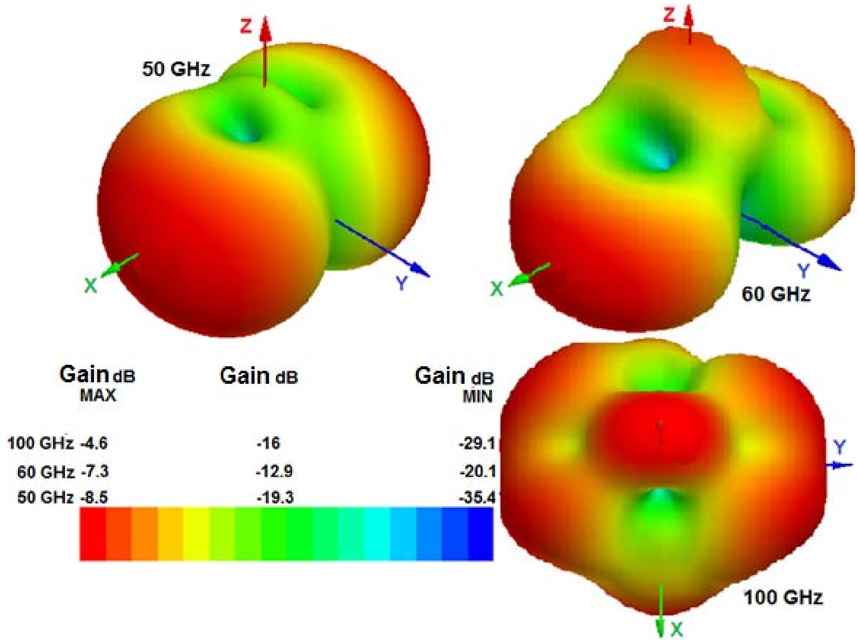

Figure 5. Radiation pattern and antenna gain at 50 GHz, 60 GHz, 100 GHz.

4. Comparison of the Designed Antenna vs. the State-of-the-Art

This section compares the achieved performance vs. known works published in recent literature, e.g., Ref. [31,37,40,67,69,75–94]. Specifically, Table 2 compares the proposed design to [31,37,40,67,79,83] in terms of area, gain, HPBW and bandwidth.

Table 2. Comparison to the state-of-the-art.

Antenna	Area, mm^2	Feed/Match Circuit	Gain, dB	HPBWxy	Bandwidth
This work	0.512	Included	−7.3 @ 60 GHz	110°	51 to 100 GHz
[31,37]	0.023	Not included	−26.5 @ 60 GHz	60°	51 to 66 GHz
[40], Dipole	375	Included	5.8 @ 10 GHz	65°	8 to 11 GHz
[40], Vivaldi	300	Included	2.8 @ 10 GHz	85°	9 to 11 GHz
[67]	156	Included	5 @ 60 GHz	184°	57 to 64 GHz
[79]	2	Included	−30 @ 3 GHz	N/A	N/A
[83]	1.4	Not included	−38.65 @ 60 GHz	33°	6 GHz

With respect to antennas in the sub-10 GHz domain [40,69], the area occupation of the antenna design in Section 3 is limited to about 0.6 mm^2. This size is compliant with integration on a single-chip. On the contrary, the size of the antennas proposed in Ref. [40,69] is orders of magnitude higher than the on-chip bow-tie antenna in this work. Indeed, in Ref. [40], the authors present a 3 cm^2 dipole antenna, operating at 10 GHz, with a 2.8 dBi gain and a HPBW of 85 degrees at 10 GHz. Still at 10 GHz, in Ref. [40], the authors also present a 3.75 cm^2 Vivaldi antenna with a gain of 5.8 dBi and a HPBW of 65 degrees.

With respect to other on-chip antennas, operating at around 60 GHz, and proposed in literature, the antenna design in Section 3 offers a better trade-off between size, gain, bandwidth and HPBW. For example, the zig-zag antenna adopted for WiNoC in [31] has been designed with a trace width of 10 µm, with an arm length of 60 µm and a bend angle of 30 degrees. The axial length of the zig-zag antenna is 0.38 mm. The substrate is represented by a 2 µm thick SiO_2 layer, with a relative dielectric permittivity constant εr of 3.9. The substrate is a high-resistivity silicon substrate with a thickness of 633 µm and electrical parameters of $\rho = 5$ kΩ·cm and $\varepsilon r = 11.7$. The same antenna has also been adopted in [37]. The zig-zag antenna has a lower size, 60 µm × 380 µm, than the proposed bow-tie antenna, although the reported area for the zig-zag antenna does not consider the feeding and impedance matching network. The maximum gain of the zig-zag antenna is only −26.8 dBi at 60 GHz: i.e., the gain is about 19 dB lower than the antenna design proposed in this work. The connection distance using the zig-zag antenna is limited to 2 cm in [31]. For example, in a complex MPSoC design with a size L of some centimeters per side, e.g., the INTEL48 core in [95] with L about 2.5 cm, the tiles that are placed in the layout at opposite parts of the MPSoC can have a distance (along the diagonal of the chip) up to 3.5 cm. Moreover, the return loss for the zig-zag antenna is below −10 dB only in the spectrum range from 51 GHz to 66 GHz. Instead, the proposed bow-tie antenna has an upper bound limit of 100 GHz. In terms of HPBW, along the X–Y plane of interest, the zig-zag antenna has a value of about 60 degrees, almost halved vs. the 110 degrees of the proposed design, see Figure 3.

The half-wave dipole and the double-slot antennas proposed in 65 nm SOI technologies in Ref. [59], having a comparable size to the bow-tie design, reach a positive gain of a few dBi, but use a PEC (Perfect Electric Conductor) plane under the chip. Similarly, the slot bow-tie antenna in [62] has an area 2.5 times larger than the proposed design; realized in 180 nm SiGe technology, and using a PEC layer under the substrate, [66] achieves a gain from −3 dBi to 0 dBi operating from 70 GHz to 110 GHz. However, for this antenna, the radiation pattern is directed along the Z-axis, which is unsuitable for WiNoC applications where the communication is towards co-planar nodes. High gain antennas have been proposed at 60 GHz such as the Fan-like antenna in [67]. The antenna in [67] exhibits a beamwidth of 184 degrees, a gain varying from 1.6 dBi to 6.4 dBi from 57 GHz to 64 GHz, but for an area of 156 mm^2, which is orders of magnitude higher than our proposed design. Some antennas operating at around 60 GHz are reviewed in [93,94], but their area occupation is at least tens of mm^2. Therefore, they are more suited for wireless sensor networking applications, in off-chip short-range communications, rather than for WiNoC.

As far as the antennas at sub-GHz are concerned, as in Ref. [68,70,71,81], the gain of the antennas is higher than the gain of the proposed bow-tie antenna, but the bandwidth in [68,70,71,81] is so low that the data-rate is limited to a few kb/s. Such antennas are suitable for wireless sensor networks, but not for on-chip high-rate connections among several processors or between a processor and a memory tile.

Carbon Nanotube (CN) antennas have also been proposed in literature in Ref. [75–77] to achieve a Terahertz frequency operating range. The CN antennas, operating in Terahertz frequency range, can provide much higher communication data rates than on-chip antennas, operating up to 100 GHz. The CN antennas can also have extremely high current density, compared with copper, thus allowing for a higher transmission power. Therefore, they can be suitable for long-distance communications. However, CN antennas are still facing significant manufacturing challenges.

The design of Ultra Wide Band (UWB) antennas was also proposed for on-chip wireless communication in Ref. [78–80]. The UWB antenna design approach can provide high bandwidth, low power and short-range communication for WiNoCs. However, the UWB-based antenna in Ref. [78–80], implemented in a 180 nm CMOS technology as a meander-type dipole antenna with a length of about 3 mm, and integrated in a complete on-chip transceiver, allows for a transmission range limited to 1 mm. The area occupation of the antenna in the layout of Ref. [79], including the feeding circuitry, is about 2 mm^2, i.e., 4 mm × 0.5 mm. The short transmission range, compared with the current die area, would require multi-hop wireless communication across the chip, which makes it less efficient for a communication distance above 1 mm.

Another class of antennas proposed for WiNoC is the PLPA (planar log-periodic on-chip antenna) one, see Ref. [82–84]. The authors of [82–84] propose the design of an on-chip PLPA with a bandwidth of about 10% of the central frequency, e.g., 6 GHz of bandwidth around a central frequency of 60 GHz and featuring end-fire directivity. It is to be noted that the PLPA in [82–84] can also resonate at other frequencies, e.g., 44 GHz. From CAD simulations, the HPBW of the PLPA is 33° along the end-fire direction, whereas the HPBW along the elevation is 30°. At 60 GHz, the antenna gain is −38.65 dBi. The longest dimension of the antenna is 1.1825 mm, which is comparable to the wavelength of the signal in the dielectric medium. The area is about 1.4 mm^2, but this value does not include the feeding network, which instead is included in the area values of the other antennas considered in Table 2. It is worth noting that the performance of the PLPA in [82–84] at 60 GHz, in terms of bandwidth, gain and HPBW, is lower than the design proposed in this work.

Several on-chip antennas are proposed by Kenneth et al. in [85–92]. With respect to these designs, the bow-tie antenna proposed in this work stands out for its large bandwidth, which is an added value of the selected bow-tie approach. More in detail, Kenneth et al., in [85], discuss the impact of on-chip metal interference structures, such as a power grid, local clock trees and data lines, on the performance of on-chip antennas. In Ref. [86], Kenneth et al. propose on-chip wireless interconnections for clock signal distribution. In Ref. [87–92], Kenneth et al. present several on-chip antennas operating at 24 GHz, 5.8 GHz and 60 GHz. Particularly, a communication range of 10 m operating at 100 kb/s is possible using on-chip antennas at 24 GHz (a 3-mm long zig-zag dipole antenna fabricated on a 20-Ω-cm substrate and having an efficiency of 25%). At 5.8 GHz, using a pair of 6-mm long monopoles, Kenneth at al. demonstrated that a communication range of 30 m can be achieved. A bond wire antenna, operating at 60 GHz, has also been proposed with an efficiency of about 15%.

5. Impact of the Proposed Antenna on the NoC Infrastructure Performance

This section evaluates the impact of the proposed antenna on the performance of the whole NoC infrastructure, and hence on the performance of an MPSoC, with respect to the use of a zig-zag antenna, as in [31,37]. It is worth noting that the higher HPBW of our design vs. zig-zag antenna in [31,37] leads to a larger number of cores that can be reached by the WiNoC.

Moreover, the increased antenna gain of about 19 dB (−7.5 dBi in our case vs. −26.5 dBi in [31,37]) can be exploited to reduce the power consumption of the NoC infrastructure, and hence of the MPSoC. Indeed, in the link budget of a wireless connection, the received power in dB depends on the transmitted power plus the gain of the transmitting and receiving antennas (i.e., twice the gain of the antenna in dB if the same antenna is used during transmission and receiving phases), minus the path loss. By increasing the antenna gain by 19 dB, adopting the design proposed in Section 3 instead of a zig-zag antenna topology, then to achieve the same distance with the same path loss of [31,37], the transmitted power can be decreased by about 38 dB. For example, instead of transmitting 1 mW of power (which is drained from the power supply), the WiNoC transceiver can transmit about 200 nW, with a power saving by a factor 5.

Finally, the larger antenna bandwidth, measured in GHz (see Table 2), can be exploited to sustain a higher bit-rate vs. [31,37], measured in Gb/s, when using the same transceiver and the same modulation and coding scheme (i.e., with equal spectrum efficiency, measured as b/s/Hz).

6. Conclusions

The design of a mm-wave antenna for wideband wireless communications on-chip, WiNoC, is presented in this work. WiNoC is an emerging trend in on-chip communications to solve power consumption and latency issues of conventional metal-wires in the case of links above 1 cm in size (e.g., distant tiles in a multi-processor system-on-chip). The aim is to interconnect multiple macrocells of homogenous or heterogeneous MPSoCs. The proposed bow-tie antenna design has been characterized in the range from 50 GHz to 100 GHz in terms of area, efficiency, and beamwidth. With respect to the state-of-the-art, the antenna stands out for its better trade-off in terms of size, gain, HPBW and bandwidth. With respect to the zig-zag antenna, typically used as a reference for WiNoC design in literature, the proposed design stands out for its much higher gain, about 19 dB higher and almost doubled beamwidth. The higher gain is useful to connect tiles at opposite sides of large MPSoC designs (in [31], the zig-zag antenna is limited to 2 cm) or—giving the same distance and path loss—to reduce the transmitted power, thus saving power.

Conflicts of Interest: The author declares no conflict of interest.

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