

Review

# CMOS Inverter as Analog Circuit: An Overview

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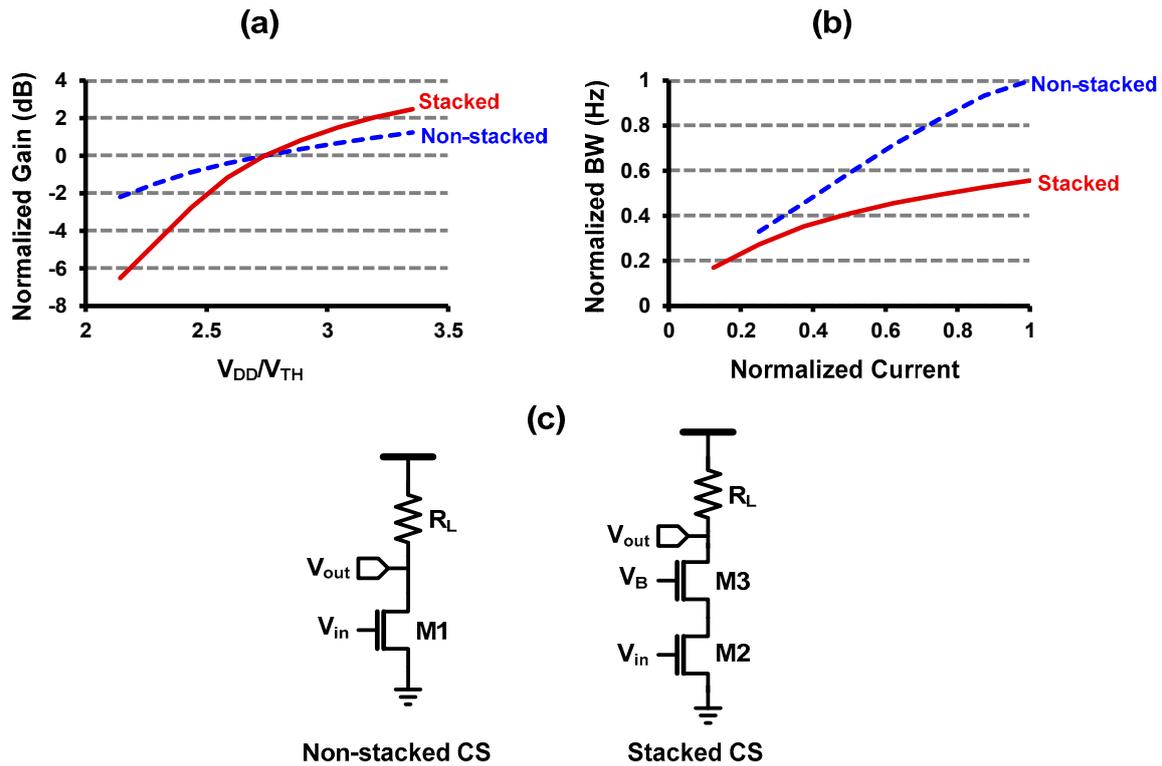


**Abstract:** Since the CMOS technology scaling has focused on improving digital circuit, the design of conventional analog circuits has become more and more difficult. To overcome this challenge, there have been a lot of efforts to replace conventional analog circuits with digital implementations. Among those approaches, this paper gives an overview of the latest achievement on utilizing a CMOS inverter as an analog circuit. Analog designers have found that a simple resistive feedback pulls a CMOS inverter into an optimum biasing for analog operation. Recently developed applications of the resistive-feedback inverter, including CMOS inverter as amplifier, high-speed buffer, and output driver for high-speed link, are introduced and discussed in this paper.

**Keywords:** analog; analog and mixed signal; amplifier; CMOS; driver; high-speed buffer; high-speed I/O; Integrated circuit; Inverter

## 1. Introduction

Since the 1960s, scaling of silicon technologies (Moore's law) has dominantly driven the semiconductor industry, as the scaling is actually the almighty knob for all the challenges we have had; lower power consumption, higher speed, and higher density. However, the main focus of the scaling has been the improvement of digital circuit, for example high  $I_{on}/I_{off}$  ratio, as the computing capability has been constrained by the power consumption, instead of the speed of the transistor [1,2]. Such digital-driven scaling leads to several issues in analog circuit design. For instance, the intrinsic gain of transistor has been significantly reduced due to the short-channel effect. Moreover, the threshold voltage of transistor has not been scaled at the same rate of the supply voltage scaling, in order for suppressing the leakage current [3]. That means the "normalized" voltage headroom for analog circuit has been reduced. Therefore, adopting conventional gain-boosting techniques (i.e., cascode) becomes more and more difficult in modern CMOS technology [4]. What makes things worse is that the gate-overdrive voltage of analog circuits should be decreased as the voltage headroom reduces, which increases the sensitivity of analog circuits to the device mismatch [5]. We can observe such trend in Figure 1, which compares the stacked common-source (CS) amplifier to the non-stacked CS amplifier [6,7]. Figure 1a,b shows the normalized gain of CS amplifiers with respect to  $V_{DD}/V_{TH}$  and the normalized large-signal bandwidth with respect to the normalized current dissipation, respectively. The gain of the stacked topology decreases much steeper than that of the non-stacked, which means that the gain enhancement from the cascode topology becomes less attractive in the modern CMOS technology where the voltage headroom is reduced. Moreover, the achievable bandwidth of the stacked amplifier is much less than the non-stacked amplifier even when it dissipates more current, because the increased self-loading from the stacked transistor degrades the rise/fall time. In addition, [6] revealed that the input-referred noise becomes even worse in the stacked topology because the transconductance  $g_m$  increases due to the reduced gate-overdrive voltage.



**Figure 1.** Comparison of stacked over non-stacked structure using common-source (CS) amplifier topology. (a) Gain degradation as a function of  $V_{DD}/V_{TH}$  [6], (b) large-signal bandwidth degradation as a function of current consumption [7], (c) circuit diagram of a CS amplifier.

In summary, what we could observe from the CMOS scaling trend is that the scaling has focused on improving the digital circuits; hence, the performance of analog circuits has been degraded due to the short-channel effect and the reduced voltage headroom. The analog circuit designers have come up with the fact that a CMOS inverter, which is the representative of the digital circuit family, can be the most powerful circuit in modern CMOS technologies, even in the analog domain [8,9]. First, there is no stacking; thus, it has not been affected by the reduced voltage headroom. Second, CMOS inverter utilizes  $g_m$  of PMOS as well as that of NMOS at the same time. When we compare the two circuits given in Figure 2, we can find that they have the same load capacitance, including the self-loading. However, in case of the CMOS inverter, the overall  $g_m$  is the sum of  $g_{mN}$  and  $g_{mP}$ ; thus, we can get a higher bandwidth. This aspect becomes much powerful in recent process technologies, where strained silicon technique enhances the PMOS current density as much as that of NMOS [10–12]. In fact, when we consider the sizing, the P/N ratio of the inverter for analog intent is different to the digital intent. In order technology where the strained silicon technique is not adopted, digital inverter has PMOS which is generally twice larger than NMOS, because we have to match the strength of PMOS and NMOS, since we assume that only one of the PMOS and NMOS is turned on at a time. However, in such analog inverter, the optimum is at around P/N ratio of unity, where we can achieve the highest  $g_m$  per input capacitance [13]. Note that the PMOS and NMOS continuously run together in analog mode. That means we were not able to fully utilize the  $g_{mP}$  in older technology nodes. In other words, the strained silicon boosts the current density of PMOS to be matched to that of NMOS, and therefore it makes the analog inverter become more powerful.

Some readers may wonder how a CMOS inverter acts like an analog circuit, because it is a representative digital circuit. In fact, the boundary of analog and digital is ambiguous, but “biasing” can be used to distinguish them, which is explained in Figure 3. The blue line shows the input-output transfer curve of an inverter. Note that the blue lines are the same for both figures. When we see the big picture (large signal), we can find a digital circuit. However, when we focus on a certain operating

point (small signal), we can find an analog circuit. We can also find that the maximum gain is achieved at the point where the input and output are the same, that is, at the switching threshold. Analog designers found that such optimum bias point can be achieved with the self-biasing using the resistive feedback, as shown in Figure 4.

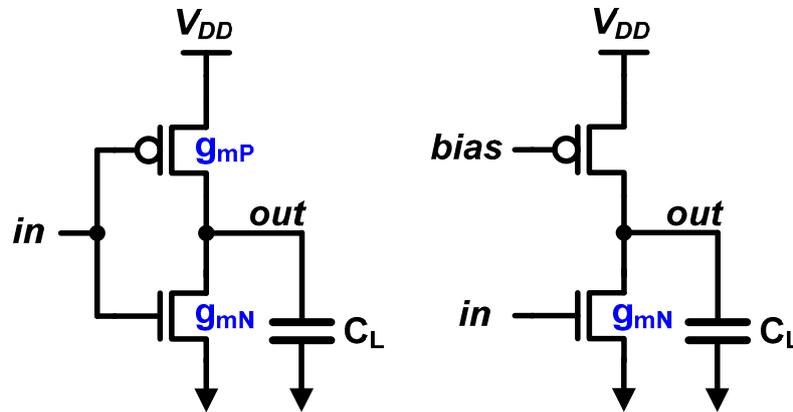


Figure 2. Utilization of  $g_m$  of PMOS in a CMOS inverter.

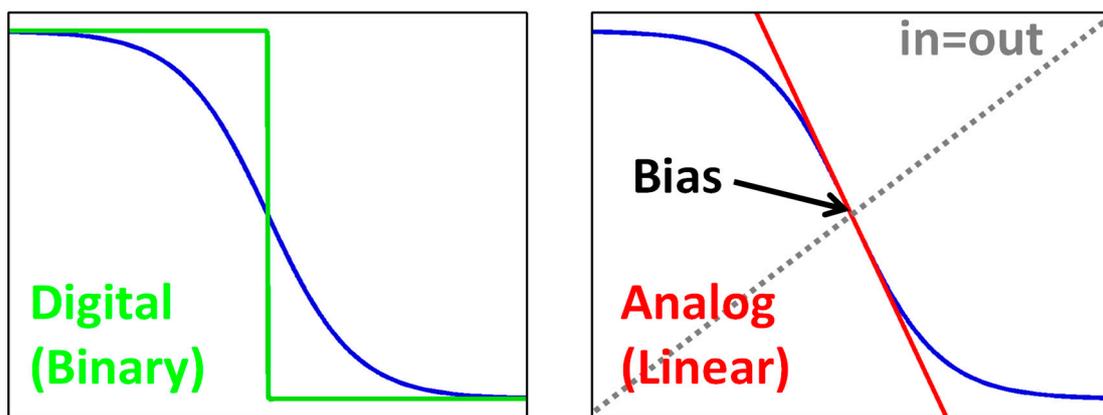


Figure 3. Inverter gain curve and distinction between digital and analog.

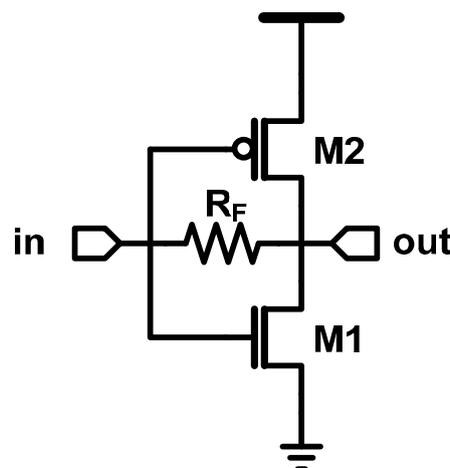


Figure 4. CMOS inverter with resistive feedback.

Nowadays, in order to take advantage of the CMOS inverter in modern process technology, there has been a lot of approaches to adopt CMOS inverter into analog circuits. This paper focuses on the applications of high-speed analog circuits, and introduces three examples of that, amplifier in optical

communication receivers [6,14–30], high-speed clock and data buffer [13,31–41], and output driver for high-speed I/O transmitter [13,40,42–50].

## 2. CMOS Inverter as an Amplifier

The first example we are going to cover is the use of a CMOS inverter as a high-speed amplifier, which is mostly adopted in optical communication receiver. In optical communication, high-speed serial data is transmitted by modulating the amplitude of light. At the receiving side, a photodetector (PD) converts the received light signal to the photocurrent. Due to the limited PD responsibility as well as and the limited extinction ratio at the transmit side, typically, the amplitude of photo-current signal ranges from tens of uA to hundreds of uA. In order to be processed in a CMOS integrated circuit (IC), the current-mode signal should be converted to voltage-mode. Thus, a trans-impedance amplifier is used at the very front-end of an optical receiver. As a result, the overall performance of the receiver is predominantly determined by the trans-impedance amplifier (TIA). Since there is an inherent trade-off between TIA gain/noise and bandwidth, compound semiconductor process was traditionally preferred to build the optical interface IC due to their high-speed characteristic. However, since continuous advance of CMOS technology has reduced the gap, nowadays, CMOS technology is becoming the mainstream for optical interface ICs.

We can see a brief history of CMOS TIA for optical receiver in Figure 5. The most primitive TIA is a resistor. But there is a strict trade-off between gain and bandwidth, because the gain equals the resistance  $R$  and the bandwidth is  $1/2\pi RC_{PD}$ . In addition, the signal-to-noise (SNR) is another main issue of concern. The total integrated noise due to the thermal noise of the resistor is given as to:

$$\overline{V_{n,out}^2} = \frac{kT}{C_{PD}}, \tag{1}$$

where  $k$  is the Boltzmann constant and  $T$  is the absolute temperature. Then, the input-referred noise is obtained by dividing (1) with the trans-impedance gain  $R$  as:

$$\overline{i_{n,in}^2} = \frac{kT}{R^2 C_{PD}}, \tag{2}$$

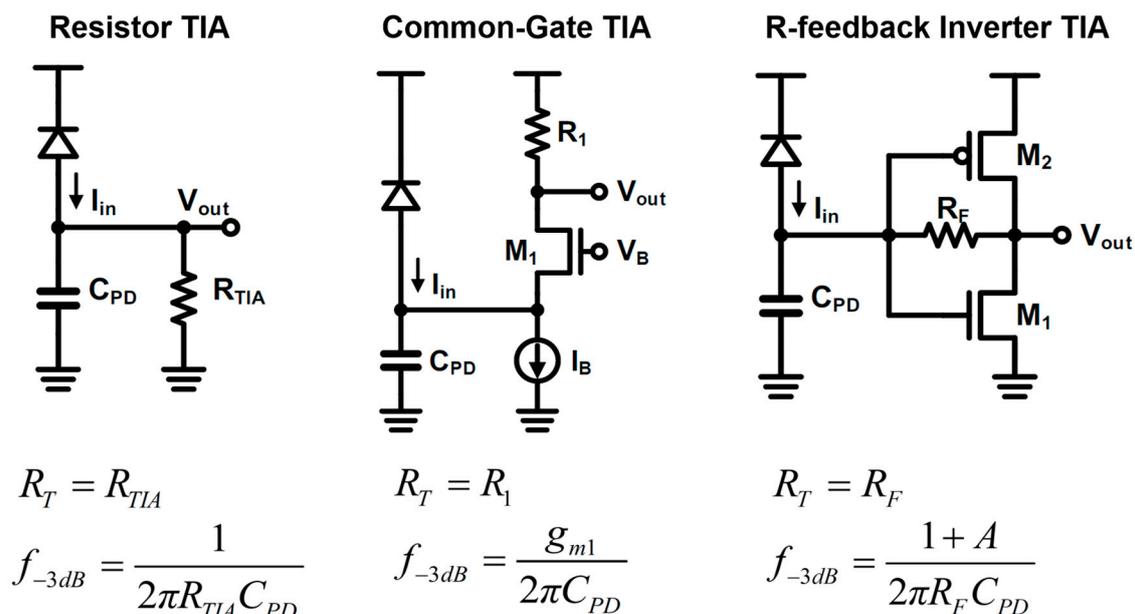


Figure 5. Trans-impedance amplifier examples.

From (2) we can obtain the SNR to:

$$SNR = \frac{C_{PD}}{kT} I_{in}^2 R^2, \quad (3)$$

where we can observe that higher gain leads to a better SNR, which implies the trade-off of gain/noise over the bandwidth. Many circuit designers have tried to find a way to break the trade-off, and they found that the common-gate (CG) amplifier can break the trade-off. Because the photo-current directly flows to the load resistor, the trans-impedance gain equals to the resistance. On the other hand, the input impedance of the CG amplifier is  $1/g_m$ , so the pole at the input of CG amplifier is given as to:

$$f_{-3dB} = \frac{g_{m1}}{2\pi C_{PD}} \quad (4)$$

Note that there is no R term in, which implies that the aforementioned trade-off is now broken, since  $C_{PD}$  is generally much larger than the load capacitance of the CG amplifier. Since the  $1/g_m$  can be reduced by drawing more current by the current source ( $I_B$ ), we can achieve high gain as well as high bandwidth at the cost of power consumption. In addition, [51,52] proposed a regulated-cascode (RGC) TIA, which further improves the gain-bandwidth product of TIA. However, the effectiveness of such stacked configuration has been degraded due to the aforementioned scaling issue, now many researchers have ended up with the resistive feedback inverter TIA. The inverter-TIA still have a similar trade-off as the passive TIA; however, the input resistance of the resistive feedback inverter is  $R/(1 + A)$ , where A is the gain of the inverter. That means that the trade-off is relaxed by the factor of A. Additionally, note that there is no other path that the photo-current can flow; the gain of this TIA equals R. Readers may consult [28] for a detailed history of TIA evolution.

The resistive-feedback inverter TIA is also able to be combined with inductive peaking technique, to extend the bandwidth with less gain/power penalty. References [19,25] present the inverter TIA with series inductive peaking, which is illustrated in Figure 6a. Since an inductor blocks an instantaneous current flow, it enables sequential charging (or discharging) of the two adjacent capacitances (for example, PD capacitance and self-load at the input node, or self-load and load capacitances at the output node), which leads to a faster transient response. On the other hand, [6] added an inductor in series with the feedback resistor; that is, the inductive feedback as shown in Figure 6b. At a low frequency, the effect of the inductor is negligible; thus, the TIA simply follows the transfer gain of the resistive-feedback inverter. Note that such negative feedback increases the bandwidth at the cost of reduced low-frequency gain. On the other hand, the impedance of the inductor increases as the frequency increases; hence, after zero frequency, it surpasses that of the feedback resistor. That means that the total impedance in the feedback path increases, and thus the gain increases. If the inductive impedance is larger enough than the resistance, the transfer gain of the TIA follows that of the inverter without resistive feedback. At a very high frequency, the second order pole, which is introduced by the inductor and the capacitance as well as the intrinsic pole of the inverter, let the transfer gain decrease rapidly as the frequency increases. As a result, such inductive feedback leads to a high-frequency peaking, which can be used to compensate the dominant pole by the  $C_{PD}$ . Recent state-of-the-arts works in [15,24,29] have combined the series peaking and the inductive feedback, and therefore considerable high-bandwidth at a quite impressive energy efficiency is achieved. Moreover, the authors in [29] saved inductor area by incorporating T-coil inductive peaking.

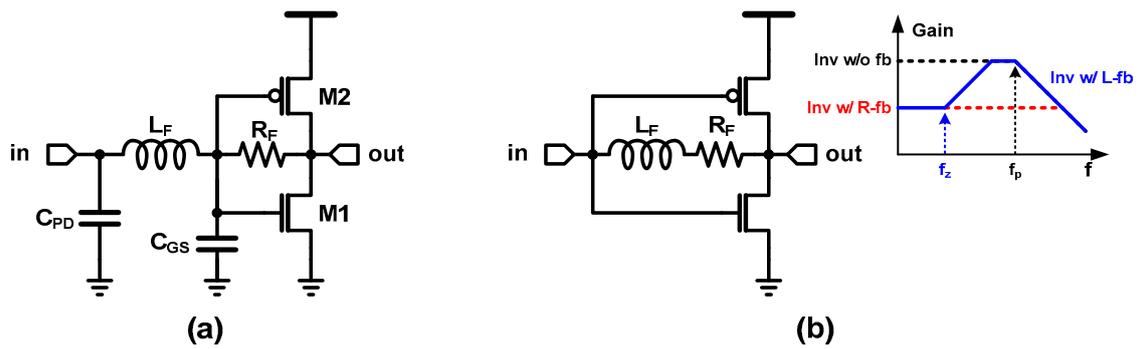


Figure 6. (a) Inverter TIA with series peaking, (b) with inductive feedback.

The application of CMOS inverter as an amplifier is not limited to the TIA. Optical receivers presented in [18,19,21,24–27] extend the usage of the CMOS inverter to the post limiting amplifier which follows the TIA. In addition, [16,17,30] present resistive-feedback-inverter-based low-noise amplifier (LNA) and variable gain amplifier (VGA), respectively. In such applications, a normal inverter stage and a resistive-feedback stage are placed alternately to retain the self-bias (resistive feedback) as well as high gain (inverter), as shown in Figure 7. Recalling Figure 3, the small-signal gain of inverter is maximized at the crossover voltage. Therefore, in order to maximize the overall gain of the amplifier chain, the common-mode voltage should be corrected. Due to the considerably large gain of the chain, the resistive feedback itself is not enough to retain a correct bias point. Such common-mode variation leads to some large-signal non-idealities, such as duty-cycle distortion. Therefore, a common-mode feedback is generally included as shown in the example of Figure 7. The DC component of the output signal is extracted through a low-pass filter (LPF) and then compared to the reference voltage (i.e., crossover voltage). The feedback adjusts the input common level until the common-mode voltage at the output becomes the same as the reference voltage.

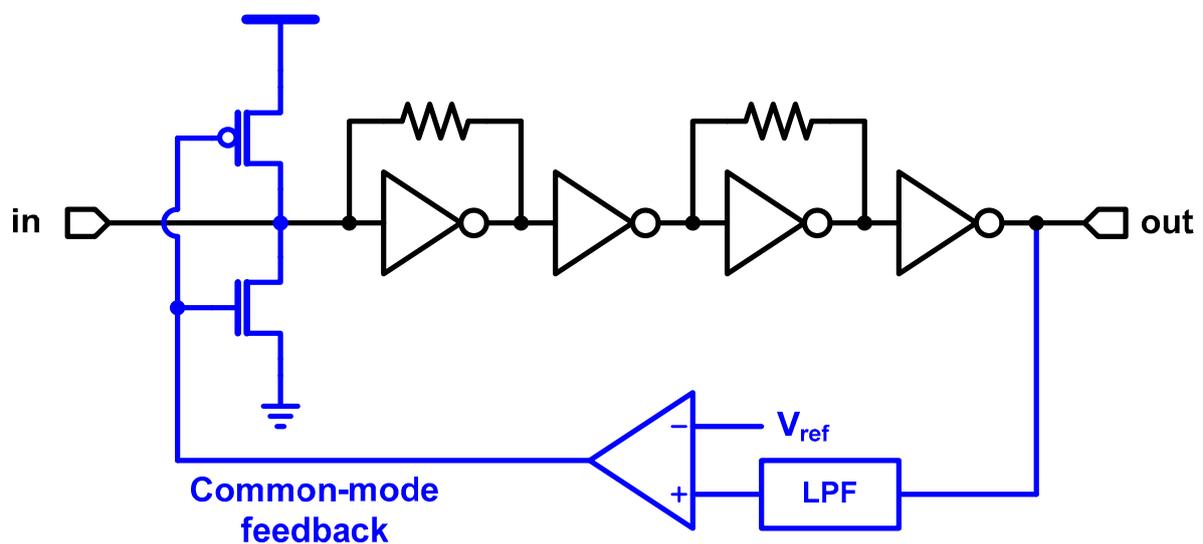


Figure 7. Inverter-based multi-stage amplifier with common-mode feedback.

To sum up, the resistive-feedback inverter has become a mainstream of TIA implementation, to fully utilize the CMOS process scaling, against the conventional TIA structures. Moreover, there have been many efforts to extend the application to other high-speed amplifiers. For evidence, taking advantage of the advanced CMOS technology node (14 nm FinFet), [25], where the inverter-based TIA and post amplifier are adopted, achieves the highest bandwidth optical receiver, which achieves 64 Gb/s with binary signaling.

### 3. High Speed Buffer

In the previous section, we focused on the small-signal behavior of CMOS inverter (with resistive feedback). Here, we will be care of more large-signal-like behavior compared to the amplifier operation. If the input signal swing is large enough, that is, entering to the noise margin region, the amplitude of the signal no longer needs to be considered as long as the gain of the “buffer” is larger than unity. However, taking into account the intrinsic gain of an inverter, the 3 dB bandwidth is typically 5–10× lower than the unity-gain bandwidth (Figure 8). If the main signal component is at between the 3 dB bandwidth and the unity-gain bandwidth, the signal experiences distortion while passing through the buffer even though the amplitude is not attenuated. For example, since the phase delay is not a constant over the frequency, a pattern-dependent jitter will be introduced to the non-return-to-zero (NRZ) datastream even if the Nyquist frequency is below the unity-gain bandwidth of the buffer [53]. Clock signal is another good and simpler example, as there is only a single frequency tone. Let us take into account additive white noise. The amplitude noise is filtered out by the noise margin of inverter; however, the phase noise propagates through the inverter. Moreover, if the clock frequency is higher than the 3 dB bandwidth, the low frequency noise has a larger gain than the fundamental frequency component. That leads to the jitter amplification [54]. Duty-cycle distortion is another important issue, since the duty-cycle is actually the DC component of the signal so the duty-cycle error is amplified after passing through a band-limited buffer [42].

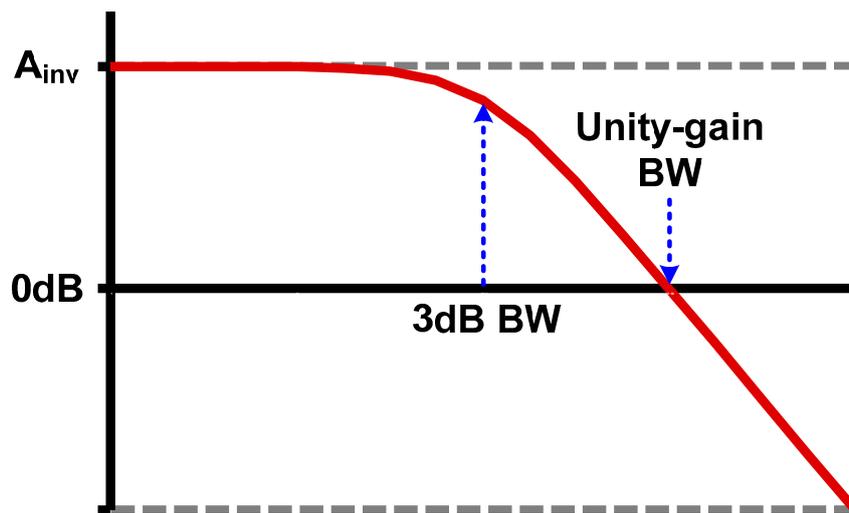


Figure 8. Magnitude response of CMOS inverter.

The above observation implies that the 3 dB bandwidth is more important than the unity-gain bandwidth while handling a high-speed analog signal, in contrary to the digital intent. The resistive feedback is also very useful to extend the 3 dB bandwidth of the inverter. We can obtain a quantitative analysis how the resistive feedback extends the bandwidth of the inverter, from the small signal model shown in Figure 9. Applying KCL to the output node, we obtain:

$$g_m v_x + \frac{v_{out}}{r_o} + j\omega C_L v_{out} = \frac{v_x - v_{out}}{R_F}, \tag{5}$$

where  $g_m$  is the sum of  $g_{mN}$  and  $g_{mP}$ . Equation (5) leads to the transfer function as:

$$\frac{v_{out}}{v_x} = \frac{1 - g_m R_F}{1 + \frac{R_F}{r_o} + j\omega R_F C_L}, \tag{6}$$

where we can achieve the 3 dB bandwidth to:

$$\omega_{3dB} = \frac{1}{r_o C_L} + \frac{1}{R_F C_L}. \tag{7}$$

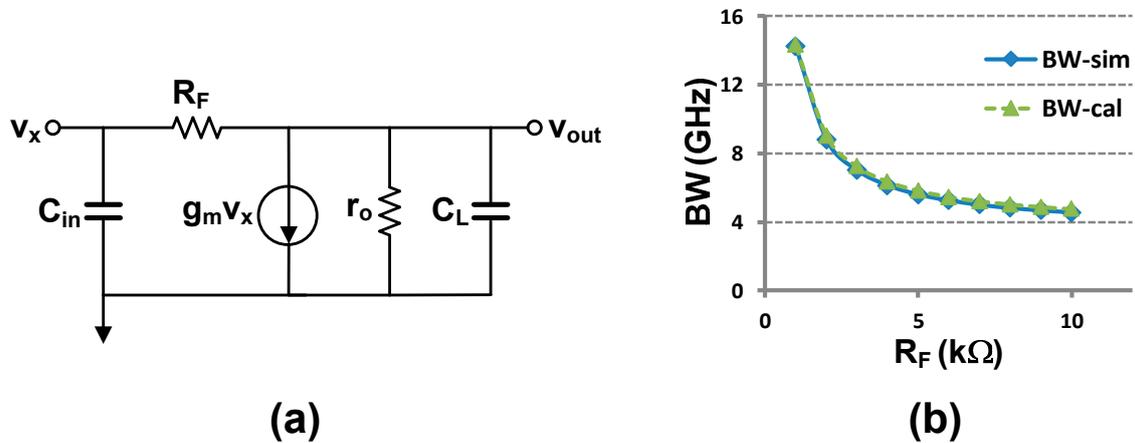


Figure 9. (a) Small signal diagram of resistive feedback inverter, (b) verification of (7).

Note that the 3 dB bandwidth of the inverter without feedback is  $1/r_o C_L$ . That is, the resistive feedback increases the 3 dB bandwidth by  $1/R_F C_L$ . Simulated bandwidth shown in Figure 9b verifies (7). Moreover, thanks to the negative feedback, this circuit is less sensitive to the PVT variations compared to the normal CMOS inverter.

On the other hand, an AC-coupling capacitor is widely used at the input of the resistive feedback inverter, for clock buffer application [32–39] (Figure 10). The primary motivations of the AC coupling for the clock buffer are as follows:

1. Since AC coupling completely blocks the DC component of the clock signal, the duty-cycle distortion does not propagate. Thanks to the self-biasing to the cross-over voltage, the duty-cycle is restored to the ideal value regardless of the input duty-cycle (Figure 11).
2. Combined with the low-pass characteristic of the inverter, AC coupling results in a band-pass characteristic. Because a band-pass filter attenuates all out-of-band noise, it suppresses phase noise and jitter from the input clock [54].
3. Because the clock buffer does not have to deal with a wide-band signal, the high-frequency cut-off frequency can be fairly high ( $< \sim 1/10$  of the clock frequency). Therefore, a small capacitor can be used [39].

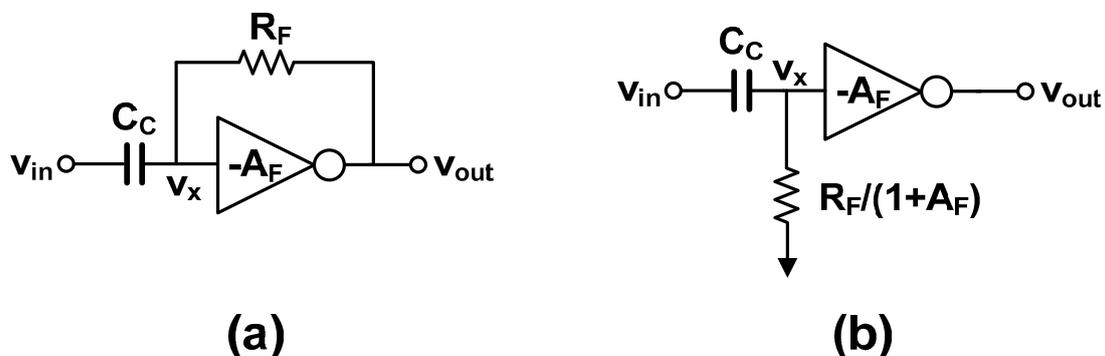


Figure 10. (a) AC-coupled resistive feedback inverter and (b) Miller approximation to calculate high-pass cut-off frequency.

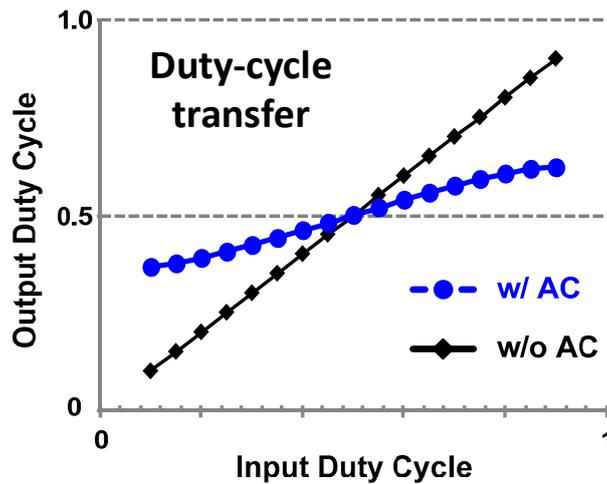


Figure 11. Duty cycle transfer curve of AC-coupled buffer.

The high-pass cut-off frequency of the AC-coupled buffer is calculated as follows. Using Miller approximation, the feedback resistance  $R_F$  is translated to the input resistance of  $R_F/(1 + A_F)$ , where  $A_F$  is the DC gain of the inverter. Then, we obtain:

$$\frac{v_x}{v_{in}} = \frac{j\omega\left(\frac{R_F}{1+A_F}\right)C_C}{1 + j\omega\left(\frac{R_F}{1+A_F}\right)C_C}, \tag{8}$$

where we can find that the high-pass cut-off frequency is:

$$\omega_{hpf} = \frac{1 + A_F}{R_F C_C}, \tag{9}$$

For reference, the overall transfer function without Miller approximation is given in [39] as:

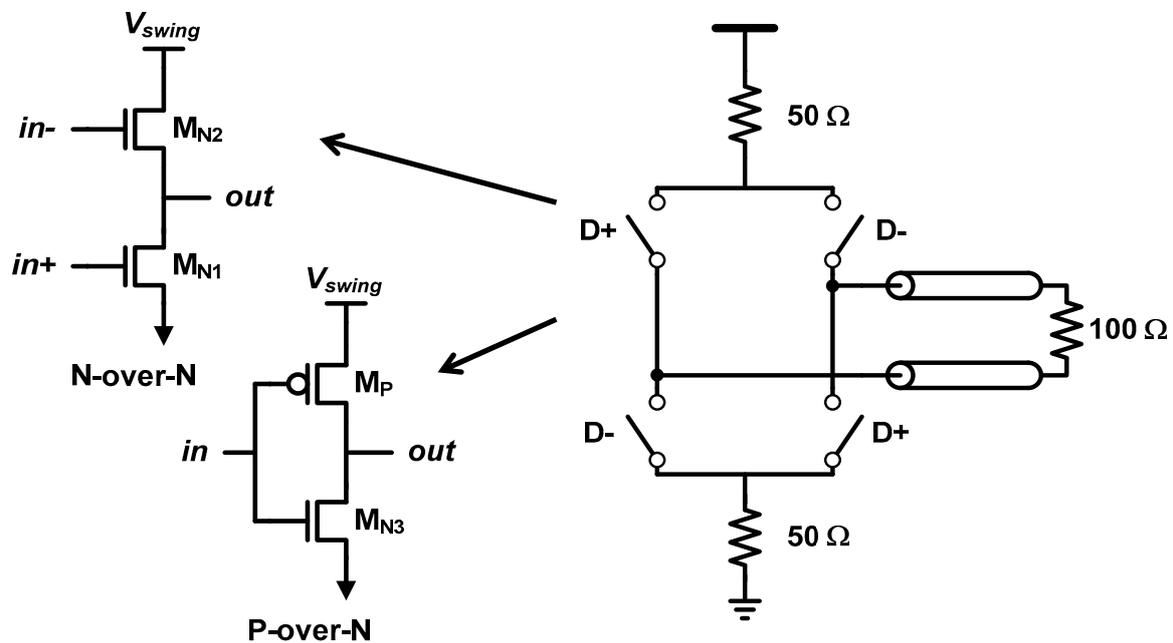
$$\frac{v_o}{v_{in}} \cong - \frac{sg_m R_F C_C}{g_m + \frac{1}{r_o} + s(C_L + C_C + \frac{R_F C_C}{r_o}) + s^2 R_F C_C C_L}, \tag{10}$$

where  $C_L$  is the load capacitance of the buffer. Figure 11 shows an example of the simulated duty-cycle transfer function of an AC-coupled inverter.

On the other hand, the bandwidth dependency on the feedback resistance can also be utilized to control the delay of a buffer chain. Conventionally, a current-starved inverter [55] or a variable capacitive-load inverter [56] have been widely used to build a variable delay line. However, basically, their mechanism is to reduce the bandwidth of CMOS inverter to increase the delay. As a result, such delay cells have a lower bandwidth than an inverter, and therefore, they have usually become the main limiting factor of the maximum speed of a chip. As a remedy, [13,40,41] proposed a resistive-feedback based delay line whose delay is controlled by adjusting the feedback resistance. As we observed in (7) and Figure 9b, the feedback extends the bandwidth of an inverter. That means that the resistive-feedback delay line actually increases the bandwidth to adjust the delay, instead of reducing the bandwidth. From another qualitative viewpoint of large signal, the resistive feedback decreases the voltage swing; therefore, the output rise/fall time is reduced. References [13,40] verified the large-signal effect as well, such that the resistive feedback reduces ISI considerably compared to the conventional delay line, at the cost of increased power consumption due to the short-circuit current induced by the reduced voltage swing.

#### 4. Output Driver for High-Speed Wireline Communication

The last example is the output driver for high-speed I/O link. On the right side of Figure 12, we can find a conceptual diagram of a source-series terminated (SST) driver, which is also known as a voltage-mode driver [35–50]. Instead of relying on a parallel resistance to match the driver’s output impedance with the characteristic impedance of the transmission channel, the SST driver adopts series termination. Such series-terminated data transmission is conceptually enabled with a series combination of a 50-Ω resistance and an ideal switch driven by NRZ data. The main advantage of SST driver over the parallel-termination counterpart, which is represented by current-mode logic (CML) driver, is its low-power consumption. Assuming terminations at both transmit and receive sides (double termination), the series termination flows the signal current to 100-Ω resistance ( $I = V_{swing}/100$ ), whereas the parallel termination flows to 25 Ω ( $I = V_{swing}/25$ ). As a result, the parallel termination dissipates 4× higher current to achieve a same voltage swing. On the other hand, the main downside of SST driver originates to the fact that there is no ideal switch in IC. There are two types of practical SST implementation, N-over-N and P-over-N configurations, as shown in Figure 12. It is well known that the N-over-N works well only for low swing applications, whereas the P-over-N is appropriate for higher swing applications. Note that the P-over-N structure is a CMOS inverter. Basically, their approach is the same. Instead of using an ideal 0-Ω switch, they utilize the finite resistance of switch transistor; if the turn-on resistance equals to 50-Ω, a single transistor can work as the combination of the ideal switch and the resistor. The 50-Ω impedance is generally calibrated by adjusting the number of activated driver slices and the gate-overdrive voltage. The main challenge here is the non-linear nature of CMOS transistor does not let the transistors have a constant resistance over the swing range [42]. For example, when the output voltage increases, the  $V_{DS}$  of the pull-down NMOS ( $M_{N1}$ ,  $M_{N3}$ ) increases and causes the NMOS to fall into the saturation region, where the output impedance becomes very high. Note that the linearity is a function of  $V_{DS}$ , and the  $V_{DS}$  range equals the output swing.



**Figure 12.** Conceptual diagram of source-series terminated (SST) driver and practical implementation of N-over-N and P-over-N SST configurations.

To resolve this issue, a series resistance is placed at the output of the SST driver, as shown in Figure 13 [37,46–48]. The turn-on resistance of the transistor is reduced here (i.e., 25 Ω) to make the sum with the series resistance be 50 Ω. The series resistor takes charge of a portion of the output swing, hence, the  $V_{DS}$  of the transistors is reduced. The downside of this approach is the increased transistor

size. If 25-Ω resistance is used, the size of transistor is doubled so that both the input capacitance and the output self-capacitance are doubled, each of which increases burdens of the pre-driver stage and degrades the bandwidth of the driver itself, respectively. Note that the transistors should operate in the linear region for better linearity, where the current density is much lower than that in the saturation region. Therefore, the device size is generally enormously large.

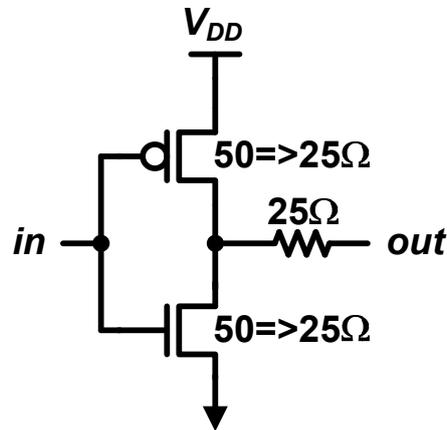


Figure 13. SST driver with series resistance.

Rather than putting a series resistor, it has been proposed that using a feedback resistor can change the game [13,40,44,50], which is shown in Figure 14. As we studied, the feedback resistor sets the biasing point that the CMOS operates in the saturation region. In addition, the DC output impedance becomes  $1/g_m$ , instead of  $1/g_{ds}$ . That means we can achieve a high current density of the saturation region and a low output impedance from  $1/g_m$  as well. In addition, the  $g_m$  is easy to be regulated by using a well-known constant- $g_m$  bias circuit [13,57].

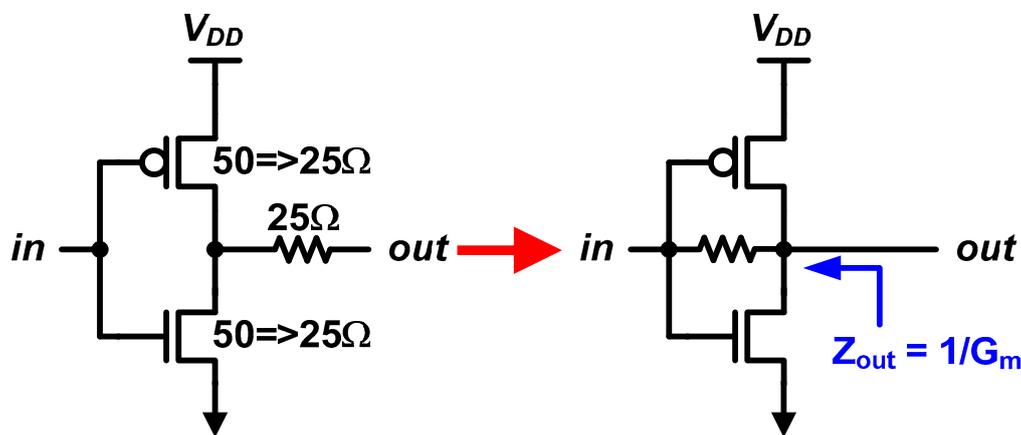


Figure 14. Output driver based on resistive-feedback inverter.

Although the feedback resistance does not affect the DC output impedance, the high-frequency output impedance, which affects the return loss of the transmitter, is a function of the feedback resistance. The output impedance is calculated as:

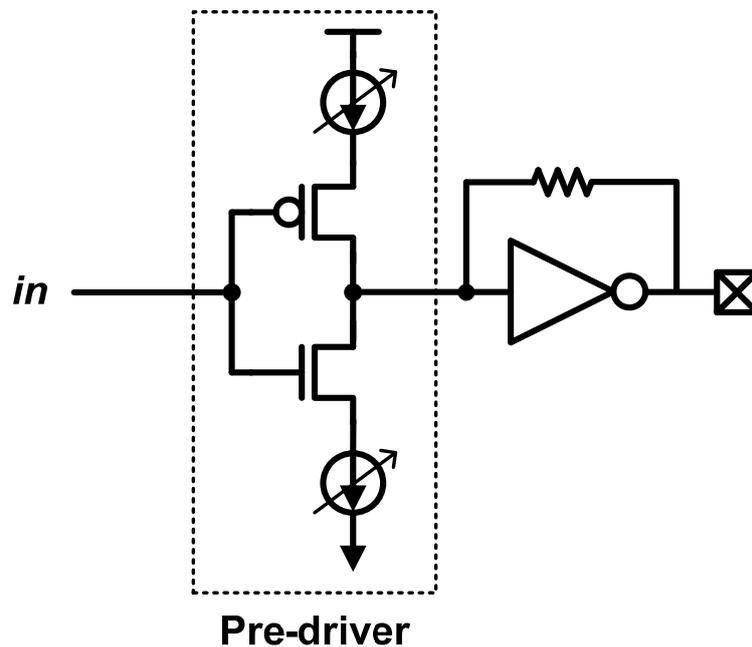
$$Z_{out} \cong \frac{1}{g_m + \frac{1}{r_o}} \cdot \frac{1 + sR_F C_{in}}{1 + sR_F C_{in} \left( \frac{1}{g_m r_o + 1} \right)}, \tag{11}$$

where  $C_{in}$  is the input capacitance of the driver [50]. We can find that the feedback introduces both zero (at  $\frac{1}{R_F C_{in}}$ ) and pole (at  $\frac{g_m r_o + 1}{R_F C_{in}}$ ). As a result, the output impedance becomes  $r_o$  at a very high frequency.

Therefore, a designer should carefully choose a proper  $R_F$  such that guarantees the zero frequency is higher than the Nyquist frequency of the transmit data.

On the other hand, there are two downsides of the resistive-feedback SST driver; low output swing and power consumption. Since the transistor should operate in the deep saturation region to have high  $r_o$ , the output impedance deviates from  $1/g_m$ , which is maintained by the constant- $g_m$  biasing, when the output swing increases. It also dissipates a higher current than that of the conventional SST driver due to the short-circuit current. However, as the data rate increases, the pre-driver's dynamic switching power, which is consumed for driving high input capacitance, dramatically increases. Note that the dynamic power is proportional to the switching frequency and the capacitance, whereas the driver's current consumption is fixed regardless of the data rate ( $I = V_{swing}/100\Omega$ ). As a result, it surpasses the static power consumption of the output driver [42]. As a result, the pre-driver power reduction, thanks to the small input capacitance of the resistive-feedback SST driver, is able to fully compensate the increased static power.

Another advantage of this driver is a simple slicing implementation because of its inherent current-driven nature. In the conventional drivers (including CML and SST), the output driver should be sliced to control the swing and the equalization coefficient; thus, it increases the complexity and the parasitic. On the other hand, in the resistive-feedback SST driver, the slicing can be included in the current-mode pre-driver as shown in Figure 15. That is, a simple current digital-to-analog convertor (DAC) in the pre-driver can replace the slicing at the output stage; thus, it significantly reduces the design complexity and parasitic effects. It has also been proven that the current DAC-based pre-driver is beneficial for pulse-amplitude modulation signaling in [40], where a fabricated 28-Gb/s PAM-4 transmitter chip is presented.



**Figure 15.** Current-mode pre-driver for resistive-feedback SST driver.

## 5. Conclusions

This paper introduces three state-of-the-art applications of CMOS inverter with resistor feedback, by providing the basic theories of those applications and the state-of-the-arts implementation results. The focus of this paper is not just enumerating the prior arts, but emphasizing the potential of CMOS inverter as an analog circuit. As discussed in the introduction, CMOS inverter becomes more powerful whereas the conventional analog circuits become less effective as technology scales down. As a result, I

believe that there are a lot of undiscovered usages of the CMOS inverter, which will need thorough examination in future research.

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