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Article

Ferroelectric Polarization Aided Low Voltage Operation of 3D NAND Flash Memories

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Abstract: In this paper, we proposed a novel structure enabling the low voltage operation of three-dimensional (3D) NAND flash memory. The proposed structure has a ferroelectric thin film just beneath the control gate, where the inserted ferroelectric material is assumed to have two stable polarization states. A voltage for ferroelectric polarization (V_{PF}) that is lower than the program or erase voltage is used to toggle the polarization state of the ferroelectric thin film, whose impact on the channel potential profile is analyzed to optimize operation voltage reduction. The channel potential of select word line (WL), where the natural local self-boosting (NLSB) effect occurs, increases due to the polarization state. Model parameters for the ferroelectric thin film of 8 nm are fixed to 15 $\mu C/cm^2$ for remanent polarization (P_r), 30 $\mu C/cm^2$ for saturation polarization (P_s), and 2 MV/cm for coercive field (E_c). Within our simulation conditions, a program voltage (V_{PGM}) reduction from 18 V to 14 V is obtained.

Keywords: 3D NAND flash memory; ferroelectric; natural local self-boosting (NLSB); program voltage for ferroelectric polarization (V_{PF})

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1. Introduction

The growing demand for data storage devices such as solid-state drives (SSD), mobile phones, and data centers has been supported by high density NAND flash memories. Their classical two-dimensional implementation [1,2] has been revolutionized to current three-dimensional (3D) NAND flash technologies based on cell stacking [3–5]. Further development is necessary to mitigate conventional cell-to-cell interference, reliability, and newly investigated issues [6–8]; which can be accomplished by operation voltage reduction of memory cells. In this paper, a low voltage NAND flash memory cell is proposed with ferroelectric thin film just beneath the control gate, where ferroelectric polarization gives an auxiliary biasing for the reduction of program or erase voltages. If the ferroelectric thin film is used, program disturb decreases because high channel potential of selected WL reduces the program disturb in the inhibited string. When the channel potential of selected WL is increased, the program disturb is decreased in the inhibited string. Therefore, we analyzed the channel potential of the proposed structure in this paper. In addition, the natural local self-boosting (NLSB) effect of selected word line (WL) in the inhibited string was analyzed according to the voltage for ferroelectric polarization (V_{PF}) [9,10]. The channel potential of proposed structure was compared with the channel potential of conventional structure. The 3D technology computer-aided design (TCAD) simulation was conducted to analyze the characteristic of the proposed structure, in which ferroelectric materials are with the ferroelectric permittivity model in ATLAS Silvaco^{TM} [11,12].

2. Proposed Structure and Operation

Figure 1 shows the proposed structure, which is composed of 16-word lines, string select line (SSL), ground select line (GSL), bit line (BL), and common source line (CSL). In this structure, the WL 8 was specified as the selected WL. The conventional structure consists of silicon, oxide, nitride, oxide, and silicon (SONOS) [13–15], where the ONO thickness combination is 8 nm, 8 nm, 4 nm. The proposed structure has ferroelectric thin film replacing the oxide beneath the control gate. Model parameters for the ferroelectric thin film are set as follows: 15 $\mu C/cm^2$ for P_r, 30 $\mu C/cm^2$ for P_s, and 2 MV/cm for E_c. The voltage for the ferroelectric polarization is smaller than the program voltage (or the absolute value of the erase voltage), and its application gives one of two stable polarization states in the ferroelectric thin film. Positive V_{PF} is applied prior to the program operation, when downward polarization is built in the ferroelectric thin film as illustrated in Figure 1. This downward polarization gives an auxiliary positive biasing on the tunnel oxide and nitride dielectric layers, which gives reduction in program voltage that is applied subsequent to the V_{PF}.

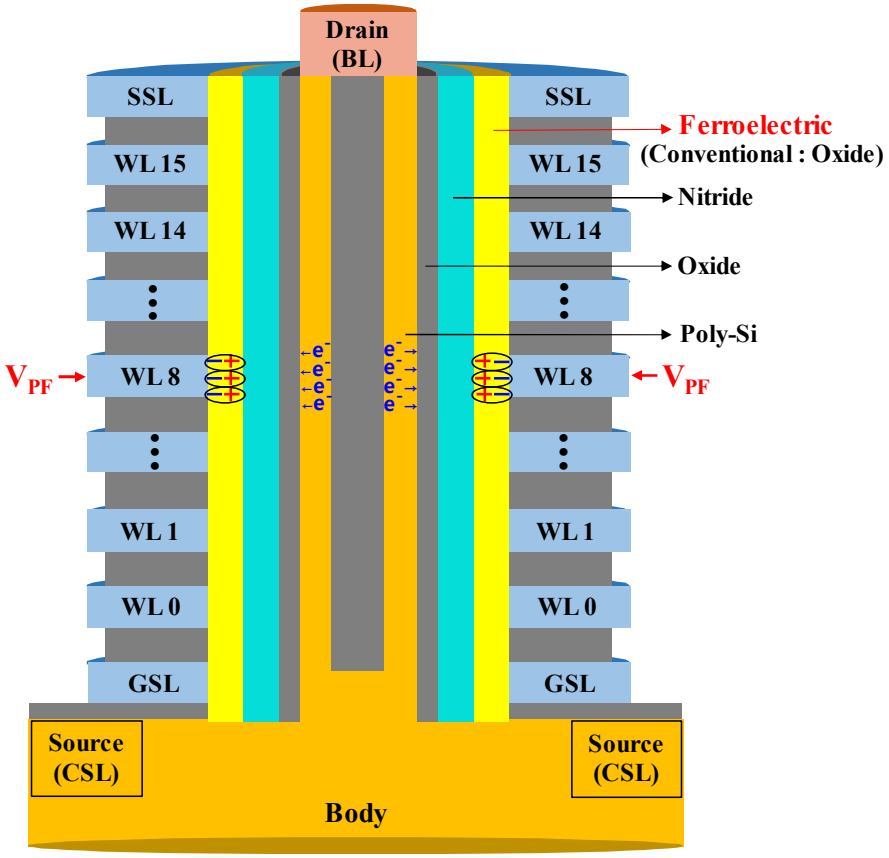

Figure 1. Proposed structure with ferroelectric thin film on top of the nitride.

Figure 2 shows the timing diagram of the WL 8 in the proposed structure. The V_{PGM} is fixed at 18 V, in addition, variable V_{PF} is applied for optimization. During the program operation, the pass voltage (V_{PASS}) of 6 V is applied to unselected WL. Meanwhile, 2.4 V is applied to SSL and bit line (BL). The channel potential profiles are collected at t_1 and t_2.

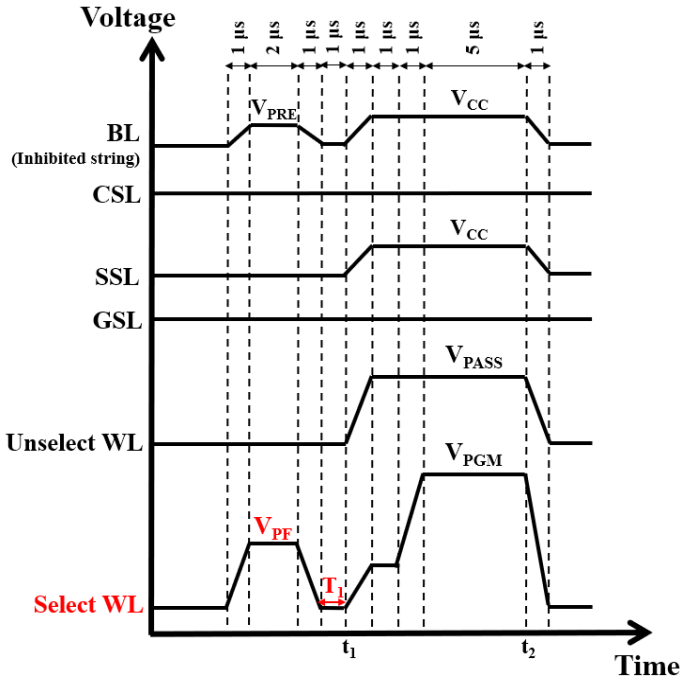

Figure 2. Timing diagram of the proposed structure. Pulse duration of V_{PF}, and the delay between V_{PF} and V_{PGM} is indicated as T_1.

3. Results and Discussions

Figure 3 shows the channel potential profiles when V_{PF} ranged from 3 V to 7 V. The V_{PF} time was fixed to 2 µs because V_{PF} time did not significantly affect the channel potential. As a result, the channel potential reached the maximum value when V_{PF} was 4 V. However, when V_{PF} is increased from 4 V to 7 V, the channel potential of WL 8 also decreased. The most suitable value of V_{PF} in this range is, therefore, 4 V, as the maximum channel potential was obtained.

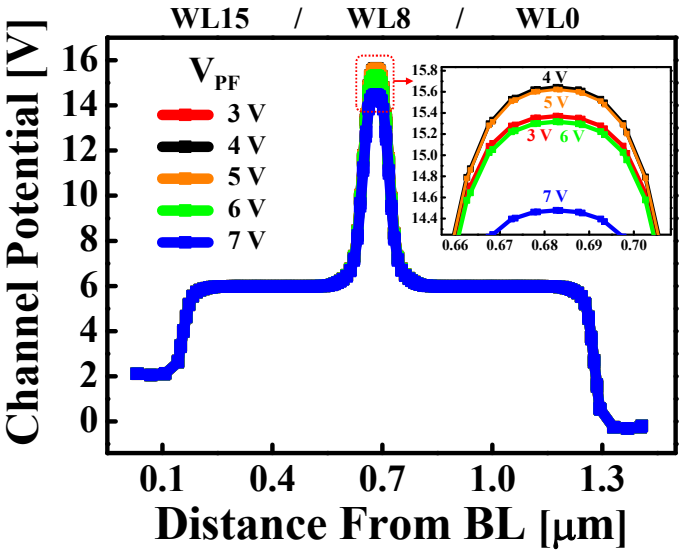

Figure 3. Comparison of the channel potential according to V_{PF} at t_2 in Figure 2.

In Figure 4, the channel potential profiles at V_{PF} of 4 V with a fixed pulse width of 2 µs, where the delay time between V_{PF} and V_{PGM} (T_1) is varied from 1 to 4 µs. In Figure 4a, when T_1 was 1 µs, the lowest channel potential was obtained. Furthermore, the channel potential increased with T_1, as the polarization phenomenon positively affected the channel

potential during T_1. As a result, with the increase of T_1, the duration in which the increased channel potential lasted longer. This conclusion is also supported by the results shown in Figure 4b. The channel potential of WL 8, where the natural local self-boosting effect occurs [10], also increased with T_1.

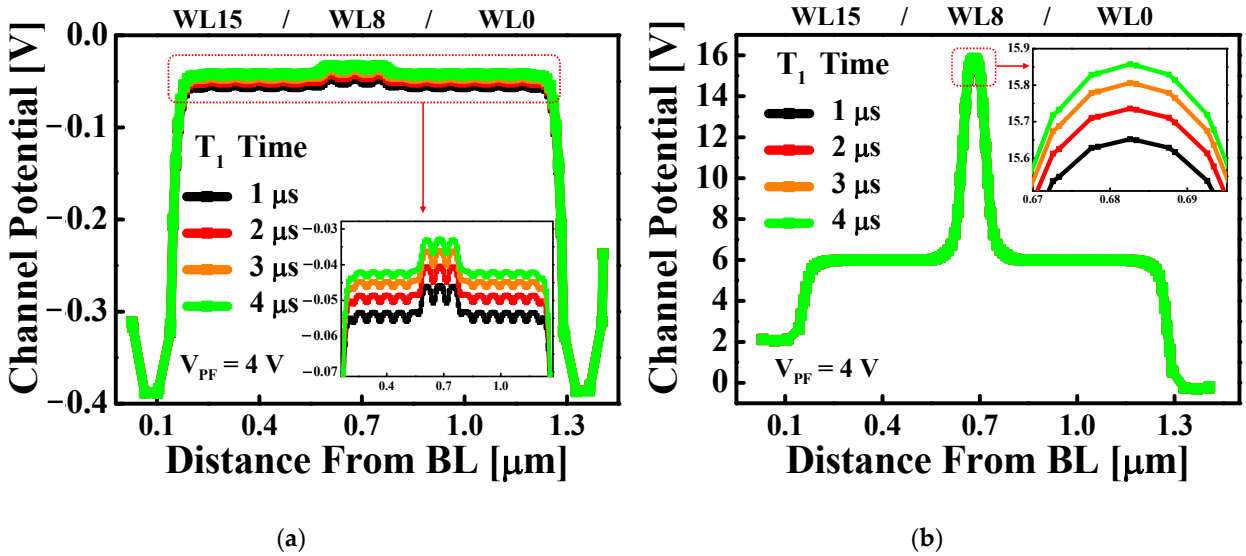

Figure 4. Channel potential profiles with various T_1 periods collected (**a**) at t_1 and (**b**) at t_2.

Figure 5a shows the channel potential profiles obtained from the proposed and conventional structures when V_{PGM} was 18 V. The highest values of channel potential of the conventional and proposed structures were 12.12 V, 13.95 V, and 15.64 V, respectively. The channel potential of proposed structure with 3.9 for ferroelectric permittivity (ε_f) is higher than that of the conventional structure. This result means the polarization phenomenon positively influenced the channel potential of WL 8. In addition, the channel potential of proposed structure with default value (200) of ε_f is highest since the more polarization occurs if the permittivity is higher. Therefore, the ferroelectric thin film can increase the channel potential because of the high permittivity and the polarization phenomenon.

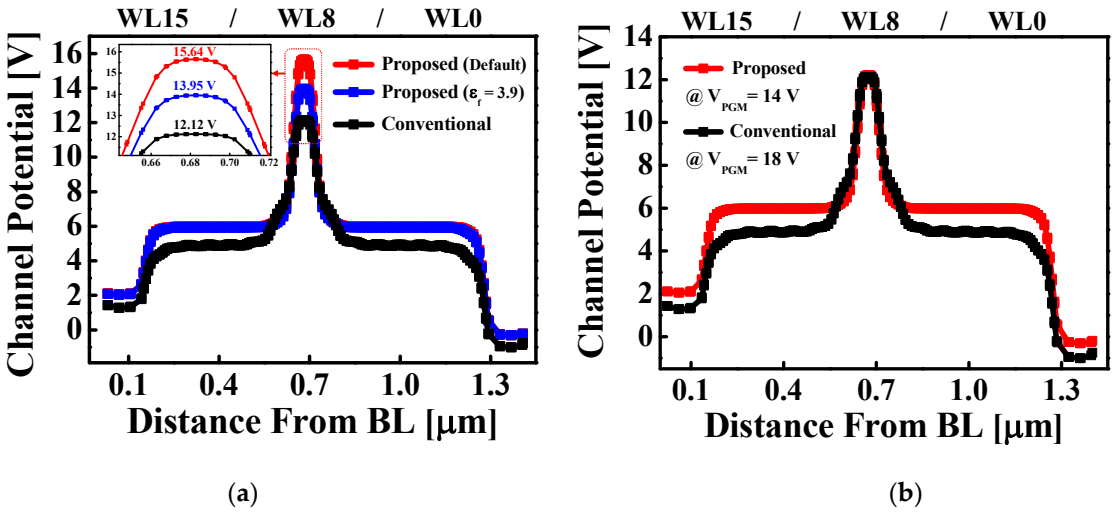

Figure 5. Comparison of the proposed structure and the conventional structure. (**a**) V_{PGM} was 18 V for structures; (**b**) V_{PGM} was 14 V for the proposed structure.

As a result, in the proposed structure, the same effect as that when 18 V is applied to the conventional structure can be obtained even if V_{PGM} is lowered. When V_{PGM} was 14 V, considering the proposed structure, the channel potential of WL 8 was the same as that of the conventional structure, as shown in Figure 5b. The voltage reduction obtained from these results is a significant advantage of the proposed structure for the 3D NAND flash memory.

When using a ferroelectric thin film, it may be difficult to make a thin film due to a process problem. In addition, since blocking oxide is used as a ferroelectric thin film, leakage current may occur. However, if several drawbacks of ferroelectric material are further studied, they can be sufficiently used in mass production because they have great advantages.

4. Conclusions

In this paper, we proposed a novel structure composed of ferroelectric material for the 3D NAND flash memory. When V_{PF} was applied to the WL 8, the channel electrons of the neighbor cells migrated to the WL 8. The channel potential increased with T_1 as the polarization phenomenon improved the channel potential during T_1. In addition, experiments with different V_{PF} were conducted to obtain the voltage (4 V) that maximized the channel potential. The maximum channel potential of the proposed structure was higher than that of the conventional structure. Therefore, the same electrical behavior of the conventional structure when V_{PGM} was 18 V can be observed when V_{PGM} was lowered to 14 V with the proposed structure, which is a significant advantage for the 3D NAND flash memory.

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