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A Novel Single-Switch Single-Stage LED Driver with Power Factor Correction and Current Balancing Capability

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Abstract: A novel single-switch single-stage high power factor LED driver is proposed by integrating a flyback converter, a buck–boost converter and a current balance circuit. Only an active switch and a corresponding control circuit are used. The LED power can be adjusted by the control scheme of pulse–width modulation (PWM). The flyback converter performs the function of power factor correction (PFC), which is operated at discontinuous-current mode (DCM) to achieve unity power factor and low total current harmonic distortion (THDi). The buck–boost converter regulates the dc-link voltage to obtain smooth dc voltage for the LED. The current–balance circuit applies the principle of ampere-second balance of capacitors to obtain equal current in each LED string. The steady-state analyses for different operation modes is provided, and the mathematical equations for designing component parameters are conducted. Finally, a 90-W prototype circuit with three LED strings was built and tested. Experimental results show that the current in each LED string is indeed consistent. High power factor and low THDi can be achieved. LED power is regulated from 100% to 25% rated power. Satisfactory performance has proved the feasibility of this circuit.

Keywords: current balance; flyback converter; light-emitting diode (LED); power factor; single-stage

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1. Introduction

Compared with fluorescent lamps and high-intensity discharge (HID) lamps, LEDs have the advantage of being small size, long-life, easy dimming, have high luminous efficiency, better color rendering and fast response. In addition, unlike fluorescent lamps that need to use mercury metal that is harmful to the environment, LEDs do not contain any mercury and are environmentally friendly. Therefore, LED has gradually replaced fluorescent lamps and HID lamps, and has become the mainstream light source of modern lighting [1–3]. LED is a point light source with a small size, so it is difficult to dissipate heat, therefore, the power of a single LED is usually not large. For high-power LED lighting systems, multiple LEDs must be used to meet the power requirements. When many LEDs are used, the connection method is to connect multiple LEDs in series to form a LED string, and then connect the LED strings in parallel [4,5].

For parallel-connected LED strings, due to the inevitable subtle differences between each LED, when the number of LEDs in series increases, the conduction voltage difference of each string will increase, resulting in inconsistent LED currents in each string. Moreover, LEDs have negative temperature coefficient characteristics, which will strengthen the current imbalance between each string, and even result in LED thermal runaway and burn. Therefore, the research on current-balance technology of parallel LEDs is an important topic of LED lighting systems [4]. The current-mirror technology is that each LED string is connected in series with a power transistor of the same model. In theory, when the control voltage of each power transistor is equal, the current will also be equal [6,7]. The advantage of the current-mirror method is that the control circuit is simple, but the disadvantage is

that the conducting voltage of the transistors are high, resulting in high conducting losses. Therefore, current-mirror technology is only suitable for low power applications.

For medium and high-power LED drivers, many literatures have proposed LED current-balance methods, which are mainly classed into active current balancing technology [8–11] and passive current balancing technology [12–15]. The cost of active technology is higher because each LED string needs to be equipped with an independent current feedback control circuit to control its own active switch, and the current of each string can be adjusted independently, which is conducive to creating a unique lighting situation. Passive technologies do not need to use active switches and the corresponding control circuits. They only use passive components such as diodes, inductors, capacitors or transformers. Some passive approaches connect the primary windings of transformers in series to obtain the same average current in the secondary windings [12,13]. Some approaches connect each LED string in series with a high reactance capacitor. Due to the series connection, the LED current is mainly dominated by the high reactance capacitor. In this way, the impact of current imbalance caused by the difference in LED impedance is reduced [14,15]. Compared with active technologies, passive technologies do not require additional active switches and control circuits. However, these passive methods need to use bulky transformers or capacitors. This hinders the realization of a small and light-weight LED driver.

On the other hand, in order to improve power quality, increase the utilization of power equipment and reduce electromagnetic interference (EMI), advanced countries have formulated strict specifications for power factor and THDi of electrical products. For example, IEC 61000-3-2 Class D and IEEE 519 set the power factor and THDi specifications of lighting products. Therefore, the LED driver needs to add an additional ac/dc converter to perform the function of power factor correction (PFC). This results in two-stage LED drivers. The first stage is a PFC converter, and the second stage is a dc/dc converter which is used to regulate LED power. The additional PFC converter can improve the power factor and reduces THDi. However, these two-stage circuits must use more components and two control circuits. Furthermore, it takes two energy conversion processes, leading to more losses. In order to improve circuit efficiency and reduce the number of components, many researchers have proposed the single-stage solutions by integrating the PFC converter and the dc/dc converter [16–19]. In a single-stage circuit, the PFC converter and the dc/dc converter share one or more active switches. This not only saves the active switch and its control circuit, but also reduces the energy conversion process, thereby reducing the cost and improving the conversion efficiency.

In this paper, a novel single-stage circuit is proposed to drive multiple LED strings. The circuit architecture mains integrate a flyback converter and a buck–boost converter. This circuit only uses an active switch which is PWM controlled to adjust the LED power. It can achieve high power factor, low THDi and the current-balance capability.

2. Circuit Configuration and Operation Mode Analysis

2.1. Circuit Configuration

Figure 1 shows the proposed single-stage high power factor LED driver. This circuit is suitable for driving odd strings of LEDs. Figure 1a,b show the LED drivers with three LED strings and seven LED strings, respectively. This article will take Figure 1a as an example to illustrate the operation principle of the proposed circuit. The circuit configuration mainly consists of a flyback converter, a buck–boost converter, and some L-C passive components used as the current balancing circuit. Both converters share an active switch S_1. V_{in} is the mains ac voltage, L_f and C_f form a low-pass filter to remove the high-frequency current of the flyback converter. The flyback converter serves as a power-factor corrector which is designed to operate at discontinuous-current mode (DCM) to achieve high power factor and low THDi. The buck–boost converter is pulse-width modulated to adjust the power of the LED strings. By using the principle of ampere-second balance of capacitor, the current of each LED string can be equalized. The resistor R_{sense} is used to detect the current of the

LED string one, so as long as the current of the LED string one is controlled, the current of each string of LEDs can be controlled.

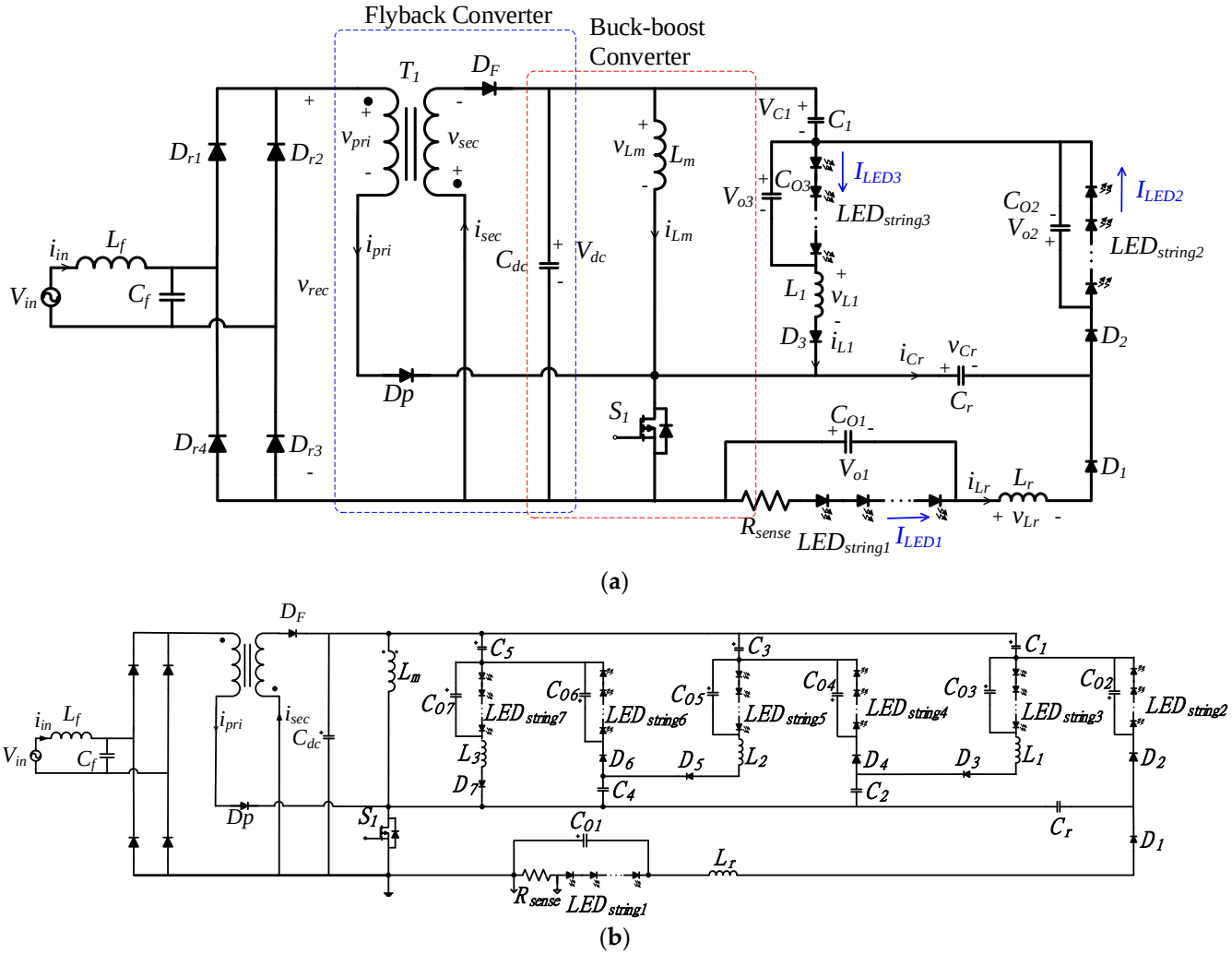


Figure 1. Proposed single-stage single-switch LED drivers (**a**) three LED strings; (**b**) seven LED strings.

2.2. Operation Mode Analysis

In order to perform the PFC function, the flyback converter is operated at DCM. In addition, the following assumptions are made to simplify circuit analysis.

1. All components are ideal.
2. The capacitors C_{dc}, C_1, C_{o1}, C_{o2}, and C_{o3} are large enough, and the voltages across these capacitors (V_{dc}, V_{C1}, V_{o1}, V_{o2}, and V_{o3}) can all be regarded as constant values.
3. The input voltage is an ideal sinewave, $v_{in}(t) = V_m \sin(\omega t)$, where V_m represents the amplitude of the input voltage, and $\omega = 2\pi f_L$ represents the angular frequency.
4. The switching frequency f_s of the active switch is much higher than the input voltage frequency f_L ($f_s >> f_L$).

All the inductors are designed to operate at DCM. At steady-state, the circuit operation can be divided into six operation modes in a high-frequency switching cycle. Figure 2 shows the current paths of each mode where v_{rec} represents the rectified input voltage. Figure 3 shows the conceptual voltage and current waveforms of the key components. The detailed analysis of each mode is described as follows:

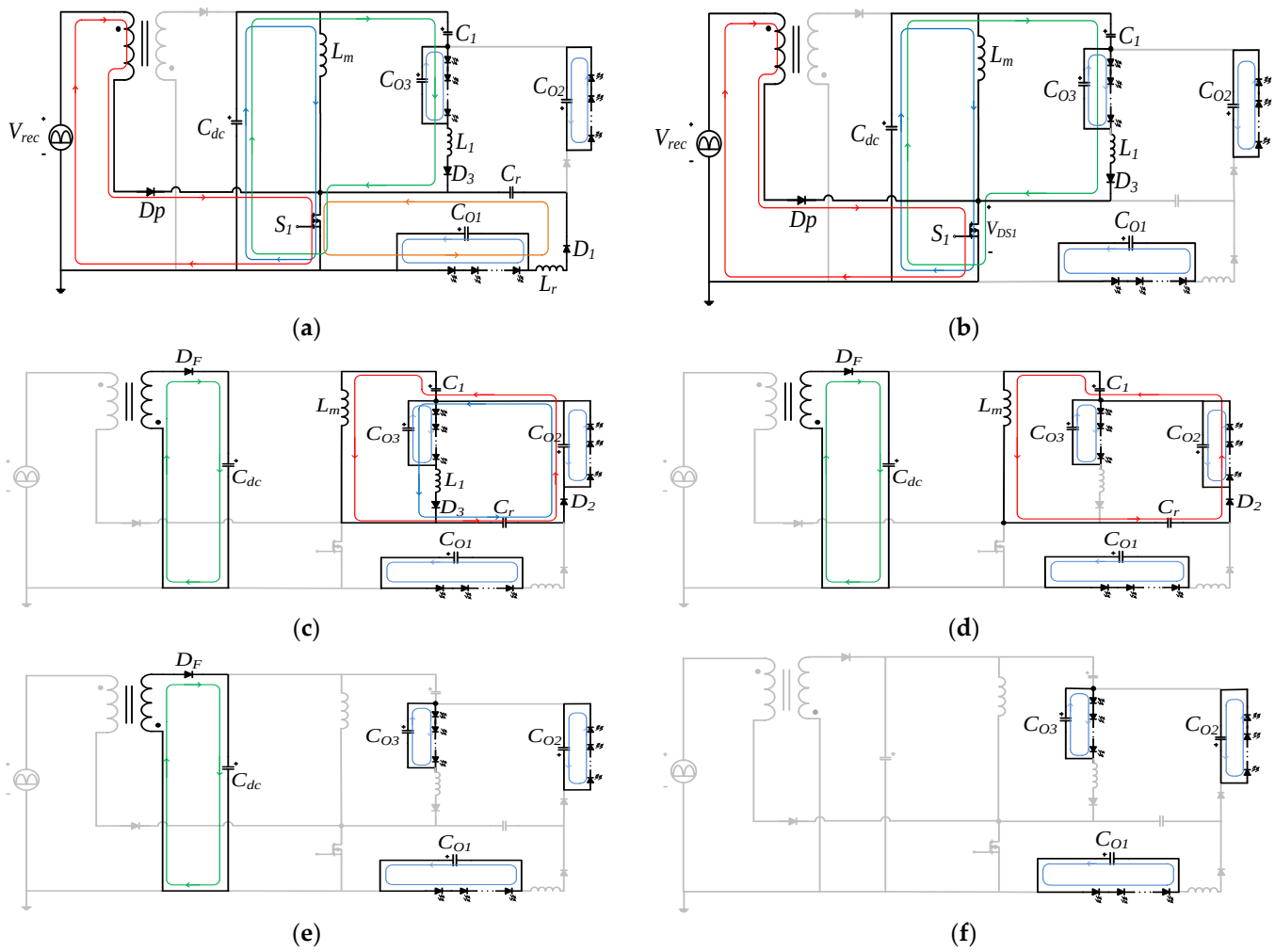


Figure 2. Operation modes (**a**) mode I; (**b**) mode II; (**c**) mode III; (**d**) mode IV; (**e**) mode V; (**f**) mode VI.

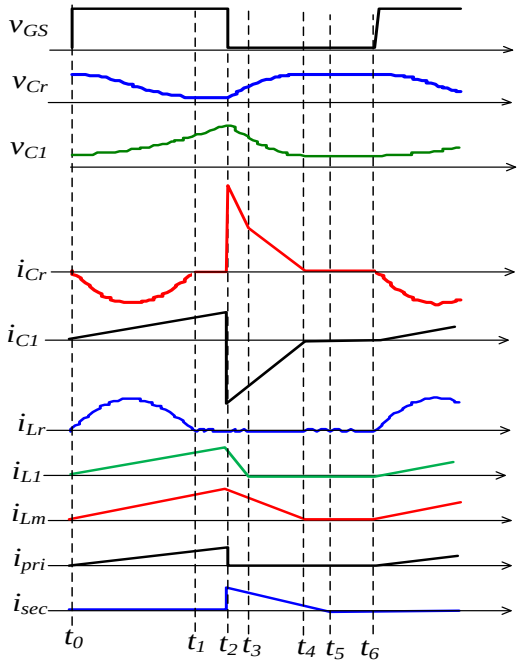


Figure 3. Conceptual voltage and current waveforms.

2.2.1. Operation Mode I ($t_0 < t < t_1$)

The operation mode I starts at time t_0 when the gate signal v_{GS1} changes from low-level to high-level, and S_1 is turned on. The rectified voltage v_{rec} is across on the primary winding of the transformer T_1, and the primary current i_{pri} rises linearly from zero.

$$i_{pri}(t) = \frac{V_m|sin(2\pi f_L t)|}{L_p}(t - t_0) \tag{1}$$

where L_p represents the inductance of the primary winding. At the same time, the voltage across the inductor L_m is equal to the dc-link voltage V_{dc}. L_m is charged and its current i_{Lm} rises linearly from zero.

$$i_{Lm}(t) = \frac{V_{dc}}{L_m}(t - t_0) \tag{2}$$

The voltage across the inductor L_1 is equal to:

$$v_{L1}(t) = V_{dc} - V_{C1} - V_{o3} \tag{3}$$

Therefore, the current i_{L1} starts to rise linearly from zero.

$$i_{L1}(t) = \frac{V_{dc} - V_{C1} - V_{o3}}{L_1}(t - t_0) \tag{4}$$

As shown in Figure 2a, C_1 is charged and its voltage rises during this mode. On the other hand, because S_1 and D_1 are conducting, the inductor L_r and the capacitor C_r form a resonant circuit. The voltage across L_r is equal to:

$$v_{Lr}(t) = v_{Cr}(t) - V_{o1} \tag{5}$$

Its state equations can be expressed as:

$$\begin{cases} L_r \frac{di_{Lr}(t)}{dt} = v_{Cr}(t) - V_{o1} \\ i_{Lr}(t) = -i_{Cr}(t) \\ i_{Cr}(t) = C_r \frac{dv_{Cr}(t)}{dt} \end{cases} \tag{6}$$

From Equation (6), the voltage across the capacitor C_r and resonant current i_{Lr} can be obtained and expressed as follows:

$$\begin{cases} v_{Cr}(t) = V_{o1} + [v_{Cr}(t_0) - V_{o1}]cos\omega_r(t - t_0) \\ i_{Lr}(t) = \frac{v_{Cr}(t_0) - V_{o1}}{Z_r} sin\omega_r(t - t_0) \end{cases} \tag{7}$$

where Z_r and ω_r represent the equivalent impedance and angular frequency of the resonant circuit, respectively.

$$\begin{cases} Z_r = \sqrt{L_r/C_r} \\ \omega_r = 2\pi f_r = \frac{1}{\sqrt{L_r C_r}} \end{cases} \tag{8}$$

The resonant frequency f_r is designed to be greater than the switching frequency f_s, and the duty ratio of S_1 is designed to be large enough so that i_{Lr} would resonant to zero before S_1 was turned off. When i_{Lr} resonates to zero at time t_1, the circuit enters the next operation mode.

2.2.2. Operation Mode II ($t_1 < t < t_2$)

In this mode, D_1 and D_2 are off due to reverse bias. Currents i_{Cr} and i_{Lr} are both zero, and the voltage across C_r remains unchanged. S_1 remains on, so i_{pri}, i_{Lm} and i_{L1} continue to rise. When the gate signal v_{GS1} changes from high-level to low-level, S_1 is turned off, and the circuit enters the operation mode III.

2.2.3. Operation Mode III ($t_2 < t < t_3$)

At the end of mode II, i_{pri}, i_{Lm} and i_{L1} reach peak values, which are represented by $i_{pri,peak}$, $i_{Lm,peak}$ and $i_{L1,peak}$, respectively. When S_1 is off, there must be current loops to maintain the flux balance of T_1, L_m and L_1. Therefore, there is an induced current in the secondary winding of T_1. The induced current i_{sec} charges the dc-link capacitor C_{dc}, and can be expressed as:

$$i_{sec}(t) = n i_{pri,peak}(t) - \frac{V_{dc}}{L_s}(t - t_2) \tag{9}$$

where L_s represents the inductance of the secondary winding, and n represents the ratio of the number of turns between the primary winding and the secondary winding ($n = N_1/N_2$). In this mode, C_1 is discharged and its voltage decreases. Meanwhile, the current of inductor L_1 flows through L_1-D_3-C_r-D_2-C_{o2}-C_{o3}, i_{L1} can be expressed as:

$$i_{L1}(t) = i_{L1,peak} - \frac{v_{Cr}(t) + V_{o2} + V_{o3}}{L_1}(t - t_2) \tag{10}$$

As shown in Figure 2c, i_{L1} charges C_r, C_{o2}, and C_{o3}. Because the peak value of i_{sec} is proportional to the input voltage, the time required for i_{sec} to decrease to zero is also proportional to the input voltage and is not a fixed value. Figure 3 shows the conceptual voltage and current waveforms when the input voltage is at the peak value. In this case, the time required for i_{sec} to drop to zero is longer than i_{Lm} and i_{L1}. In other words, i_{Lm} and i_{L1} fall to zero earlier than i_{sec}. When i_{L1} drops to zero, the circuit enters the operation mode IV.

2.2.4. Operation Mode IV ($t_3 < t < t_4$)

In this mode, S_1, D_1, and D_3 are off, D_2 is on, the inductors L_s and L_m continue to release energy, and i_{sec} and i_{Lm} continue to decrease. At time t_4, i_{Lm} drops to zero and this mode ends.

2.2.5. Operation Mode V ($t_4 < t < t_5$)

In this mode, i_{sec} continues to charge the dc-link capacitor. When i_{sec} drops to zero, the circuit enters the next operation mode.

2.2.6. Operation Mode VI ($t_5 < t < t_6$)

The currents of all inductors are equal to zero, and the LEDs are continuously lit by the energy provided by the parallel capacitors (C_{o1}, C_{o2}, and C_{o3}). When the gate signal v_{GS1} becomes high-level, S_1 is turned on again, and the circuit enters the operation mode I of the next high-frequency cycle.

3. Analysis on Current Balance and Power Factor Correction

3.1. Principle of Current Balance

According to the description of the operating mode, the discharging current of C_r flows through D_1 in mode I. Therefore, the average value of this discharge current in a high-frequency cycle is equal to the average current of the LED string one. In mode III and mode IV, C_r is charged. As shown in and Figure 2c,d, this charging current flows through D_2, so its average value is equal to the average current of the LED string two. Based on the principle of the ampere-second balance of the capacitor, that is that the net current of a capacitor will equal zero. In other words, the average value of the capacitor charging current is equal to the average value of its discharge current. Therefore, the average current of LED string one and LED string two would be equal.

$$I_{LED1} = I_{LED2} \tag{11}$$

In mode I and mode II, C_1 is charged through D_3. Similarly, the average value of the charging current of C_1 is equal to the average current of the LED string three. In mode III

and mode IV, C_1 is charged through D_2, and the average value of the discharging current of C_1 will be equal to the average current of the LED string two. Applying the ampere-second balance principle to C_1, it can be concluded that the average currents of the LED string two and the LED string three are equal.

$$I_{LED2} = I_{LED3} \tag{12}$$

Combining Equations (11) and (12), the current flowing through each LED string is equal.

$$I_{LED1} = I_{LED2} = I_{LED3} \tag{13}$$

3.2. Flyback PFC Circuit

The flyback converter is designed to operate at DCM during the entire input voltage cycle. The primary current i_{pri} of T_1 rises linearly from zero during mode I and mode II (t_0-t_2), and rises to a peak value, which can be expressed as:

$$i_{pri,peak}(t) = \frac{V_m D T_s \sin(2\pi f_L t)}{L_p} \tag{14}$$

where D represents the duty ratio of the active switch. High-power factor and low THDi can be achieved by operating the flyback converter at DCM [20]. The high-frequency components of i_{pri} can be filtered out by using the low-pass filter (L_f, C_f), so that the input current i_{in} will be equal to the average value of i_{pri} in each high-frequency cycle.

The input power is equal to the average value of the instantaneous power, which can be expressed as:

$$P_{in} = \frac{1}{2\pi}\int_0^{2\pi} V_m \sin(2\pi f_L t)\cdot i_{in}(t) d(2\pi f_L t) = \frac{V_m^2}{4L_P} D^2 T_S \tag{15}$$

Assuming that the conversion efficiency of the circuit is η, the output power is equal to:

$$P_O = P_{LED} = \eta \times P_{in} = \frac{\eta V_m^2 D^2 T_S}{4L_P} \tag{16}$$

4. Design Equations of Circuit Parameters

4.1. Design Equations of the Flyback Converter

From Equation (16), the primary inductance L_p of T_1 can be obtained, which is expressed by the following equation:

$$L_P = \frac{\eta V_m^2 D^2 T_s}{4P_o} \tag{17}$$

The transformer primary current i_{pri} rapidly drops to zero at the moment when the active switch is turned off. In order to maintain the magnetic flux balance of T_1, it will induce a current in the secondary winding. The secondary current i_{sec} can be obtained by substituting Equation (14) into Equation (9). At t_2, i_{sec} starts to decrease linearly from a peak value, and reaches zero at t_5. The fall time of i_{sec} is denoted as T_{off}.

$$T_{off} = t_5 - t_2 \tag{18}$$

The primary inductance and secondary inductance of T_1 is proportional to the square of the number of turns, that is:

$$L_s = \left(\frac{n_2}{n_1}\right)^2 L_p = \left(\frac{1}{n}\right)^2 L_p \tag{19}$$

Combining Equations (9), (14), (18) and (19) gets:

$$T_{off}(t) = \frac{V_m|\sin(2\pi f_L t)|}{nV_{dc}} DT_s \tag{20}$$

At DCM operation, T_{off} is less than (1-D)T_s.

$$T_{off}(t) = \frac{V_m|\sin(2\pi f_L t)|}{nV_{dc}} DT_s < (1-D)T_s \tag{21}$$

The longest fall time $T_{off,max}$ occurs when the input voltage is at its maximum and is equal to:

$$T_{off,max} = \frac{V_m DT_s}{nV_{dc}} \tag{22}$$

In order to operate the flyback converter at DCM during the entire line cycle, the following inequality must exist:

$$\frac{V_{dc}}{V_m} > \frac{1}{n} \cdot \frac{D}{1-D} \tag{23}$$

The higher the amplitude of the input voltage, the higher the dc-link voltage required to satisfy the inequality (23). However, since the active switch is not operated at zero-voltage switching on (ZVS), high dc-link voltage will cause more switching losses. It means that the proposed circuit is not valid for a universal input voltage range (110–220 Vrms). When the input voltage is different, the turn ratio of the coupled inductor of the flyback converter should also be different. In this way, an adequate dc-link voltage can be chosen to satisfy the inequality (23).

4.2. Design Equations of the Current Balancing Circuit

As shown in Figure 3, both inductors L_m and L_1 are operated at DCM. At steady-state operation, the average value of the inductor currents is zero. Therefore, the increase in i_{L1} when S_1 is on is the same as the decrease when S_1 is off.

$$\frac{(V_{dc} - V_{C1} - V_{O3})DT_s}{L_1} + \frac{(-V_{O3} - V_{O2} - V_{Cr})D_{off,L1}T_s}{L_1} = 0 \tag{24}$$

where $D_{off,L1}$ is defined as the ratio of the falling time of i_{L1} to T_s. Generally, the voltage and current of each LED string are approximately equal, that is V_{O1} = V_{O2} = V_{O3} = V_O, and I_{LED1} = I_{LED2} = I_{LED3} = I_{LED} from Equation (24), which gets:

$$D_{off,L1} = \frac{(V_{dc} - V_{C1} - V_O)DT_s}{2V_O + V_{Cr}} \tag{25}$$

The net change of i_{Lm} when S_1 is turned on and off is also equal to zero.

$$\frac{V_{dc}DT_s}{L_m} + \frac{(V_{C1} - V_{O2} - V_{Cr})D_{off,Lm}T_s}{L_m} = 0 \tag{26}$$

where $D_{off,Lm}$ is defined as the ratio of the falling time of i_{Lm} to T_s, and is equal to:

$$D_{off,Lm} = \frac{DV_{dc}}{V_O + V_{Cr} - V_{C1}} \tag{27}$$

As shown in Figure 1, I_{LED3} will be equal to the average current of L_1 since the net current of C_1 is zero.

$$I_{LED3} = \frac{1}{2}\frac{(V_{dc} - V_{C1} - V_{O3})D\left(D + D_{off,L1}\right)T_s}{L_1} \tag{28}$$

Substituting Equation (25) into Equation (28), the inductance L_1 can be obtained, which is expressed as follows:

$$L_1 = \frac{1}{2}\frac{(V_{dc} - V_{C1} - V_{O3})DT_s}{I_{LED3}} \cdot \left(D + \frac{(V_{dc} - V_{C1} - V_O)D}{2V_O + V_{Cr}}\right) \tag{29}$$

During mode III and mode IV, i_{LM} and i_{L1} flow through D_2, therefore, I_{LED2} can be expressed as:

$$I_{LED2} = \frac{1}{2}\left(\frac{V_{dc}DD_{off,Lm}T_s}{L_m} + \frac{(V_{dc} - V_{C1} - V_{O3})DD_{off,L1}T_s}{L_1}\right) \tag{30}$$

Substituting Equations (25), (27) and (29) into Equation (30), the inductance L_m can be obtained, which is expressed as follows:

$$L_m = \frac{V_{dc}^2 D^2 T_s (V_{dc} - V_{C1} + V_{Cr} + V_O)}{2I_{LED}(2V_O + V_{Cr})(V_O + V_{Cr} - V_{C1})} \tag{31}$$

As stated in mode I, i_{Lr} resonances to zero before S_1 being turned off. Therefore, the following inequality must exist:

$$\pi\sqrt{L_r C_r} < DT_s \tag{32}$$

The inductance L_r can be obtained from Equation (32), which is expressed as follows:

$$L_r < \frac{D^2 T_s^2}{C_r \pi^2} = \frac{D^2}{C_r \pi^2 f_s^2} \tag{33}$$

5. Experimental Results

A 90-W prototype circuit was built and tested to demonstrate the functions of power factor correction and current balancing capability. Table 1 shows the specification of the proposed LED driver. The load is three LED strings. Each string consists of 30 1-W LEDs connected in series. The rated voltage and current of each LED is 3.05 V and 0.328 A, respectively. Table 2 shows the circuit parameters. Some of the circuit parameters are designed as follows:

Table 1. Specification of the proposed LED driver.

Input voltage v_{in}	110 V ± 10% (rms), 60 Hz
Output power P_o	90 W (30 W × 3)
LED voltage V_{LED}	91.5 V (3.05 V × 30)
LED voltage I_{LED}	0.328 A
Equivalent LED Resistance R_{LED}	279 Ω
Switching frequency f_s	50 kHz
Duty ratio D	0.4

Table 2. Circuit parameters.

The low-pass inductance L_f	1.89 mH
The low-pass capacitance C_f	0.47 μF
Dc-link capacitance C_{dc}	330 μF
Output capacitance C_{o1}~C_{o3}	47 μF
Capacitance C_1	10 μF
Capacitance C_r	35.2 μF
Inductance L_p, L_s	194.7 μH
Inductances L_m, L_1, L_r	326 μH, 278 μH, 170 μH
Active switches S_1	SPW47N60C3
Bridge-rectifier diodes D_{r1}~D_{r4}	MUR460
Diodes D_p, D, D_b, D_1~D_3	C3D10060 A

5.1. Component Parameters Design

5.1.1. Primary and Secondary Inductances of Transformer T_1

The turns ratio n of T_1 is chosen as one. Assuming that the overall efficiency of the circuit is 90% and using Equation (17), the primary inductance and the secondary inductance can be calculated.

$$L_p = L_s = \frac{\eta V_m^2 D^2 T_s}{4P_o} = \frac{0.95 \times 156^2 \times 0.4^2}{4 \times 90 \times 50 \times 10^3} = 194.7\ \mu\text{H}$$

5.1.2. Inductance and Capacitance of the Resonant Circuit

The capacitance of the resonant circuit can be obtained as follows:

$$C_r = \frac{1}{2 f_s R_{LED}} = \frac{1}{2 \times 50 \times 10^3 \times 279} = 35.8\ \text{nF}$$

In order to meet Equation (33), inductance of the resonant circuit must satisfy the following inequality:

$$L_r < \frac{D^2}{C_r \pi^2 f_s^2} = \frac{0.4^2}{35.8 \times 10^{-9} \times \pi^2 \times (50 \times 10^3)^2} = 181\ \mu\text{H}$$

Here, L_r is chosen to be 170 μH.

5.1.3. Inductances of L_1 and L_m

Using Equation (23), the minimum value of the dc-link capacitance can be obtained.

$$V_{dc} > \frac{1}{n} \cdot \frac{D}{1-D} \cdot V_m = \frac{0.4 \times 156}{1 \times 0.6} = 104\ \text{V}$$

Here V_{dc} is chosen to be 110 V.

The average voltage of the resonant capacitor is approximately equal to half of its maximum voltage. Therefore, the average voltage of the resonant capacitor is equal to:

$$V_{Cr} = \frac{1}{2}\sqrt{\frac{2 I_{LED}^2 R_{LED}}{C_r f_s}} = \frac{1}{2}\sqrt{\frac{2 \times 0.328^2 \times 279}{35.8 \times 10^{-9} \times 50 \times 10^3}} = 91.56\ \text{V}$$

The inductance L_1 can be calculated by using Equation (29).

$$L_1 = \frac{1}{2}\frac{(V_{dc} - V_{C1} - V_{O3}) D T_s}{I_{LED3}} \cdot \left(D + \frac{(V_{dc} - V_{C1} - V_O) D}{2V_O + V_{Cr}} \right) = 278.3\ \mu\text{F}$$

The inductance L_m can be calculated by using Equation (31).

$$L_m = \frac{V_{dc}^2 D^2 T_s (V_{dc} - V_{C1} + V_{Cr} + V_O)}{2I_{LED}(2V_O + V_{Cr})(V_O + V_{Cr} - V_{C1})} = 325.87\ \mu\text{F}$$

5.2. Control Circuit and Experimental Results

The closed-loop control circuit of the driving circuit adopts the PWM controller (TL494), as shown in Figure 4. The output of TL494 is used to turn the active switch on and off, and its frequency can be determined by capacitor C_T and resistor R_T. The voltage across R_{sense} in the main circuit is sensed via R_1 and R_2 and compared with the internal sawtooth-wave voltage of TL494 to adjust the duty ratio of the active switch. In this way, the LED current can be regulated.

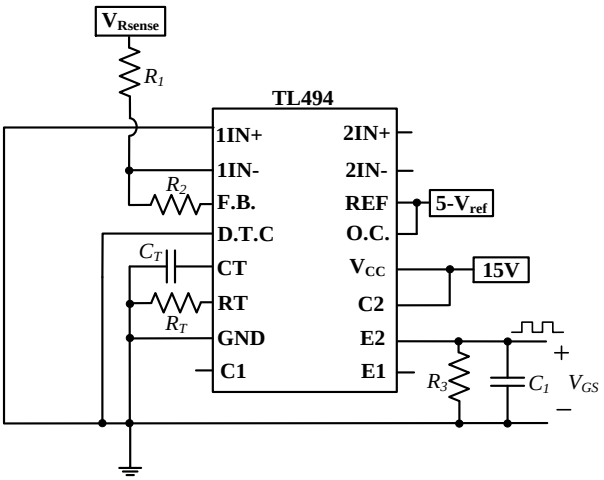


Figure 4. Closed-loop control circuit.

Figures 5–9 show the experimental waveforms when the circuit is operating at rated power (90 W). The input voltage and current waveforms are shown in Figure 5. It is demonstrated that the input current is an approximate sinusoidal wave and in phase with the input voltage. It ensures high power factor and low THDi. The measured power factor and THDi are 0.99 and 2.91%, respectively. The measured output power and total losses are 90.3 W and 10.8 W, respectively. The circuit efficiency is calculated to be 89.3%. Figure 6 shows the harmonic spectrum of the input line current. The THDi is 2.91% and all harmonics are in compliance with the IEC 61000-3-2 Class C. Figure 7 shows the waveforms of the primary and secondary currents of T_1. Both currents are operated at DCM, which is consistent with the design goal. Figure 8 shows the current waveforms of the inductors L_m, L_1, and L_r, showing that i_{Lr} has resonated to zero before the active switch is turned off; i_{L1} drops to zero before i_{Lm}, and they all operate at DCM. Figure 9 shows the current waveforms of three LED strings with the same number of LEDs, showing that the current of each string is equal. This proves the current balancing capability of the circuit.

In order to further verify the current balancing function, the circuit driving three LED strings of different numbers of LEDs was tested. The number of LEDs in the three strings are 33, 30, and 27, respectively. Figure 10 shows measured currents of the three LED strings. It was demonstrated that the current of each string still remains the same when the load power changes by plus or minus 10%.

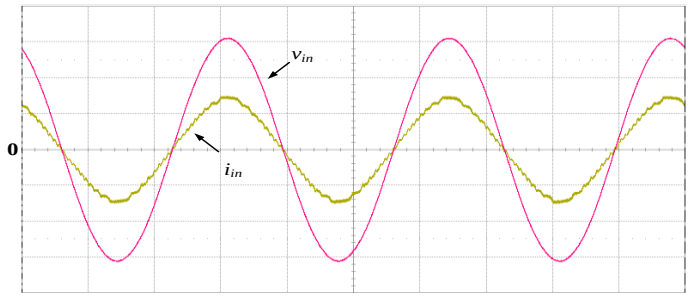


Figure 5. Input voltage and current waveforms. (v_{in}: 100 V/div, i_{in}: 1.0 A/div, time: 5 ms/div).

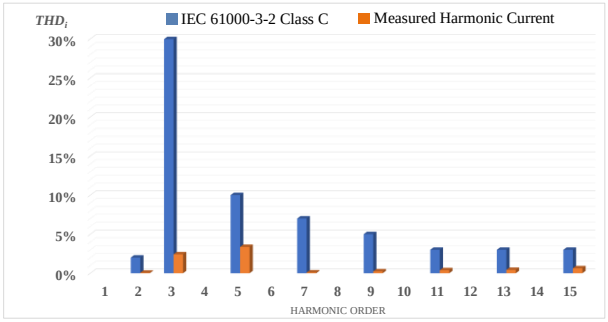


Figure 6. Harmonic spectrum of the input line current.

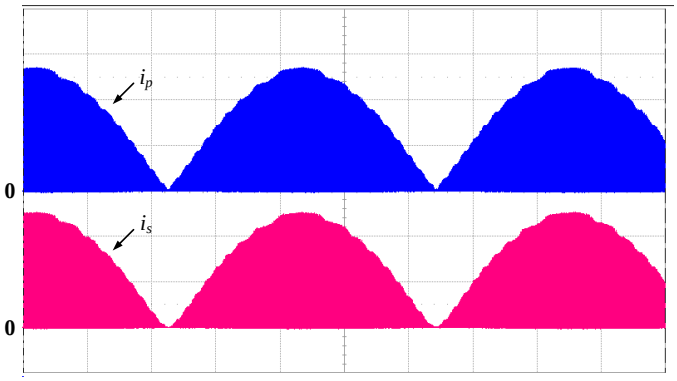


Figure 7. Primary and secondary currents of T_1. (i_p: 2 A/div, i_s: 2 A/div, time: 2 ms/div).

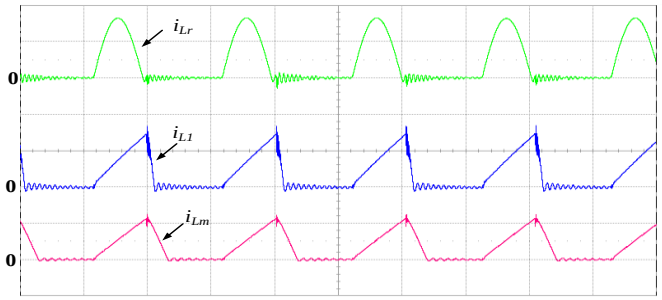


Figure 8. Current waveforms of i_{Lr}, i_{L1} and i_{Lm}. (i_{Lr}: 1 A/div, i_{Lm}: 2 A/div, i_{L1}: 1 A/div, time: 10 µs/div).

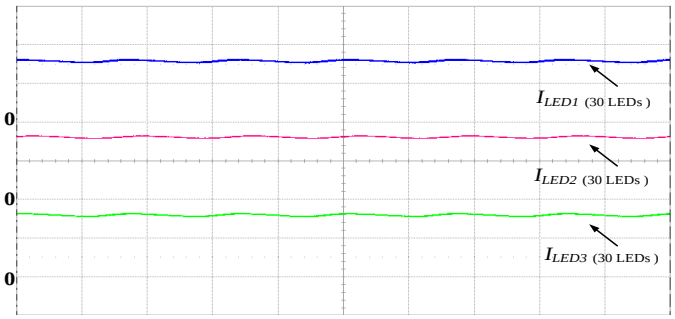


Figure 9. Waveforms of I_{LED1}, I_{LED2} and I_{LED3} with equal number of LEDs. (I_{LED1}: 200 mA/div, I_{LED2}: 200 mA/div, I_{LED3}: 200 mA/div, time: 5 ms/div).

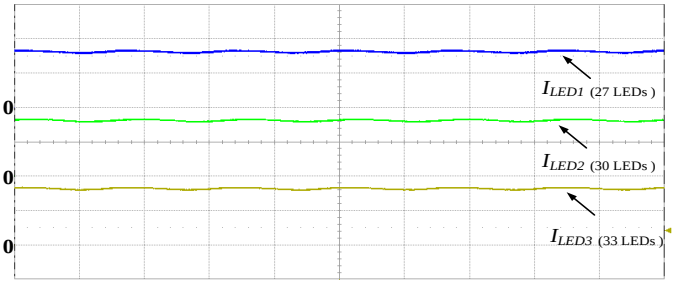


Figure 10. Waveforms of I_{LED1}, I_{LED2} and I_{LED3} with different numbers of LEDs. (I_{LED1}: 200 mA/div, I_{LED2}: 200 mA/div, I_{LED3}: 200 mA/div, time: 5 ms/div).

When the input voltage changes within a range of +/−20%, the duty cycle needs to be adjusted to maintain rated power operation. Figure 11 shows the measured efficiency at different input voltages. The circuit efficiency only slightly changes under different voltages. The LED power can be regulated by the control scheme of PWM. Figure 12 shows the currents of each string at 75%, 50% and 25% rated power. Similarly, when operating at different powers, the current of each string of LEDs is still the same. Figure 13 shows the measured efficiency at different output power. As shown, the circuit efficiency drops to 73.5% at 25% rated power. Figure 14 shows the prototype LED driver.

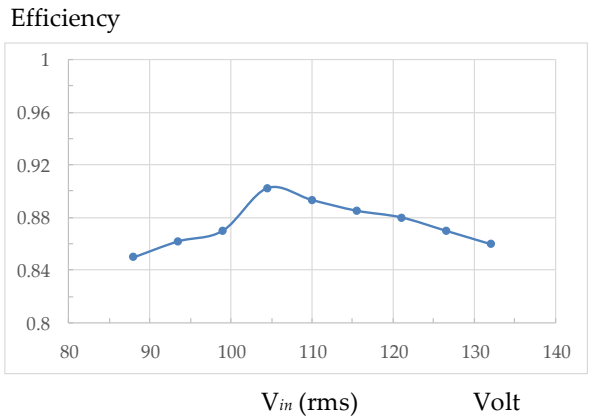
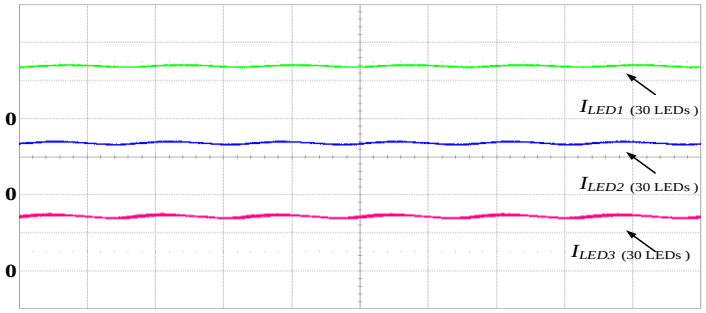
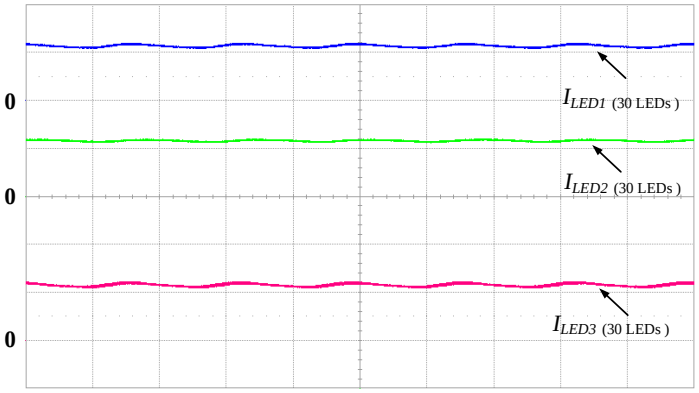


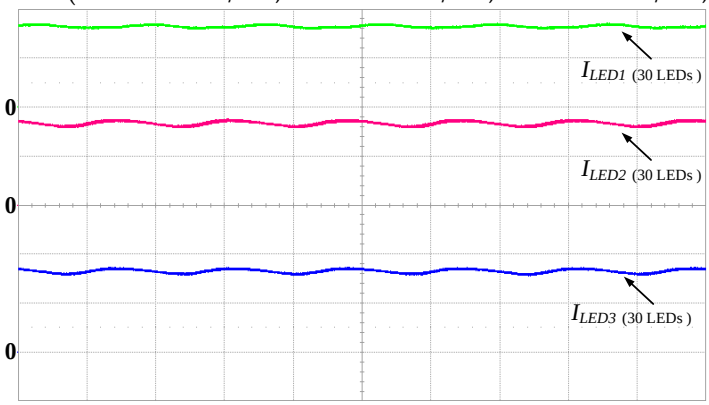
Figure 11. Measured circuit efficiency at different input voltages.



(**a**) 75% rated power (I_{LED1}: 200 mA/div, I_{LED2}: 200 mA/div, I_{LED3}: 200 mA/div, time: 5 ms/div)



(**b**) 50% rated power (I_{LED1}: 200 mA/div, I_{LED2}: 200 mA/div, I_{LED3}: 200 mA/div, time: 5 ms/div)



(**c**) 25% rated power (I_{LED1}: 100 mA/div, I_{LED2}: 100 mA/div, I_{LED3}: 100 mA/div, time: 5 ms/div)

Figure 12. LED currents at different power levels: (**a**) 75% rated power, (**b**) 50% rated power and (**c**) 25% rated power.

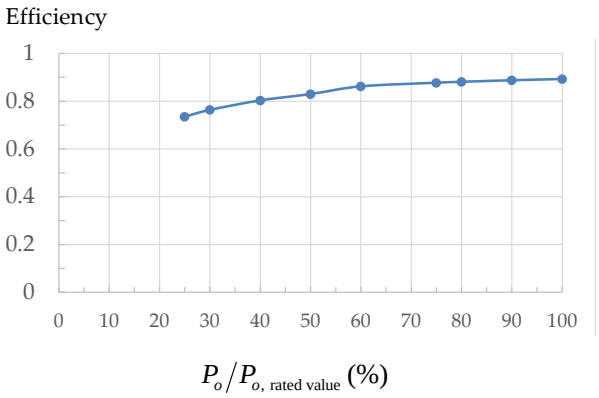


Figure 13. Measured circuit efficiency at different output power levels.

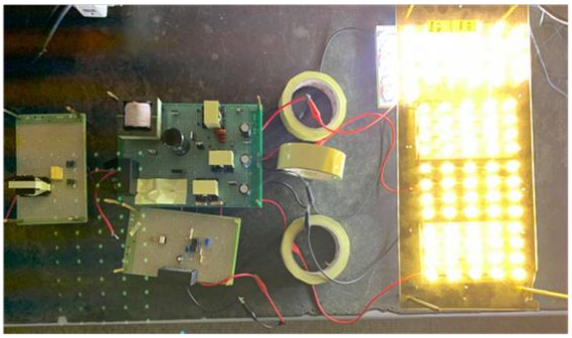


Figure 14. 90-W LED prototype circuit.

6. Conclusions

A single-stage LED drive circuit with power factor correction and current balancing capability is proposed. The circuit configuration mainly integrated a flyback converter, a buck–boost converter and a current balancing circuit. The flyback converter was used as a PFC converter, and the winding current was designed to operate at DCM to effectively reduce the THDi and improve the power factor; while the current balancing circuit applied the principle of capacitor ampere-second balance to achieve the same current for each LED string. Only one active switch was used and controlled by the method of PWM. A 90-W prototype circuit was built and tested. At rated power operation, the measured power factor was 0.99, the THDi was 2.91%, and the conversion efficiency was 89.3%. In addition, even where the number of LEDs in each string was different, the current balancing capability could still be achieved. Finally, the LED power was regulated from 100% to 25% rated power. The satisfactory experimental results have proved the feasibility of the proposed LED driver.

Author Contributions: Y.-H.Y. and H.-L.C. conceived and designed the circuit; C.-A.C. and Y.-N.C. performed circuit simulations and designed parameters of the circuit components; Z.-X.W. carried out the prototype converter, and measured as well as analyzed experimental results; H.-L.C. wrote the paper and Y.-H.Y. revised it for submission. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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