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Formulation and Analysis of Single Switch High Gain Hybrid DC to DC Converter for High Power Applications

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Abstract: The necessity for DC−DC converters has been rapidly increasing due to the emergence of RES-based electrification. However, the converter designed so far exhibits the drawbacks of lower efficiency and non-compactness in size. Hence, to rectify this problem, the new topology of a flyback converter for PV application is proposed in this work. The proposed converter exhibits reduced ripple in input current and enhances the conversion efficiency. Finally, the efficiency of this proposed converter is verified using MATLAB. The results indicate that this projected topology can be suitable for high voltage DC applications.

Keywords: Luo converter; flyback converter; PV

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1. Introduction

Isolated DC−DC converters have been extensively utilized in many higher power applications, because of their higher efficiency, easy voltage gain and lower ripple content. As a result, numerous topologies of DC−DC converters have emerged in recent years. However, PV-based applications require high gain converters so as to increase their efficiency for high power applications.

The traditional DC−DC converters, namely BOOST and buck boost topology, exhibit high ripple content as their output [1–4]. Similarly, they also suffer from voltage polarity problems. Thus, to overcome this deficiency in the conventional converters, modifications in converter have been introduced. However, the gain of this converter is very small. Similarly, to overcome the leakage reactance issue, magnetically coupled converters have been developed. The main drawbacks of these converters are high ripple content and higher switching losses [5]. Hence, a new buck-boost topology was formulated by [6]. This circuit results in high power loss. Then, cascaded type converters [7] were introduced. However, in this circuit, as the capacitor is in operation under a discontinuous mode of operation, the efficiency is reduced.

This can be effectively solved by using the SEPIC converter [8]. It results in a lower duty cycle with increased gain. This in turn, decreases the voltage stress across the switches. Hence, ripples in the current are reduced. The SEPIC converter under bridgeless topology was developed by [9]. However, it is applicable only for high power AC applications. Thus, a modified SEPIC converter was formulated [10], which is suitable for medium power applications. For high power applications the Re-Lift converters have recently been developed [11,12]. They result in reduced voltage stress, but the main drawback is the high inductance.

LLC converters were introduced [13], for high power applications, but the utilization of transformers led to higher loss. Later, Ćuk converters came into existence [14–16]. Among these, the Luo converters are becoming more popular due to their high output gain

and less voltage ripple at the output [17–20].While designing the converters, the switches play a major role. This has led to the development of multichip power modules (PMs) using SiC MOSFETs [21]. These types of devices require a cautious design to handle (i) the power dissipated by devices, and (ii) their high switching frequency [22]. Similarly, the designers should concentrate on electrothermal (ET) effects and the impact of parasitics [23]. So, many researchers have concentrated on the design of PMs using SiC MOSFETs. This approach is utilized while designing a DC converter for renewable energy applications. Keeping this in view, this work proposed a hybrid combination of the Luo with flyback converter which exhibits a higher voltage gain and less ripple content with SiC MOSFETs as switches.

2. Design of Proposed System

In this configuration, the formulated converter (specifications given in Appendix A) acts as a voltage regulator between PV source and load. Figure 1 presents the block diagram of a formulated work.

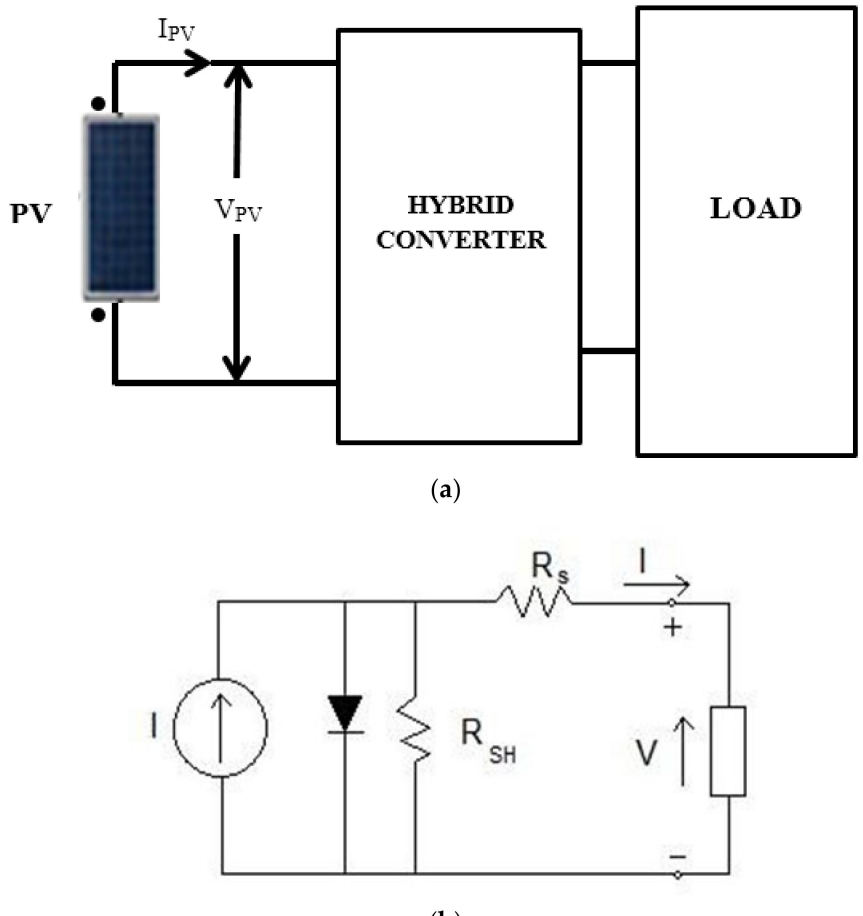


Figure 1. (**a**) Schematic diagram of a proposed module. (**b**) Diode model of a PV cell.

Design procedure of the proposed system is as follows.

2.1. Design of PV Array

A PV array of capacity 5 kW is chosen for the proposed design. The design of chosen PV array is depicted as follows.

A mathematical description of a photovoltaic cell and its equivalent circuit is depicted in Figure 1b.

The equivalent circuit of this model comprises a current source, series and parallel resistor and a diode. Thus the output current obtained from the photovoltaic array is given as

$$I = I_{sc} - I_d \quad (1)$$

where
I_{sc}—Short circuit current
I_d—Current across the diode
Thus, the proposed PV array can be designed [24–28] as follows
For a 5 kW, 250 V, current at MPP (Impp) can be valued as
Impp = Pmpp/Vmpp.
From this, the number of modules connected in parallel/series is calculated as follows
No. of series modules,
Ns = Vmpp/Vm
No. of parallel modules,
Np = Impp/Im

2.2. Proposed Converter

This proposed converter is a combination of a switched inductor, Luo and flyback converter. The proposed converter is shown in Figure 2a and its waveforms are shown in Figure 2b.

The advantage of the proposed converter is as follows: it provides continuous operation with the help of a coupled inductor.

Thus, an operation of a circuit is considered as six modes and is described below

Mode 1 ($t_0 - t_1$)

All the charges in the capacitors are nullified at this condition ($t = t_0$).

Mode 2 ($t_1 - t_2$)

Switch S_1 is turned on at zero voltage during $t = t_1$.Thus, the current across i_{lm} is given as

$$\frac{di_{lm}}{dt} = \frac{V_1 + \frac{V_c}{n}}{L_m} \quad (2)$$

where n-turns is the ratio of the coupled inductor.

In this circuit, during S_1 ON the current induced on the secondary side of the coupled inductor starts charging the switching capacitor (C_1 and C_2).

Therefore, the current on the secondary side of the coupled inductor, i_{l2}, charges C_3 and C_4.

$$\frac{di_{lm}}{dt} = \frac{V_1 + \frac{2V_c}{n}}{L_m} \quad (3)$$

At that time, i_{l2} is negative and hence its magnitude starts decaying.

Mode 3 ($t_2 - t_3$)

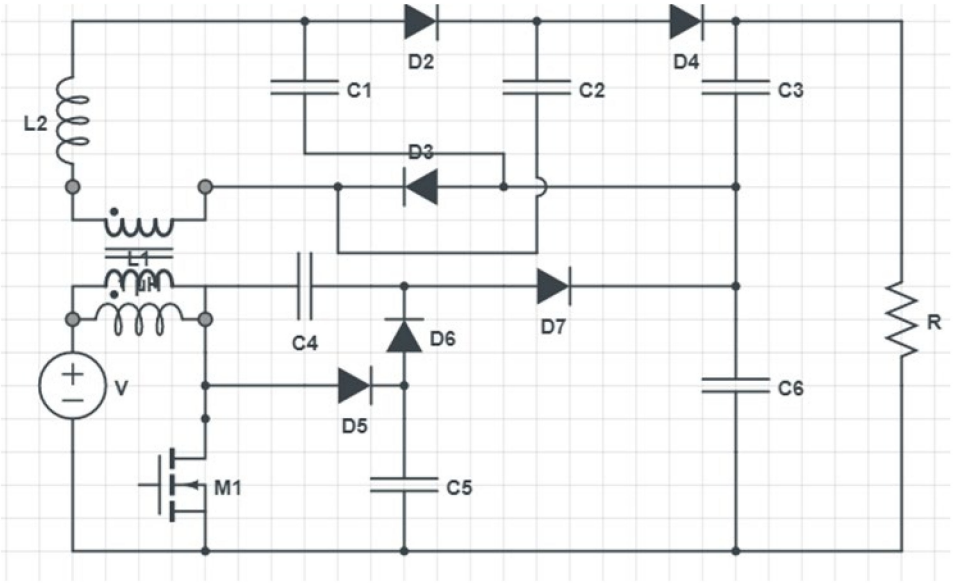
At this time, i_{l2} reaches zero. Hence, the change of the direction in i_{l2}, makes the C_1 and C_2 discharge their charges to C_3. Thus, current across the inductor i_m during this interval is depicted as

$$\frac{di_{lm}}{dt} = \frac{V_1 + \frac{(2V_c - V_{c3})}{n}}{L_m} \quad (4)$$

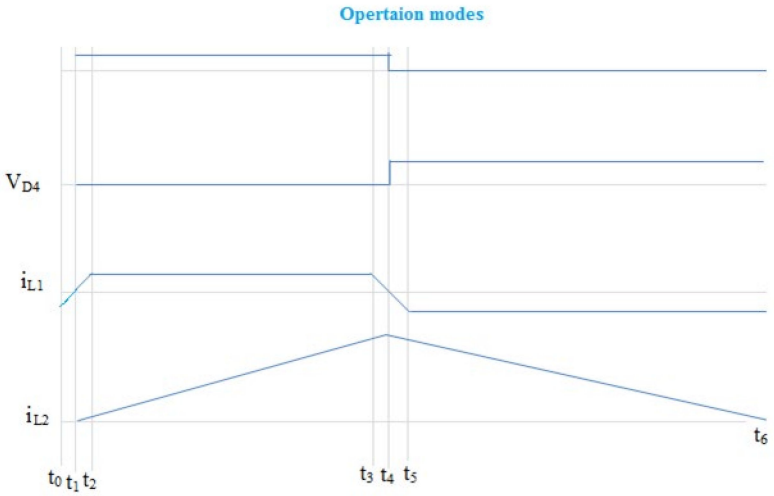
Mode 4 ($t_3 - t_4$)

During $t = t_3$, S_1 is turned off. The current across i_m charges Vc4.

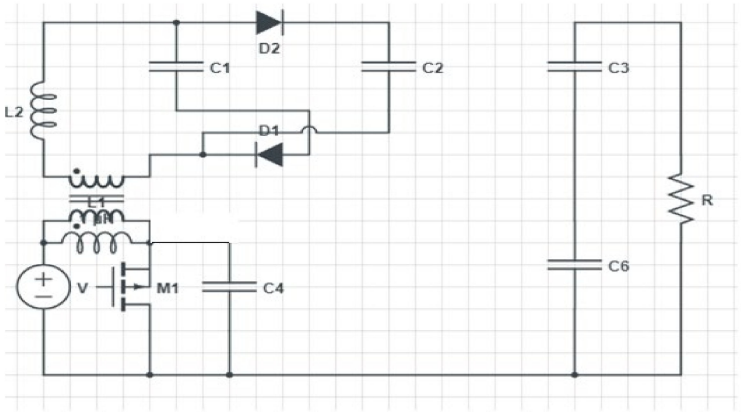
However, V_{c4} is smaller than V_o, the voltage stress over S_1 is comparatively low. Hence, the additional clamp circuit is not required.



(a)

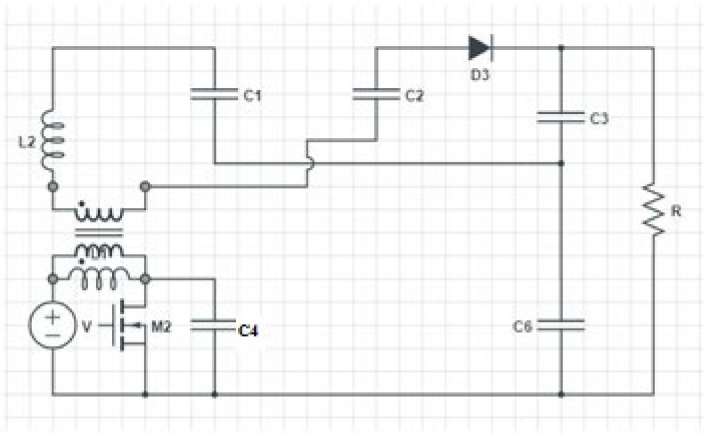


(b)

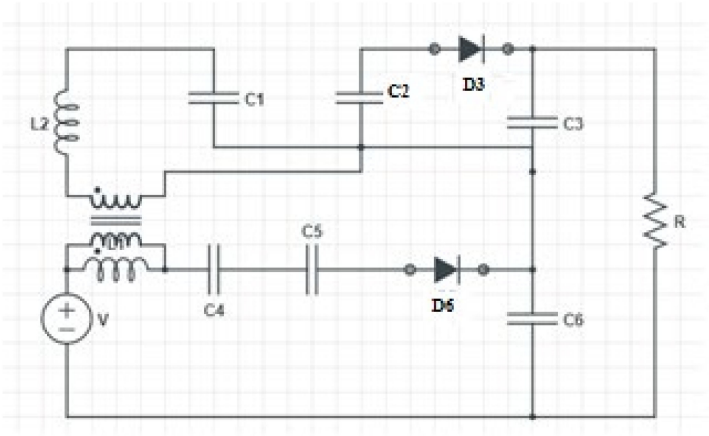


(c)

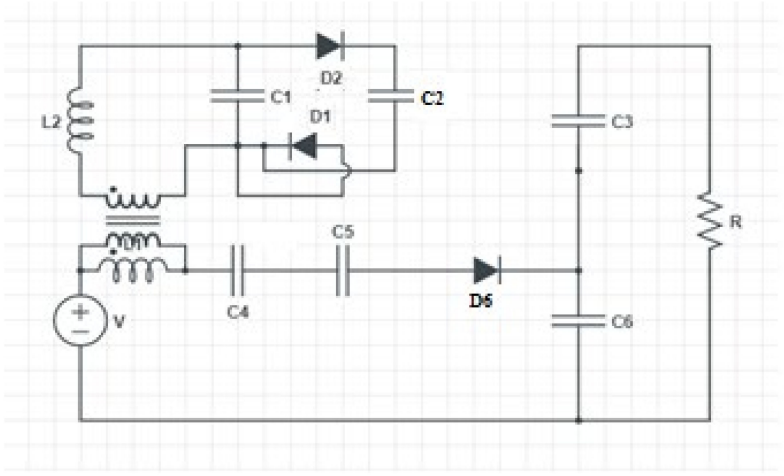
Figure 2. *Cont*.



(d)



(e)



(f)

Figure 2. (**a**) Schematic diagram of proposed converter (**b**) Steady state waveforms (**c**) Mode 2 operation. (**d**) Mode 3 operation. (**e**) Mode 4 operation. (**f**) Mode 5 operation.

Mode 5 ($t_4 - t_5$)

In this stage, again i_{l2} gets reversed and current across the inductor i_m is about

$$\frac{di_{lm}}{dt} = \frac{V_1 - V_{C4} + \frac{V_b}{n}}{L_m} \quad (5)$$

Mode 6 ($t_5 - t_6$)

During t = t_5, the current across the inductor remains the same as the previous mode. Thus, the output voltage (V_o) of this converter can be calculated as

$$V_o = V_{C3} + V_{C6} \tag{6}$$

Some modes of operation (mode 1 and mode 5) are ignored.

Then by relating voltage second balance analysis over (L_m and L_2) in modes 3 and 6, the relationship between V_1, V_O, V_C, V_{C3} and V_{C4} can be derived as,

$$V_{C4} = \frac{2 - D}{1 - D} V_1 \tag{7}$$

$$V_c = \frac{D}{1 + D} V_{C3} \tag{8}$$

Then by rearranging Equations (5)–(8) the voltage gain of this proposed converter can be expressed as,

$$M = \frac{V_o}{V_1} = \frac{2 + n + nD - D}{1 - D} \tag{9}$$

From the above equation, it is concluded that based on the turns ratio (n) between mutual inductance (L_{m1} and L_{m2}), the voltage gain of the converter can be varied.

Analysis of Ripple Minimization

While considering ripple minimization, the capacitor and inductors utilized in design should be considered as larger as given in equation 3. But during the switching period, the voltage across the inductor is zero. Similarly, voltage ripple across C1 and C4 are also zero due to large value. Hence, the input voltage retains constant value over the switching period. The ripple current across the inductor is considered as zero as average inductor voltage is zero.

Analysis of switching loss

When the switch is turned on, negative current through the diode discharges and creates zero voltage condition. Thus, in turn reduces the turn-on loss then hard switching. So, it is concluded that switching loss is reduced.

2.3. Design of Controllers

FOPID Controller

In order to improve the system control performances, in many industrial applications fractional order PID controllers have recently been used. The FOPID controller is the extension of the conventional PID controller based on fractional calculus and is shown in Figure 3.

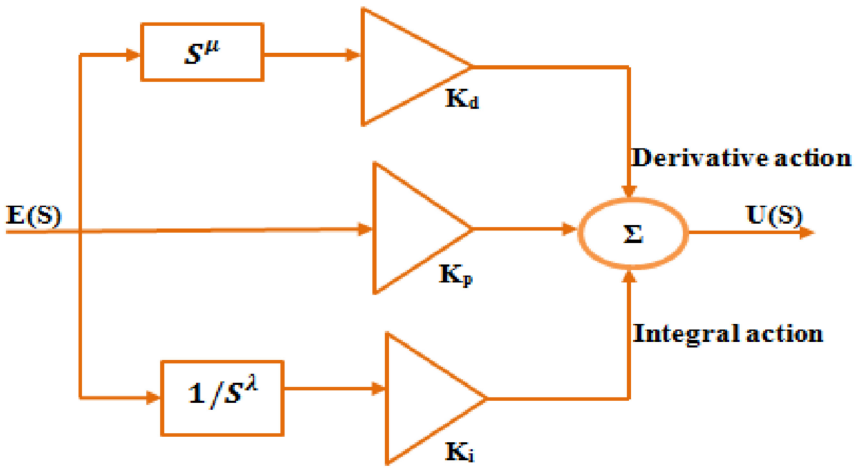


Figure 3. Block diagram of FOPID controller.

The transfer function of PI $^{\lambda}$ D $^{\mu}$ is given in the equation as,

$$C(S) = \frac{U(S)}{E(S)} = K_p + K_i S^{-\lambda} + K_d S^{\mu} \quad (10)$$

The positive real numbers are λ and μ, respectively.

The proportional, integral and derivative gain constants are K_p, K_i and K_d, respectively.

3. Simulation Results and Discussion

To demonstrate the effectiveness of the proposed converter, simulations were performed appropriately using MATLAB software.

Performance of the proposed system with PV under open loop control

The input parameters of a solar array are irradiation and temperature. In this work, the irradiation value is varied accordingly, as shown in Figure 4. Similarly, the temperature remains constant at 25 °C.

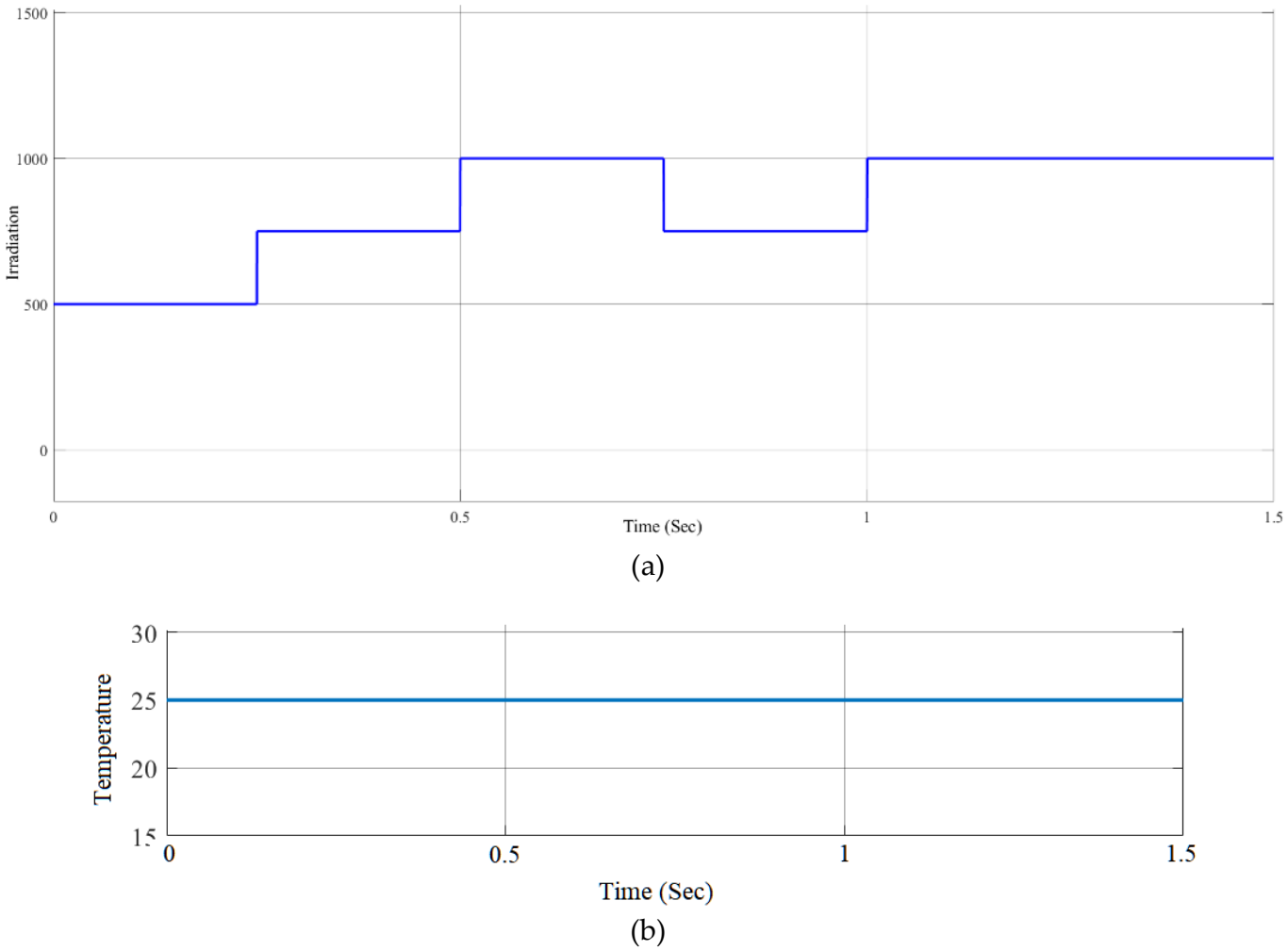


Figure 4. Performance of system (**a**) irradiationand (**b**) temperature.

Figure 5 shows the PV indices such as solar insolation level; PV output power and proposed converter voltage. From the above Figure, it is also concluded that the energy obtained from PV is maximized with the help of the proposed converter and a stable power with less oscillations is obtained.

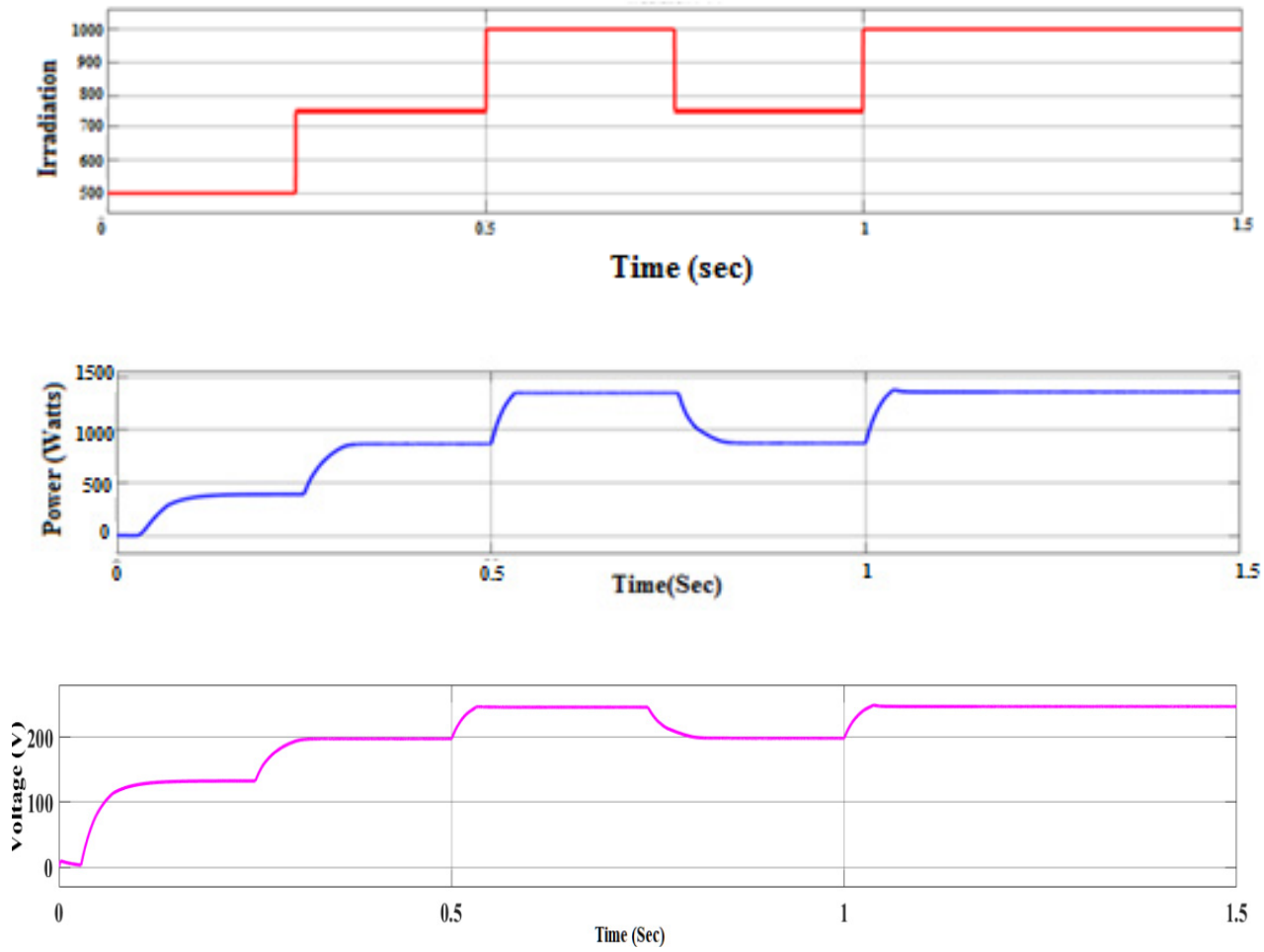


Figure 5. Output PV power and converter voltage with respect to irradiance.

Performance of Proposed Converter

Figure 6 depicts the output current and voltage of the proposed converter.

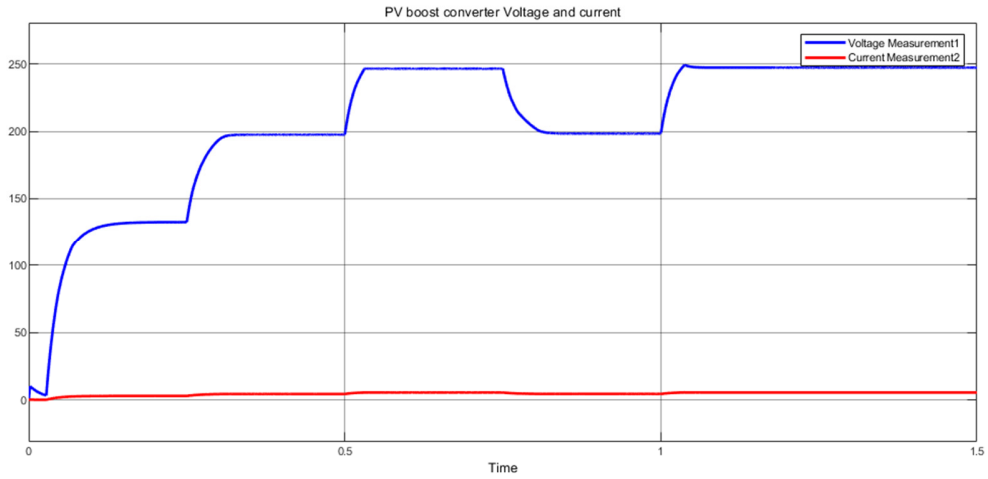


Figure 6. Output voltage/current of the converter.

From the above figure, it is observed that the high frequency switching eliminates the ripple contents in the output.

Closed loop analysis

From the above analysis, it is depicted that the open circuit voltage is highly influenced by the increase in the panel temperature. The drop in the open circuit voltage with the increase in temperature, PV output power will decrease. Hence the voltage supplied to the load gets distorted. Hence in order to maintain the constant voltage at the load side, Controllers are implemented.

Figure 7 displays the output voltage of the proposed converter.

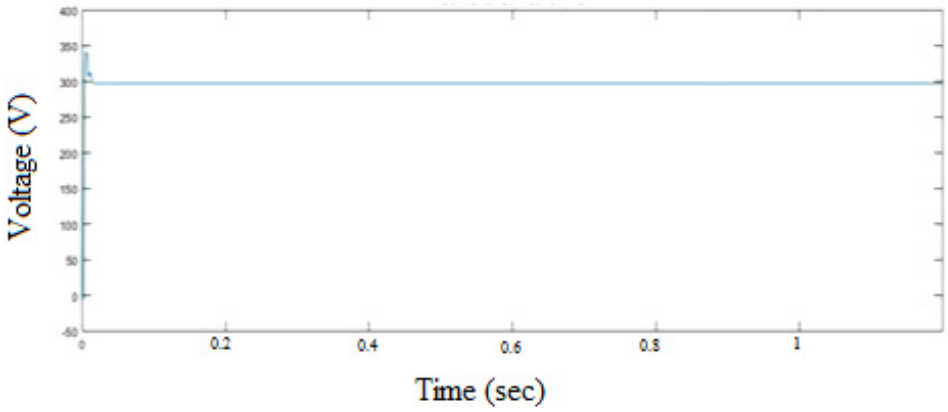


Figure 7. Converter output voltage waveform.

Hardware analysis

Thus, to examine the effectiveness of the proposed converter simulated in MATLAB, a 100 W prototype converter was modeled. Figures 8 and 9 depict the pictures of the prototype of the proposed converter examined in the laboratory.

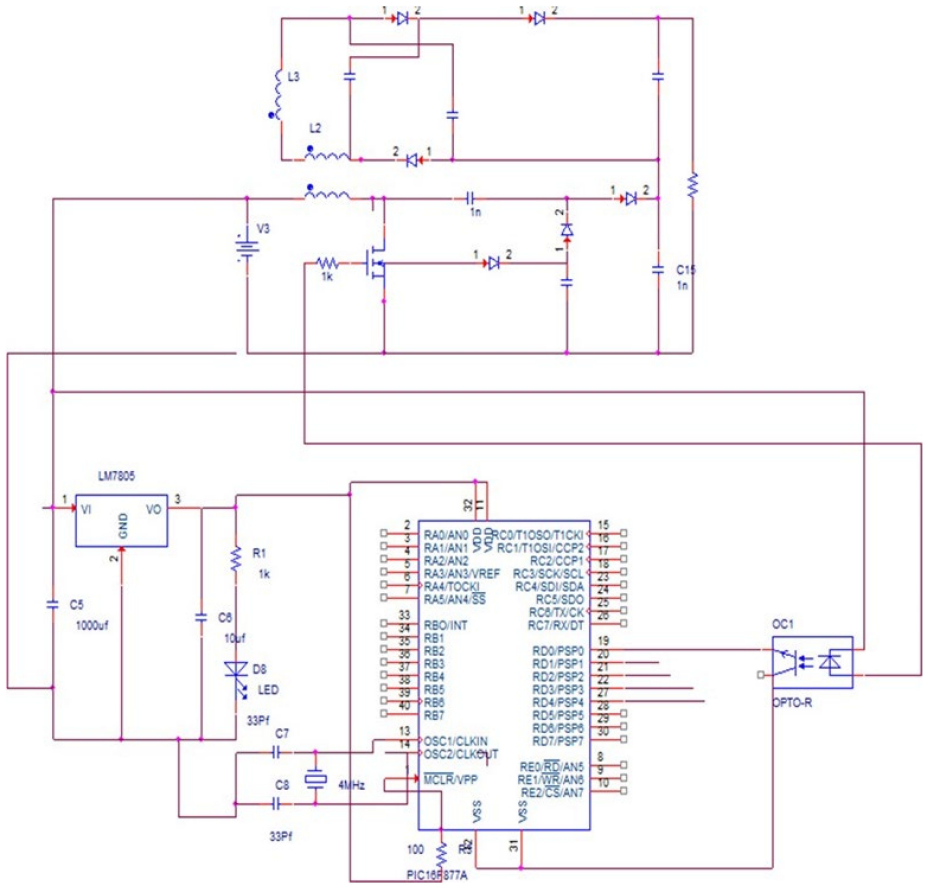


Figure 8. Hardware layout.

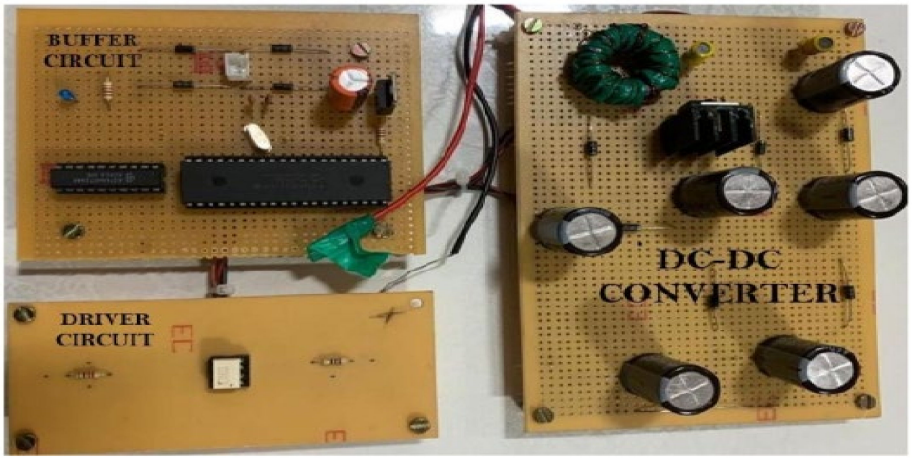
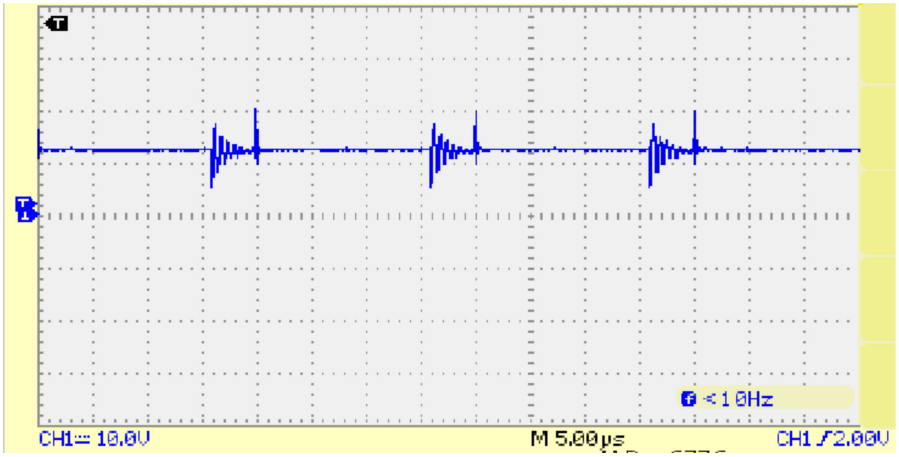
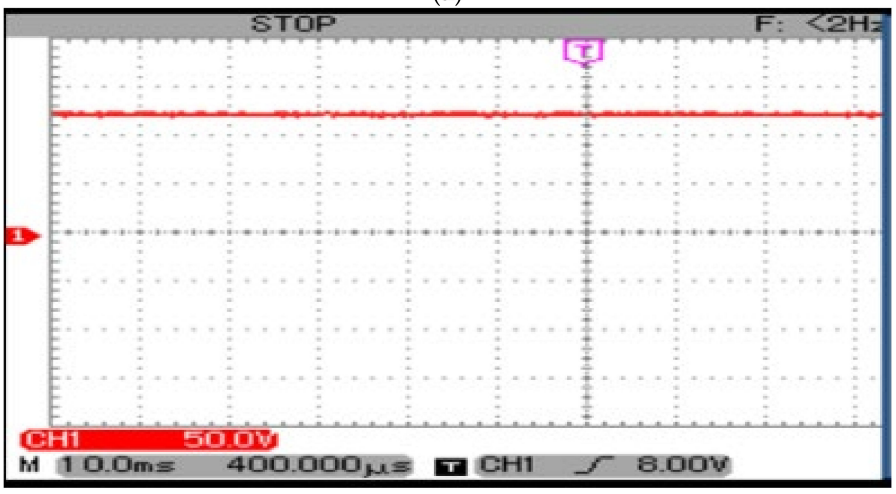


Figure 9. Experimental setup of proposed converter.

Figure 10a,b depicts the input/output voltage and current waveforms of the proposed converter.

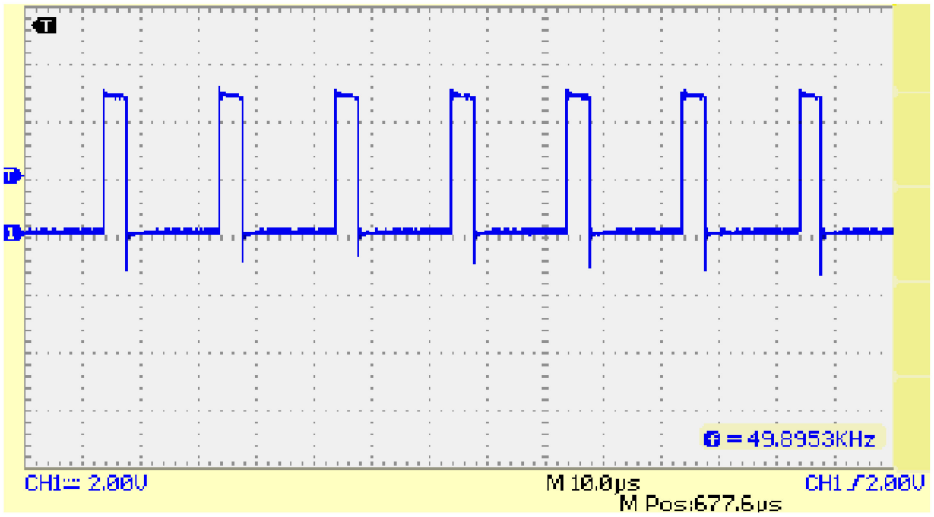


(**a**)



(**b**)

Figure 10. *Cont.*



(**c**)

Figure 10. (**a**) Input voltage waveform of the proposed converter, (**b**) output voltage waveform of the proposed converter, (**c**) switching pulse to the switch S_1.

Figure 10c depicts the switching pulses applied to the switch S1 of the proposed converter, which is about 0.50.

Figure 11 compares the voltage gain (M) of the Different DC−DC converter under various duty ratios (k).

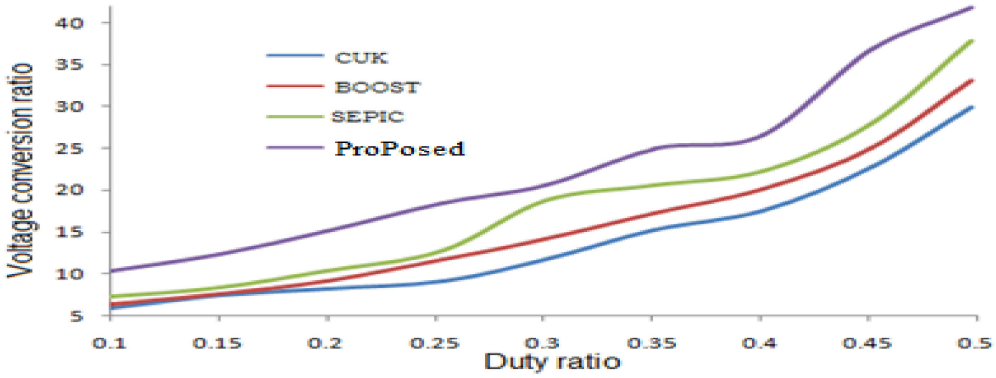


Figure 11. Voltage conversion ratio versus duty ratio.

From the above graph, Figure 11, shows that voltage transfer gain (M) of boost, Ćuk and SEPIC DC–DC converters is identical. However, the proposed converter has a higher voltage transfer gain. When choosing a DC−DC converter, efficiency plays a vital role for RES applications. Figure 12 shows the comparison of the efficiency of various converters with respect to input voltage.

From the above graph, it is inferred that the proposed converter has a higher efficiency at higher input voltage. Hence, it is clear that for medium-power applications the Ćuk, and SEPIC converters are more suitable whereas boost converters are suitable for applications which need only low power. Thus, it is visualized that for high power RES, the proposed converter is the suitable one.

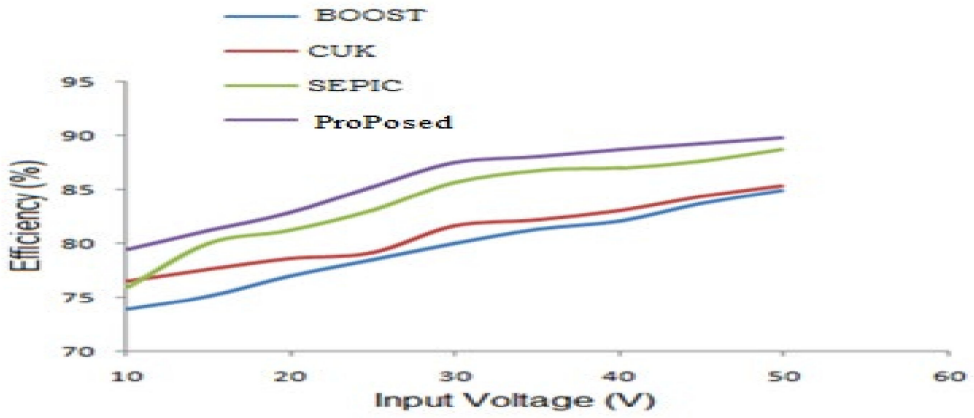


Figure 12. Efficiency versus input voltage.

From the Table 1, it is concluded that the utilization coupled inductor in this converter improves the voltage gain of the converter by more than 10 times that of a conventional boost converter. Hence, this converter can be utilized for PV applications. Thus, the voltage stress across the switch of the proposed converter is very low compared to that of the conventional boost converter. Hence, the proposed converter exhibits lower conduction loss.

Table 1. Performance comparison with traditional converter.

Topology	Boost Converter	Proposed Converter
Voltage gain	$\frac{1}{1-D}$	$\frac{2+n+nD}{1-D}$
No. of switches	1	1
No. of diodes	1	5
Voltage stress across the switch	V_o	V_{C4}
Diode voltage stress	V_o	V_{c3}, V_{c4}
Switching condition	Hard switching	ZVS
Coupled inductor utilization	-	Yes

Table 2 deals with the comparisons with the other converters which implement coupled-inductor topology. From the results, it was found that the proposed converter exhibited higher voltage gain than the others.

Table 2. Comparisons with other relevant converters.

Converters	Voltage Gain
Chen et al. (2015)	$\frac{n+2-D}{1-D}$
Luo converter	$\frac{2-D}{1-D}$
Proposed converter	$\frac{2+n+nD}{1-D}$

4. Conclusions

In this study, a hybrid DC−DC converter was designed for high power applications. This is the combination of a Luo converter with a flyback converter. In this work, a voltage multiplier circuit was implemented to boost the voltage level. Thus, the operation of the circuit was carried out with a single switch; the switching losses were comparatively low.Thus the performance of the formulated converter was examined using both simulation and experimental results. To increase the dynamic behavior of the converter, controllers were implemented. In this work, a FOPID controller was chosen to improve the dynamic

behavior of the proposed system. From the simulation results, the efficiency of the proposed FOPID controller is proven. From the simulated and experimental results, it is evident that this converter exhibits higher efficiency.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A. Proposed Converter

Parameters	Values
fsw	20 kHz
C	500 mF
C1, C2	36 mF
C3, C4	57 μF
Lm	617 mH
Lk2	17.1 μH

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