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Self-Biased and Supply-Voltage Scalable Inverter-Based Operational Transconductance Amplifier with Improved Composite Transistors

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Abstract: This paper deals with a single-stage single-ended inverter-based Operational Transconductance Amplifiers (OTA) with improved composite transistors for ultra-low-voltage supplies, while maintaining a small-area, high power-efficiency and low output signal distortion. The improved composite transistor is a combination of the conventional composite transistor and forward-body-biasing to further increase voltage gain. The impact of the proposed technique on performance is demonstrated through post-layout simulations referring to the TSMC 180 nm technology process. The proposed OTA achieves 54 dB differential voltage gain, 210 Hz gain–bandwidth product for a 10 pF capacitive load, with a power consumption of 273 pW with a 0.3 V power supply, and occupies an area of 1026 µm². For a 0.6 V voltage supply, the proposed OTA improves its voltage gain to 73 dB, and achieves a 15 kHz gain–bandwidth product with a power consumption of 41 nW.

Keywords: Operational Transconductance Amplifier (OTA); inverter-based OTA; push-pull based OTA; improved forward-body-bias; composite transistors; supply-voltage scalable; Ultra-Low-Voltage (ULV); Ultra-Low-Power (ULP)

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1. Introduction

The development of electronic devices that are increasingly less dependent on battery charging requires Integrated Circuits (ICs) able to operate with Ultra-Low-Voltage (ULV) supply with an Ultra-Low-Power (ULP) consumption. A recent approach to address this request relies on digital-based and supply-voltage scalable ICs [1–9]. In this framework, the design of ULV Operational Transconductance Amplifiers (OTA) with appreciable performance (i.e., rail-to-rail input/output voltage swing and high transconductance–gain independent of process, supply voltage, and temperature variations [10]) becomes more and more challenging.

Inverter-based OTA topologies [11,12] and their respective ULV variations [13,14] have been proposed, as well as push–pull-based, bulk-driven OTAs [15–18]. An improved single-ended OTA has been proposed in [19], exploiting the properties of improved composite transistors [20] into a variation of the bulk Nauta inverter-based OTA [21]. This approach improves the voltage gain for a single-stage amplifier but shows a limited input voltage swing.

This work further exploits the improved composite transistors of inverters [19] into a single-ended version of the fully differential OTA in [14]. This results in an enhanced voltage gain, a higher linearity and a lower power consumption at the minimum supply voltages.

In Section 2, the improved composite transistor technique is briefly reviewed. Then, in Section 3, the employed self-biased inverter with the forward body bias is described.

Based on this, in Section 4, the proposed inverter-based OTA is described. In Section 5, the characteristics of the proposed OTA are then verified and compared through post-layout simulations with similar circuits designed in the 180 nm technology process. Finally, in Section 6, conclusions are drawn.

2. Composite Transistor Forward-Body-Biasing Analysis

Figure 1 represents an N-type improved composite transistor. It consists of a series connection of two independently forward-body-biased N-type Metal-Oxide Semiconductor (MOS) transistors M_{N1} and M_{N2}, as first proposed in [20] and described in detail in [19], by using the Unified Current Control Model (UICM) all-region transistor model [22].

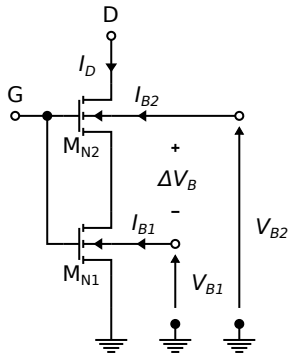


Figure 1. Improved composite transistor.

Considering that $I_D = I_{DN1} = I_{DN2}$, M_{N1} operates in the linear region, M_{N2} operates in the saturation region, and both transistors operate in weak inversion, the improved composite transistor drain current I_D can be calculated as follows:

$$I_D \approx 2 \cdot I_{SH} \cdot S_{eq} \cdot e^{\frac{V_G + (n-1)V_{B1} - V_T}{n\phi_t} + 1} \tag{1}$$

where

$$I_{SH} = \mu C'_{ox} n \frac{\phi_t^2}{2} \tag{2}$$

is the sheet normalization current, V_G and V_{B1} are, respectively, the transistor M_{N1} gate and bulk terminal voltages referenced to the ground, V_T is the threshold voltage, n is the slope factor, ϕ_t is the thermal voltage, μ is the charge mobility, and C'_{ox} is the gate oxide capacitance per area.

The improved composite transistor equivalent aspect ratio S_{eq} is defined as:

$$S_{eq} = \frac{S_{N1} \cdot \beta S_{N2}}{S_{N1} + \beta S_{N2}} = \frac{\beta k}{\beta k + 1} \cdot S_{N,1} \tag{3}$$

where

$$\beta \approx e^{\frac{(n-1)\Delta V_B}{n\phi_t}} \tag{4}$$

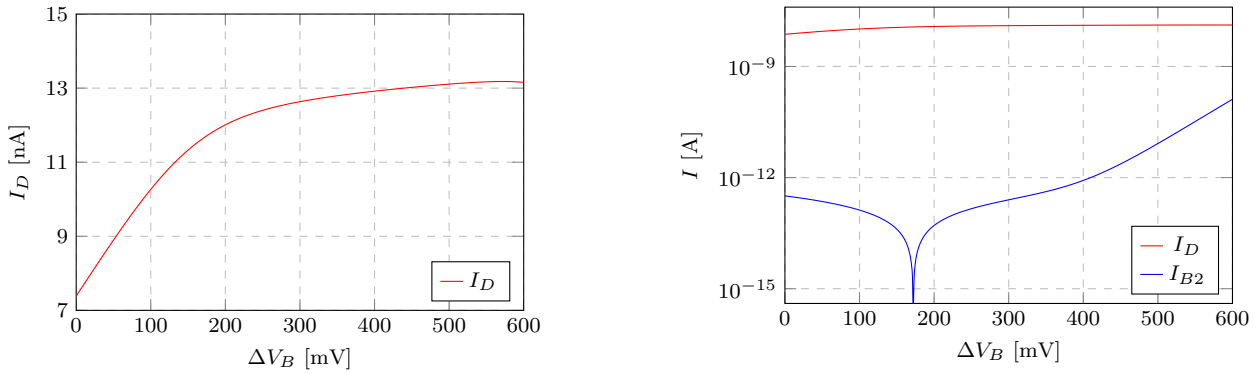
represents a correction factor for the current drain I_D definition due to the difference between the body-bias of the series transistors M_{N2} and M_{N1} $\Delta V_B = V_{B2} - V_{B1}$, assuming the transistors are operating in weak inversion, and

$$k = \frac{S_{N2}}{S_{N1}} \tag{5}$$

is the ratio between transistors M_{N1} and M_{N2} physical aspect ratios S_{N1} and S_{N2}.

Figure 2a shows how the drain current increases with V_{B2} for equally sized transistors with 1.26 um width and 0.42 length, in the TSMC 180 nm Complementary Metal-Oxide Semiconductor (CMOS) technology process, operating at 27 °C, for $V_G = V_D = 300$ mV,

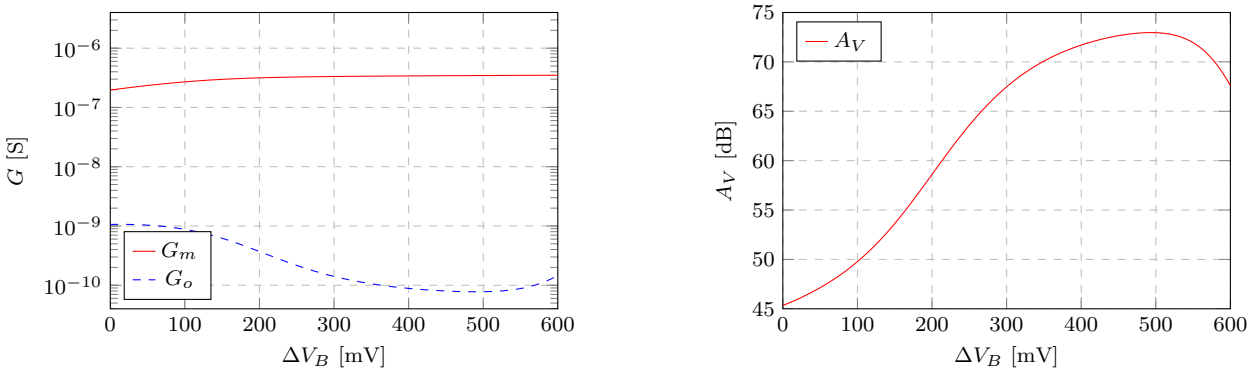
$V_{B1} = 0.0$ V, $V_{B2} = V_{B1} + \Delta V_B$, and ΔV_B ranging from 0 to 600 mV. Figure 2b shows how the parasitic substrate current I_{B2} increases with V_{B2}. When V_{B2} is approximately 170 mV, I_{B2} is almost zero, as V_{B2} is almost equal to the transistor M_{N2} source terminal voltage. For voltages higher than 170 mV, M_{N2} is forward-body-biased and increases exponentially for voltages higher than 400 mV.



(**a**) (**b**)

Figure 2. Improved composite transistor simulation results for $V_G = V_D = 300$ mV, $V_{B1} = 0.0$ V and $0 \leq V_{B2} \leq 600$ mV: (**a**) drain current I_D on y-axis nA range versus $\Delta V_B = V_{B2} - V_{B1}$; and (**b**) drain current I_D and the parasitic substrate current I_{B2} versus $\Delta V_B = V_{B2} - V_{B1}$.

Referring to the same specification, Figure 3a shows the improved composite transistor transconductance $G_m = (dI_D/dV_G)$ and output conductance $G_o = (dI_D/dV_D)$, and Figure 3b shows its intrinsic voltage gain A_V, which is the ratio between G_m and G_o. Figure 3b shows how A_V increases exponentially with ΔV_B till $\Delta V_B \approx 300$ mV. Then, A_V increases with a reduced slope until it reaches its peak at $\Delta V_B = 500$ mV. In particular, A_V is increased by an order of magnitude (20 dB) for $\Delta V_B = 250$ mV and almost two orders of magnitude (38 dB) for $\Delta V_B = 500$ mV .



(**a**) (**b**)

Figure 3. Improved composite transistor simulation results for $V_G = V_D = 0.3$ V, $V_{B1} = 0.0$ V and $0 \leq V_{B2} \leq 0.6$ V: (**a**) transconductance G_m and output conductance G_o versus $\Delta V_B = V_{B2} - V_{B1}$; and (**b**) intrinsic voltage gain A_V versus $\Delta V_B = V_{B2} - V_{B1}$.

3. Proposed Inverter Made of Composite Transistors with Forward-Body-Bias

Figure 4a,b shows, respectively, N-type and P-type rectangular transistor arrays [23,24] M_{NxA} and M_{PxA}. The PMOS devices are 2:1 parallel arrays (two single P-MOS transistors of size W_P/L_P in parallel), whereas the NMOS devices are 1:2 series arrays (two single N-MOS transistors of size W_N/L_N in series). Both NMOS and PMOS single transistors that build each N-type and P-type transistor array have identical width and lengths and aspect ratios, but the PMOS equivalent transistors have an aspect ratio four times larger

than the NMOS equivalent transistors in order to balance the PMOS pull-up and NMOS pull-down networks. The same ratio between pull-up and pull-down networks could be achieved by using a single PMOS transistor with channel widths four times larger than the single NMOS transistors channel width while keeping the transistor length identical, but this would increase the inverter total active area by 25%.

The improved composite transistor can be represented as single transistors with an equivalent aspect ratio S_{eq} as in (3).

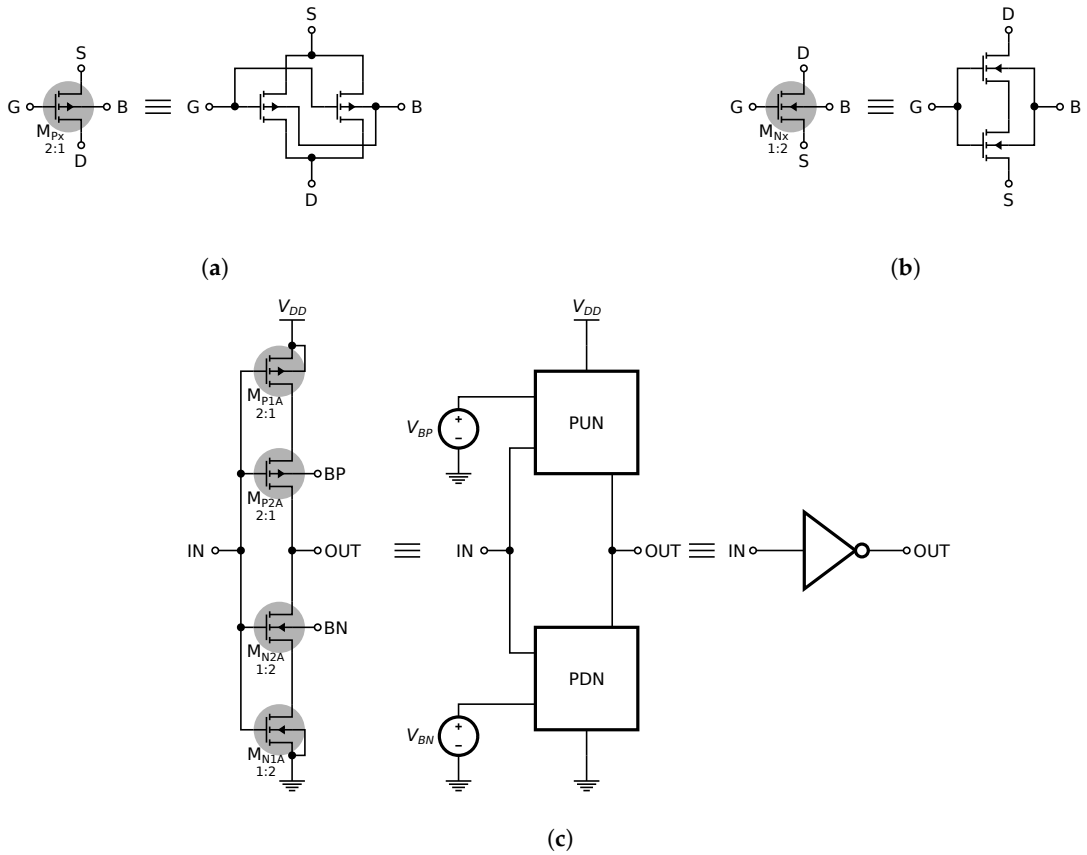


Figure 4. Transistors arrays: (**a**) P-type 2:1 parallel transistor array and; (**b**) N-type 1:2 series transistor array; (**c**) transistor-level schematic of the proposed inverter made of composite transistors with forward-body-bias and equivalent representations as an inverter.

Two N-type and 2 P-type transistor arrays, respectively, M_{P1A}, M_{N2A} and M_{P1A}, M_{P2A}, are placed in series as in Figure 4c to build an inverter.

The inverter small-signal voltage gain A_V is equal to the ratio between an equivalent inverter transconductance G_m and output conductance G_o.

$$A_V = G_m R_o = \frac{G_m}{G_o} \tag{6}$$

These G_m and G_o are, respectively, functions of the PMOS and NMOS equivalent transistors gate-drain small-signal transconductance g_{mg} and drain conductance g_{md}, as derived from Equations (7) and (8), accordingly to the UICM model approximation to the transistor weak inversion operation [22]. These small-signal parameters are a function of the quiescent current I_Q [21] (also known as short-circuit current), slope factor n, the thermal voltage ϕ_t and the early voltage V_A.

$$G_m = g_{mg_P} + g_{mg_N} = \frac{I_Q}{\phi_t}\left(\frac{1}{n_P} + \frac{1}{n_N}\right) \approx \frac{2I_Q}{n\phi_t} \tag{7}$$

$$G_o = g_{md_P} + g_{md_N} \approx I_Q \left(\frac{1}{V_{A_P}} + \frac{1}{V_{A_N}} \right) \tag{8}$$

Therefore, the inverter small-signal voltage gain A_V can be rewritten as:

$$A_V = G_m R_o = \frac{G_m}{G_o} \approx \frac{2}{n\phi_t \left(\frac{1}{V_{A_P}} + \frac{1}{V_{A_N}} \right)} \tag{9}$$

This schematic in Figure 4c can be equivalently translated into a pull-up and pull-down network (respectively, PUN and PDN) of an inverter biased by two additional voltages V_{BP} and V_{BN}. This represents an equivalent inverter made of composite transistors with a forward-body-bias. Such an inverter is the building block of the proposed inverter-based OTA described in this paper.

4. Proposed Operational Transconductance Amplifier

Differential inverter-based OTAs can use positive feedback and active load [11,13], or forward common-mode cancellation [12,14], to attenuate common-mode signals , as shown in Figure 5.

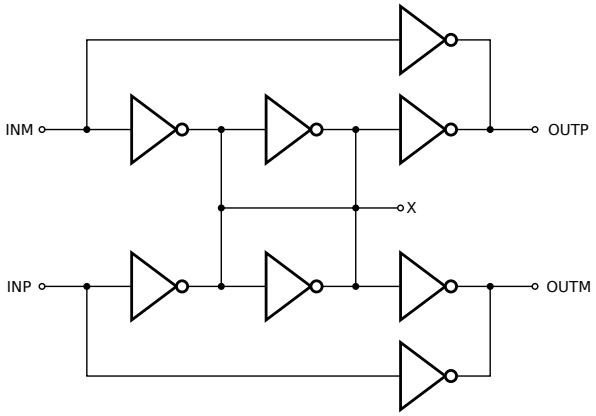
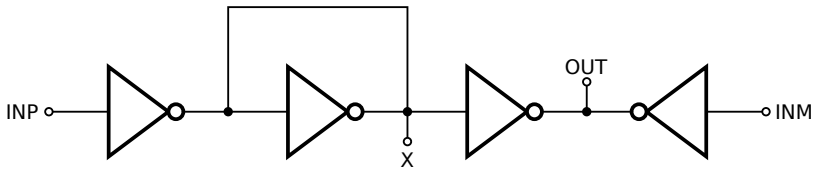
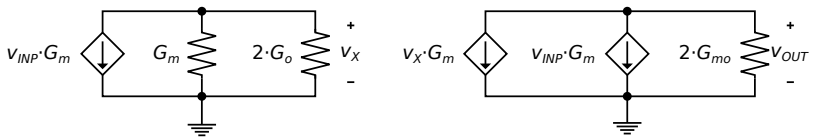


Figure 5. Fully-differential inverter-based Operational Transconductance Amplifier (OTA) with forward common-mode cancellation [12].

Figure 6a shows the single-ended version based on the fully-differential OTA shown in Figure 5.



(**a**)



(**b**)

Figure 6. Single-ended inverter-based OTA: (**a**) simplified schematic, and (**b**) respective small-signal representation.

The small-signal circuit of this OTA is shown in Figure 6b, where the corresponding transconductance and output conductance are represented as G_m and G_o, and its unloaded low frequency voltage gain A_V can be modeled as G_m/G_o, as described in Equation (8).

The small-signal differential output voltage v_{OUT} at very low frequencies can be expressed as

$$v_{OUT} = -(v_X + v_{INM}) \cdot \frac{G_m}{2G_o} = \left(\frac{G_m}{G_m + 2G_o} \cdot v_{INP} - v_{INM} \right) \cdot \frac{G_m}{2G_o} \tag{10}$$

Considering that $v_{INP} = -v_{INM}$, the small-signal differential voltage gain A_{VDIFF} can be derived as

$$A_{VDIFF} \approx \frac{G_m}{2G_o} = \frac{A_V}{2} \tag{11}$$

and, considering that $v_{INP} = v_{INM}$, the common-mode voltage gain A_{VCM} can be derived as

$$A_{VCM} = \left(\frac{G_m}{G_m + 2G_o} - 1 \right) \frac{G_m}{2G_o} = \frac{A_V}{A_V + 2} \approx 1 \tag{12}$$

Figure 7 shows the proposed inverter-based OTA, which is equivalent to the OTA shown in Figure 6a, but the former has two inverters in parallel for each one represented in the latter. All inverters are identical and made of improved composite transistors. By doubling each inverter, the common-centroid technique can be used to design this OTA layout. Furthermore, by using N inverters in parallel, the OTA transconductance is multiplied by N, and both mismatch and noise are reduced by $\sqrt{N}$. Obviously, power consumption and area also multiplied by N. Since the OTA output conductance is also multiplied, the OTA voltage gain remains the same.

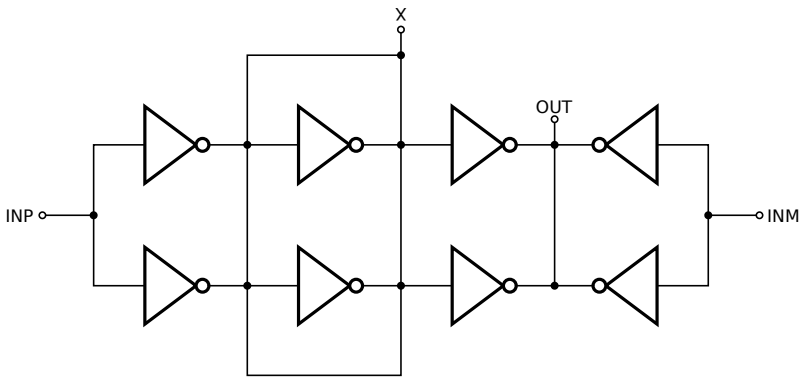


Figure 7. Proposed single-ended, inverter-based OTA with improved composite transistor circuit schematic.

Figure 8 shows the transistor-level proposed OTA schematic. As shown in Figure 3b, the intrinsic voltage gain A_V can be increased by means of the two bulk terminals of the composite transistor. The higher their voltage difference ΔV_B, the higher the intrinsic voltage gain A_V. Therefore, in order to maximize A_V with no additional supply voltages, the transistors pull-down networks are connected to the ground or to the supply voltage V_{DD}. In particular, bulk terminals of the transistors $M_{N1A\text{-}D}$ are connected to the ground, whereas those of the transistors $M_{N2A\text{-}D}$ are tied to the node BN, which is connected indirectly to the supply voltage V_{DD}. In fact, BN is connected to the drain of transistor M_{P2E} and both transistors M_{P1E} and M_{P2E} are pseudo-resistors with very large resistances. Thus, if the substrate parasitic current increases, the pseudo-resistor voltage drop increases and limits it to relatively insignificant levels [21,25]. Notice that for FD-SOI process technologies [26], those transistors would not be necessary because there is no parasitic substrate

current. Symmetrically, the same body-bias is applied to the pull-up network referring to the BP node.

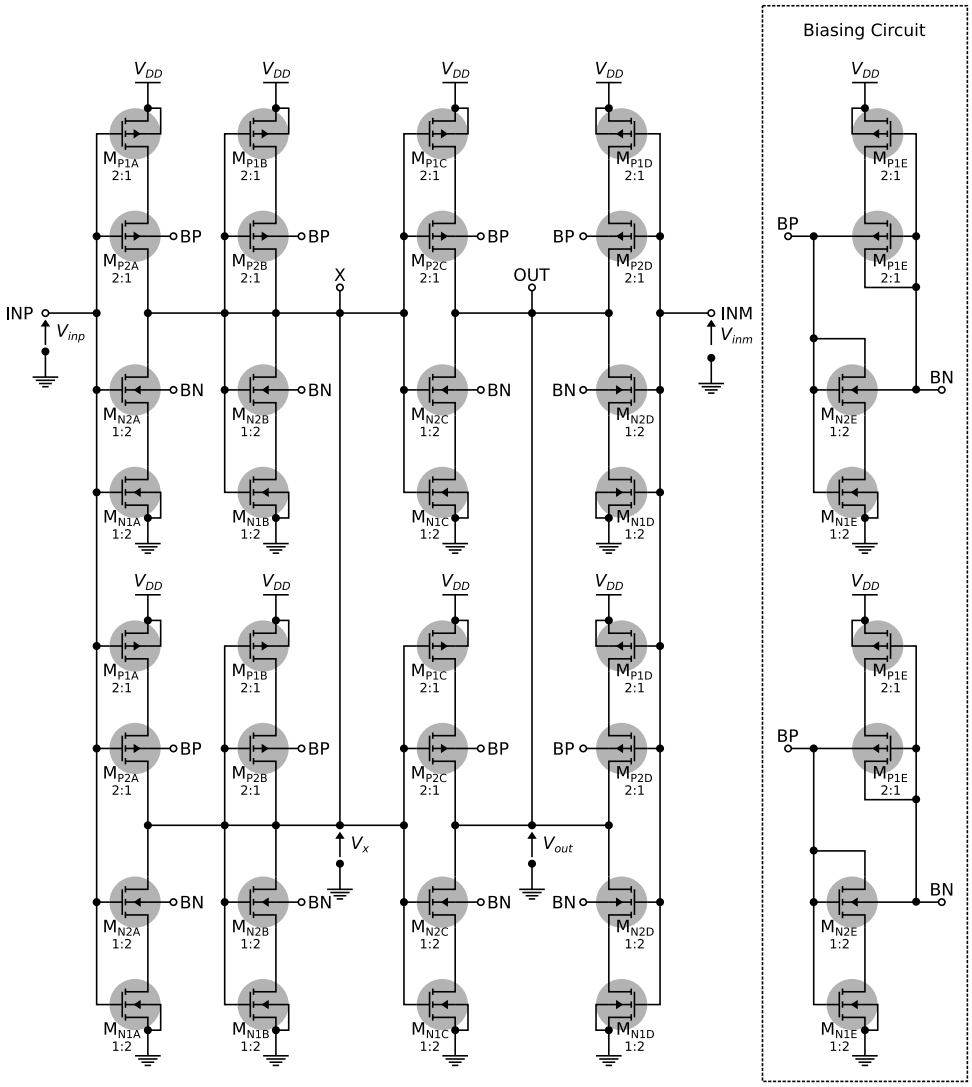


Figure 8. Proposed single-ended inverter-based OTA transistor-level circuit schematic.

Figure 9 shows the proposed OTA layout. The width W of each unit transistor is set on the basis of the minimum sizing requirement of the isolated n-well and p-well.

Based on this, all the unit transistors, both PMOS and NMOS have an identical aspect ratio equal to

$$\left(\frac{W}{L}\right)_N = \left(\frac{W}{L}\right)_P = \left(\frac{1.26\,\mu\text{m}}{0.42\,\mu\text{m}}\right) \tag{13}$$

All inverters are doubled in order to use the common-centroid layout technique. The transistors located at the edge of the layouts are the pseudo-resistors used to limit the substrate current and also function as dummies.

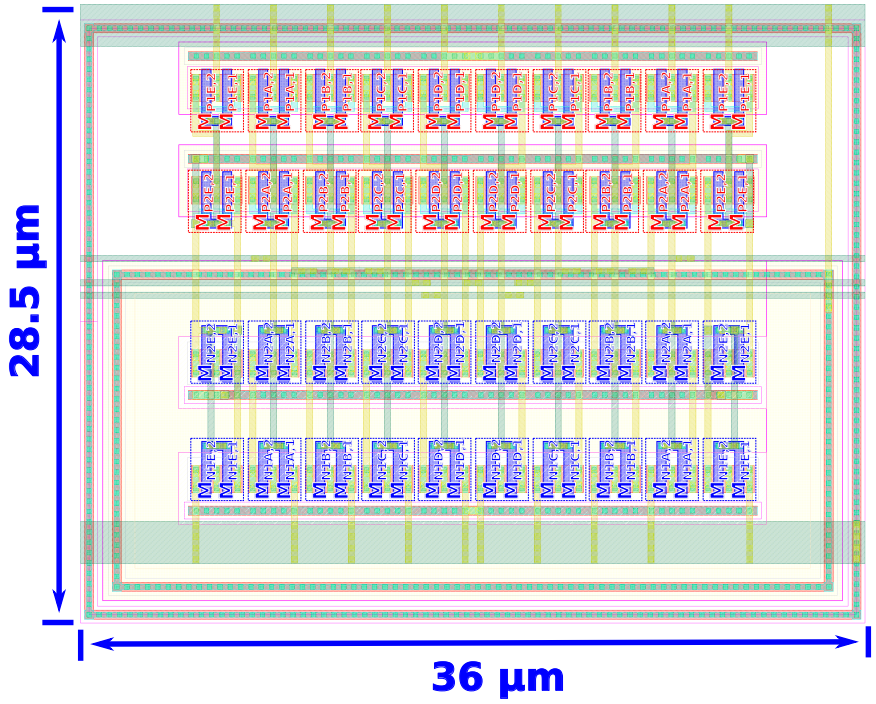
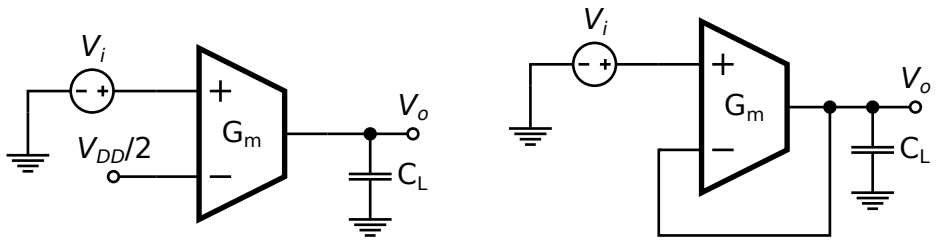


Figure 9. Layout view of the proposed inverter-based operation transconductance amplifier.

5. Simulation Results

The performance of the proposed OTA, designed in TSMC 180 nm CMOS technology, operating at 27 °C, at 0.3 and 0.6 V supply voltages, has been validated by using an open-loop and non-inverting buffer OTA test-bench circuits with a 10 pF capacitive load C_L, as shown in Figure 10a,b.



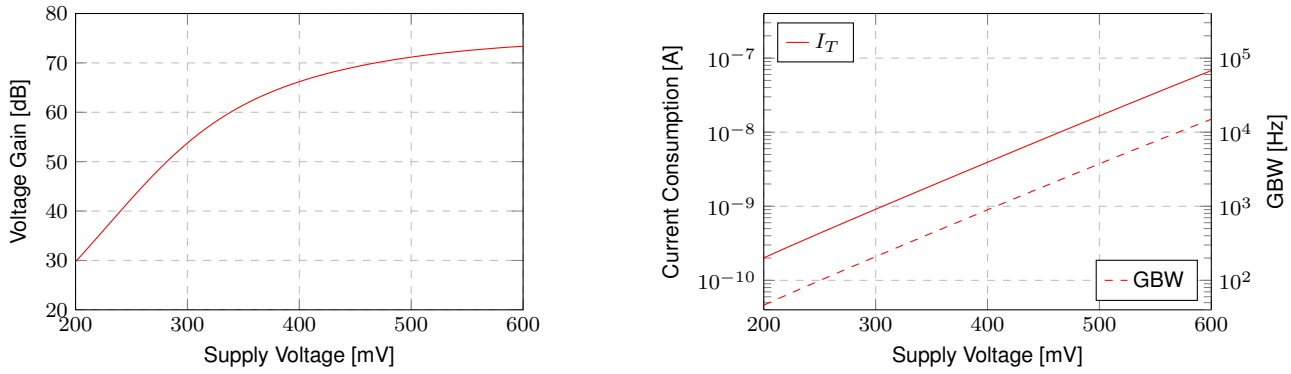
(**a**) (**b**)

Figure 10. OTAs testbench circuits: (**a**) open-loop (Gm-C integrator); (**b**) non-inverting buffer.

5.1. Open-Loop Analysis

Figure 11 shows how voltage gain and power consumption are affected by the supply voltage variation. In particular, Figure 11a shows that, at the lowest supply voltages, the voltage gain increases exponentially until the supply voltage reaches approximately 400 mV. At higher supply voltages, the improved composite transistor voltage gain technique progressively loses its effectiveness, as expected from the results shown in Figure 3b.

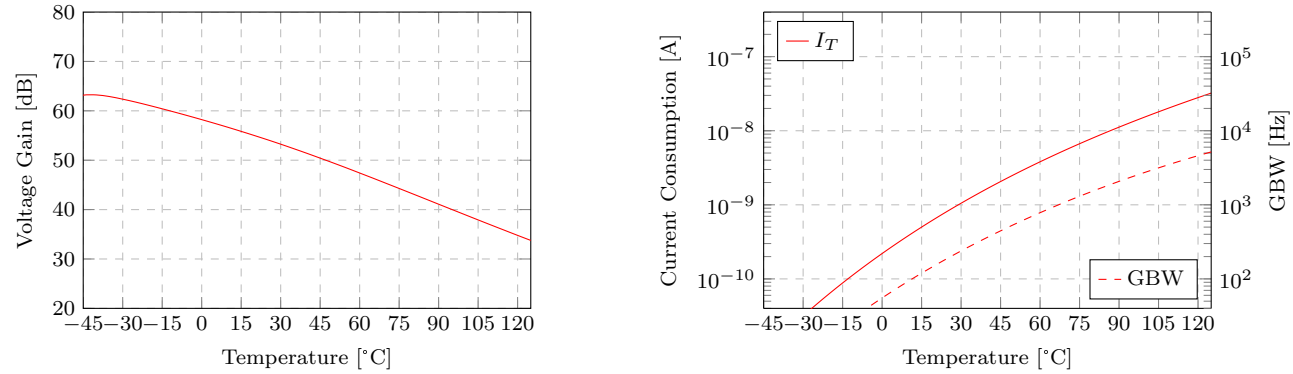
Figure 11b shows how the current consumption and the gain–bandwidth product (GBW) are affected by the supply voltage variation. The OTA power consumption increases exponentially with the supply voltage, and its gain–bandwidth product GBW increases proportionately, as the inverter transconductance G_m for the weak inversion operation is also proportional to its current consumption [21,22].



(**a**) (**b**)

Figure 11. Voltage supply dependence: (**a**) voltage gain; (**b**) total current consumption I_T and gain–bandwidth product (GBW).

Figure 12a,b shows how voltage gain and power consumption are affected by temperature variation for a 0.3 V voltage supply. As temperature increases, the voltage gain decreases, as a direct result from G_m and β reduction, as can be directly inferred from (6) and (4). Furthermore, as the temperature increases, the total current increases as a consequence of the threshold voltage reduction, and GBW increases accordingly.

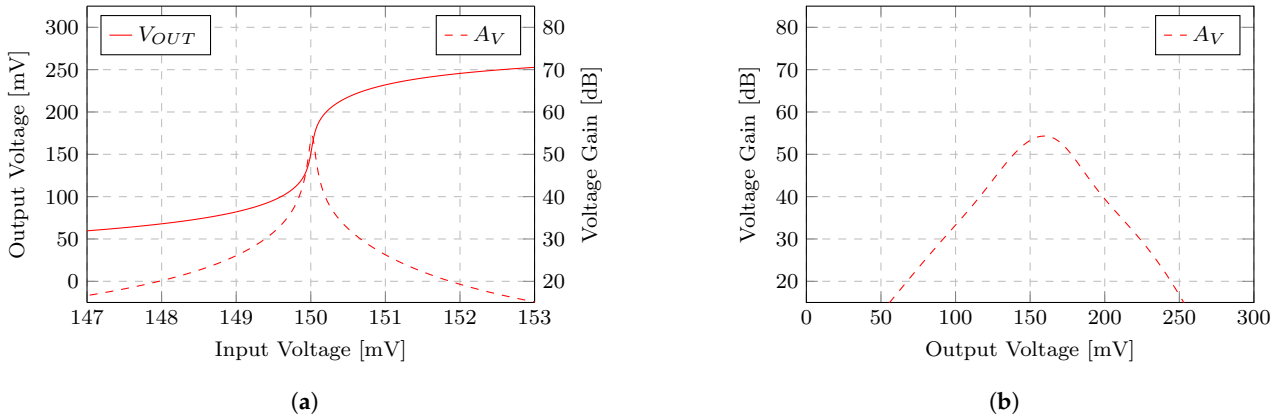


(**a**) (**b**)

Figure 12. Temperature dependence: (**a**) voltage gain, (**b**) total current consumption I_T and gain–bandwidth product (GBW).

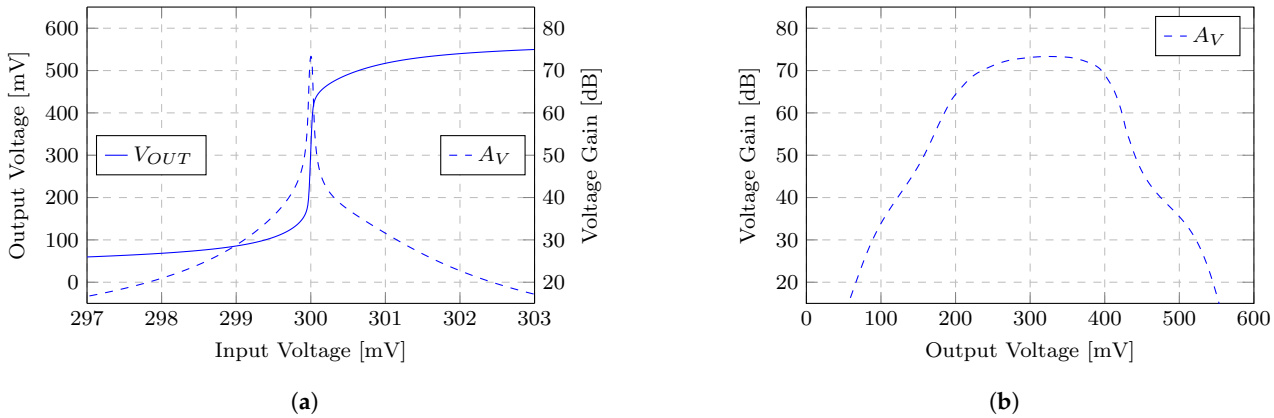
Figure 13a,b, respectively, show the proposed OTA input–output characteristic and the gain of the OTAs versus output voltage for a voltage supply $V_{DD} = 0.3$ V, while Figure 14a,b show the results for $V_{DD} = 0.6$ V. It can be noticed that in Figures 13b and 14b, the output voltage affects the OTA voltage gain as a consequence of the reverse transistor current and channel length modulation [22]; therefore, the output conductance G_o varies

accordingly. For these reasons, considering a gain $A_V > 30$ dB, output voltage swings between 100 and 500 mV can be obtained for the proposed OTA while supplied with $V_{DD} = 0.6$ V. The output range limitation is imposed by either PMOS or NMOS transistors entering the linear region outside these limits. For $V_{DD} = 0.3$ V, the reverse transistor current dominates the output conductance G_o behavior and voltage gain reaches its peak while the input is about half V_{DD}. This is a very important aspect, as small-signal voltage gain can be misleading because it shows only the maximum voltage gain, and voltage gain should be large for a large output voltage range to ensure good signal linearity for any OTA applications with feedback circuits.



(**a**) (**b**)

Figure 13. DC open-loop results for $V_{DD} = 0.3$ V: (**a**) input–output characteristic, and (**b**) voltage gain.



(**a**) (**b**)

Figure 14. DC open-loop results for $V_{DD} = 0.6$ V: (**a**) input–output characteristic, and (**b**) voltage gain.

Figure 15a–d shows the AC differential voltage gain, common-mode rejection ratio (CMRR), output phase and power supply rejection ratio (PSRR) curves, respectively. As expected, voltage gain and GBW exhibit large variations according to voltage supplies. The proposed OTA has voltage gains of 54 and 72 dB and a GBW of 102.1 and 14.95 kHz for $V_{DD} = 0.3$ and $V_{DD} = 0.6$, respectively. As the proposed OTAs is a single-stage amplifier, its phase margin is 90°. The CMRR are 54 and 72 dB, and PSRR are 59 and 79 dB, respectively.

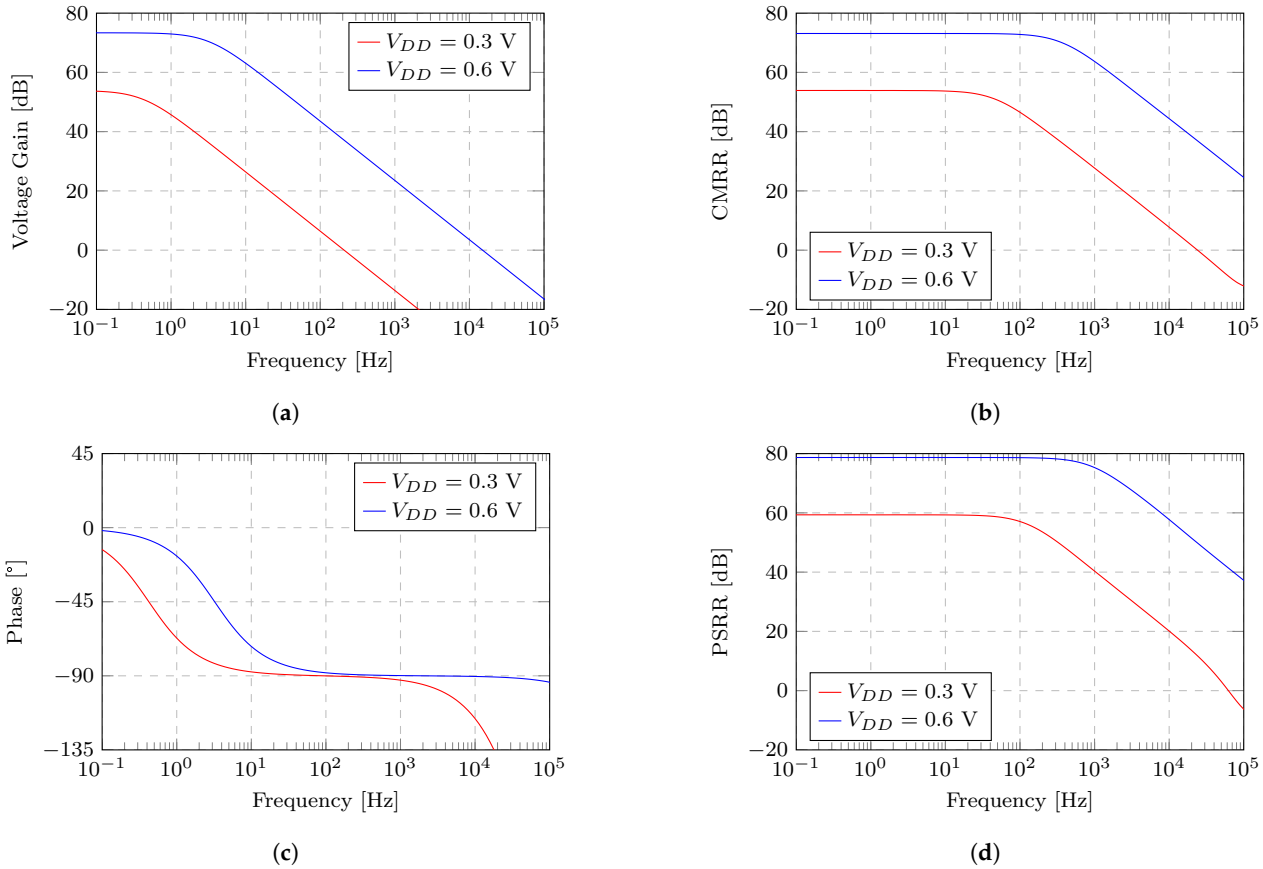


Figure 15. Open-loop AC simulation results: (**a**) voltage gain; (**b**) common-mode rejection ratio (CMRR); (**c**) phase; (**d**) power supply rejection ratio (PSRR).

Figure 16 shows the proposed OTA equivalent input referred noise. For $V_{DD} = 0.3$, it has equivalent input noises of 2.16 $\mu V/\sqrt{Hz}$, at 1 kHz, and 34.7 μV integrated input noise from 1 to 210 Hz. For $V_{DD} = 0.6$, it has equivalent input noises of 362 $nV/\sqrt{Hz}$, at 1 kHz, and 39.5 μV integrated input noise from 1 to 15 kHz.

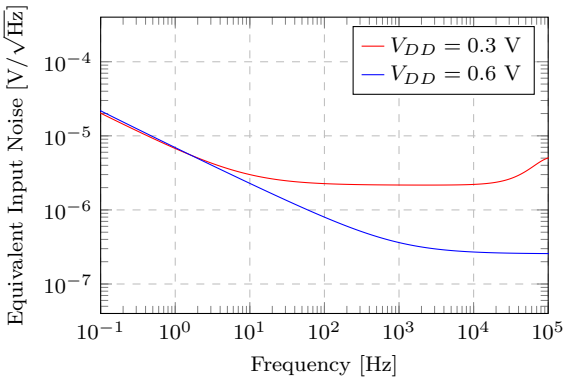
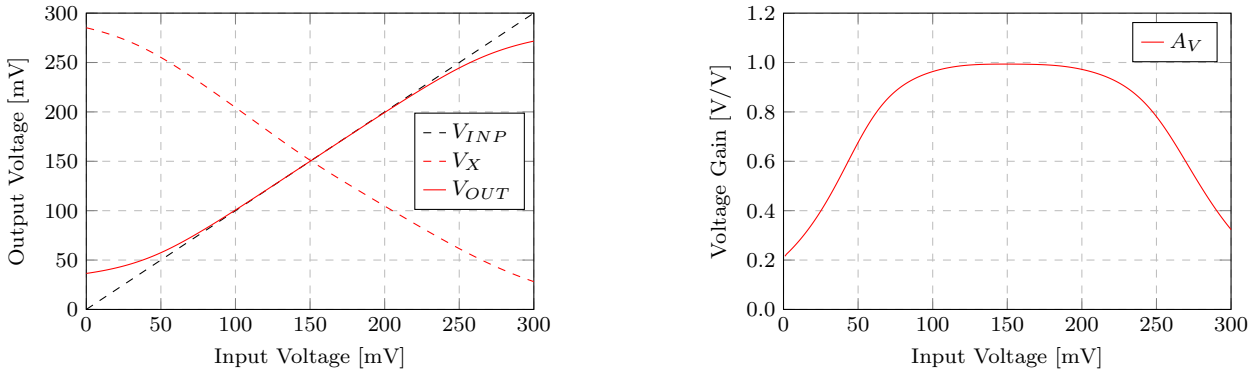


Figure 16. Input referred noise.

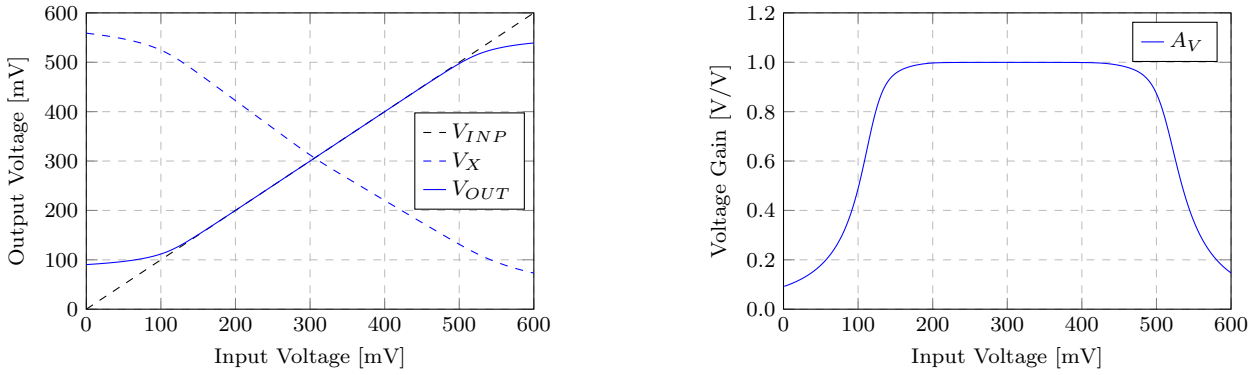
5.2. Unity-Gain Buffer Analysis

As with the output voltage swing limitations observed in open-loop DC simulations (as in Figure 10a), the non-inverting buffer simulations (as in Figure 10) also reveal the limits of input voltage swing, which are shown in Figures 17 and 18.



(**a**) (**b**)

Figure 17. Non-inverting buffer DC simulation results for $V_{DD} = 0.3$ V: (**a**) input–output characteristic and (**b**) voltage gain.



(**a**) (**b**)

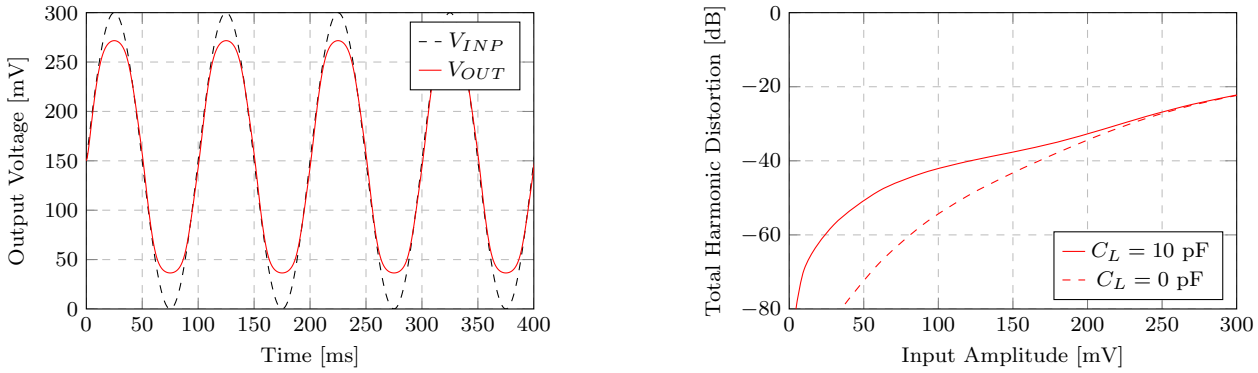
Figure 18. Non-inverting buffer DC simulation results for $V_{DD} = 0.6$ V: (**a**) input–output and (**b**) voltage gain.

In particular, Figure 18a shows how the output voltage saturation is a consequence of the voltage gain from the input INP to node X (see Figure 7). The X node voltage potential V_X can be expressed as approximately $V_{INP} - V_Q \approx -(V_X - V_Q)$, where V_Q is the inverter quiescent voltage [21]. As expected, V_X is approximately the inverted positive input voltage signal V_{INP}. However, V_X is clipped at approximately 100 and 500 mV for the proposed OTA for $V_{DD} = 0.6$ V, as the inverting voltage buffer does not work properly as the transistors enter the linear operation region.

Figures 17a,b and 18a,b show the main difference between the proposed OTA operation at different voltage supplies for the non-inverting buffer configuration. For $V_{DD} = 0.6$ V, the OTA has a more linear output due to its higher open-loop voltage gain and larger output voltage excursion, as expected. The OTAs proposed in [19] use a similar topology with half the number of inverters, but the V_X voltage excursion is also limited by the transistor slope factor n, which further limits those OTAs input range compared to the OTAs proposed in this work.

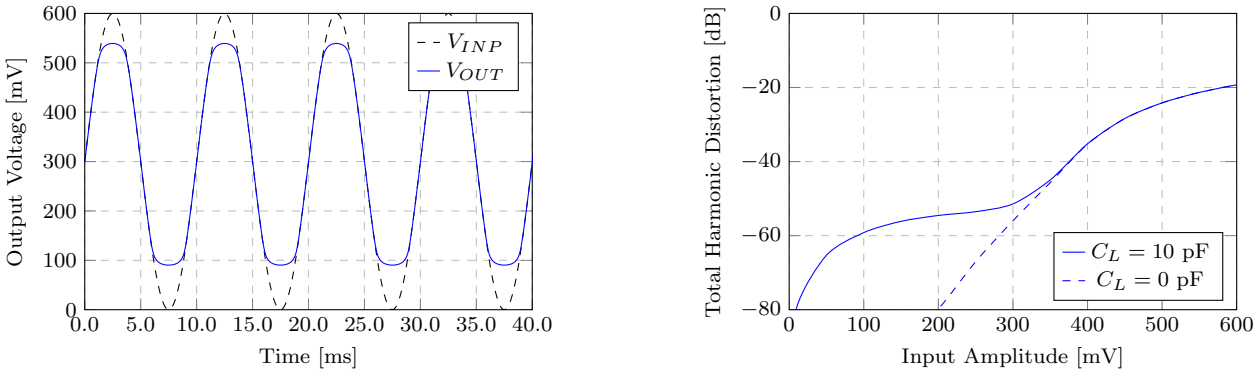
The same limitations, from the point of view of time-domain, are shown in Figures 19a,b and 20a,b for a rail-to-rail input sine-wave for $V_{DD} = 0.3$ V and $V_{DD} = 0.6$ V, respectively. The corresponding total harmonic distortion (THD) is displayed in Figures 17b and 18b for a 10 pF capacitive load C_L and no load except from the input impedance resulted from connecting the OTA output to the inverting input. A total harmonic distortion of 1% is achieved for input peak-to-peak amplitudes ranges of 300 and 375 mV for $V_{DD} = 0.3$ V and $V_{DD} = 0.6$ V, respectively. For lower input voltage amplitudes and no output load, the proposed OTA shows an even better linearity, achieving 80 dB THD for a 200 mV input amplitude for $V_{DD} = 0.6$ V. This is a direct consequence of the DC characteristic curves shown in Figure 18a,b, due to its higher open-loop voltage gain and that GBW is many times higher for lower capacitive loads. By analyzing Figure 18b, it

is made clear that the main limitations to the output signal linearity are the signal frequency, OTA GBW and the OTA DC characteristic curve.



(**a**) (**b**)

Figure 19. Non-inverting buffer transient simulation results: (**a**) sine-wave output response; (**b**) total harmonic distortion.



(**a**) (**b**)

Figure 20. Non-inverting buffer transient simulation results: (**a**) sine-wave output response; (**b**) total harmonic distortion.

5.3. Monte Carlo Simulation Results

Table 1 summarizes the corner simulation results. As expected, the greatest deviations from typical corner results are GBW and power for SS (Slow-Slow) and FF (Fast-Fast) corners. The worst corners for intrinsic input offset are SF (Slow-Fast) and FS (Fast-Slow), as the inverter transistor dimensions were optimized for the typical corner TT. As explained before, the OTA linearity is a function of the internal node voltage V_X, and input signal frequency and GBW. For better performance stability, PVT variability could be reduced by extra biasing circuits [21] or calibration [27].

Table 2 summarizes the mean μ and the standard variation σ from 1000 Monte Carlo simulation runs. Process and mismatch variations are analyzed individually and combined. The OTA results show that gain–bandwidth product GBW, total current I_{DD}, and power consumption are greatly affected by the process variability, as suggested by corner results. The power efficiency Figure of Merit, FoM, defined as $100 \times (\text{GBW} \cdot C_L)/I_T$, shows a negligible variation, since GBW is somehow proportional to I_T, as shown in Figure 11b. It is the same for the open-loop voltage gain. As a main drawback, the mismatch variations strongly affect the offset voltage V_{OS} of both OTAs. The simulations show 8.7 and 8.9 mV input offset voltage for 3σ mismatch variation for $V_{DD} = 0.3$ V and $V_{DD} = 0.6$ V, respectively.

Table 1. Corner results.

	V_{DD} (V)	GBW (kHz)	I_T (nA)	FoM (V^{-1})	A_V (dB)	V_{OS} (mV)	Power (nW)
TT	0.3	0.209	0.911	229	54	0.002	0.273
	0.6	14.95	67.95	220	73	0.003	40.77
SS	0.3	0.070	0.307	227	54	−0.020	0.092
	0.6	5.188	23.24	223	72	0.001	13.94
SF	0.3	0.338	1.414	239	54	0.338	0.424
	0.6	25.35	113.8	223	73	0.018	68.26
FS	0.3	0.241	1.097	220	53	−0.564	0.329
	0.6	15.25	73.47	208	73	−0.010	44.08
FF	0.3	0.615	2.642	233	53	0.025	0.793
	0.6	42.49	195.9	217	72	0.006	117.5

Table 2. Monte Carlo results.

	V_{DD} (V)	GBW (kHz)		I_T (nA)		FoM (V^{-1})		A_V (dB)		V_{OS} (mV)		Power (nW)	
		μ	σ	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ
Proc.	0.3	0.228	0.080	0.992	0.339	229	4	54	0.2	0.002	0.006	0.297	0.101
	0.6	16.25	5.630	74.01	25.68	220	3	73	0.4	0.003	0.004	44.40	15.41
Mis.	0.3	0.210	0.009	0.915	0.020	230	8	54	0.6	0.060	2.984	0.275	0.006
	0.6	15.05	0.602	68.27	1.567	220	7	73	0.3	0.038	3.034	40.96	0.940
All	0.3	0.230	0.080	1.000	0.334	230	9	54	0.6	0.008	2.918	0.299	0.100
	0.6	16.34	5.678	74.27	25.48	220	8	73	0.7	0.060	2.955	44.56	15.29

5.4. Performance Comparison

Table 3 summarizes the proposed OTA results and compares them to the state-of-art counterparts. The state-of-art OTAs can be categorized by the input terminal of their first stage amplifier block, and can be gate-driven [19,21,24,27–31] and bulk-driven [18,28,32–34]. Gate-driven OTAs are usually more power-efficient, as the bulk-drain transconductance is a fraction of the gate-drain transconductance, while bulk-driven OTAs have an extended voltage input range, which leads to less signal distortion for larger voltage signal amplitudes.

Additionally, the OTAs reported in Table 3 are classified as single-ended and fully differential. The fully differential circuits use more area and power, but their signals are more insensitive to power and common-mode fluctuations, and they have increased voltage range and output less distortion.

The proposed OTAs main feature is its voltage gain per number of stages, while still maintaining a relatively small area, a high power-efficiency figure of merit, and a high linearity for an extremely low voltage supply. A higher voltage gain could be achieved by using more amplifier stages; however, it would come at the cost of more area and the need for a stability compensation circuit.

The best power-efficient design for a 0.3 V supply voltage was proposed in [27], with a 1020 FoM. The proposed design has a 229 FoM, which is 4.45× smaller. However, it has a 1% THD for a 120 mV peak-to-peak amplitude signal, while the former has a 3% THD for a 100 mV peak-to-peak amplitude signal. As compared to the other state-of-art designs with supply voltage under 0.3 V, despite having a single gain stage, it still has the second best voltage gain. The best voltage gain under 0.3 V supply voltage [32] is 60 dB; however, as it is a multiple-stage OTA design, it has an area 25× larger, whereas the proposed OTA would have a 40 dB voltage gain for the same supply voltage at 0.25 V. The best voltage gain among all OTAs [18] has an 81 dB voltage gain at a 0.4 V supply voltage. The proposed OTA can achieve a 66 dB voltage gain with a single gain stage alone at 0.4 V supply voltage and has a total area about 5× smaller.

Table 3. Perfomance comparison.

	[28] +	[30] *	[24] +	[27] *	[29]	[31] *	[21] *	[28] +	[32] +	[33] +	[34] *	[18] *	[19] *	**This Work** *		**Unit**
Technology	180	130	130	180	130	180	180	180	130	65	65	180	180	180		nm
Input	GD	GD	GD	GD	GD	GD	GD	BD	BD	BD	BD	BD	GD	GD		-
Output	FD	FD	FD	SE	SE	FD	FD	FD	SE	FD	SE	FD	SE	SE		-
N. of Stages	2	2	1	2	2	1	1	2	2	3	2	2	1	1		-
Die Area	17,000	-	52,000	1426	982	800	-	26,000	83,000	5000	3000	5000	727	1026		µm²
VDD	0.5	0.3	0.25	0.3	0.3	0.3	0.5	0.5	0.25	0.35	0.3	0.4	0.3	0.3	0.6	V
Power	75,000	1800	55	2	2.4	10.5	140	17,000	18	17,000	51	300	0.50	0.273	40.8	nW
Voltage Gain	62	50	25	35	30	23	64	52	60	43	60	81	51	54	**73**	dB
V. Gain/ N. Stages	31	25	25	18	15	23	64	26	30	14	30	41	51	54	73	dB
CMRR	75	-	43	-	-	-	54	78	-	46	126	126	37	54	73	dB
PSRR	81	-	47	-	-	-	51	76	-	35	90	79	41	59	79	dB
Offset Voltage	6.0	-	-	-	-	-	-	9.0	8.4	-	7.3	-	5.4	8.7	8.9	mV
Input R. Noise	225	38	139		-	-	-	225	3300		2820	213	809	2160	362	$nV/\sqrt{Hz}$
THD	1	-	0.1	3	1	-	-	1	0.2	0.3	-	-	1	1	1	%
Input Range	712	-	19	100	270	-	-	400	150	-	-	-	35	120	370	mV
GBW	10,000	9100	7.23	0.89	0.25	8.0	100	3600	1.88	3600	70	280.4	0.74	0.21	15.0	kHz
Phase Margin	60	76	90	76	-	86	90		53	56	53	59	90	90	90	°
C_L	20	2	30	80	150	10	10	20	15	3	5	5	10	10	10	pF
FoM	133	303	143	1020	468	229	370	22	29	22	20	187	443	229	220	V^{-1}
Voltage Gain Improvement Technique	MGS/PF	MGS	RA	DIG	DIG	-	TA	MGS/PF	MGS/PF	MGS	MGS	MGS	ICT	ICT	ICT	-

+ Measured, * Simulated, GD: Gate-Driven, BD: Bulk-Driven, FD: Fully-Differential, SE: Single-Ended. FoM = $100 \cdot (\text{GBW} \cdot C_L)/I_T$. MGS: Multiple Gain Stages, PF: Positive Feedback, RA: Rectangular Arrays, DIG: Digital OTA, TA: Trapezoidal Arrays, ICT: Improved Composite Transistors.

The best comparison can be made with the inverter-based OTA proposed in [21], as it was designed for the same process using the same transistor dimensions and voltage supply. For $V_{DD} = 0.3$ V, it has 1.4× more area and about half of its power-efficiency FoM; however, it has a 3.4× larger input voltage excursion for the same THD. It also has a slightly larger voltage gain.

6. Conclusions

This paper shows how to maximize the gain of an inverter-based OTA topology with independently forward-body-biased composite transistors without reducing its input voltage swing. Compared with other state-of-art OTAs in similar operation conditions, the proposed OTAs have the largest voltage gain by the number of amplifier gain stages (54 dB at 0.3 V V_{DD} and 73 dB at 0.6 V V_{DD}), while still keeping a relatively small die area (1026 μm^2). Notice that the same technique could also be exploited in fully differential inverter-based OTA topologies.

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Abbreviations

The following abbreviations are used in this manuscript:

CMOS	Complementary Metal-Oxide Semiconductor
CMRR	Common-Mode Rejection Ratio
FoM	Figure of Merit
GBW	Gain–Bandwidth Product
OTA	Operational Transconductance Amplifier
PSRR	Power Supply Rejection Ratio
THD	Total Harmonic Distortion
UICM	Unified Current Control Model
ULP	Ultra-Low-Power
ULV	Ultra-Low-Voltage

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