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A 17.8–34.8 GHz (64.6%) Locking Range Current-Reuse Injection-Locked Frequency Multiplier with Dual Injection Technique

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Abstract: A 17.8–34.8 GHz (64.6%) locking range current-reuse injection-locked frequency multiplier (CR-ILFM) with dual injection technique is presented in this paper. A dual injection technique is applied to generate differential signal and increase the power of the second-order harmonic component. The CR core is proposed to reduce the power consumption and compatibility with NMOS and PMOS injectors. The inductor-capacitor (LC) tank of the proposed CR-ILFM is designed with a fourth-order resonator using a transformer with distributed inductor to extend the locking range. The self-oscillated frequency of the proposed CR-ILFM is 23.82 GHz. The output frequency locking range is 17.8–34.8 GHz (64.6%) at a 0-dBm injection power without any additional control including supply voltage, varactor, and capacitor bank. The power consumption of the proposed CR-ILFM is 7.48 mW from a 1-V supply voltage and the die size is 0.75 mm × 0.45 mm. The CR-ILFM is implemented in a 65-nm CMOS technology.

Keywords: current-reuse; dual injection technique; fourth-order resonator; injection-locked frequency multiplier

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1. Introduction

Recently, injection-locked frequency multipliers (ILFM) have been actively studied to realize millimeter (mm)-wave local oscillator (LO) signals [1,2]. The reason is that the mm-wave frequency is used in fifth generation (5G) and sixth generation (6G) wireless communications. In addition, the LO in the mm-wave band should have a low-phase noise performance and wide tuning range in the multiband applications. To satisfy this performance, ILFM has been used in several stages in recent years [3,4]. Meanwhile, frequency modulated continuous wave (FMCW) radar applications also require wideband performance in the mm-wave band including industrial–scientific–medical (ISM) bands, e.g., 24 GHz and 77 GHz, to realize wideband chirp waveform [5,6]. The ILFM is a good solution that can easily generate mm-wave signals using LC oscillation in various applications.

Figure 1 shows the block diagram of a conventional phase-locked loop (PLL) with a frequency multiplier used to synthesize mm-wave signals. As can be seen from the figure, conventional PLLs consist of a phase-frequency detector (PFD), charge pump (CP), low-pass filter (LPF), voltage-controlled oscillator (VCO), and divider chain. F_{ref} and F_{out} mean the reference frequency and output frequency, respectively. The frequency multiplier is added to synthesize the mm-wave signals without affecting the gain of the VCO (K_{VCO}) of the PLL [7–9]. Generally, doubler [10] and tripler [11,12] are determined according to multiplying ratio. A frequency doubler that receives the second-order harmonic component as an input signal consumes less power than a frequency tripler that receives the third-order harmonic component as an input signal. Thus, in this paper, the frequency multiplier as

a frequency doubler is proposed. There are three types of frequency multipliers: digital-based frequency multipliers, harmonic signal multipliers, and LC-based injection-locked frequency multipliers (ILFMs). The digital-based frequency multiplier is implemented with digital logics and is used to multiply low frequencies, e.g., the reference frequency of PLLs and digital clocks [13,14]. The output frequency range of digital-based frequency multipliers has been measured to be 2.6–5.2 GHz [13] and 0.96–1.44 GHz [14]. Figure 2 shows block diagrams of the harmonic signal multiplier and LC-based ILFM. The harmonic signal multiplier consists of harmonic generator, notch filter, and driving amplifier as shown in Figure 2a [15,16]. The harmonic signals are generated by nonlinear devices and are filtered with a notch filter. The filtered signal is amplified by a driving amplifier. When a harmonic signal frequency multiplier is used as a frequency doubler, the output signal is twice the input signal f_0, i.e., $2f_0$. Although this method can easily generate very high frequencies, it has critical drawbacks. Because there are harmonic components of many orders, a large-size notch filter must be used. In addition, the harmonic components are smaller than the fundamental signal; thus, the signal needs to be amplified, and the power consumption of this driving amplifier is very large. The harmonic refection technique has been proposed to obtain a high frequency roll-off for the mm-wave application [15], and the frequency multiplier chain has been proposed to synthesize terahertz-frequency signals [16]; their outputs are 93 GHz and 288 GHz, respectively, albeit with large power consumption of 438 mW [15] and 284 mW [16], respectively. The LC-based ILFM consists of an injector, LC band-pass filter (BPF), and core, as shown in Figure 2b. The injector is designed as a non-linearity-based device and generates the harmonic components of the input signal frequency. In the figure, I_{inj} is the current generated by injector, I_{so} is the current generated when ILFM self-oscillates, and I_{tot} is the sum of I_{inj} and I_{so}. BPF is designed as a LC resonator and filters the input signal frequency. The $-g_m$ core supplies the energy consumed by the LC resonator. ILFM self-oscillates when an input signal is not applied to the injector. Because ILFM is based on an oscillator-based design, it consumes less power than the harmonic signal multiplier and operates at a higher frequency compared to the digital-based frequency multiplier. Furthermore, ILFM can generate output signals at a large voltage swing level with a low-power injection signal. However, ILFM has narrow locking range. To overcome this issue, varactors and capacitor bank are often used, although the phase noise performance degrades when the operating frequency is very different from the self-oscillation frequency [12,17]. To design a wide locking range and low phase noise ILFM, a high-order transformer and the current boosting technique have been investigated [18]. ILFM with high-order transformer has a locking range of 22.8–43.2 GHz; however, the unlocking part in the locking range occurs at −1.5 dBm input power. In addition, the sixth-order transformer design is very complex.

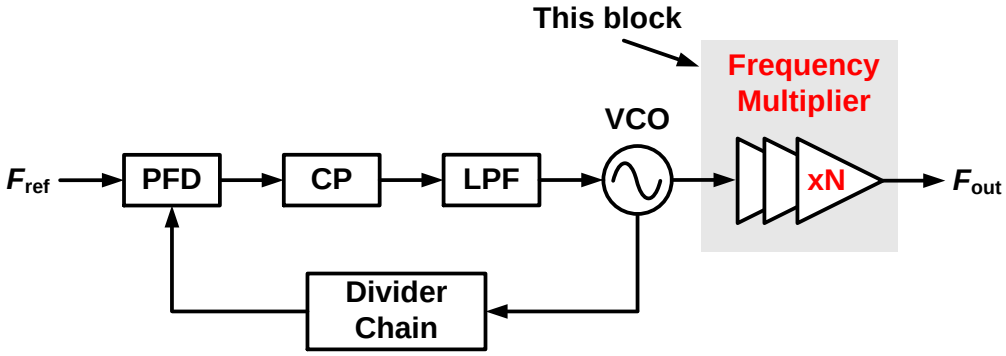


Figure 1. Conventional phase-locked loop with mm-wave frequency multiplier.

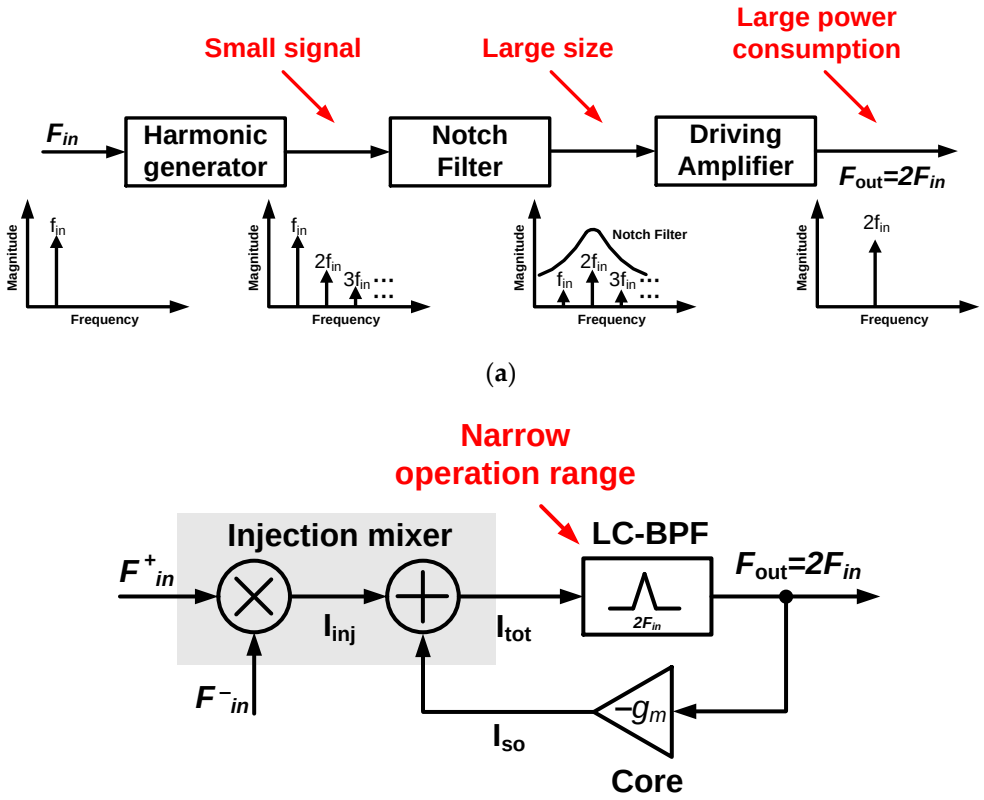


Figure 2. Two kind of frequency multipliers block diagram: (**a**) harmonic component multiplier; (**b**) injection-locked frequency multiplier (ILFM).

In this paper, the current-reuse (CR)-ILFM with dual injection technique and fourth-order resonator using a transformer with distributed inductors is proposed. The rest of this paper organized as follows. In Section 2, the proposed CR-ILFM is described in detail. In addition, the progression of locking range analysis in the time domain and phase domain is reported. Furthermore, the locking range difference of ILFMs with second- and fourth-order resonators with a distributed inductor are simulated. In Section 3, measurement results including the locking range, output power, and phase noise are reported. Finally, in Section 4, the conclusions are drawn.

2. Proposed CR-ILFM

2.1. Dual Injection and Current-Reuse Core

Figure 3 shows a schematic of ILFMs with single injection and dual injection technique. ILFM is composed of the LC-BPF (L_1, C_1), cross-coupled pair core (M_1, M_2), injector (M_3, M_4), and output buffer. The differential input signal ($V_{in,w+}$, $V_{in,w-}$) is biased at the injector, as shown in Figure 3a. This injector generates only even harmonic components by non-linearity characteristic. The output signal of the injector containing the desired $2w_0$ component, as well as the other even harmonic components, is applied to the NMOS cross-coupled pair. Meanwhile, a PMOS injector is required to inject a differential even harmonic signal to the core. However, it is difficult to realize because of bias issue. As a result, injection signal is generated as unbalanced signal.

The proposed CR-ILFM can be applied dual injection by changing the core. The couple of the injector is composed of NMOS pair (M_3, M_4) and PMOS pair (M_5, M_6) to make harmonic components differential as shown in Figure 3b. The PMOS and NMOS injector can generate balanced signal to the core and increase the effective power of injection signal compared to the conventional ILFM with single injection. In addition, the couple of

injectors still cancel out odd harmonic components including the fundamental signal. The CR core that is replaced by PMOS (M_2) has the best compatibility with the dual injection technique. This is because half of the supply voltage to fix the center-tap bias is required to operate the PMOS and NMOS injectors at the same time. In addition, the CR core reduces the power consumption by turning the MOSFETs on and off simultaneously [19–24].

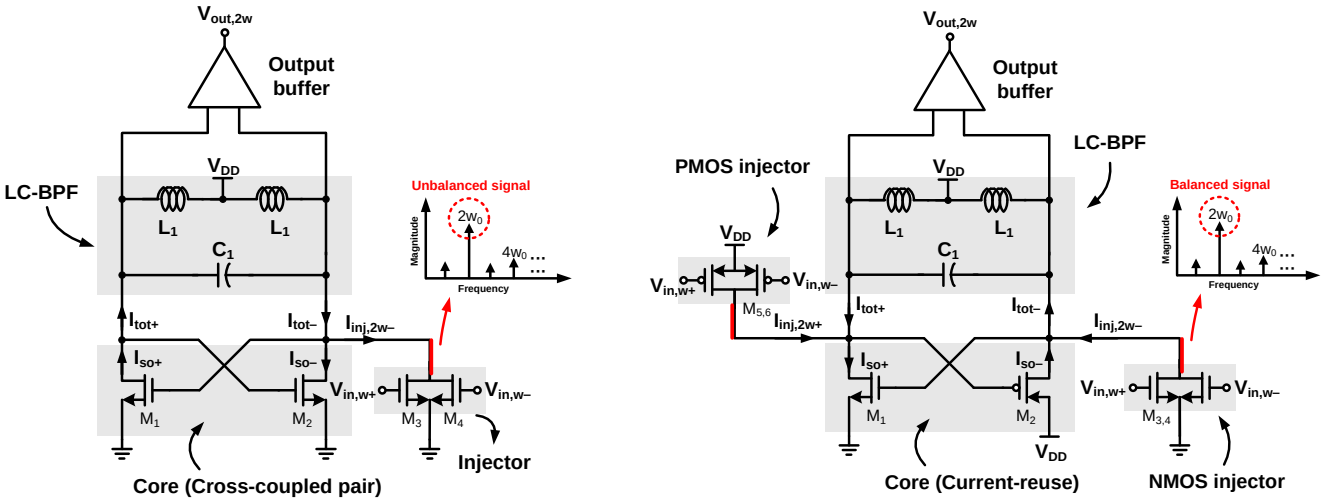


Figure 3. Schematic of (**a**) the conventional ILFM with single injection on cross-coupled pair and (**b**) the proposed ILFM with dual injection on current-reuse (CR) core.

Figure 4 shows the magnitude flow of the single and dual injection signal generated by injector. If a sinusoid is applied to a nonlinear system, the output signal generally exhibits frequency components that are integer multiples of the input frequency. If the input voltage signal equal to $A\cos(w_0 t)$, then:

$$\begin{aligned} V &= a + bA\cos w_0 t + c(A\cos w_0 t)^2 + d(A\cos w_0 t)^3 + \cdots \\ &= \left(a + \tfrac{cA^2}{2}\right) + \left(bA + \tfrac{3dA^3}{4}\right)\cos w_0 t + \tfrac{cA^2}{2}\cos 2w_0 t + \tfrac{dA^3}{4}\cos 3w_0 t + \cdots, \end{aligned} \tag{1}$$

where "a", "b", "c", and "d" are constants, and "A" is the magnitude of the input signal. If the differential input voltage signal is applied to the injector, then:

$$\begin{aligned} V_{injector} = a \quad & + bA\cos w_0 t + c(A\cos w_0 t)^2 + d(A\cos w_0 t)^3 + \cdots \\ & + a - bA\cos w_0 t + c(A\cos w_0 t)^2 - d(A\cos w_0 t)^3 + \cdots \\ & = (2a + cA^2) + cA^2\cos 2w_0 t + \cdots. \end{aligned} \tag{2}$$

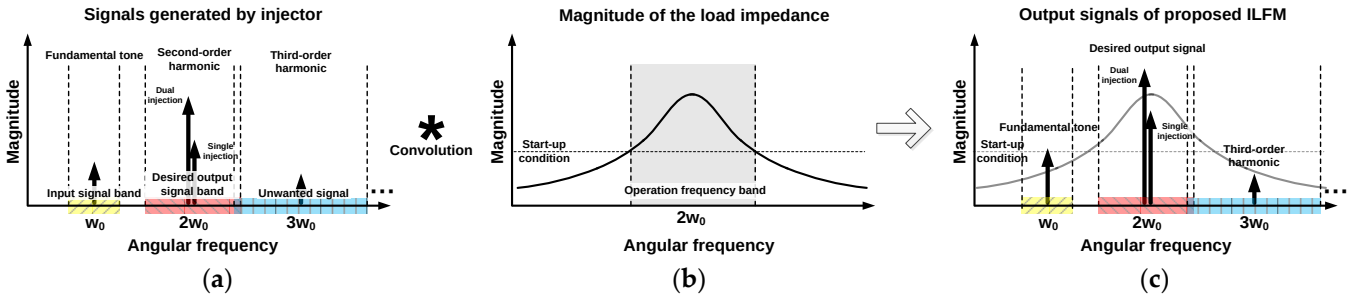


Figure 4. Magnitude flow of the single and dual injection signal. (**a**) Signal magnitude by injector; (**b**) magnitude of the load impedance; (**c**) output signal magnitude.

In (2), the first term on the right-hand side is a DC quantity and the second term is the second-order harmonic. The fundamental and odd harmonic signals are canceled out. In the frequency doubler application, second-order harmonic is the desired output signal, and other harmonics including the fundamental tone are unwanted signals. The magnitude of the second-order harmonic component of the proposed ILFM with dual injection is approximately twice that of conventional ILFM with single injection. The injection signal is convoluted with the magnitude of the load impedance, which is determined by LC-BPF. The magnitude of the load impedance has a 3 dB bandwidth and is not an ideal "Dirac-delta function". Therefore, the fundamental tone signal and other unwanted signals are also amplified even if the load impedance is set to $2w_0$. However, the start-up condition, which is determined by the "Barkhausen formula" should be met to be locked:

$$|g_m| \cdot |Z_L| \geq 1, \tag{3}$$

where g_m is the transconductance of the core, and Z_L is the load impedance. If the input signal is increased, the difference in magnitude between the desired signal and the unwanted signal can eventually become similar. If the minimum operating frequency is $2f_{0,\min}$ and the maximum operating frequency is $2f_{0,\max}$, then $2f_{0,\max} < 4f_{0,\min}$ should be satisfied. Otherwise, the ILFM may be locked at the wrong frequency. When $2f_{0,\max} = 4f_{0,\min}$, the maximum locking range is as follows:

$$Locking\ Range = \frac{f_{\max} - f_{\min}}{f_{\min} + \frac{f_{\max} - f_{\min}}{2}} \cdot 100(\%), \tag{4}$$

$$Locking\ Range\Big|_{2f_{0,\max}=4f_{0,\min}} = 66.7\%. \tag{5}$$

The ideally maximum locking range of injection-locked frequency doubler is 66.7%.

Figure 5 shows the phase difference of the ILFM applied conventional and proposed injection technique in the phase domain and time domain. As shown in Figure 5a, the phasor rotates clockwise and the current in ILFM is expressed in terms of I_{tot}, I_{so}, and $I_{inj,2w}$. The current equation is:

$$I_{tot} = I_{so} + I_{inj}, \tag{6}$$

where the total current is sum of the self-oscillation current and injection current. The injection current changes the phase of the output signal. The force to change the phase determines the frequency locking range of ILFM because the phase is the integral of the frequency. "α" is the phase difference between the self-oscillation current and total current, or phase of the injection current. The maximum phase difference is determined when:

$$\sin \alpha_{\max} = \frac{I_{inj}}{I_{so}}, \tag{7}$$

is satisfied [25]. When I_{inj} and I_T are orthogonal to each other, the phase difference has a maximum value. If I_{inj} is greater than I_{so}, the circuit acts as a buffer, not an injection-locked frequency multiplier circuit. Thus, we can assume that the following condition is satisfied:

$$|I_{so}| > |I_{inj}|, -\frac{\pi}{2} \leq \alpha_{\max} \leq \frac{\pi}{2}. \tag{8}$$

If I_{so} in (7) is fixed, $\alpha_{\max}$ increases as the magnitude of I_{inj} increases. Here, I_{inj} can be expressed as:

$$I_{inj} = g_{m,inj} \cdot V_{input}, \tag{9}$$

where $g_{m,inj}$ is the transconductance of the injector, and V_{input} is the input voltage signal. By (7) and (9),

$$\sin \alpha_{\max} = \frac{g_{m,inj} \cdot V_{input}}{I_{so}}, \ (-\frac{\pi}{2} \leq \alpha_{\max} \leq \frac{\pi}{2}). \tag{10}$$

To increase g_m, the size of the core MOSFET must be increased. However, this method is limited by the increase in the parasitic capacitance and harmonic signal amplitude. In the frequency synthesizer circuit, V_{input} is the output signal of the VCO, which is limited value. Therefore, it is more efficient to take advantage of increased magnitude by using a dual injection technique than a single injection technique. According to (2), (10), when using the proposed dual injection technique, V_{input} and $\sin(\alpha_{max})$ are twice larger than that of when using a conventional single injection. $I_{tot,dual}$ is the sum of $I_{inj,dual}$ and I_{so}, and $I_{tot,single}$ is the sum of $I_{inj,single}$ and I_{so}. $\Delta\alpha_{dual}$ is the difference between I_{so} and $I_{tot,dual}$, and $\Delta\alpha_{single}$ is the difference between I_{so} and $I_{tot,single}$. As in (7), the maximum phase difference is determined when I_{tot} and I_{inj} are orthogonal. $I_{inj,dual}$ is larger than $I_{inj,single}$, and $\Delta\alpha_{dual}$ is larger than $\Delta\alpha_{single}$. Therefore, the locking range of ILFM with dual injection technique is wider than that of with single injection technique. As shown in Figure 5b, there are three kinds of voltage signals. The first kind is produced when ILFM self-oscillates, and the second and third kinds are the output signal of ILFM with single and dual injections, respectively. The output signal of ILFM can be pushed and pulled by the injection signal, which means that it can be changed both directions: increased frequency and decreased frequency. The conclusions that the locking range is increased when using a dual injection technique than when using a single injection technique are drawn to be the same in the time domain and phase domain.

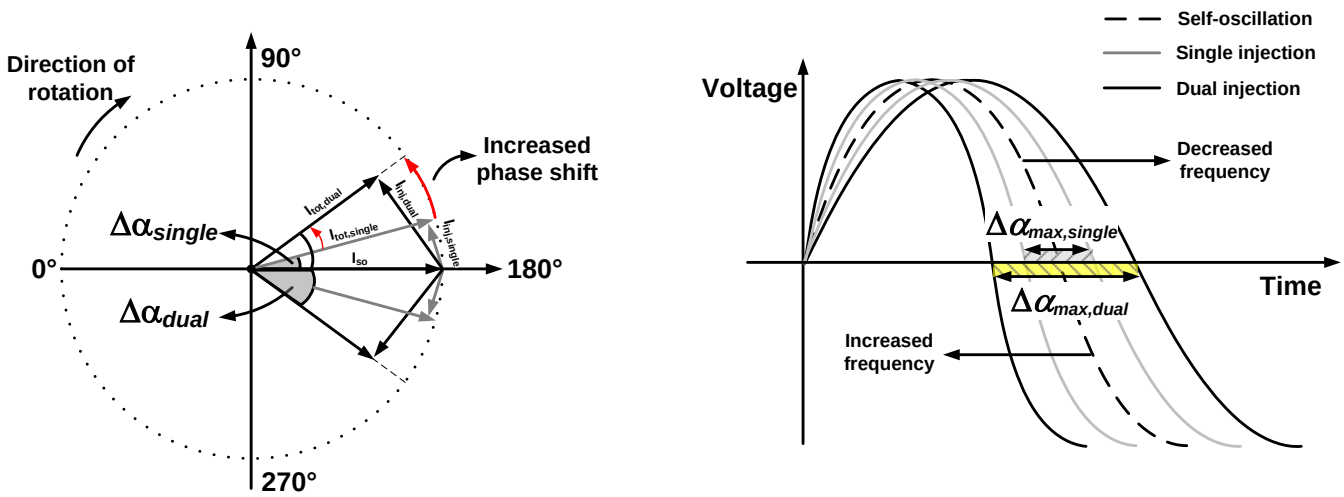


Figure 5. Maximum phase difference between ILFMs with single and dual injection technique in the (**a**) phase domain and (**b**) time domain.

2.2. Fourth-Order Resonator

Figure 6 shows a block diagram of the variable resonators and magnitude plots according to the angular frequency. Figure 6a shows a graph of the second-order resonator consisting of L and C. This resonator has one pole; the resonance angular frequency can be expressed as:

$$w_0 = \frac{1}{\sqrt{LC}}, \tag{11}$$

and its quality factor (Q) decides the 3-dB bandwidth:

$$Q = 2\pi \frac{E_{stored/period}}{E_{dissipated/period}} = \frac{w_0}{BW_{3dB}}, \tag{12}$$

where $E_{stored,period}$ is the energy stored in the oscillating resonator, $E_{dissipated,period}$ is the energy dissipated per period by parasitic resistance, and BW_{3dB} is the 3-dB bandwidth.

The bandwidth can be increased by reducing the parasitic resistance at the layout stage, and there is a tradeoff between the bandwidth and magnitude. Therefore, the start-up condition and bandwidth must be determined carefully. Figure 6b shows the increase in the bandwidth using a fourth-order resonator. The fourth-order resonator consists of L_1, L_2, C_1, and C_2. If the values of both inductance and capacitance are similar, then poles can be calculated as follows:

$$w_L = \frac{1}{\sqrt{(1+k)LC}}, \; w_R = \frac{1}{\sqrt{(1-k)LC}}, \tag{13}$$

where "k" is the coupling factor. If the transformer is in a strong coupling, the distance between the two poles increases. This implies a wider locking range, however, there would be a new minimum value between the two poles. If the new minimum value is smaller than that in the start-up condition, ILFM unlocks at the new minimum frequency. The magnitude of the load impedance is increased by adding a distributed inductor (L_3) to the fourth-order resonator, as shown in the Figure 6c. The load impedance is determined as follows:

$$Z_L(s) = \frac{(1-k^2)L_1L_2C_2s^3 + L_1s}{(1-k^2)L_1L_2C_1C_2s^4 + (L_1C_1 + L_2C_2)s^2 + 1} \cdot (1 + 2L_3C_1s^2). \tag{14}$$

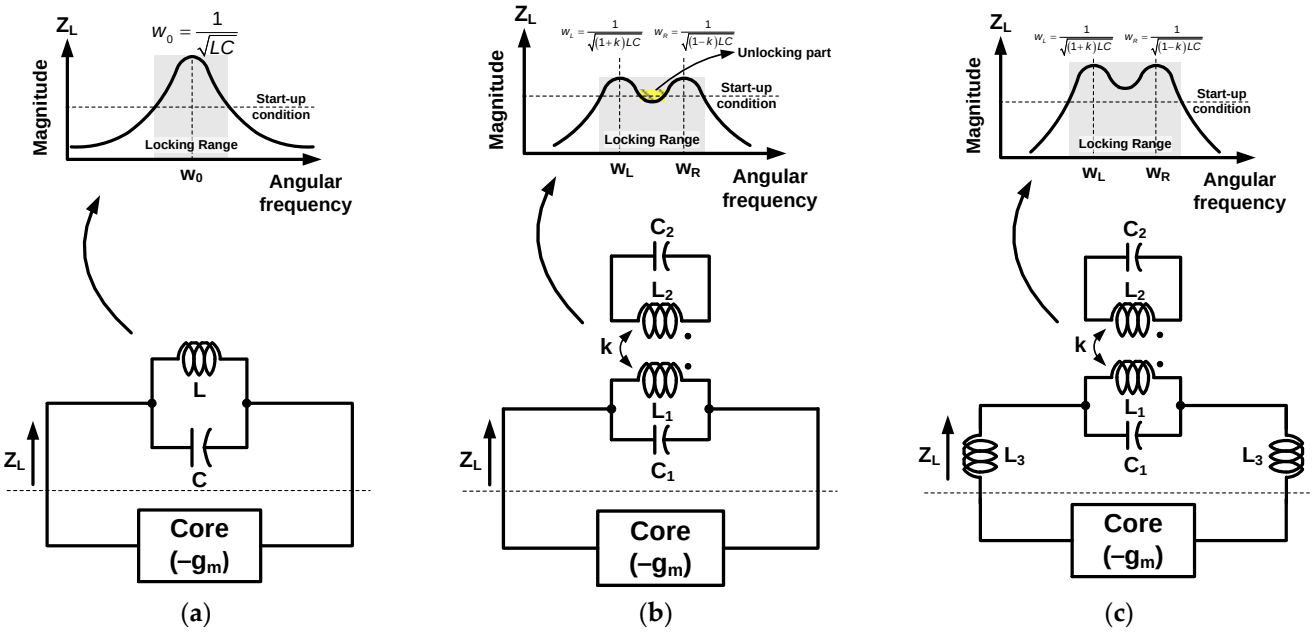


Figure 6. Block diagrams of variable resonators and magnitude plots according to the angular frequency: (**a**) second-order resonator; (**b**) fourth-order resonator; (**c**) fourth-order resonator with distributed inductor.

The last term in the right-hand side of (14) includes the L_3 value. Therefore, the magnitude of the load impedance can be increased by adding the distributed inductor. In addition, L_3 does not directly affect to the value of the poles. Therefore, the load impedance can be increase by properly adjusting L_1 and L_3.

Figure 7 shows the simulated bode plot with the variable resonators described in Figure 6. Figure 7a shows the magnitude of the load impedance. The pole of the second-order resonator exists near 24 GHz and the two poles of the fourth-order resonator are properly separated by the coupling factor. However, there is a part that does not satisfy the start-up condition; this part will be unlocking part. The distributed inductor is used to increase the magnitude of the load impedance sufficiently. The range beyond the start-up condition in the fourth-order resonator obtained using the distributed inductor is

approximately 16–35 GHz. This is not the locking range, but simply a range that satisfies (3). Figure 7b shows the phase plot. The maximum value of the phase, $\pm\alpha_{max}$, is determined using (10). From the figure, the phase range within the $\pm\alpha_{max}$ obtained using the fourth-order resonator is wider than that obtained using the second-order resonator owing to the phase ripple. Furthermore, the resonator with the distributed inductor has subtle ripples, which greatly reduce the average slope of its phase. The locking range satisfies the magnitude and phase conditions ((3) and (10), respectively), the simulated locking range of the proposed ILFM is 19–35 GHz (59%).

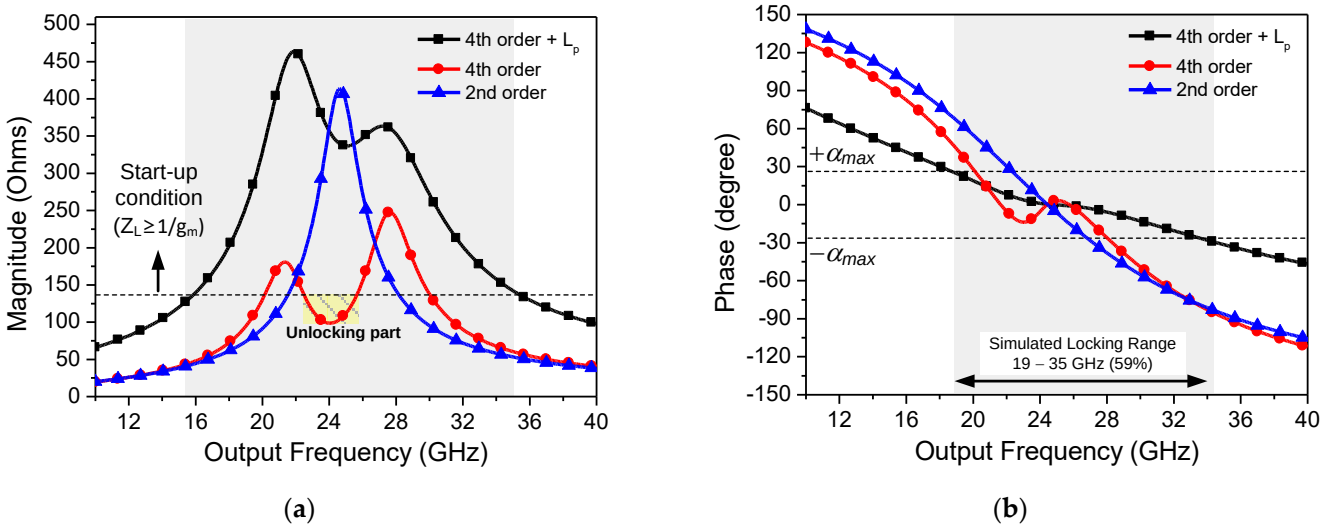


Figure 7. Simulated bode plot of the ILFM with variable resonators: (**a**) magnitude plot; (**b**) phase plot.

2.3. Proposed CR-ILFM

Figure 8 shows a schematic of the proposed CR-ILFM, which consists of fourth-order resonators (L_1, C_1, L_2, and C_2), a distributed inductor (L_3), CR cores (M_1, M_3), center-tap generators (M_2, M_4), injectors (M_5–M_8), and an output buffer. The input differential signal, $V_{inj,w+}$ and $V_{inj,w-}$, is applied to the injector through the DC blocking capacitor, C_{DC}. The DC input signal is generated by the center-tap generator, which is one of the reference bias circuits. V_{CT} is fixed at half of the supply voltage because the current flow in M_2 and M_4 are approximately same. The additional external control is not required, and the circuit is simplified because the center-tap generator is integrated. If the values of $V_{inj,DC}$ and V_{CT} are separated to control the DC, the capacitive coupling from the external node, such as RF pads and printed circuit boards (PCBs), will be stronger. Meanwhile, the size of the center-tap generator is greater than that of the core because it should not affect the operation of the core. The output signal is from the primary coil. Generally, the node of the secondary coil is connected to the output node in the mm-wave applications. However, the signal from the secondary coil is very small because the signal is induced by weak inductive coupling. If the output node is connected directly to the primary coil node, the resonant frequency can be lowered because the input capacitance is added. Therefore, C_1 should be determined by considering the input capacitance of the output buffer to obtain large power of the output signal and to obtain the desired resonance frequency. Table 1 lists the design parameters of the proposed CR-ILFM. As shown in Table 1, C_1 is 79 fF. The input capacitance of the output buffer is 26.3 fF, the effective primary resonator capacitance is 105.3 fF, and the coupling factor is designed to be 0.3.

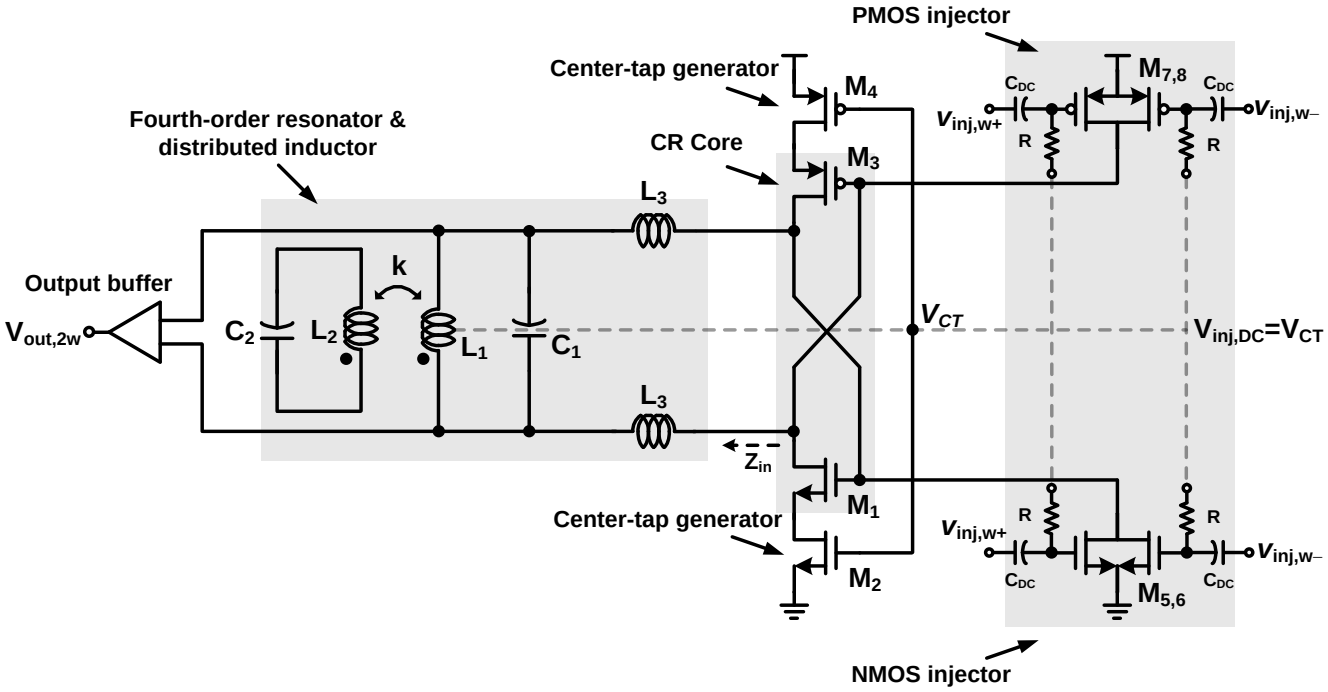


Figure 8. Schematic of the proposed current-reuse injection-locked frequency multiplier (CR-ILFM).

Table 1. Design parameters of the proposed current-reuse injection-locked frequency multiplier (CR-ILFM).

Design Parameter	Value
NMOS unit size (W/L)	2 mm/0.06 mm
PMOS unit size (W/L)	5 mm/0.06 mm
Finger of M_1, M_3	15
Finger of M_2, M_4	50
Finger of M_5–M_8	12
L_1	72 pH
L_2	151 pH
L_3	160 pH
k	0.3
C_1	79 fF
C_2	190 fF

3. Measurement Results

Figure 9 shows the measurement setup for the proposed CR-ILFM. The measurements were made using a power supply to bias the DC signal, signal generator for an input signal, signal analyzer for the output signal, and the probe station. In the probe station, the RF pads of the device under test (DUT) were connected using a ground-signal-ground (GSG) tip, and the RF cable was used to connect the device. The GSG tip and RF cable have a loss of approximately 2.5 dB and 3 dB, respectively. The above loss calibration is performed based on 28 GHz. An Anritsu's MG3694C (Atsugi, Kanagawa, Japan), which can generate signals from 1 Hz to 40 GHz, is used as signal generator, and a KEYSIGHY's N9030B (Keysight, Santa Rosa, CA, USA) which can analyze signals from 2 GHz to 50 GHz, is used as a signal analyzer. The power consumption of the proposed CR-ILFM core is 7.48 mW, and the output buffer consumes 2.9 mW from the 1 V power supply. This power consumption is analyzed when the CR-ILFM is operated at 28 GHz with a power of 0 dBm injection signal. As the input frequency decreases and the power of the input signal decreases, the power consumption of the CR-ILFM decreases slightly.

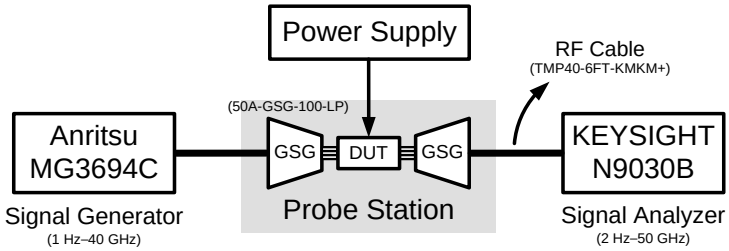
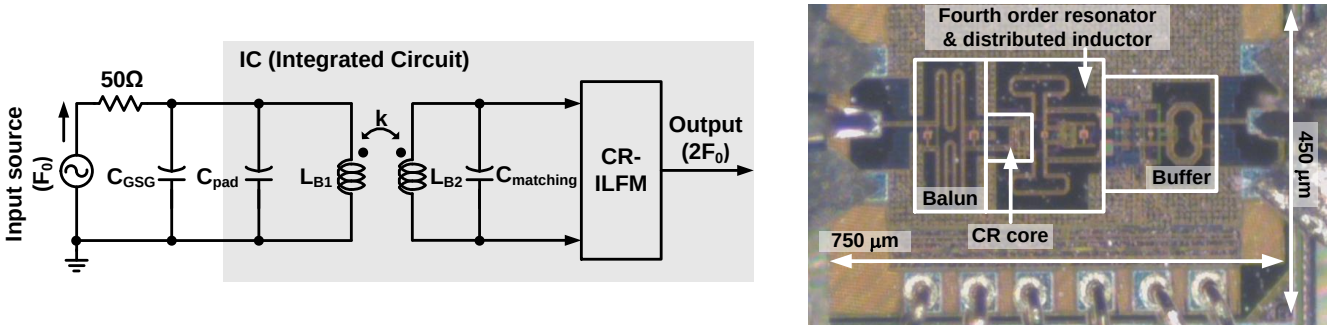


Figure 9. Measurement setup for the proposed CR-ILFM.

Figure 10a shows a schematic of the measurement environment of the overall CR-ILFM. The balun consists of L_{B1} and L_{B2} and is integrated with the CR-ILFM; C_{pad} is the parasitic capacitance of the GSG RF pads, which is very small. The input source and resistance of 50 Ω are the signal generator model; C_{GSG} is the parasitic capacitance of the GSG probe tip; $C_{matching}$ is used to move the self-resonance frequency, which induces a high impedance and can cause loss of input signals, to the unused frequency band. Figure 10b shows the die photograph of the proposed CR-ILFM, which includes the balun. The die size including RF pads and balun is 0.75 mm × 0.45 mm and the size of the core chip including the core, balun, and output buffer is 0.52 mm × 0.25 mm.



(**a**) (**b**)

Figure 10. (**a**) Modeling of the measurement environment of the overall CR-ILFM; (**b**) die photograph.

Figure 11a shows the simulated locking range of the ILFMs. The locking range of ILFM with second- and fourth-order resonator is 22–28.4 GHz and 20–28.8 GHz, respectively. However, there is an unlocking part between approximately 23 GHz and 25 GHz. The proposed ILFM has a locking range between 19 GHz and 35 GHz at an input signal power of 0 dBm. Figure 11b shows the simulated and measured (with 1-V supply voltage) locking range of the proposed CR-ILFM. From the figure, the simulated locking range is 19–35 GHz (59%). The measurement results show that the lower and higher operating frequencies are decreased by 1.2 GHz and 0.2 GHz, respectively, compared to the simulated results. The operating frequency decreased despite considering pressure-voltage-temperature (PVT) variations and the parasitic capacitance in the simulations owing to the parasitic components introduced by the probe station setup and wire bonding and various coupling effects in the PCB.

Figure 12a shows the measured output power of the proposed CR-ILFM when the 0-dBm input power is applied from 1-V supply voltage. The CR-ILFM has the highest output power at a free-running frequency of 24 GHz. The measured output power is calibrated values for 2.5-dB loss of RF cable and 3-dB loss of GSG pin. The measured phase noise is shown as Figure 12b. The phase noise of 12-GHz input signal is about 6 dB better than that of 24-GHz output signal of the CR-ILFM. It is very similar to the theoretical phase noise difference value. The phase noise of the output signal is −99.9 dBc/Hz at 100 kHz and −123.5 dBc/Hz at 1 MHz.

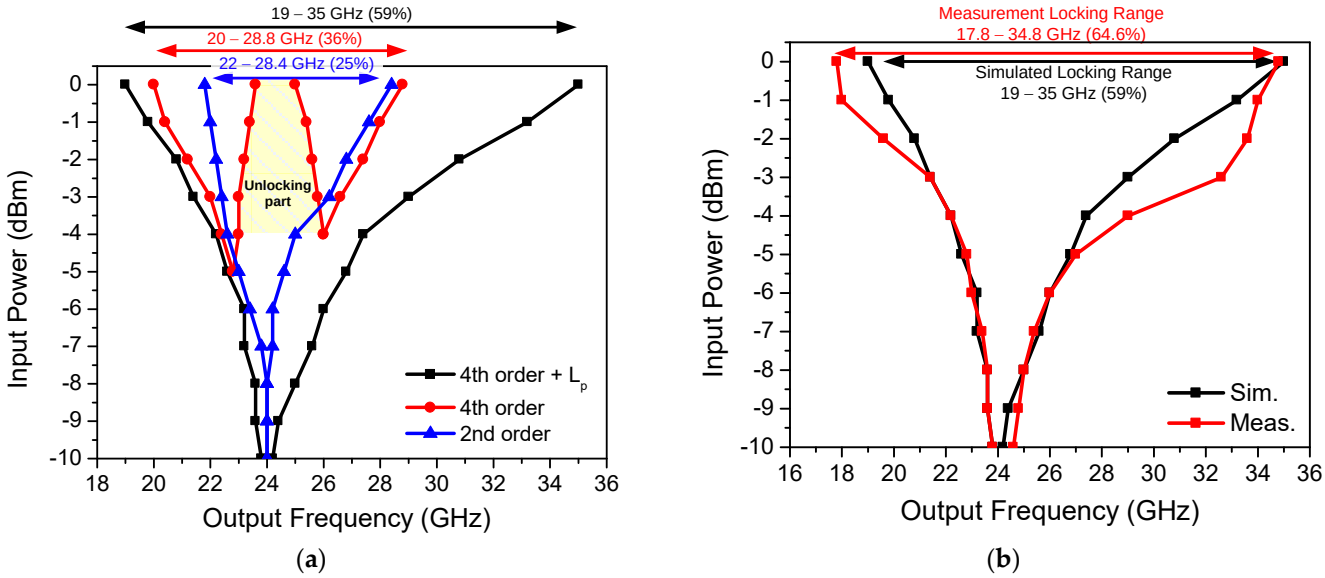


Figure 11. (**a**) Simulated locking range of the ILFMs; (**b**) comparison locking range between simulated and measured locking range of the proposed CR-ILFM.

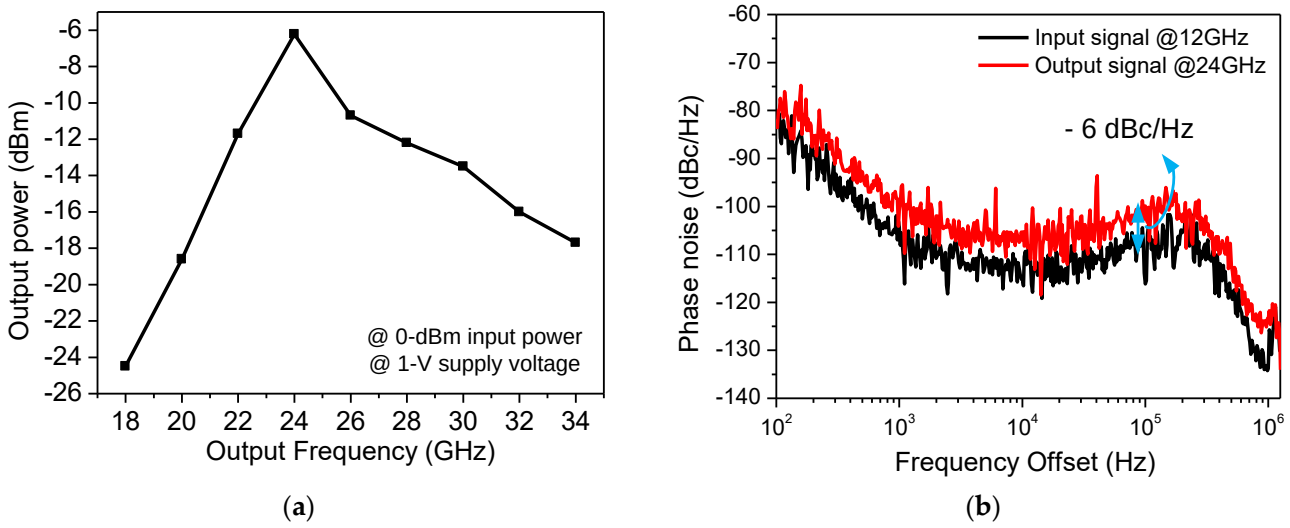


Figure 12. (**a**) Measured output power when the 0-dBm input power is applied and (**b**) measured phase noise.

Figure 13 shows the full-span spectrum of the output signal of the proposed CR-ILFM. The output power is −13.74 dBm and the free-running frequency is 23.82 GHz, and there are no harmonic components when the CR-ILFM self-oscillates as shown in Figure 13a. Figure 13b shows the full-span spectrum of the output signal when the CR-ILFM is locked at 24-GHz. In this case, the output power is −11.73 dBm, and the harmonic rejection ratio (HRR) between the desired signal and fundamental tone is approximately 25 dBc, and that of the third-order harmonic is 22 dBc. Figure 13c,d show the full-span output signal spectrums when the CR-ILFM is locked at the minimum and maximum frequency, respectively. The output powers are −31.17 dBm and −21.87 dBm. The HRRs are approximately greater than 10 dBc. The proposed CR-ILFM can be locked at the higher and lower frequency ranges, but the HRR will be reduced. Therefore, the locking range of the CR-ILFM is defined as 17.8 GHz to 34.8 GHz, with an HRR of approximately 10 dBc. All measured spectrum results are obtained with a 0 dBm input power applied from a 1 V supply voltage.

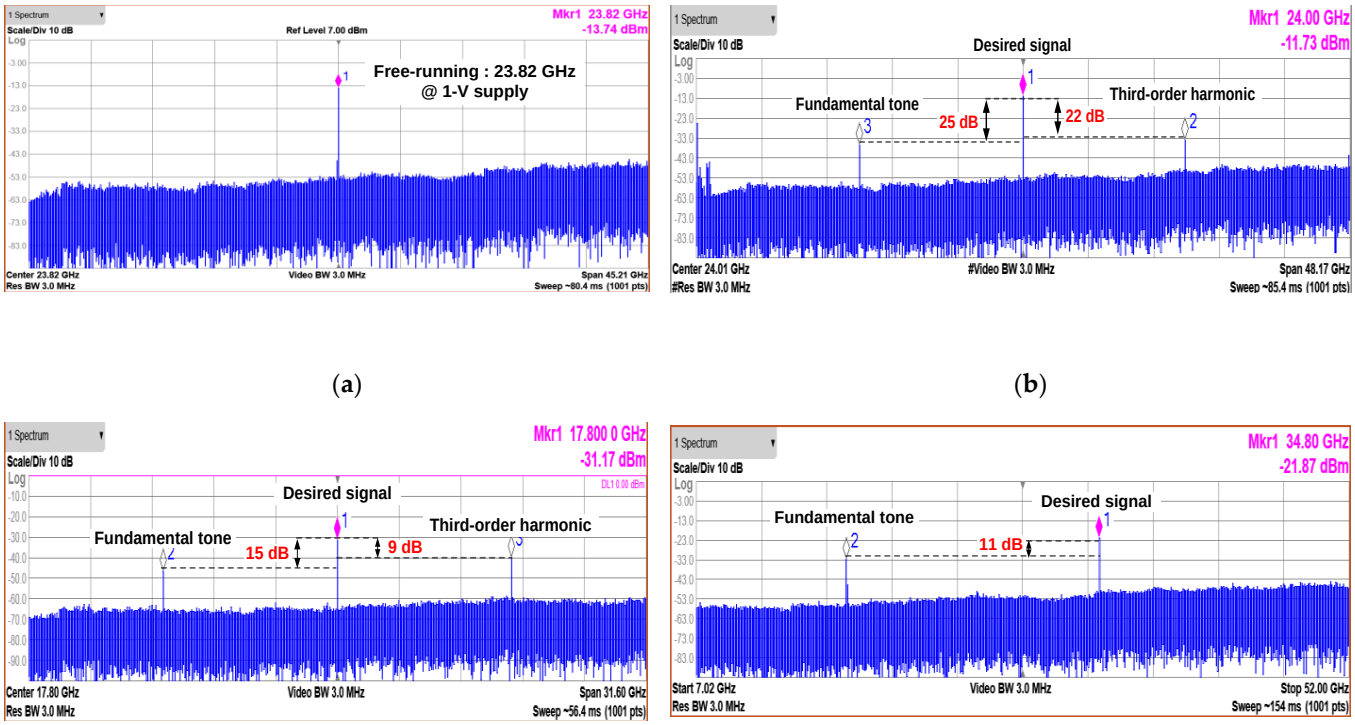


Figure 13. Full-span spectrum of the output signal of the proposed CR-ILFM. (**a**) Self-oscillation. (**b**) 24 GHz locking. (**c**) 17.8 GHz locking (minimum locking frequency). (**d**) 34.8 GHz locking (maximum locking frequency).

Table 2 presents the performance values of different mm-wave ILFMs. The CR-ILFM developed in this study has the widest locking range (64.6%) and highest figure of merit (FoM) values among the investigated ILFMs. Furthermore, the other ILFMs do not show full-span spectrums at the edge frequency of the locking range. Thus, HRR at the edge frequency of the locking range are unknown. Reference [18] is expected to output unwanted harmonic components at edge frequency of the locking range. In Reference [26], a reasonable locking range (53.1%) was obtained because a dual injector was used. Generally, the output power of ILFMs with a multiplication ratio of 2 or 2.5 [26,27] is larger than that of ILFMs with a multiplication ratio of 3 [11,25,28,29]. The ILFM developed in this study has the largest output power among the LC-based ILFMs investigated. An injection-locked ring-oscillator (ILRO) with several digital logic stages was previously developed [30]. Although ILRO has a large output power, owing to the several gain stages, it also has large power consumption.

Table 2. Performance comparison of mm-wave ILFMs.

		This Work	[18] 19′MTT	[26] 14′JSSC	[8] 18′JSSC	[11] 19′TCAS1	[27] 13′MTT	[28] 18′JSSC	[29] 08′MTT	[30] 19′JSSCL
Technology		65-nm CMOS	65-nm CMOS	65-nm CMOS	65-nm CMOS	130-nm CMOS	40-nm CMOS	130-nm CMOS	180-nm CMOS	28-nm CMOS
Core topology		CR-ILFM	ICB-ILFM	Sixth-order resonator-based ILFM	ILFM with frequency-tracking loop	HPS-ILFM	CR-ILFM	ILFM with frequency-tracking loop	Subharmonic ILFM	ILRO
Self-oscillation frequency (GHz)		23.82	-	28.1	29.25	24.44	50	30.1	26.49	-
Input signal power (dBm)		0	0	- **	-	0	–5	- **	4	–6
Output freq. locking range	GHz	17.8–34.8	22.8–43.2 ^	20.6–35.5	26.5–29.7	22.5–26.5	22.8–24.4	26.5–29.7	33.9–48.6	49.25–50.33
	%	64.6	61.8	53.1	11.4	14.8	12.7	11.4	35	6.1
Output signal power (dBm)		−6.23	−20	−14.49 ***	-	−17	−14.36 ***	−23.3 ***	−6.85	1
Phase noise (dBc/Hz)	At 100 kHz	−99.9@24 G	−94.7@28 G	−84.0@25.5 G	−92.6@29.3 G	−130@26.5 G	−110@24.45 G	−86.8@26.5 G	−122.5@39.6 G	-
	At 1 MHz	−123.5@24 G	−114.0@28 G	−112.4@25.5 G	−115.6@29.3 G	−132@26.5 G	−115@24.45 G	−106.8@26.5 G	−126.5@39.6 G	−117.7@49.8 G
Output phase type		Diff.	Diff.	Diff.	Quad.	Quad.	Diff.	Quad.	Diff.	Diff.
Supply voltage (V)		1	1.2	2.5	0.9–1.35	1.3	1.1	1.3	1.5	0.9
Total power consumption (mW)		10.38 (7.48 *)	14.8 (5.0 *)	21.8	24.3	10.4	(2.53 *)	49.7	2.95	34 (25 *)
FoM (%/mW)		6.22	4.18	2.44	0.47	1.22	2.41	0.23	5.02	1.4
Chip size (mm^2)		0.75 × 0.45	0.67 × 0.70	1.85 × 1.13 ^^	0.85 × 0.55	0.5 × 0.25 †	0.55 × 0.36	0.28 × 0.55 †	0.66 × 0.69	0.1 mm^2

FoM: Locking range/power consumption [%/mW]. *: Only core power consumption. **: On-chip PLL signal source. ***: Without loss calibration. ^: Phase noise degradation. ^^: Including multiple ILFM sizes. †: Only core size.

4. Conclusions

In this paper, the CR-ILFM with a 64.6% locking range is proposed. A dual injection technique is applied to generate balanced even harmonic components while decreasing the power of the fundamental tone and odd harmonic components. The CR core is adopted to reduce the power consumption and fit the proper interface with the NMOS and PMOS injectors. The proposed CR-ILFM core dissipates 7.48 mW from a 1-V supply voltage. The fourth-order resonator with distributed inductor is proposed to widen the locking range. The output frequency locking range is determined to be 17.8–34.8 GHz (64.6%) when a 0-dBm input power is applied. The proposed CR-ILFM does not require additional control components, such as varactors and external bias circuits. The die size is 0.75 mm × 0.45 mm, and the CR-ILFM is implemented in a 65-nm CMOS technology.

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