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Comparison of Total Ionizing Dose Effects in 22-nm and 28-nm FD SOI Technologies

Zongru Li *, Christopher Jarrett Elash, Chen Jin, Li Chen, Jiesi Xing, Zhiwu Yang and Shuting Shi

Department of Electrical & Computer Engineering, University of Saskatchewan, Saskatoon, SK S7N 5A9, Canada; chris.elash@usask.ca (C.J.E.); chj482@usask.ca (C.J.); li.chen@usask.ca (L.C.); jiesi.xing@usask.ca (J.X.); zhy606@usask.ca (Z.Y.); shs085@usask.ca (S.S.)

* Correspondence: zol668@usask.ca

Abstract: Total ionizing dose (TID) effects from Co-60 gamma ray and heavy ion irradiation were studied at the 22-nm FD SOI technology node and compared with the testing results from the 28-nm FD SOI technology. Ring oscillators (RO) designed with inverters, NAND2, and NOR2 gates were used to observe the output frequency drift and current draw. Experimental results show a noticeable increased device current draw and decreases in RO frequencies where NOR2 ROs have the most degradation. As well, the functionality of a 256 kb SRAM block and shift-register chains were evaluated during C0-60 irradiation. SRAM functionality deteriorated at 325 krad(Si) of the total dosage, while the FF chains remained functional up to 1 Mrad(Si). Overall, the 22-nm FD SOI results show better resilience to TID effects compared to the 28-nm FD SOI technology node.

Keywords: 22-nm FD SOI; 28-nm FD SOI; Co-60; flip-flop (FF); heavy ion; radiation effects; ring oscillator (RO); static random-access memory (SRAM); total ionizing dose (TID)

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1. Introduction

Integrated circuits (ICs) can experience various functionality issues when subjected to prolonged doses of radiation. These effects are often a reliability concern in long-term space missions where devices can spend years exposed to constant sources of radiation. Total ionizing dose (TID) effects in ICs can result in changes to gate propagation delays, leakage currents, and even loss of device functionality [1]. When ICs are exposed to ionizing radiation, positive charges are accumulated within the gate oxide and field oxide layers, thus resulting in less gate control of the device and an increased leakage current [2]. For PMOS transistors, the result of these charges can result in the device failing to turn on, whereas NMOS transistors become difficult to turn off [1,2]. The mechanisms of TID effects in bulk technologies are often simpler due to the inclusion of only one gate oxide layer; however, fully depleted silicon on insulator (FD SOI) technologies feature a more complex response to TID effects [3].

Transistors in the latest FD SOI technologies are fabricated on a very thin silicon (Si) layer over a buried oxide layer (BOX). With each transistor fabricated on a Si Island and isolated from other transistors by the BOX layer, the volume of active Si is minimal for each transistor. This allows for superior gate control over the channel region while reducing nodal capacitances, which yields faster logic gate switching times over those for bulk technologies. However, because FD SOI technologies have an additional parasitic structure due to the BOX layer, effects due to TID are more complex than bulk devices [4–9]. The BOX layer introduces a two-dimensional coupling effect between the front and back interfaces of the channel. This doubled coupling becomes a critical contribution to the ionizing dose response of FD SOI devices. In this case, FD SOI technologies tend to be more sensitive to TID than their bulk counterparts [10,11]. This is important to note due to the attractiveness of FD SOI technologies for use in space missions because of the technologies' inherent resilience to particle-induced single event effects (SEEs) [3,9]. There are already some

experimental results from previous research on TID effects in the 28-nm FD SOI technology node [2,9]. These results show that a TID-induced gate delay increased significantly in that technology node, as well as leakage currents which impose barriers for it to be used for some space applications where tolerance to high total absorbed dose levels is required. Therefore, it is essential to investigate TID effects in the 22-nm FD SOI technology node and compare them with the results from the 28-nm FD SOI technology node.

To evaluate TID effects, a 22-nm FD SOI test chip was designed and fabricated. Ring oscillators (ROs), flip-flop (FF) chains, and a static random access memory (SRAM) block were chosen as the testing vehicles for evaluating the technology's susceptibility to TID effects; including both Co-60 and heavy ions irradiation sources [12]. RO circuits can offer insights into gate delays due to changes in the frequency of the circuits, as well as changes in power consumption as dosage increases. The FF chains and the SRAM block can be used to offer a broad perspective on device functionality. A similar test chip with 28-nm FD SOI technology was also fabricated previously, and the results from that test chip will be used in this paper for comparison purposes between the two technologies [9].

The organization of the rest of this paper is as follows. In Section 2, details of the test circuits are introduced. In Section 3, details of the test chip design and experimental setup are described. In Section 4, the experimental results will be presented and discussed. Lastly, conclusions are drawn in Section 5.

2. Description of Test Circuits

2.1. Ring Oscillators

Individual transistors are the ideal test vehicles for evaluating TID effects; however, there are many challenges regarding fabrication and testing. Additional design procedures are necessary to avoid the antenna effects during fabrication, leading to additional measurement errors. As explained by [13], measuring the change in the delay of a single transistor is difficult in practice, and can severely skew the results if the transistor has large variations in fabrication. Instead, ring oscillator (RO) circuits use the average parameter values of all transistors in the circuit, and as such, are well suited for the TID characterization of circuit-level parameters such as gate delay and power usage [8,14,15]. The use of averaged measurements allows for averaging statistical variations between individual gate parameters, thus ensuring that statistical variations between individual transistors in the RO circuit are incorporated into the overall RO characteristics [8]. Additionally, since ROs are often used for clock generation sources, it is important to understand how their performance can change as the dosage of ionizing radiation increases.

RO circuits are designed using an odd number of logic gates connected in a loop, which results in an unstable circuit oscillating at a fixed frequency. The oscillating frequency depends on the number of stages in the loop. The RO frequency is determined by the following equation:

$$f = \frac{1}{2 \times n \times t} \tag{1}$$

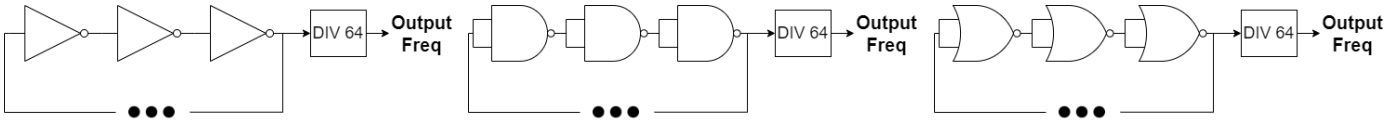
where f is the RO frequency, n is the number of stages in the RO loop, and t is the average delay of each RO stage. The equation for a single inverter delay is given below:

$$Delay_{inv} = \frac{C_L \times V_{DD}}{\frac{W}{L} \times \mu \times C_{ox} \times (V_{DD} - V_{th})^2} \tag{2}$$

where C_L is the load capacitance, V_{DD} is the supply voltage, W and L are the width and length of the gate, μ is the carrier mobility, C_{ox} is the capacitance of the oxide layer, and V_{th} is the gate threshold voltage [16]. TID effects will alter both the mobility and the threshold of the device, which will thus result in a measurable difference in the delay of the gate, and therefore the frequency of the oscillator.

A variety of different ROs were constructed with 2-input NAND (NAND2) gates, 2-input NOR (NOR2) gates, and inverters, as shown in Figure 1. For each type of gate,

multiple ROs were designed, each with a different number of gates to achieve different oscillating frequencies. It should be noted that they were designed based on the cells from the standard cell library without any special layout design techniques. The inverter ROs included four different frequency options, and the NAND2 ROs and NOR2 ROs both had three different frequency options. Tables 1–3 show the ROs' expected oscillation frequencies normalized to their respective fastest oscillation frequency as measured by post-layout simulations from the foundry supplied process design kit (PDK).



(**a**) (**b**) (**c**)

Figure 1. Three different RO designs: (**a**) Inverter-based RO design; (**b**) NAND2-based RO design; (**c**) NOR2-based RO design.

Table 1. Inverter-based programmable RO simulation results.

Delay Block	Number of Delay Stages	Output Frequency (n.u.)
S0	21	1.00
S1	29	0.77
S2	45	0.57
S3	69	0.36

Table 2. NAND-based programmable RO simulation results.

Delay Block	Number of Delay Stages	Output Frequency (n.u.)
S0	13	1.00
S1	23	0.68
S2	49	0.39

Table 3. NOR-based programmable RO simulation results.

Delay Block	Number of Delay Stages	Output Frequency (n.u.)
S0	13	1.00
S1	23	0.68
S2	49	0.38

The output of oscillators for each respective gate was connected to a multiplexer and a frequency divider circuit, as shown in Figure 2. The inclusion of the divider was needed as the high frequencies of the oscillators were not able to be directly captured by the chip's IO pads, which are limited to 50 MHz. A reference RO used for comparison purposes was previously fabricated in the 28-nm FD SOI technology node. It was constructed with 44-stage inverters and a nominal oscillating frequency of 1 GHz.

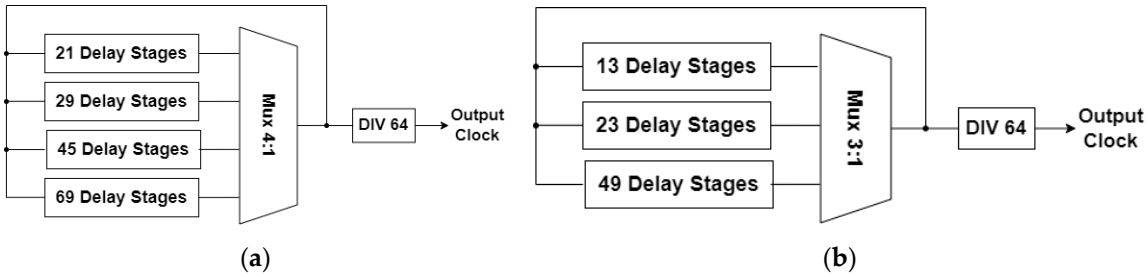


Figure 2. Schematic designs of different gate-based ROs: (**a**) Inverter-based RO schematic design; (**b**) NAND2 or NOR2-gate-based RO schematic design.

2.2. Flip-Flop Chains

The designed FF block included 14 different FF chains, which were comprised of a conventional master-slave transmission gate FF and 13 different radiation-hardened FF designs. The FFs were connected as shift register chains with 12,000 stages in each chain. The shift registers were clocked through an external clock signal and received input data via an IO pad. The reversed clock scheme was used to help avoid hold-time violations, as shown in Figure 3. While the power draw of each FF chain is slightly different due to the inherent design differences, together they offer an appropriate testing platform for determining changes in IC power usage as the dose rate increases, as well as changes in device functionality.

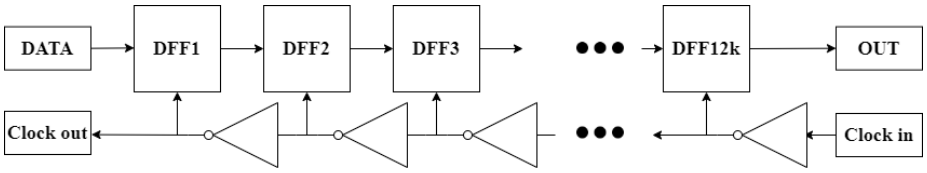
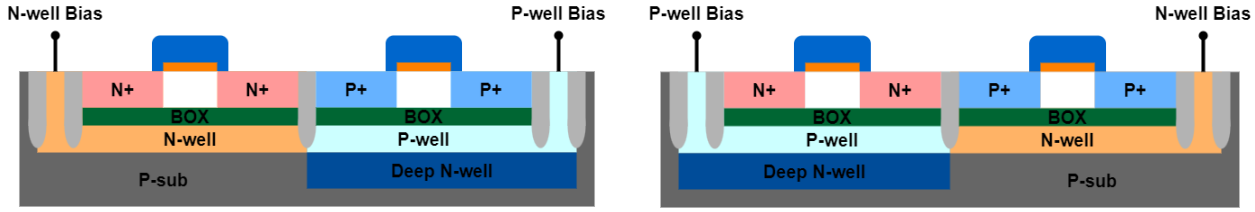


Figure 3. Flip-flop chain and the clock data flow for the shift register design.

2.3. SRAM Block

A forward body bias (FBB) transistor configuration was chosen for the SRAM array, as shown in Figure 4a. The FBB transistor configuration allows for higher drive and lower threshold voltages, whereas the conventional reverse body bias (RBB) configuration, shown in Figure 4b, can limit leakage currents by increasing the threshold voltage of the device. Traditionally, SOI technologies were prone to TID-induced leakage currents causing operational failures [17]. However, recent FD SOI technologies, such as 28-nm and 22-nm, have shown a significantly higher tolerance for TID exposures with limited increases in leakage currents, especially when the total absorbed dose is within 100 krad(Si) [18]. In this case, the usage of the RBB configuration to limit the operational performance of ICs was not as appealing as before. Instead, the usage of the FBB configuration to improve the performance of an IC design has become more valuable than the traditional RBB configuration. To investigate TID effects on an SRAM with FBB configuration, a 256 kbit SRAM block was designed with a memory compiler. The SRAM block featured a 15-bit address line, an 8-bit data line, as well as a read/write enable and clock input. It was a single-port SRAM configured as 32 K $\times$ 8 memory with 256-cells on a bit-line. It included additional features such as bit-line redundancy, a pipeline mode, and power-gating. Inside of the SRAM design, it included cell arrays and various peripheral circuits such as row/column decoders, self-timing generators, sense amplifiers, and buffers. As SRAMs are commonly used in circuit designs, it is important to evaluate their performance under TID effects.



(**a**) (**b**)

Figure 4. (**a**) Flipped well configuration (FBB); (**b**) regular well configuration (RBB).

3. Test Chip Design

A test chip consisting of the three types of circuits previously discussed was developed and fabricated in a commercial 22-nm FD SOI technology, as shown in Figure 5. All FF chains shared the same data input. The outputs of the SRAM block and FF chains were connected to the IO pads for external error detection, and the outputs of the RO circuits were connected to the IO pads for the frequency measurements. The nominal core logic supply voltage for this technology was 0.8 V, and the IO voltage was 1.8 V. Functional verification testing was carried out on the fabricated SRAM and FF chains with all 0s, 1s, and checker-board input patterns before irradiation.

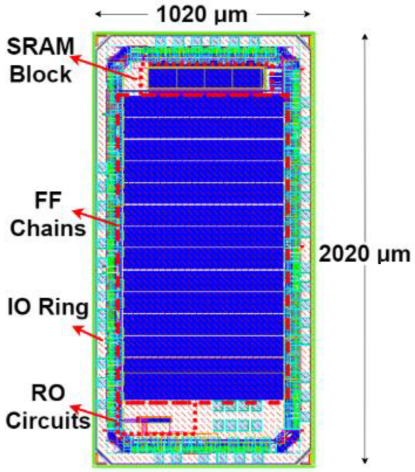


Figure 5. Test chip overall layout.

A testing system consisting of power supplies, an FPGA board, and a microcontroller used during testing. The test chip was soldered onto a custom-made daughter board and was connected to the FPGA via a DIMM connection. During testing, the FFs, SRAM, and ROs were powered at their nominal voltage of 0.8 V. The FF chains were clocked at 1 MHz with the 'all 0' data input pattern, and current readings were taken from the power supplies every minute. The SRAM block was also clocked at 1 MHz, and a checker-board data pattern was used. At the beginning of testing, all addresses in the SRAM were written with the test data. Then, the content of the SRAM was continually read out to check if the data were still appropriately stored. If there was a mismatch in data, the system would record the event and attempt to repair the address with the correct test data, and the process would continue. If the address data could not be repaired, then that address location was considered non-functional and recorded.

During testing, the ROs were also powered at their nominal voltage of 0.8 V. The output pins of the ROs were connected to counters inside the FPGA and monitored the number of oscillations of each RO within a 0.1 s period. By knowing the number of oscillations for a given period, the frequency of each RO was able to be determined. During testing, all collected data on the FPGA were transferred to a microcontroller via a serial connection,

where the data were logged and recorded so that testing personnel could evaluate the experimental data in real-time.

4. TID Experimental Results and Discussions

The TID experiments were performed by using a Gammacell 220 Co-60 chamber (Figure 6) at the University of Saskatchewan, Saskatoon, SK, Canada. The Gammacell 220 chamber can provide an irradiation rate of 108.2 rad(Si) per minute. The total absorbed dose during the experiments was 1 Mrad.

Figure 6. Gammacell 220 Co-60 Irradiator.

The frequencies of the ROs were recorded during the TID testing and plotted in Figure 7. It should be noted that the observed experimental data are a linear trend, so a first-order polynomial curve fitting was implemented to understand this trend better. It is interesting to note that the ROs with the same gate type experienced the same decreasing rate in their output frequency during testing. This can simply be attributed to the same gate delay degradation during TID testing.

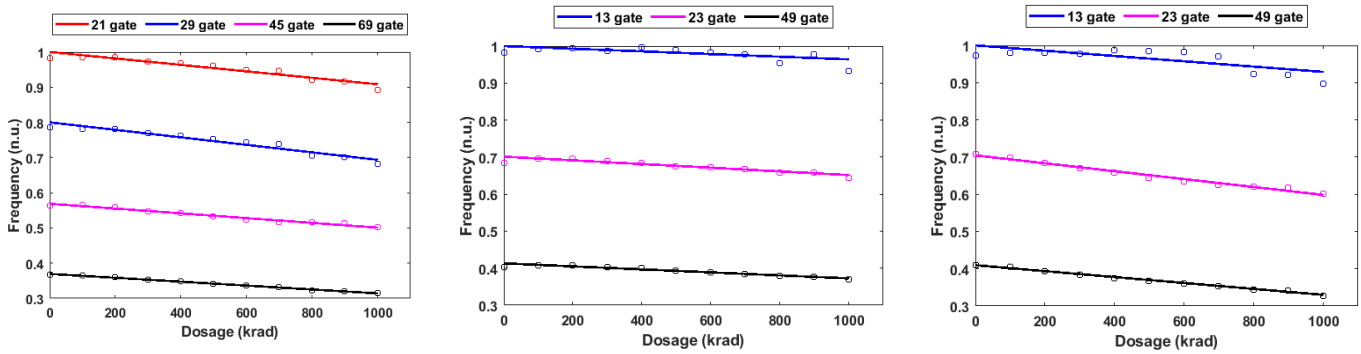


Figure 7. RO frequencies vs. total absorbed dose during Co-60 test: (**a**) Inverter-based ROs; (**b**) NAND2-based ROs; (**c**) NOR2-based ROs.

The relative change in frequency was calculated from the ROs designed with inverters, NAND2, and NOR2 gates and listed in Table 4. For the inverter-based RO, the relative decrease in frequency was the average of the drops in four different stage options; for the NAND2 and NOR2-based ROs, the average value of the drops in three different stage options was used to calculate the relative decrease in frequency. From the results, a trend emerged showing that ROs built using different gates were impacted by TID effects at differing rates.

Table 4. RO frequency differences from 0 krad(Si) of exposure to 1000 krad(Si) during Co-60 test.

RO Type	Relative Decrease in Frequency
Inverter	−12.3%
NAND2	−6.8%
NOR2	−14.1%

Table 4 shows that the frequencies of the NAND2 ROs were least affected by the TID, whereas the NOR2 ROs were most affected. It is noted that the NAND2 gates have two NMOS transistors in series and two PMOS in parallel, whereas the NOR2 gates have two PMOS transistors in series and two NMOS in parallel. The sizing of the NMOS and PMOS network of the NAND2 and NOR2 gates used in the ROs was designed such that the rising and falling time were roughly equal. In general, the positive charge trapped in the BOX under the transistors due to TID irradiation results in a negative shift of the threshold voltage, which leads to an increased driving current of the NMOS transistor and reduced driving current for the PMOS transistors in the gates. Findings in [2] show that the PMOS driving current is significantly reduced compared to the increase in the NMOS driving current in 28-nm FD SOI technology, which leads to the monotonic decrease in the frequency with the irradiation dose. The experimental results in this paper also show the same trends. The results of the NAND2 and NOR2 ROs further validate this since NOR2 has two PMOS transistors in series, which further degrades the delay of the gate, and hence reduces the frequency of the ROs.

TID testing with heavy ion irradiation was conducted at the Texas A&M University (TAMU) Cyclotron Institute. An irradiation rate of 60.9 rad(Si) per second was provided. Figure 8 shows the change of the frequencies as the increase in the heavy ions TID exposure for the inverter-based RO (45 stages), NAND2-based RO (23 stages), and NOR2-based RO (23 stages). The results still show that the NOR2 RO has the largest frequency degradation, while the NAND2 RO has the least, which was demonstrated from the previous analysis. In addition, it can be observed that the degradation of the RO frequency from the Co-60 test is much more than the heavy ion test. Despite the use of the High-K dielectric gates in advanced technologies, which can help to reduce the radiation-induced voltage shift in the gate insulator, the radiation-induced charge in SOI buried oxides and shallow trench isolation oxide (STI) can cause degradation or failures as well [19]. Electron-hole pairs are generated in the oxide layers when applying high-energy ionizing radiation, but most holes and electrons can immediately recombine. For high LET particles, such as heavy ions, they generate high-density charge pairs, making the initial recombination rate significantly large. The charge pair line density is relatively small for the low LET particles, such as Co-60, which reduces the initial recombination rate. Compared to the heavy ions, the Co-60 has a better ability and efficiency to create the trapped charges in oxide layers [9], as reported in [20,21], respectively.

Another inverter-based RO in 28-nm technology was used for comparison. There are 45 stages in the 28-nm RO, and 44 of them are also used as delay stages contributing to other designs. A multiplexer was used to switch between these two modes, as shown in Figure 9. When the select input is high, the design will work as an RO. The 28-nm RO was also based on the conventional inverter without any layout optimizing techniques, which is the same as the 22-nm design, making these two designs fully comparable. The frequency versus total dose for two inverter-based ROs (45 stages and 69 stages, respectively) in the 28-nm and 22-nm FD SOI technologies are plotted in Figure 10. These results show that during the Co-60 test at 850 krad(Si) of dosage, the 28-nm RO had a frequency decrease of over 30% from the initial, compared to the 14.5% decrease in 22-nm RO. During the heavy ion test, at 200 krad(Si) of dosage, the 28-nm RO had a frequency decrease of around 1.8% from the initial, compared to a less than 0.5% decrease in the 22-nm RO. These results show that the degradation in frequency for the 22-nm inverter-based RO has significantly improved. This indicates that the PMOS driving current is less affected by the TID effects for the 22-nm

technology node, which could be due to manufacturing improvements. It is known that a thinner SiO_2 BOX layer can lead to a milder TID effect [18,22]. The thicknesses of the BOX and the SOI body of the 28-nm FD SOI technology are 25-nm and 7-nm [23], and those are 20-nm and 6-nm in the 22-nm FD SOI technology node, respectively [24]. The BOX of the 22-nm process is 25% thinner than that of the 28-nm process, so a less positive charge will be deposited in the BOX of the 22-nm process during irradiation. This will cause less interference with the threshold voltage of the 22-nm process, eventually leading to better resilience to TID effects.

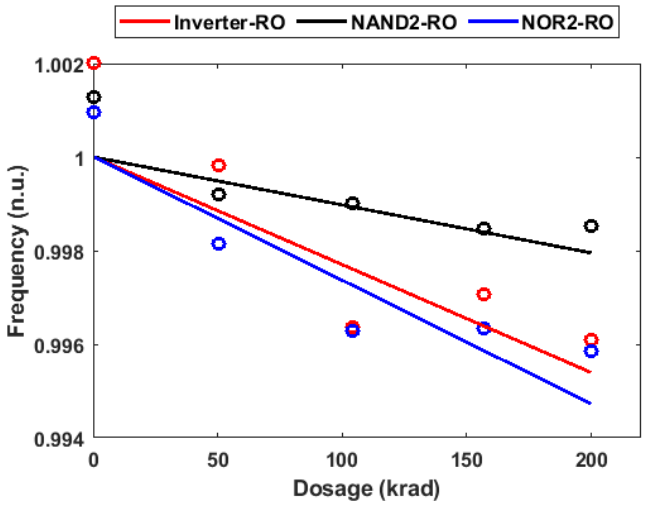


Figure 8. RO frequencies vs. total absorbed dose during heavy ion test.

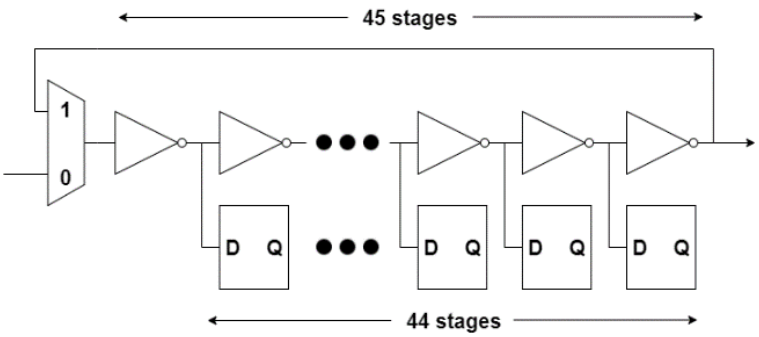


Figure 9. Schematic of the 28-nm RO design.

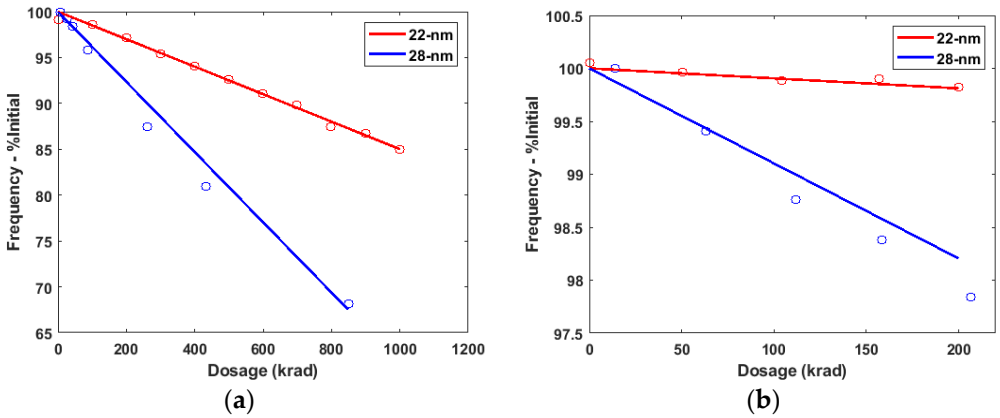


Figure 10. RO frequencies from 22-nm and 28-nm test for (**a**) Co-60 test; (**b**) heavy ion test.

Figure 11 shows the change in power supply current as the TID exposure increased for both 22-nm and 28-nm test circuits for Co-60 irradiation. Both of the plots are normalized. The current of 22-nm influenced by cumulative TID exposure is very similar to that of the 28-nm test. However, the current of the 22-nm test increased by approximately 18 times after 800 krad(Si) dosage compared to the initial starting current, while the 28-nm showed a 10 times increase. The increase in driving and leakage currents in the transistors can explain this increase in the current draw as the dose rate increases. These data show that TID effects are still prominent in the 22-nm FD SOI node. In addition, in the 22-nm technology node, the increase in the leakage current shows a linear trend from low doses to high doses.

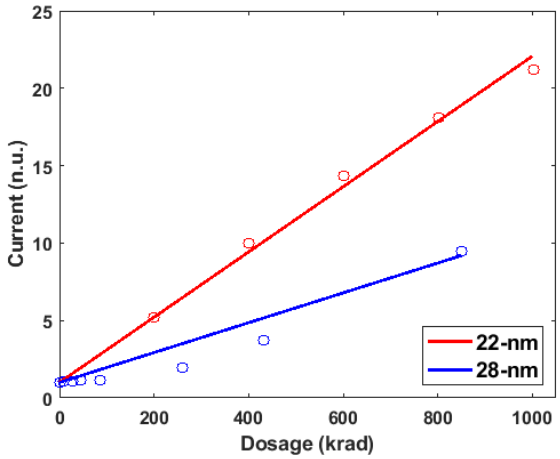


Figure 11. Current from 22-nm and 28-nm tests during Co-60 test.

The SRAM operated normally during testing until its functionality deteriorated at 325 krad(Si) of the total dosage. At this point, the number of recorded errors increased drastically, and every address showed a loss in functionality by 332 krad(Si) of the total dosage. A series of troubleshooting tests were performed to try and return functionality back to the SRAM block. These included resetting the test program, power cycling the SRAM, and clocking the SRAM at a slower rate of 100 kHz. None of these methods yielded any results, and the SRAM block was presumed dead. The FFs were still functional after the 1000 krad(Si) total absorbed dose, and no error was observed on any of the FF chains. In this case, it is believed that the SRAM storage cells themselves did not fail at 325 krad(Si), but instead, some part of the peripheral circuitry became damaged. For example, the internal operation of the SRAM block is controlled by a self-timing, asynchronous circuit, which could fail due to the increased delay, and this would explain why the entirety of the SRAM block failed at the same time instead of a more gradual loss in functionality. In this case, this timing issue caused by TID should be taken into account when designing the memory. For example, the self-timing circuit in the SRAM should be designed to be tolerant of the additional delay induced by the TID. Another method is to apply the back-gate voltage to the peripheral circuitry. When applying the back-gate voltage to circuits in the flipped well configuration, the drive current will be enhanced, and the delay will be reduced, which should effectively mitigate the TID effect in the peripheral circuitry.

5. Conclusions

Three types of RO circuits were designed and fabricated to evaluate the effects of frequency and leakage currents while exposed to gamma radiation. Results were compared with the previous 28-nm FD SOI node, and they show that the 22-nm FD SOI node had less frequency degradation compared to the 28-nm node. Among the three types of ROs, all showed degradations due to the TID, but the NOR ROs yielded a worse performance than that of the inverter ROs and NAND ROs due to the significantly reduced driving current in PMOS transistors during TID testing. The reduction rate of the RO frequency during the Co-60 was much higher than that of the HI test. The power supply current increased

as the dosage increased similarly to that of the 28-nm node. The SRAM failed when the cumulated dose reached 325 krad(Si), but the FF chains were still functional through the test up to 1000 krad(Si). These results indicate that additional attention must be paid when designing complex circuits for radiation-hardened applications.

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