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TAISAM: A Transistor Array-Based Test Method for Characterizing Heavy Ion-Induced Sensitive Areas in Semiconductor Materials

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Abstract: The heavy ion-induced sensitive area is an essential parameter for space application integrated circuits. Circuit Designers need it to evaluate and mitigate heavy ion-induced soft errors. However, it is hard to measure this parameter due to the lack of test structures and methods. In this paper, a test method called TAISAM was proposed to measure the heavy ion-induced sensitive area. TAISAM circuits were irradiated under the heavy ions. The measured sensitive areas are 1.75 μm^2 and 1.00 μm^2 with different LET values. TAISAM circuits are also used to investigate the layout structures that can affect the sensitive area. When the source region of the target transistor is floating, the heavy ion-induced sensitive area decreases by 28.5% for the target PMOS transistor while it increases by more than 28% for the target NMOS transistor. When the well contacts are added, the heavy ion-induced sensitive area decreases by more than 25% for the target PMOS transistor while it remains unchanged for the target NMOS transistor. Experimental results directly validate that the two structures significantly affect the heavy ion-induced sensitive area.

Keywords: radiation effect; radiation test method; heavy ion; sensitive area; parasitic bipolar amplification

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1. Introduction

When a high energy incident particle strikes a semiconductordevice, it interacts with the semiconductor material and loses energy along its incident path [1,2]. The lost energy transfers to the semiconductor atoms and ionizes electron–hole pairs [3]. These ionized electron–hole pairs move into the entire semiconductor device due to drift and diffusion. Transistors collect the ionized electron–hole pairs, which produce unwanted transient currents in circuit nodes [4,5]. These transient currents propagate along the circuit path and produce soft errors according to the circuit responses [6]. They may result in serious consequences to the entire chip, system, or even a spacecraft [7]. The heavy ion-induced sensitive area is an essential parameter for space-application integrated circuits. It is useful to evaluate and mitigate the soft errors. For instance, the multiple-node charge collection effect significantly increases heavy ion-induced soft errors [8,9]. Increasing the distance between transistors in layout is a useful hardening method for mitigating soft errors induced by this effect [10–12]. However, due to the lack of heavy ion-induced sensitive area data, it is difficult for circuit designers to determine the required increased distance. Some previous works have reported standard cell-based test circuits to indirectly investigate the heavy ion-induced sensitive area [13,14]. However, it is hard to accurately obtain the sensitive area data due to the large layout area of standard cells. Therefore, it is necessary to propose novel test methods that can directly measure the heavy ion-indued sensitive area. In this paper, a special test method called Transistor Array-based Ion Sensitive Area Measurement (TAISAM) is presented to directly measure the heavy ion-induced sensitive

area. The test principle is similar with the SRAM-based measurement [15]. A transistor array is used to quantify the transistors that are struck by heavy ions. Then, the heavy ion-induced sensitive area is calculated by multiplying the equivalent area of each transistor test chip that contains TAISAM circuits that were designed and fabricated by the commercial 65 nm bulk CMOS technology, irradiated under the heavy ions. The heavy ion-induced sensitive areas are reported and discussed based on the experimental results.

2. TAISAM Test Structure

The basic TAISAM cell topology is shown in Figure 1. It consists of a conventional D flip-flop and a target transistor (PMOS or NMOS). The gate of the target transistor is fixed to a constant voltage to switch off the transistor. The gate voltage is connected to power for target PMOS transistor while it is connected to the ground for a target NMOS transistor. The drain region of the target transistor is connected to the D flip-flop, and the source region of the target transistor is connected to power or ground. Due to the special connection of test circuits, the stored value of D flip-flops determines the heavy ion sensitivity of target transistors. For instance, when the stored value of D flip-flops is zero, the drain voltage of target PMOS transistor is also zero. The drain voltage is lower than the gate/source voltage and the ionized electron–hole pairs can be collected by target PMOS transistor. Therefore, the target PMOS transistors are sensitive to heavy ions. Otherwise, when the stored value of D flip-flops is one, the drain voltage of target PMOS transistor is also one. The drain voltage is equal to the gate/source voltage and the ionized electron–hole pairs cannot be collected by PMOS transistor; thus, the target PMOS transistors are insensitive to heavy ions.

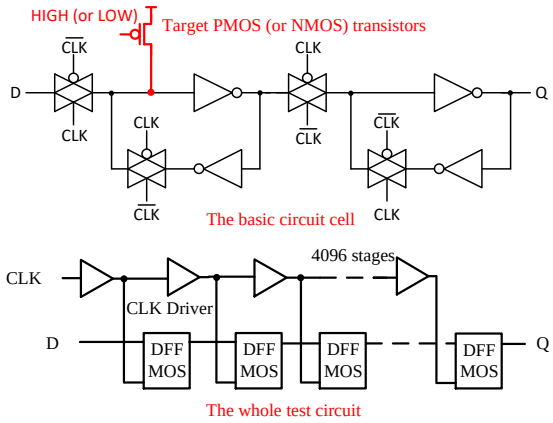

Figure 1. The basic TAISAM cell contains a flip-flop and a target transistor. Several TAISAM cells consist of an entire test circuit.

Four thousand and ninety-six stage basic cells are used to constitute a shift register circuit. All target transistors are placed uniformly and side-by-side to constitute a 256 × 16 transistor arrays, as shown in Figure 2. The target transistor arrays and the D flip-flops are placed separately to make sure a heavy ion only strikes the transistor arrays or the D flip-flops each time. If a heavy ion strikes the center region of the transistor arrays, transistors inside the heavy ion-induced sensitive area collect the ionized electron–hole pairs and produce transient currents at the storage node of D flip-flops simultaneously. If the number of collected electron–hole pairs is larger than the critical charge of D flip-flops, the initial value would be changed by transient currents. It causes single-event upset (SEU) effect. Then, the changed values shift to the outputs of the circuit. The number of transistors which inside the heavy ion-induced sensitive area is determined by counting the changed values on the output port of the test circuit. Based on the number of SEU, the heavy ion-induced sensitive area is calculated by the following equation:

$$S_{ion} = N_{\max} \times S_{transistor} \quad (1)$$

where $N_{\max}$ is the maximum number of SEU. $S_{transistor}$ is the equivalent area of each transistor. Note that both D flip-flops and target PMOS transistors are sensitive to heavy ions. It may cause SEUs when a heavy ion strikes the D flip-flop layout or the transistor array layout. Due to the large layout area of one D flip-flop, the number of SEUs is lower than that when a heavy ion hits the transistor array. When a heavy ion strikes the transistor array, there are two situations. If the heavy ion strikes the edge of transistor array, it does not fully reveal the heavy ion-indued sensitive area. The number of SEU is smaller than when a heavy ion strikes the center of the transistor array. Therefore, the maximum number of SEU represents a heavy ion hit the center of the transistor array. The heavy ion-induced sensitive area is calculated by the maximum number of SEU.

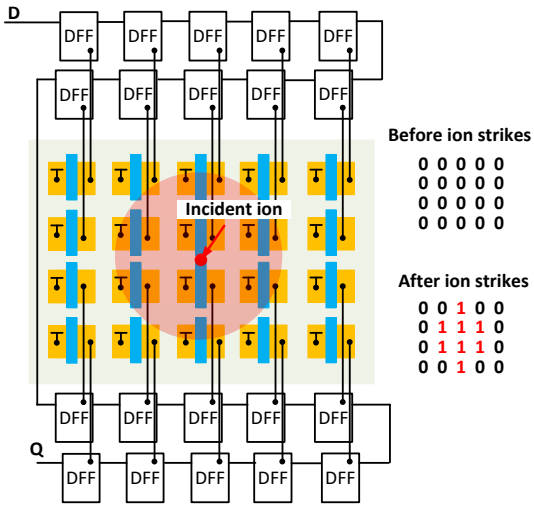

Figure 2. The layout schematic of a TAISAM circuit. The transistor array is placed in the center region and the flip-flops are placed beside the transistor array.

In addition to obtaining a statistical value of the heavy ion-induced sensitive area, TAISAM is also able to draw planar maps of the heavy ion-induced sensitive area. For instance, the diameter of the heavy ion-induced sensitive area in the horizontal and vertical directions can be evaluated by the output data after one ion striking, as shown in Figure 3. Moreover, TAISAM can also map the heavy ion-induced sensitive areas with different critical charge values. Since the target transistor-induced SEU is dependent on the critical charge of the D flip-flop, it can adjust the critical charge values to obtain different heavy ion-induced sensitive areas. According to these measured results, the entire heavy ion-induced sensitive area with different charge values can be determined.

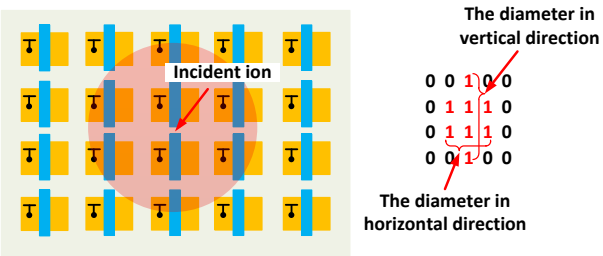

Figure 3. TAISAM can be used to determine the diameter of the ion-induced sensitive area.

3. Test Chip Design and Experimental Setup

A test chip layout was designed by the commercial 65 nm bulk CMOS technology. It consisted of six TAISAM circuits (A–F) with different transistor arrays. The detailed descriptions of these test circuits are shown in Table 1. Test circuits A and B consisted of normal transistor arrays, as shown in Figure 4. The source region is connected to

power for target PMOS transistors in test circuit A and it is connected to ground for target NMOS transistors in test circuit B. Test circuit C and D consisted of transistor arrays with the floating source structure. The source region of target transistors is not connected to power or ground. For PMOS transistors, the floating source structure breaks the parasitic bipolar conduction of drain-well source [16]. This structure mitigates the parasitic bipolar amplification (PBA) effect and may significantly affect the ion-induced sensitive area. For NMOS transistors, the source region could not help collect ionized electron–hole pairs because of the floating structure. Therefore, it may also affect the ion-induced sensitive area. N-well or P-well contacts are, respectively, added near the edge of transistor arrays in test circuit E and F. They are used to investigate the influence of well contacts on the heavy ion-induced sensitive area.

Table 1. Transistor array types in the test chip.

No.	Transistor Array Description
A	Normal PMOS array
B	Normal NMOS array
C	PMOS array (Source float)
D	NMOS array (Source float)
E	PMOS array (Well contact)
F	NMOS array (Well contact)

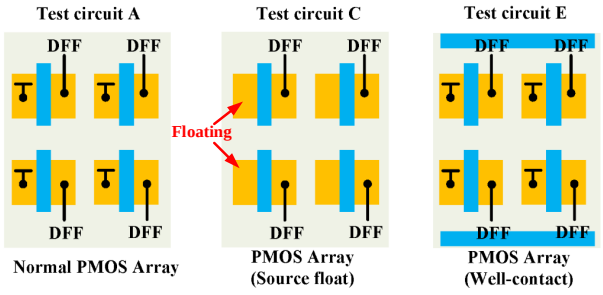

Figure 4. The schematic of the different transistor arrays.

The detailed test chip layout is shown in Figure 5. The test chip size is 0.9 mm height and 0.6 mm width. The width and length of the target transistor sizes are 0.12 μm and 0.06 μm, respectively. The distance between two target transistors is 0.13 μm, which is the minimum value of the layout spacing rule. The height of a transistor array in the vertical direction is 3.87 μm and it is 264.4 μm in the horizontal direction. Based on our previous experimental results, heavy ions impacted no more than three inverters when the LET is smaller than 40 MeV·cm^2/mg [13]. The calculated diameter of heavy ions is no more than 2 μm. Therefore, the size of the transistor array is enough to measure the heavy ion-induced sensitive area. The layout area of a transistor array is 1024 μm^2 and the equivalent area of each target transistor is 0.25 μm^2. It is worth to note that the layout of the target transistor array is placed in the central area while the layout of the D flip-flop is placed above and below the target transistor array. The target transistor arrays and the D flip-flops in the layout are separated to ensure a heavy ion only strikes one of them. The D flip-flop with PMOS/NMOS balanced X1 driven strength is used to connect the target transistor, since it had the minimum critical charge value to made an exact measurement.

Heavy ion experiments were conducted at the HI-13 Tandem Accelerator in China Institute of Atomic Energy and the Heavy Ion Research Facility in Lanzhou (HIRFL) cyclotrons in Institute of Modern Physics, Chinese Academy of Sciences. Three heavy ions with different parameters were used, as shown in Table 2. The heavy ion dose rate was 1×10^4 ions/(cm^2·s), which was determined by the test chip area and the operation frequency. This dose rate value makes sure that the data can be shifted to the output ports before the next heavy ion struck the test circuit. The fluence rate was 1×10^7 ions/cm^2 to make sure enough measurement data are obtained. The number of heavy ions is a factor to

impact TAISAM measurement results. TAISAM circuits are used to investigate the sensitive area when one heavy ion hit the circuits. During the heavy ion experiment, it could not control the heavy ion incident locations. If the number of heavy ions is small, heavy ions may not hit the center of transistor arrays and the measurement results could not fully reveal the ion-induced sensitive area. When the number of heavy ions is large, it increases the probability that heavy ions hit the center of transistor arrays. The measurement results can fully reveal the ion-induced sensitive area. The entire test system consisted of a test chip and other necessary chips, such as field programmable gate arrays (FPGAs) and serial communication chips. The test chip's operation frequency is 40MHz and the serial interface's baud rate is 115,200 bps. FPGAs connected all input and clock ports of the test chip to provide input and clock signals. They were also used to capture output signals and count SEUs when the test chip was irradiated. By conducting these heavy ion experiments, the error counts were exported to the computer by the serial communication interface.

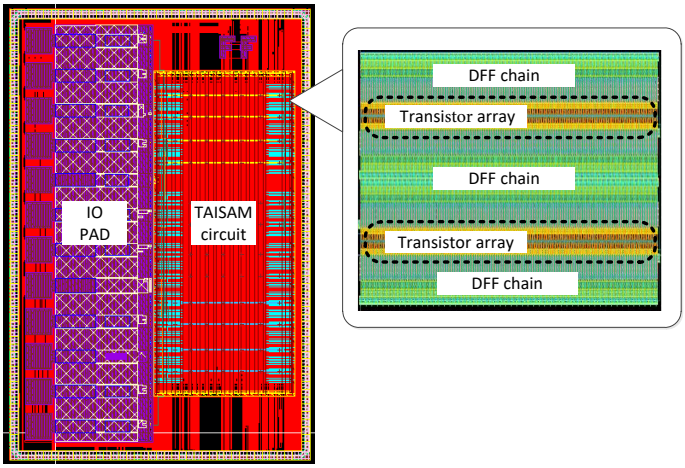

Figure 5. The detailed layout placement in the test chip.

Table 2. Heavy ions used in the experiment.

Ion	Energy at the Silicon Surface (MeV)	Effective LET (MeV·cm^2/mg)	Range (um)
Cl	165	15.2	51.8
Ge	205	37.6	35.5
Kr	835.5	39.8	41.2

The test chip layout was fabricated by the commercial 65 nm bulk CMOS technology. To avoid experimental result variations caused by the sample, five test chips were packaged and were irradiated in the same dynamic test mode. In previous studies, the dynamic test mode had been widely used to estimate the SEU sensitivity of circuits [17–20]. In this paper, TAISAM circuits were irradiated with constant 0 data or constant 1 data. Since the input data were fixed, soft errors owing to the clock tree were avoided. The transient response in the clock tree may cause the data to shift forward without any error. Therefore, SEU only occurred when a heavy ion struck target transistors or D flip-flops.

4. Experimental Results and Discussion

By comparing the experimental results of each test chip, the number of SEUs shows the same distributions. Figure 6 shows one test chip's experimental result with different LET values. The statistical SEU distributions show obvious discrepancies with different data patterns. When the input data are a constant 0, both PMOS transistors and D flip-flops are sensitive to heavy ions for test circuit A. When the input data are a constant 1, only D flip-flops are sensitive to heavy ions for test circuit A. Similarly, SEU distributions are observed for test circuit B. The max number of SEU also shows a difference between the two different input data.

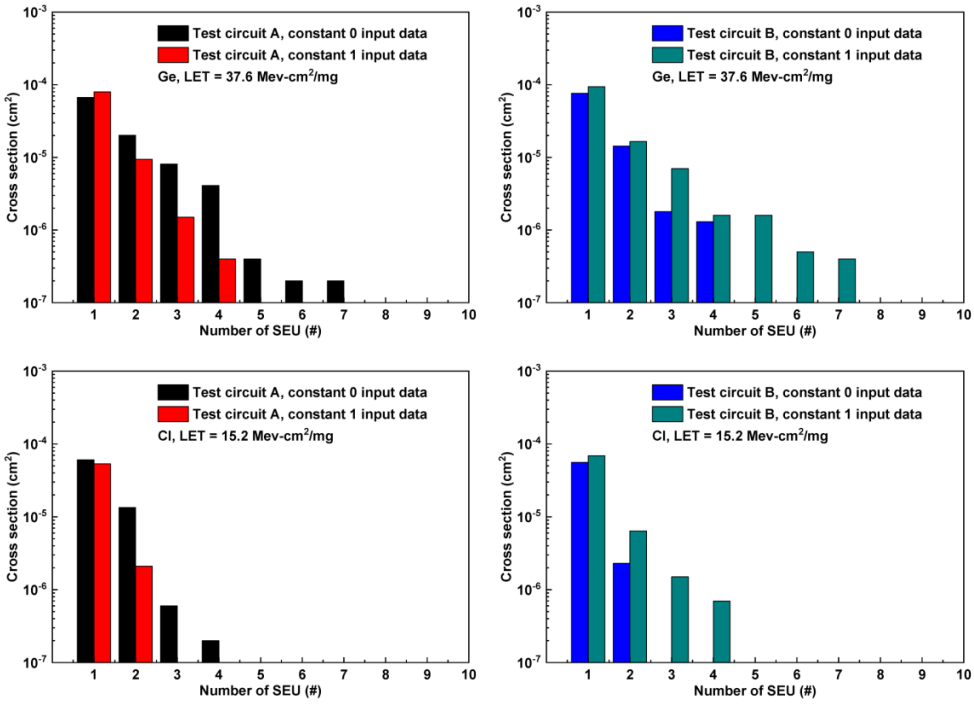

Figure 6. Measured results with different LET values. Test circuit A and B have the normal connections of target transistors.

For test circuit A, when both target transistors and D flip-flops are sensitive to heavy ions, the maximum number of SEU is 7. When only D flip-flops are sensitive to heavy ions, the maximum number of SEU is 4. Measured results confirm that the number of SEU 5, 6, and 7 are obtained when a heavy ion strikes target transistors. The number of SEU 5 and 6 may occur when a heavy ion strikes the edge region of the transistor arrays. However, it does not fully reveal the heavy ion-induced sensitive area. Therefore, the heavy ion-induced sensitive area can be determined by the maximum number of SEU. According to the Equation (1), the measured heavy ion-induced sensitive areas are 1.75 μm^2 and 1.00 μm^2 when the LET values are 37.6 MeV·cm^2/mg and 15.2 MeV·cm^2/mg, respectively.

Figure 7 shows the measured heavy ion-induced sensitive areas of test circuits A–D. For PMOS transistors, the source and drain region are P type doping. The N-well region is N type doping. The source-well drain constitutes a parasitic PNP junction transistor. When a heavy ion hit PMOS transistors, the ionized electron–hole pairs not only diffuse to the PMOS transistors but also lead to the collapse of the N-well potential. The lower N-well potential activates the parasitic PNP junction transistor. It results in the charge injection from the source region to the drain region and causes the PBA effect. Therefore, although the ionized electron–hole pairs may not diffuse to the PMOS transistors, they may also be impacted by heavy ions. The source floating structure breaks the parasitic PNP junction transistor. In our experimental results, the floating source structure hardly affects the heavy ion-induced sensitive area at low LET value. However, it significantly reduces the heavy ion-induced sensitive area at high LET value. The PBA effect slightly causes the injection of holes into the N-well at lower LET value due to the perturbation of N-well voltage is not obvious [21–23]. The PBA effect does not increase the density of the ionized electron–hole pairs at low LET value and the heavy ion-induced sensitive area does not change at low LET values.

However, the perturbation of N-well voltage results in the injection of holes into the N-well at high LET value. The injected holes increase the density of the ionized electron–hole pairs and affect more transistors. Since the floating source structure of target PMOS transistors mitigates the PBA effect, the measured heavy ion-induced sensitive area in test circuit C decreases by 28.5% compared with the data of test circuit A. For NMOS transistors,

the floating source structure significantly affects the heavy ion-induced sensitive area at both low and high LET values. The source region of NMOS transistors could not help collect the ionized electron–hole pairs because of the floating structure [24]. The ionized electron–hole pairs can simultaneously affect more NMOS transistors by drifting and diffusing. Therefore, the floating source structure increases the heavy ion-induced sensitive area. The measured results in test circuit D increases by 28.5% and 50% compared with the data of test circuit B.

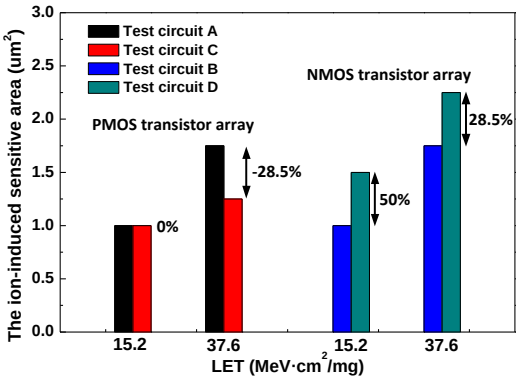

Figure 7. Effect of floating source regions on the measured ion-induced sensitive area with different LET values. Test circuit A and B have the normal connections of target transistors. The source regions of target transistors in test circuit C and D are floating.

Figure 8 shows the measured heavy ion-induced sensitive areas of test circuit A, B, E, and F. For PMOS transistors, the heavy ion-induced sensitive area significantly decreases by 25% and 28.5% with different LET values. The additional N-well contacts not only mitigate PBA effect but also help collect the ionized electron–hole pairs in the N-well. Thus, the measured results in test circuit E are smaller than that in test circuit A.

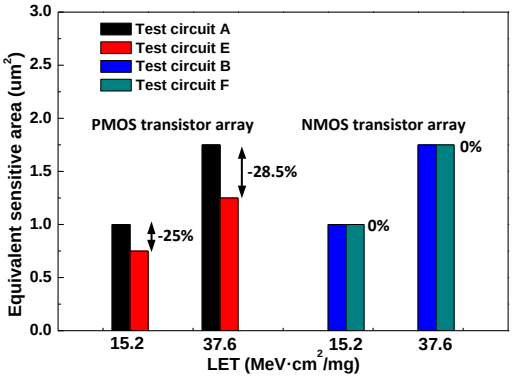

Figure 8. Effect of well contacts on the measured ion-induced sensitive area with different LET values. Test circuit A and B have the normal connections of target transistors. The well connections are added beside the target transistors in test circuit E and F.

However, the additional P-well contact has no effect for the heavy ion-induced sensitive area at both low and high LET values. Different from the N-well contact, the additional P-well contact slightly affects the ionized electron-hole pairs due to the ionized electrons and holes can spread through the entire substrate [25]. Therefore, although the P-well contact was added in test circuit F, the measured result is same as that in test circuit B. Experimental results directly confirm that only the N-well contact can affect the heavy ion-induced sensitive area.

In previous works, heavy ions with different types and energies may produce different sensitivity to circuits even if they have the same LET value [26]. One potential mechanism is that the tracks of ions in semiconductor materials are different. When heavy ions pass

through semiconductor materials, some ion tracks prefer straight lines while other ion tracks prefer curves. Although the LET values of incident ions are same, the number of ionized electron–hole pairs may be different and they may produce different sensitivities to circuits. In this paper, TAISAM was also irradiated with ions that have the same LET but different types and energies. The measured results are shown in Figure 9. The maximum number of SEU is not changed even though the incident heavy ions are different. Thus, the calculated heavy ion-induced sensitive area has no change. One reason is that these ions have the similar tracks when they pass through semiconductor materials. Experimental results indicate that the heavy ion-induced sensitive area is only dependent on the LET values for some ions.

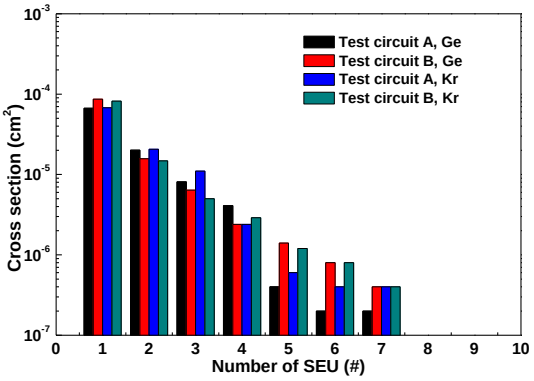

Figure 9. Measured results with different ion energies and species. The incident heavy ions have the similar LET values. However, they have different incident range and energies at the silicon surface.

5. Conclusions

The heavy ion-induced sensitive area is an important parameter for space application integrated circuits. It is essential to characterize it experimentally. This paper has presented a transistor array-based test method called TAISAM, which is used to investigate the heavy ion-induced sensitive area. TAISAM circuits were irradiated under heavy ions. Experimental results were reported, and the heavy ion-induced sensitive area was calculated. The source floating structure and the additional N-well connections are better for PMOS transistors in terms of decreasing the sensitive area because they mitigate the parasitic bipolar amplification effect. However, the source floating structure is worse for NMOS transistors because it does not help collect ionized electron–hole pairs. The additional P-well connection has no effect for the heavy ion-induced sensitive area. Experimental results are consistent with mechanism analyses.

Author Contributions: Conceptualization, J.S.; methodology, Y.C.; validation, B.L. and Z.W.; writing—original draft, J.S.; writing—review and editing, R.S. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The datasets used and/or analyzed during the current study are available from the corresponding author upon reasonable request.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

TAISAM	Transistor Array-based Ion Sensitive Area Measurement
LET	linear energy transfer
SEU	single-event upset
PBA	parasitic bipolar amplification
FPGAs	field programmable gate arrays

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