electronics

MDPI

Article

Ultra-Low-Cost Design of Ripple Carry Adder to Design Nanoelectronics in QCA Nanotechnology

Mohsen Vahabi [1,*], Ali Newaz Bahar [2,3], Akira Otsuki [4,5,6,*] and Khan A. Wahid [3]

[1] Department of Electrical Engineering, Islamic Azad University of Science and Research Tehran (Kerman) Branch, Kerman 7718184483, Iran
[2] Department of Information and Communication Technology (ICT), Mawlana Bhashani Science and Technology University, Tangail 1902, Bangladesh; bahar.ict@mbstu.ac.bd
[3] Department of Electrical and Computer Engineering, University of Saskatchewan, Saskatoon, SK S7N 5A9, Canada; khan.wahid@usask.ca
[4] Facultad de Ingeniería y Ciencias, Universidad Adolfo Ibáñez, Diagonal Las Torres 2640, Peñalolén, Santiago 7941169, Chile
[5] Department of Civil, Environmental and Natural Resources Engineering, Lulea University of Technology, SE 971 87 Lulea, Sweden
[6] RIKEN Center for Advanced Photonics, RIKEN, Wako 351-0198, Saitama, Japan
* Correspondence: mohsen.vahabi@iauk.ac.ir (M.V.); akira.otsuki@uai.cl (A.O.)

Abstract: Due to the development of integrated circuits and the lack of responsiveness to existing technology, researchers are looking for an alternative technology. Quantum-dot cellular automata (QCA) technology is one of the promising alternatives due to its higher switch speed, lower power dissipation, and higher device density. One of the most important and widely used circuits in digital logic calculations is the full adder (FA) circuit, which actually creates the problem of finding its optimal design and increasing performance. In this paper, we designed and implemented two new FA circuits in QCA technology and then implemented ripple carry adder (RCA) circuits. The proposed FAs and RCAs showed excellent performance in terms of QCA evaluation parameters, especially in cost and cost function, compared to the other reported designs. The proposed adders' approach was 46.43% more efficient than the best-known design, and the reason for this superiority was due to the coplanar form, without crossovers and inverter gates in the designs.

Keywords: full adder; ripple carry adder; coplanar; cost function; quantum-dot cellular automata; energy dissipation

Citation: Vahabi, M.; Bahar, A.N.; Otsuki, A.; Wahid, K.A. Ultra-Low-Cost Design of Ripple Carry Adder to Design Nanoelectronics in QCA Nanotechnology. *Electronics* **2022**, *11*, 2320. https://doi.org/10.3390/electronics11152320

Academic Editor: Flavio Canavero

Received: 29 June 2022
Accepted: 22 July 2022
Published: 26 July 2022

1. Introduction

As the advancement and development of integrated circuits progressed day by day and the lack of response of the complementary metal–oxide–semiconductor (CMOS) technology due to the problems at the nanoscale, new technologies at the nanoscale were introduced. These were technologies such as: carbon nanotubes, quantum-dot cellular automata (QCA), nanomagnetic logic, resonant tunneling diodes, and spin-wave devices. One of the most promising alternatives to replace CMOS technology is QCA technology. It is due to the extraordinary features and benefits of QCA, which are high switch speed, an operating frequency in the terahertz frequency range, very low power dissipation, extremely high device density, and implementation at the level of atoms and molecules.

To implement bistable and local QCA paradigm interactions, several different implementations have been proposed, such as atoms, molecules, and semiconductors that have been studied based upon electrostatic interactions [1]. In addition, various experimental devices [2,3] have been developed and successfully tested [2,3]. There are four types of QCA. Molecular and magnetic QCA are operable at room temperature while metal and semiconductor QCA operate at around cryogenic temperatures.

Furthermore, several typical clock schemes have been proposed for QCA circuits to realize the specifications of standard units and develop routing and placement algorithms [4,5]. All the concepts presented in this paper were based on a QCA semiconductor. Adders are one of the main building blocks of many VLSI systems, such as microprocessors and various processors. One of the most important and widely used circuits in mathematical computations of digital logic is the full adder (FA) circuit; the optimal design and performance improvement of this circuit has special importance. Improvements to this circuit will result in improved and optimized performance for more complex circuits [6,7]. Moreover, cost-effective and efficient design of FA and RCA circuits can achieve more efficient and cost-effective complex circuits.

Therefore, in the present article, two designs and implementations of this circuit were presented. To show the performance improvement, we implemented and applied these FA designs in designing and implementing the RCA circuits. This article is composed as follows: Section 2 presents the background of QCA and an overview of previous works. The design, implementation, and simulation results of the proposed FA and RCA circuits are presented in Section 3. Tables and diagrams for comparison and evaluation of important QCA parameters are presented in Section 4, the energy dissipation analysis in Section 5, and the conclusions of this article are presented in Section 6.

2. QCA Basics

2.1. The QCA Cells Basics

Similar to transistors in CMOS circuits, QCA cells serve as the primary units of the QCA circuits for the design and development of computing and communication devices. Each QCA cell is composed of four holes (quantum dots) and two electrons are trapped inside it (Figure 1a). Because of the Columbic effects, the electrons are always in a position where there is the minimal potential energy, and the electrons are placed diagonally inside the holes. By placing the electrons diagonally, two logical structures "0" and "1" (polarizations −1 and +1, respectively) are created [8,9], as shown in Figure 1b.

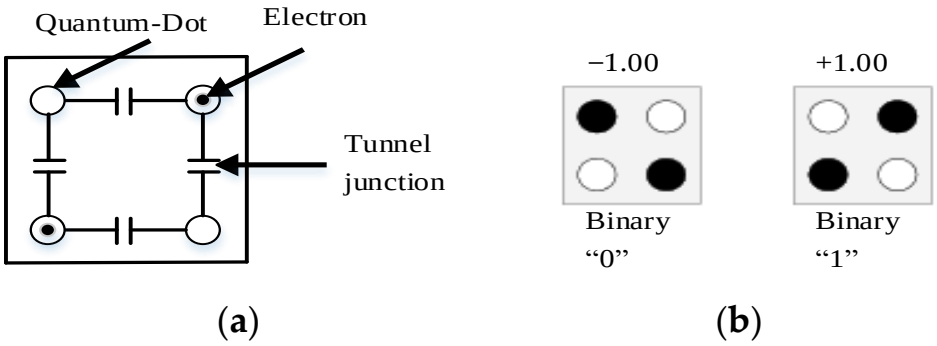


Figure 1. Schematics of QCA (**a**) cell, and (**b**) two structures logical values QCA cells.

Four-phase clocks are also used as clocking in the QCA design to reduce the signal metastability and ensure the correct propagation of signals in the circuit [9] (Figure 2).

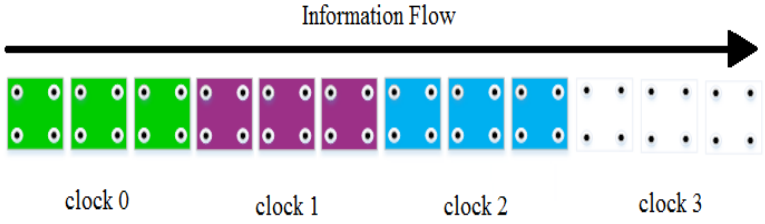


Figure 2. Clock zones for QCA wire.

QCA wire is used to communicate between gates, blocks, and QCA circuits, and it is created by placing the QCA cells next to each other [8,10]. The majority gate (MV) is one of

the most widely used gates in the design of the QCA circuits and is among the basic gates of this technology. The MV has the number of individual inputs and one output that the majority votes of the inputs determine the amount (value) of the output. One of the most widely used MV gates in the design of the QCA circuits is the three-input MV gate, whose two examples are given in Figure 3, and in the proposed designs, we used both types [8,11] separately.

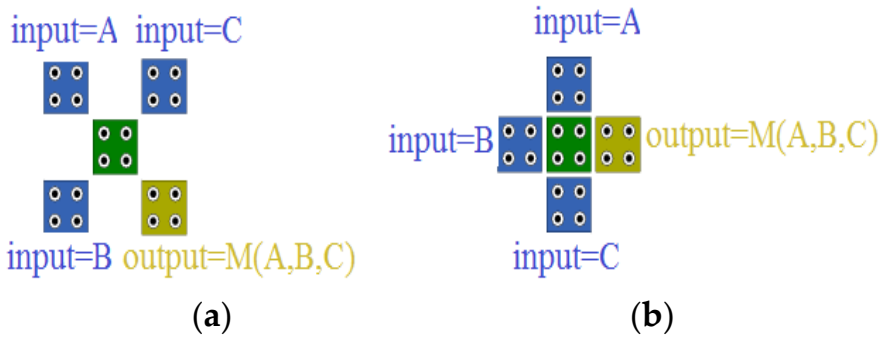


Figure 3. (**a**) Inverted MV gate, and (**b**) Regular MV gate.

2.2. Overview of FA/RCA Designs

The design of the full adder circuit is of special importance due to its many usages. In QCA technology, due to the high capability and implementation of composite gates, using majority gates and XOR gates independently and without using base gates (NOT gates, AND gates and OR gates) has caused this block (FA circuit) to be implemented without using base gates. This has led to the optimization and improvement of the main and basic parameters of QCA technology, including the number of cells, the occupied area, latency, and finally the implementation cost. For this reason, the implementation of composite and complex circuits using independent XOR gates (without the use of base gates in the implementation), improves the main QCA parameters and ultimately reduces the implementation cost and cost function. Thus, various designs and implementations for the FA circuit have been introduced. They have been introduced in multi-layer designs [12–15] with a high cost of implementation while some others are coplanar [16–18] which use rotational cells in the implementation; we do not consider these in this work due to their high cost of implementation and low sustainability. Some others [19–21] were coplanar and the implemented crossovers were based on the QCA's clocking. This type of design also has a higher cost function due to the use of crossovers and inverter gates and not moving toward design and implementation without crossovers and inverter gates. As a result, in this paper, we proposed the FA design in a coplanar manner without the 45 cells, inverter gates, and crossovers. The design and implementation of FAs and RCAs are the first to be presented without the use of inverter gates in the implementation. However, all the proposed designs in this article and the QCA circuit parameters, such as cell number, the occupied area, latency, and cost function, were superior to previous works.

3. The Proposed Circuits

Adder blocks are one of the most important computational circuits, and they are used as the most applied arithmetic blocks. Among adder blocks, the FA block is one of the most common and principal computational blocks. In most FA circuit designs with QCA technology, the majority and inverter gates are prevalently used. In this work, the proposed FA and 4-bit RCA designs were implemented using the XOR gate while a nothing inverter gate (NOT gates) and a crossover were used to implement the proposed designs. Such designs and implementations are very important because it can achieve a lower cost function and ultimately lead to lower implementation costs than other designs.

3.1. The FA Circuit Design and Implementation

One of the most important and applied circuits and computing blocks of digital logic is the full adder (FA) circuit because this block is the main component of more complex circuits and computational systems. Improving and optimizing the performance of this circuit will improve and optimize larger and more complex circuits. Therefore, we designed and implemented two novel FA circuits with the "implementation with XOR gate" designed method. All of these designs were coplanar (single layer), and nowhere in these designs were inverter gates and crossovers not used. The Schematic logic diagram of these designs is shown in Figure 4.

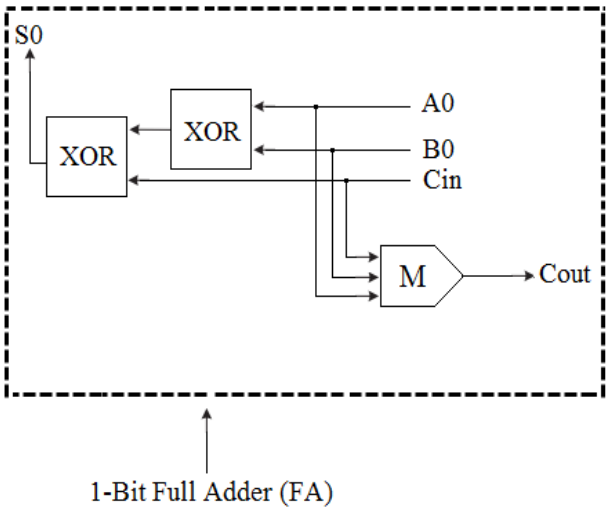


Figure 4. Schematic logic diagram of the novel FA circuits.

Figure 5a shows the implementation of the proposed (a) FA circuit. A0, B0 and Cin are the input cells, and Sum and Cout are the output cells of this design. This circuit contains 37 normal cells, 0.5 cycle latency, and a 0.031 μm^2 occupied area. Figure 5b also shows the implementation of the proposed (b) FA circuit. This circuit also contains 35 normal cells, 0.5 cycle latency, and a 0.027 μm^2 occupied area. As shown in Figure 5, the difference between the two proposed FAs (a and b) is in their majority gate (MV) that gives the Cout output. The proposed FA circuit (a) is based on a regular MV and the proposed FA (b) is based on an inverted MV. Since the latency of both outputs (Cout and SUM) are similar for both the proposed FA circuits, they give similar simulation outputs. Therefore, for the sake of brevity, we provided only one of the simulation results in exchange for similar inputs. Figure 6 shows the simulated output of these circuits. The evaluation of our proposed FA circuits in this research in comparison with previous works is given in Section 4. All the proposed designs of this research were significantly superior to all previous designs in terms of basic QCA parameters, such as cell number, the occupied area, and latency.

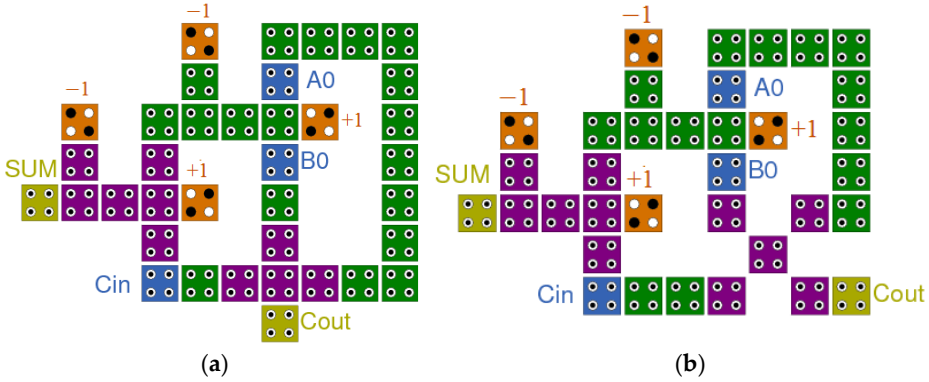


Figure 5. The QCA layout with (**a**,**b**) FA circuits.

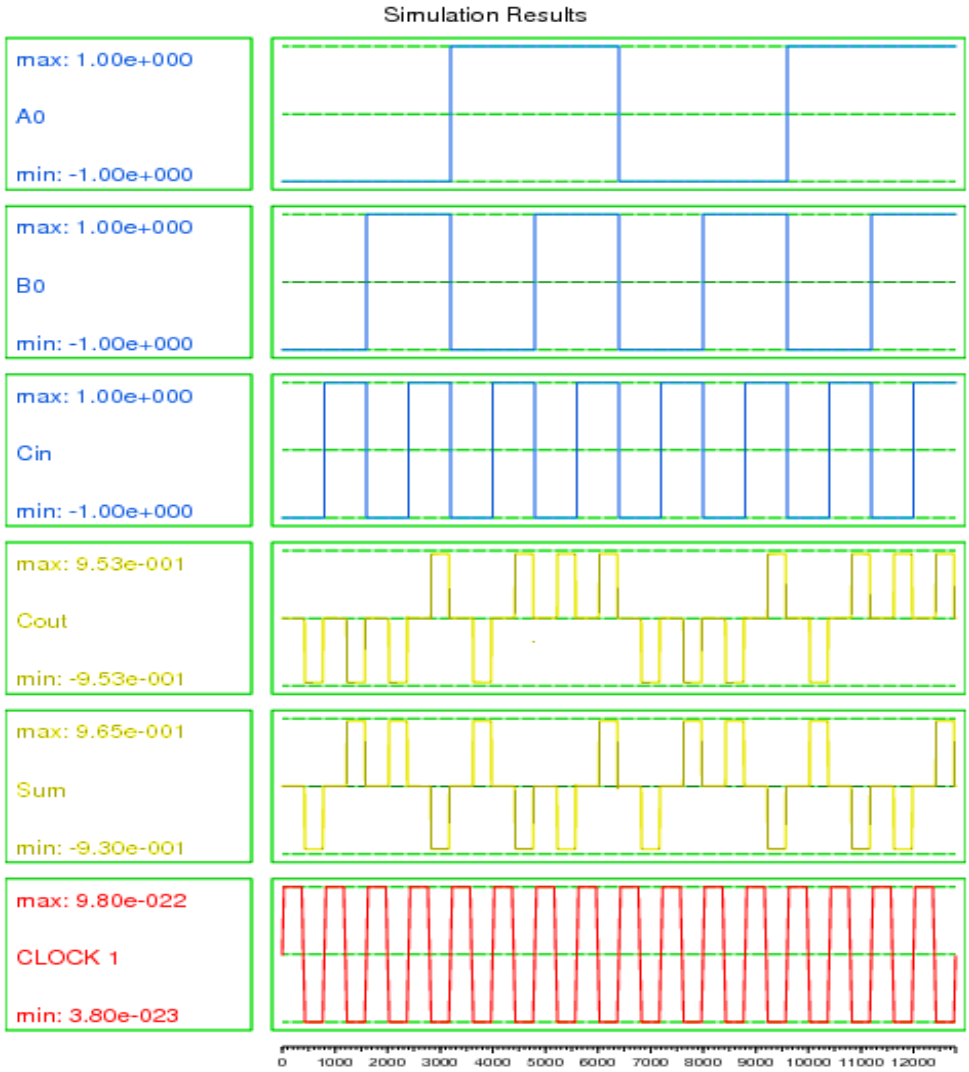


Figure 6. Simulation results of the proposed (**a**,**b**) FA circuits.

3.2. The RCA Circuit Design and Implementation

In this section, we designed two 4-bit RCA circuits using each of the proposed FA designs in the previous section. All these designs were coplanar (single layer). The block diagram of the two proposed 4-bit RCA designs is shown in Figure 7. Shown in this figure is a 4-bit adder using four full adders. This adder design is referred to as "ripple carry" since the carry ripples from one FA to another. As can be seen, A3, A2, A1, and A0 (untitled Bus A); B3, B2, B1, and B0 (untitled Bus B); and Cin are the input cells; and Cout, S3, S2, S1, and S0 (untitled Bus Sum) are the output cells in this block diagram. As a result, by using the two implementation hardware designs in Figure 5 and based on the block diagram of Figure 7, it is possible to achieve the two-implementation hardware of the 4-bit ripple carry adder circuit. Figure 8A shows the design and implementation of the proposed (A) 4-bit RCA circuit. This implementation includes 233 normal cells, 1.25 cycle latency, and 0.28 μm^2 of the occupied area. Figure 8B also shows the design and implementation of the proposed (B) 4-bit RCA circuit, which includes 209 normal cells, 1.25 cycle latency, and a 0.25 μm^2 occupied area. The difference between the two proposed 4-bit RCAs (A and B) is in their using MV gates. The proposed 4-bit RCA circuit (A) is based on a regular MV while the proposed 4-bit RCA (B) is based on an inverted MV. Since the latency of both outputs are similar for the both proposed 4-bit RCA circuits, they give similar simulation outputs. Therefore, for the sake of brevity, we provided only one of them in exchange for

similar inputs. Figure 9 also shows the output of the simulation of these two proposed 4-bit RCA circuits.

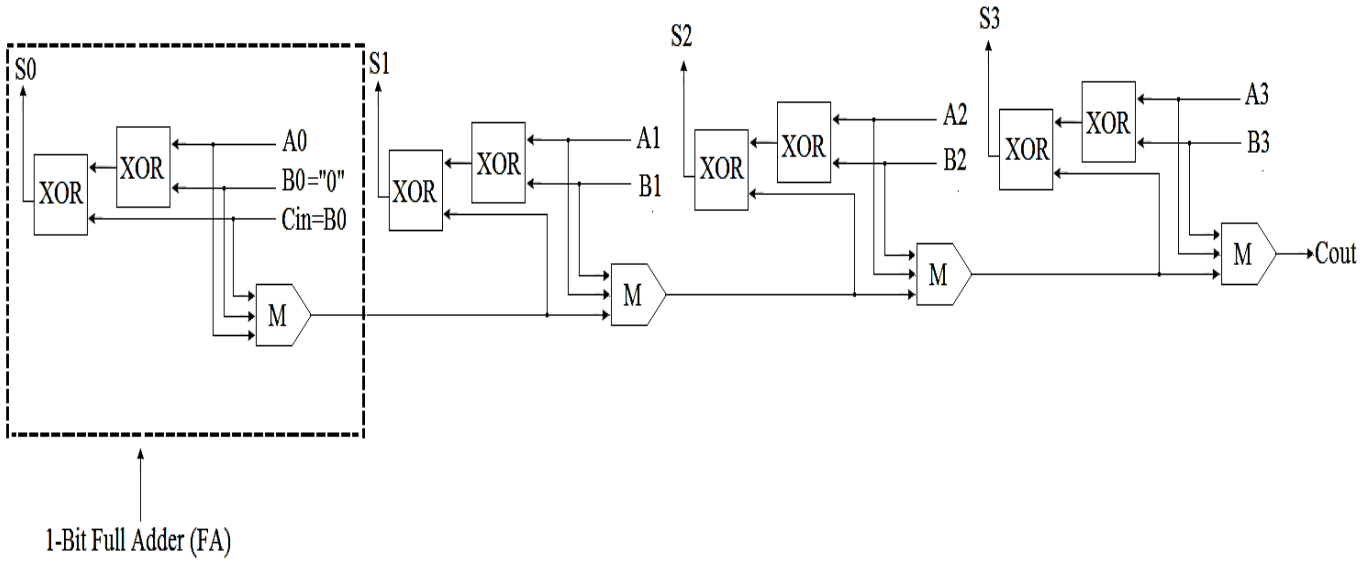
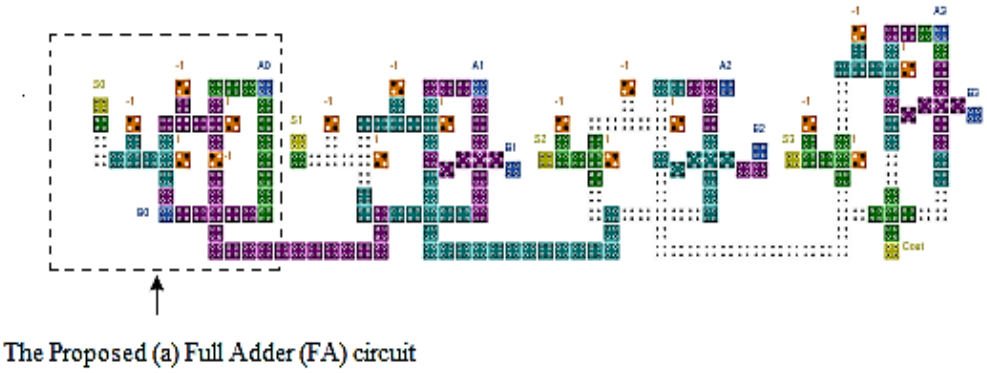
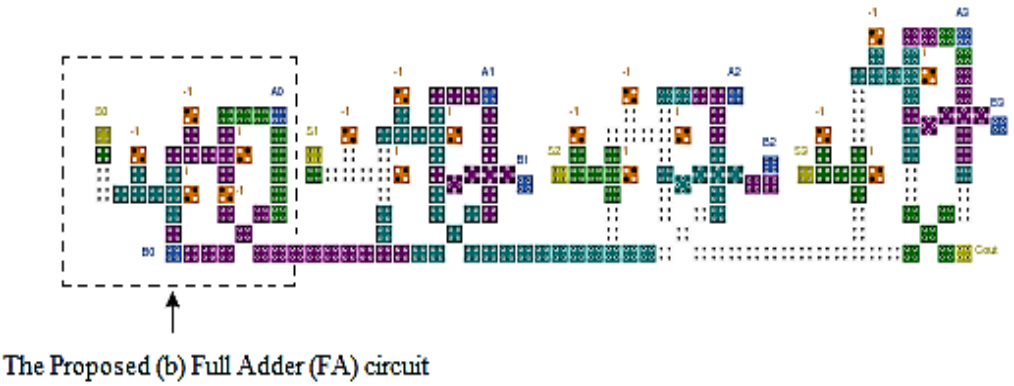


Figure 7. Logical diagram of the proposed 4-bit RCA circuit.



(**A**)



(**B**)

Figure 8. The proposed (**A**,**B**) 4-bit RCA circuits.

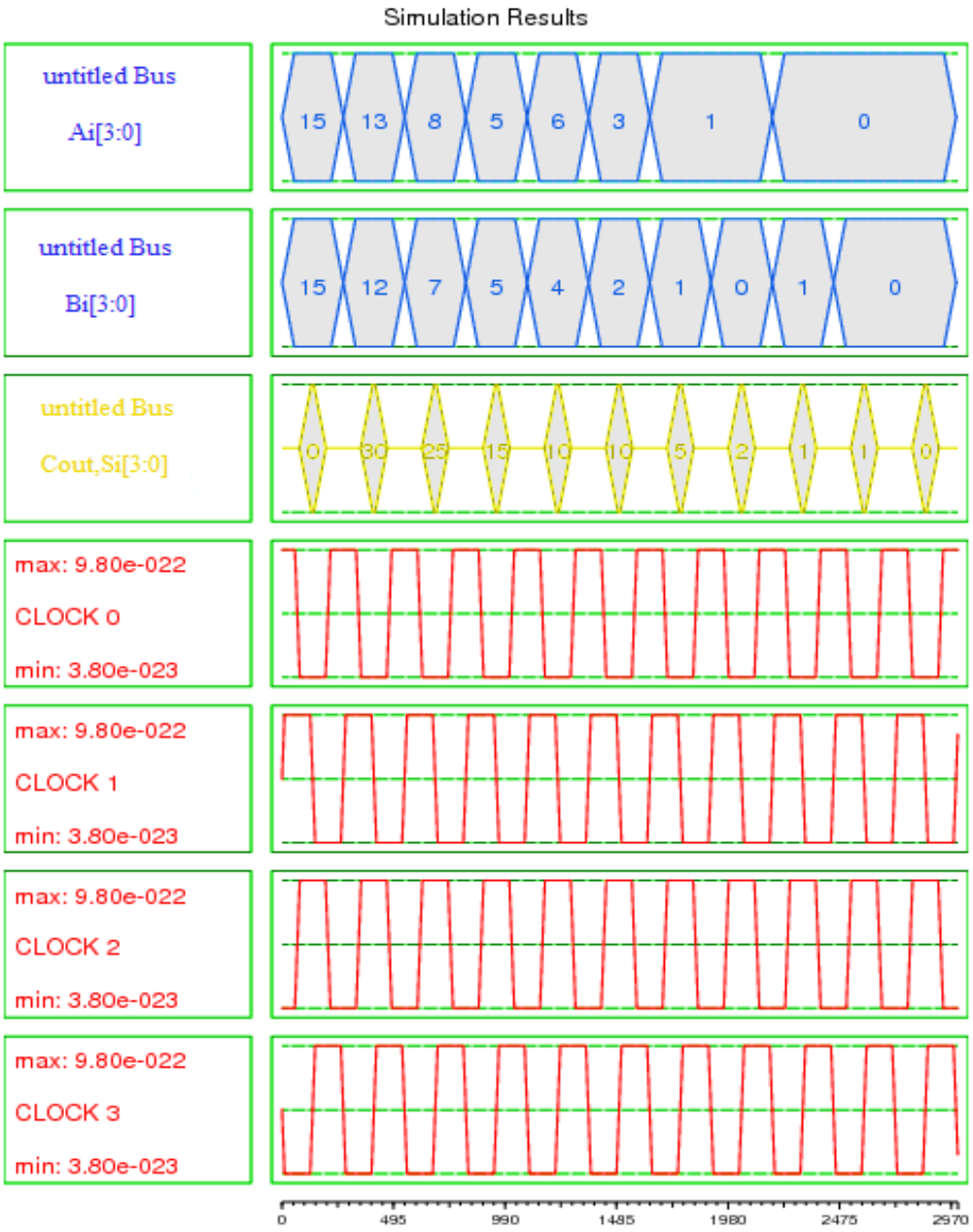


Figure 9. Simulation results for the proposed (**A**,**B**) 4-bit RCA circuits.

4. Performance Evaluation

In this part, a comparative evaluation and analysis of the proposed 4-bit RCA circuits with previous works are given. For this evaluation, the number of cells, area, and latency of the proposed circuits are simulated with the QCA designer tool. We used QCADesiner 2.0.3 version and verified our designs by the Bistable Approximation and Coherence Vector simulation engine. Table 1 lists a brief description of the coherence vector simulation parameters used by the QCA Designer tool. The simulation results of the proposed FAs and 4-bit RCAs circuits of this research are also given in Tables 2 and 3, respectively. One of the most important evaluation criteria for QCA circuits is cost function as reported in literature [22]. Equation (1) shows this evaluation criterion. Cost function is a composite measure, consisting of certain criteria that M indicates the number of majority gates, I the number of inverter gates, C the number of crossovers, and T also indicates the amount of output latency. The coefficients L, K, and P are also determined based on the importance of power dissipation, the occupied area, complexity, and latency, respectively. As shown in

Table 3, our proposed adders (i.e., Proposed (A) and Proposed (B)) have a better advantage than the previous paradigms due to less use of the MV numbers. The reduction of the cost function is about 46.43% and 60.23% in comparison to [19,23], respectively. Moreover, the complexity is reduced by about 25% and 12.5% in comparison to [19,23], respectively, and the delay is about 28.57% and 54.55% in comparison to [19,23], respectively.

$$Cost\ Function = (M^K + I + C^L) \times T^P, 1 \leq K, L, P \quad (1)$$

$$Cost_{Area\text{-}Delay} = A \times T^P, 0 \leq p \leq 2 \quad (2)$$

Table 1. Simulation parameters of the coherence vector tool.

Parameter	Value
cell width	18 nm
cell height	18 nm
relative permittivity	12.9
dot diameter	5 nm
number of samples	12,800
convergence tolerance	0.001
clock high	9.8×10^{-22} J
clock low	3.8×10^{-23} J
clock amplitude factor	2
radius of effect	65 nm
layer separation	11.5 nm
maximum iteration per sample	100

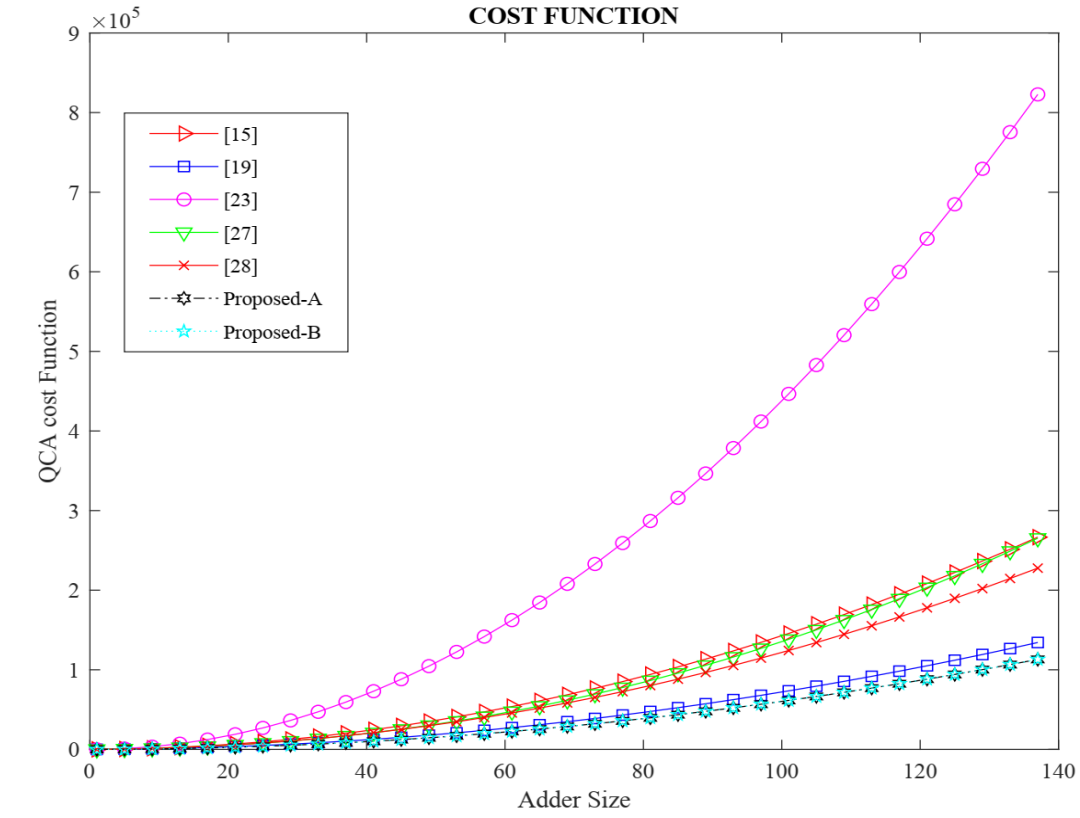
Table 2. Comparison analysis of the novel FA circuits in comparison with others.

Circuit	Area (μm^2)	Cell Count	Latency (clock)	NOT Gate Count	Crossover Type
FA [1]	0.057	60	1	1	not required
FA-1 [8]	0.043	45	0.75	0	not required
FA-2 [8]	0.037	43	0.75	0	not required
FA [18]	0.076	61	0.5	4	coplanar (rotated cells)
FA [19]	0.043	59	1	2	coplanar (clocking based)
FA [20]	0.047	58	1	4	coplanar (clocking based)
FA [21]	0.047	56	1	2	coplanar (clocking based)
FA [23]	0.025	37	1	1	not required
FA [24]	0.043	44	1.25	6	not required
FA [25]	0.0.39	37	0.75	2	not required
FA [26]	0.03	37	0.75	2	not required
Proposed (*a*)	0.031	37	0.5	0	not required
Proposed (*b*)	0.027	35	0.5	0	not required

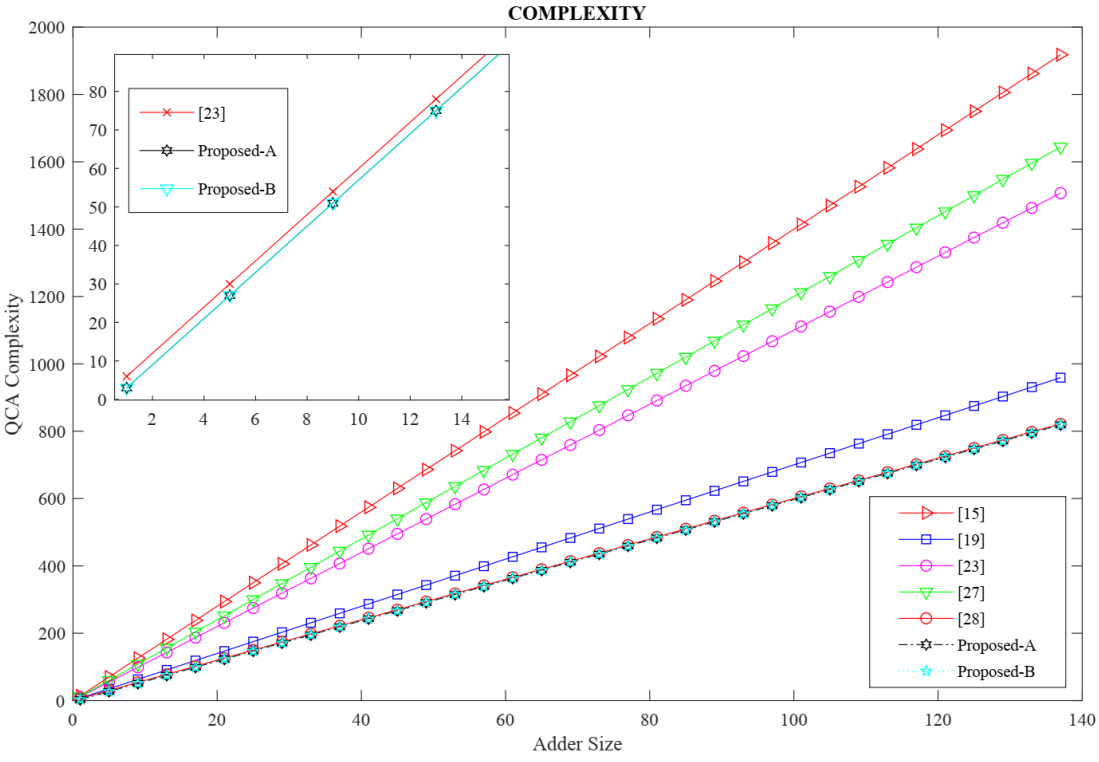
Table 3. Comparison analysis of the novel proposed 4-bit RCA circuits comparison with others.

Circuit	Area (μm^2)	Cell Count	Delay (clock)	Cost	Cost Function P, K, L = 1
FA [15]	0.24	237	1.5	0.36	84
FA [19]	0.29	262	1.75	0.51	49
FA [23]	0.36	250	2.75	0.99	66
FA [27]	0.29	308	2	0.58	96
FA [28]	0.37	269	3.5	1.29	154
Proposed (A)	0.28	233	1.25	0.35	26.25
Proposed (B)	0.25	209	1.25	0.31	26.25

As shown in Table 3, the coefficients of K, L, P are considered equal to one (K, L, P = 1). To evaluate the performance of the novel RCAs in comparison with the performance of the previous paradigms, this evaluation has been performed. Figure 10a shows the evaluation and comparison of the cost function criterion at K, L, P = 1. The cost function of our proposed designs is significantly superior to all previous designs. The reasons for this superiority are due to the absence of the inverter gates, a crossover, and also fewer MV gates used in the implementation of our proposed designs. These comparisons and evaluations were performed in a size range of $1 \leq n \leq 128$. Another evaluation was performed by using Equation (2) where A represents the occupied area and T represents the latency [22]. Figure 10b shows the comparison diagram of the complexity criterion, and it indicates our proposed designs in this research are superior to all previous works due to the less occupied area and less delay. In this comparison, the number of MV gates, the number of NOT gates, and the number of crossovers were considered, assuming that the cost of multi-layer crossovers is three times that of a coplanar (single layer) [22]. To measure the complexity of the novel proposed RCAs (n-bit) against previous designs, this evaluation was performed in the range of $1 \leq n \leq 128$. As shown in Figure 11 for the review of this evaluation parameter, in this evaluation criterion, our proposed RCAs designs are significantly superior to all previous paradigms. Figure 10c also shows the delay criterion in order to measure the speed of QCA Adders. This comparison was also performed in the range of $1 \leq n \leq 128$, and the fastest QCA Adder is related to our proposed designs, which are coplanar. As a result, in this evaluation criterion, our proposed QCA Adders designs are also superior to previous designs.



(**a**)



(**b**)

Figure 10. *Cont*.

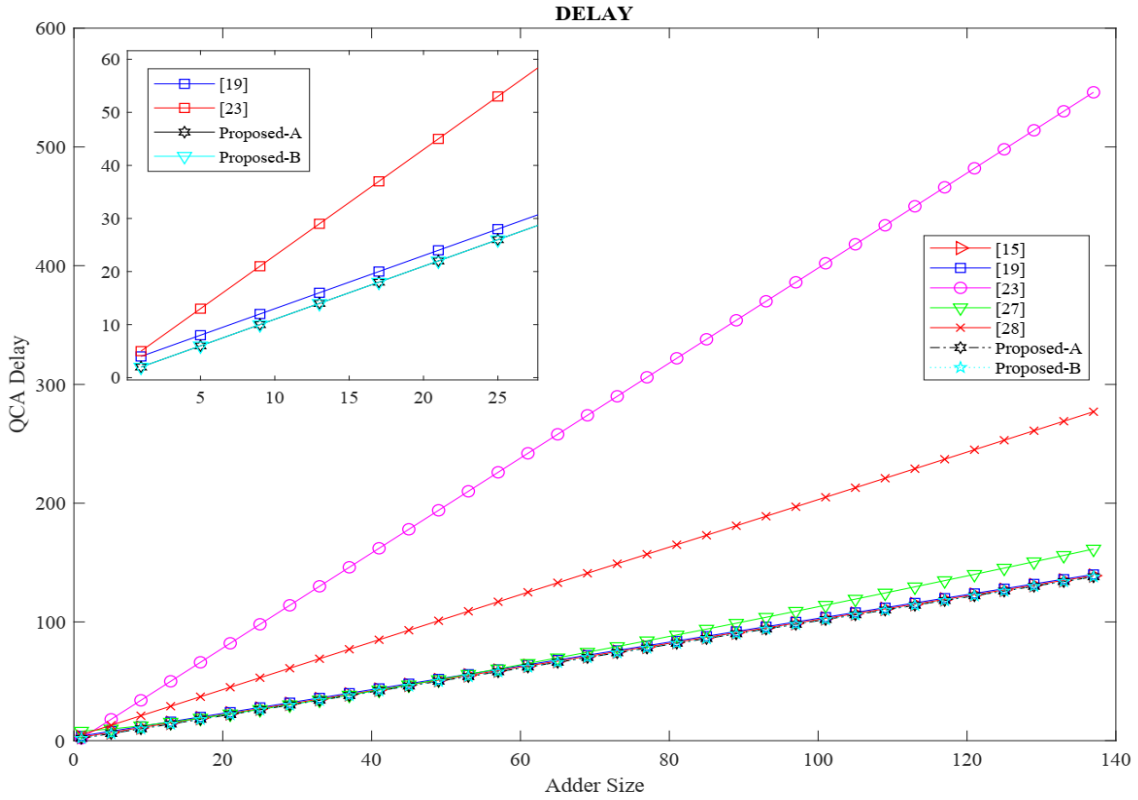


Figure 10. Comparison and evaluation of QCA adders with (**a**) cost function, (**b**) complexity and (**c**) delay criterions.

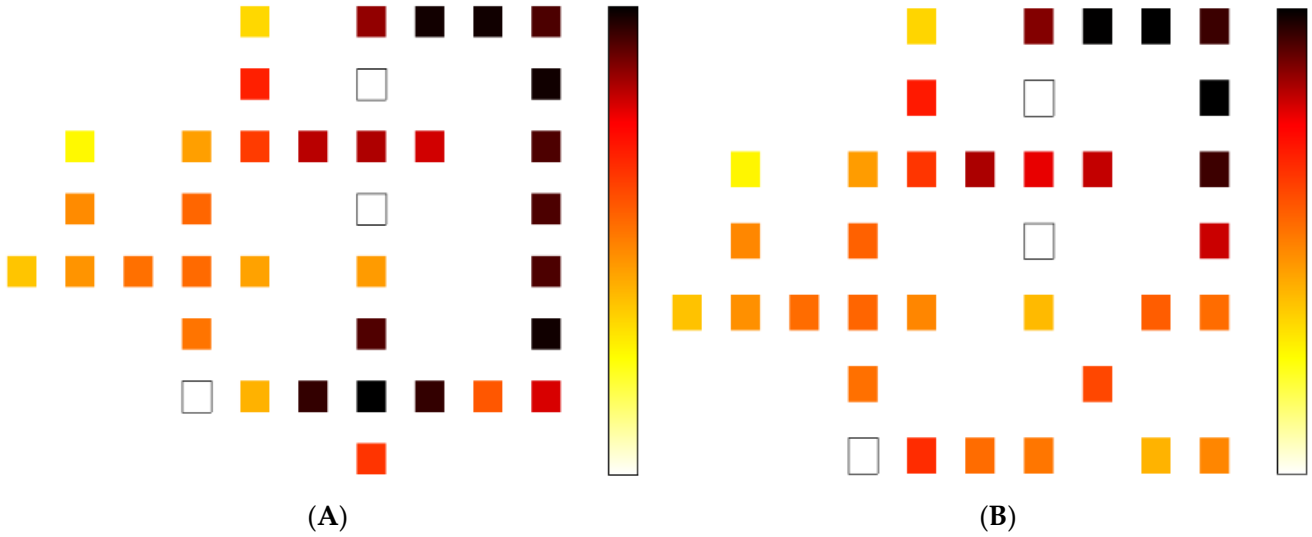


Figure 11. Thermal hotspots of the full adders (**A**) (FA-1) and (**B**) (FA-2) at 0.5 Ek.

5. Energy Dissipation Analysis

One of the important parameters for evaluating performance and efficiency in the design of electronic devices is energy dissipation. The high-power estimation method [29] is the most common method for power approximation. In this section, a power dissipation analysis was performed using QCAPro tool [30]. In the calculations, the power

consumption of all QCA cells is assumed to be the same amount. Therefore, the equation for instantaneous power is given by:

$$P_{total} = \frac{dE}{dt} = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt} \cdot \vec{\lambda}\right] + \frac{\hbar}{2}\left[\vec{\Gamma} \cdot \frac{d\vec{\lambda}}{dt}\right] \tag{3}$$

where $\vec{\lambda}$ the coherence vector and $\vec{\Gamma}$ is the state energy vector. The vector $\vec{\lambda}$ indicates the current state of a cell and the vector $\vec{\Gamma}$ signifies the steady state of the cell. The total energy dissipation in a time period $[-t, t]$ and was estimated as follows:

$$E_{diss} = \frac{\hbar}{2}\int_{-t}^{t} \vec{\Gamma} \cdot \frac{d\vec{\lambda}}{dt} = \frac{\hbar}{2}\left(\left[\vec{\Gamma} \cdot \vec{\lambda}\right]_{-t}^{t} - \int_{-t}^{t} \vec{\lambda} \cdot \frac{d\vec{\Gamma}}{dt} dt\right) \tag{4}$$

and the power dissipation model can be estimated as follows:

$$P_{diss} = \frac{E_{diss}}{T_c}\left\langle \frac{\hbar}{2T_c}\vec{\Gamma}_+ \times \left[\frac{\vec{\Gamma}_-}{\left|\vec{\Gamma}_-\right|}\tanh\left(\frac{\hbar\left|\vec{\Gamma}_-\right|}{k_B T}\right) - \frac{\vec{\Gamma}_+}{\left|\vec{\Gamma}_+\right|}\tanh\left(\frac{\hbar\left|\vec{\Gamma}_+\right|}{k_B T}\right)\right]\right\rangle \tag{5}$$

Using the value of clock low and high energies, the average leakage and switching power can be expressed as follows:

$$P_{avg}^{leak} = \frac{1}{2^r}\sum_{i\,=\,r+1}^{N} p_{i,n\to m}^{leak} \tag{6}$$

$$P_{avg}^{switch} = \frac{1}{2^r}\sum_{i\,=\,r+1}^{N} p_{i,n\to m}^{switch} \tag{7}$$

Table 4 shows the energy dissipation data of different multipliers at the 0.5 Ek, 1.0 Ek, and 1.5 Ek tunneling energy for the novel proposed FAs circuits. As shown in Table 4, for the proposed full adder A (FA-1), the energy dissipates are 60.22, 75.74, and 94.99 meV at 0.5, 1.0, and 1.5 Ek, respectively, while for the proposed full adder B (FA-2), the energy dissipates are 49.79, 65.67, and 84.81 meV at 0.5, 1.0, and 1.5 Ek, respectively. Figure 11 shows the thermal hotspots of our proposed full adders (FA-1 and FA-2) at 0.5 Ek where the dark cells indicate higher energy dissipated cells.

Table 4. Energy consumption analysis of different multipliers at different tunneling energy levels at temperature *2 K*.

FA Circuit	Avg Leakage Energy (meV)			Avg Switching Energy (meV)			Avg Energy Dissipation (meV)		
	0.5 E_K	***1 E_K***	***1.5 E_K***	***0.5 E_K***	***1 E_K***	***1.5 E_K***	***0.5 E_K***	***1 E_K***	***1.5 E_K***
FA-1	11.12	32.92	58.37	49.1	42.82	36.62	60.22	75.74	94.99
FA-2	11.64	33.18	57.45	38.15	32.49	27.36	49.79	65.67	84.81
FA-[1]	15.37	44.87	76.92	61.87	56.03	51.61	77.24	100.9	128.53
FA-[8]-1	13.91	40.87	72.13	55.13	48.1	41.32	69.04	88.97	113.45
FA-[8]-2	14.15	43.37	77.91	56.98	46.54	42.47	71.13	89.91	120.38
FA-[18]	29.19	84.83	148.5	127.94	108.82	91.46	157.13	193.65	239.97
FA-[19]	19.2	587.5	102.8	108.99	95.14	81.56	128.19	682.59	184.32
FA-[20]	16.93	51.11	91.37	104.91	92.41	80.36	121.84	143.52	171.73
FA-[21]	14.95	47.9	87.32	92.15	80.63	69.3	107.1	128.53	156.62
FA-[23]	11.22	32.95	58.43	64.03	56.66	49.46	75.25	89.61	107.89
FA-[24]	17.3	45.89	76.92	41.11	34.33	28.86	58.41	80.22	105.78
FA-[25]	15.48	43.11	75.92	42.91	36.72	29.65	58.39	79.83	105.57
FA-[26]	13.96	37.77	63.88	29.55	24.65	20.4	43.51	62.42	84.28

6. Conclusions

Many of the RCA designs in QCA technology were implemented with multi-layers but using rotational cells (45° cells). Furthermore, designing coplanar crossovers with adjacent clock phases in large designs increased latency. For these reasons, we used the minimum crossovers and 45° cells (rotational cells) in our designs. This led to the efficient RCA design of our proposed designs because they were designed as a coplanar (single layer) and with the minimum number of NOT gates, crossovers, and rotational cells. This made the implemented circuit more stable and robust than previous designs and also significantly superior to previous designs in terms of basic parameters, the number of cells, the occupied area, latency, cost function and cost area-delay. We used the proposed FA in 4-, 8-, 16-, 32-, 64-, and 128-bit ripple carry QCA adder. Due to the comparison and evaluation of the cost function parameter, the cost of implementing the n-bit RCA of our proposed designs was much lower. The proposed design was 46.43% more efficient in cost function than the best-known design [19] and the reasons for this were due to our innovative and creative design in using the minimum crossovers and inverter gates in the designs. The results showed that the proposed design was more efficient and cost-effective than the existing designs. Therefore, they can be used effectively in the design of more complex circuits and systems and improve and optimize composite and complex circuits.

Author Contributions: Conceptualization, M.V.; methodology, M.V.; validation, M.V. and A.N.B.; formal analysis, M.V.; investigation, M.V. and A.N.B.; writing—original draft preparation, M.V.; writing—review and editing, A.N.B., A.O. and K.A.W.; supervision, A.N.B., A.O. and K.A.W. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Data are contained within the article.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Wang, L.; Xie, G. A Novel XOR/XNOR Structure for Modular Design of QCA Circuits. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *67*, 3327–3331. [CrossRef]
2. Snider, E.G.; Orlov, A.O.; Amlani, I.; Zuo, X.; Bernstein, G.H.; Lent, C.S.; Merz, J.L.; Porod, W. Quantum-dot cellular automata: Review and recent experiments (invited). *J. Appl. Phys.* **1999**, *85*, 4283–4285. [CrossRef]
3. Macucci, M.; Gattobigio, M.; Bonci, L.; Iannaccone, G.; Prins, F.; Single, C.; Wetekam, G.; Kern, D. A QCA cell in silicon-on-insulator technology: Theory and experiment. *Superlattices Microstruct.* **2003**, *34*, 205–211. [CrossRef]
4. Edrisi Arani, I.; Rezai, A. Novel circuit design of serial–parallel multiplier in quantum-dot cellular automata technology. *J. Comput. Electron.* **2018**, *17*, 1771–1779. [CrossRef]
5. Vankamamidi, V.; Ottavi, M.; Lombardi, F. Two-dimensional schemes for clocking/timing of QCA circuits. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2007**, *27*, 34–44. [CrossRef]
6. Vahabi, M.; Lyakhov, P.; Bahar, A.N. Design and Implementation of Novel Efficient Full Adder/Subtractor Circuits Based on Quantum-Dot Cellular Automata Technology. *Appl. Sci.* **2021**, *11*, 8717. [CrossRef]
7. Bhargav, A.; Huynh, P. Design and Analysis of Low-Power and High Speed Approximate Adders Using CNFETs. *Sensors* **2021**, *21*, 8203. [CrossRef]
8. Vahabi, M.; Lyakhov, P.; Bahar, A.N.; Wahid, K.A. Design and Implementation of New Coplanar FA Circuits without NOT Gate and Based on Quantum-Dot Cellular Automata Technology. *Appl. Sci.* **2021**, *11*, 12157. [CrossRef]
9. Tougaw, P.D.; Lent, C.S. Logical devices implemented using quantum cellular automata. *J. Appl. Phys.* **1994**, *75*, 1818–1825. [CrossRef]
10. Kim, H.-I.; Jeon, J.-C. Quantum LFSR Structure for Random Number Generation Using QCA Multilayered Shift Register for Cryptographic Purposes. *Sensors* **2022**, *22*, 3541. [CrossRef]
11. Lent, C.S.; Tougaw, P.D.; Porod, W. Quantum cellular automata: The physics of computing with arrays of quantum dot molecules. In Proceedings of the PhysComp 94: Workshop on Physics and Computing, Dallas, TX, USA, 17–20 November 1994; pp. 5–13.
12. Cho, H.; Swartzlander, E.E. Adder and multiplier design in quantum-dot cellular automata. *IEEE Trans. Comput.* **2009**, *58*, 721–727. [CrossRef]

13. Pudi, V.; Sridharan, K. Low Complexity Design of Ripple Carry and Brent–Kung Adders in QCA. *IEEE Trans. Nanotechnol.* **2011**, *11*, 105–119. [CrossRef]
14. Hayati, M.; Rezaei, A. Design of novel efficient adder and subtractor for quantum-dot cellular automata. *Int. J. Circuit Theory Appl.* **2014**, *43*, 1446–1454. [CrossRef]
15. Mohammadi, M.; Mohammadi, M.; Gorgin, S. An efficient design of full adder in quantum-dot cellular automata (QCA) technology. *Microelectron. J.* **2016**, *50*, 35–43. [CrossRef]
16. Hanninen, I.; Takala, J. Robust adders based on quantum-dot cellular automata. In Proceedings of the 2007 IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP), Montreal, QU, Canada, 9–11 July 2007.
17. Ahmad, F.; Bhat, G.M.; Khademolhosseini, H.; Azimi, S.; Angizi, S.; Navi, K. Towards single layer quantum-dot cellular automata adders based on explicit interaction of cells. *J. Comput. Sci.* **2016**, *16*, 8–15. [CrossRef]
18. Erniyazov, S.; Jeon, J.-C. Carry save adder and carry look ahead adder using inverter chain based coplanar QCA full adder for low energy dissipation. *Microelectron. Eng.* **2019**, *211*, 37–43. [CrossRef]
19. Abedi, D.; Jaberipur, G.; Sangsefidi, M. Coplanar Full Adder in Quantum-Dot Cellular Automata via Clock-Zone-Based Crossover. *IEEE Trans. Nanotechnol.* **2015**, *14*, 497–504. [CrossRef]
20. Sandhu, A.; Gupta, S. Performance evaluation of an efficient five input majority gate design in QCA nanotechnology. *Iran. J. Sci. Technol. Trans. Electr. Eng.* **2019**, *8*, 194–205. [CrossRef]
21. Safoev, N.; Jeon, J.-C. Design of high-performance QCA incrementer/decrementer circuit based on adder/subtractor methodology. *Microprocess. Microsyst.* **2020**, *72*, 102927. [CrossRef]
22. Liu, W.; Lu, L.; O'Neill, M.; Swartzlander, E.E. A First Step Toward Cost Functions for Quantum-Dot Cellular Automata Designs. *IEEE Trans. Nanotechnol.* **2014**, *13*, 476–487. [CrossRef]
23. Moosavi, N.; Navi, K.; Aghazarian, V. Ultra-Low Cost Full Adder Cell Using the nonlinear effect in Four-Input Quantum Dot Cellular Automata Majority Gate. *Int. J. Nonlinear Anal. Appl.* **2020**, *11*, 1–16. [CrossRef]
24. Zoka, S.; Gholami, M. A novel efficient full adder–subtractor in QCA nanotechnology. *Int. Nano Lett.* **2018**, *9*, 51–54. [CrossRef]
25. Majeed, A.H.; Bin Zainal, M.S.B.; Alkaldy, E.; Nor, D.M. Full Adder Circuit Design with Novel Lower Complexity XOR Gate in QCA Technology. *Trans. Electr. Electron. Mater.* **2020**, *21*, 198–207. [CrossRef]
26. Sasamal, T.N.; Mohan, A.; Singh, A.K. Optimal realization of full adder in QCA using 5-input majority gate. In Proceedings of the 2020 International Conference on Industry 4.0 Technology (I4Tech), Pune, India, 13–15 February 2020.
27. Hashemi, S.; Tehrani, M.; Navi, K. An efficient quantum-dot cellular automata full-adder. *Sci. Res. Essays* **2012**, *7*, 177–189.
28. Balali, M.; Rezai, A.; Balali, H.; Rabiei, F.; Emadi, S. Towards coplanar quantum-dot cellular automata adders based on efficient three-input XOR gate. *Results Phys.* **2017**, *7*, 1389–1395. [CrossRef]
29. Srivastava, S.; Sarkar, S.; Bhanja, S. Estimation of Upper Bound of Power Dissipation in QCA Circuits. *IEEE Trans. Nanotechnol.* **2008**, *8*, 116–127. [CrossRef]
30. Srivastava, S.; Asthana, A.; Bhanja, S.; Sarkar, S. QCAPro-an error-power estimation tool for QCA circuit design. In Proceedings of the 2011 IEEE International Symposium of Circuits and Systems (ISCAS), Rio de Janeiro, Brazil, 15–18 May 2011.