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A 1.2 V 0.4 mW 20~200 MHz DLL Based on Phase Detector Measuring the Delay of VCDL

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Abstract: A delay locked loop (DLL) based on a Phase Detector, which Measures the Delay of the Voltage-controlled delay line (PD-MDV), which is t_{VCDL}, with efficient and stable locking performance was proposed. In contrast to conventional phase detectors, the PD-MDV measures t_{VCDL} more accurately; thus, it can always generate the correct up/down (UP/DN) pulses. The proposed technique prevents becoming stuck in the fastest operation, in which UP pulses continue to appear even when $t_{VCDL} < t_{REF}$, where t_{REF} is the reference time, which is an input of the DLL. In the reverse case, the PD-MDV prohibits DN pulses from continuing to appear under the condition $t_{VCDL} > t_{REF}$, thereby freeing the DLL from harmonic locking and becoming stuck in the slowest operation. The proposed phase detection scheme was verified under various conditions, including process corners, temperature variations, and abrupt changes in t_{REF}. The proposed 1.2 V, 20~200 MHz DLL with the PD-MDV was designed using the 65 nm process, with a power consumption of 0.4 mW at 200 MHz.

Keywords: delay locked loop; false lock; harmonic locking; stuck in; phase detector; fast locking; voltage-controlled delay line

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1. Introduction

The delay locked loop (DLL), first published in 1961 [1], is a circuit with a long history of dedicated research. The conceptual diagram of a basic DLL is shown in Figure 1. The phase detector (PD) detects the phase difference between the reference clock (REF) and the delayed version of the REF signal (DLY), and this difference is converted into the control voltage (V_{CTRL}) via a charge pump and loop filter. V_{CTRL} and bias voltage (V_{BP}) for PMOS that copies the current by V_{CTRL} become the input of the voltage-controlled delay line (VCDL) and adjusts the phase of the DLY signal. Therefore, the DLL is a negative feedback system that minimizes the phase difference through V_{CTRL}.

Owing to its simplicity, the PD structure shown in Figure 1 is the most widely used one. Up (UP) and down (DN) as outputs of the PD indicate the two outputs of D flip-flops (DFFs). As shown in case A of Figure 2, if the rising edge of REF is faster than DLY after both D flip-flops are reset at the same time, the pulse width of the UP becomes wider than that of DN. The wider the UP width, the shorter the delay because the output V_{CTRL} of the loop filter goes up. On the other hand, as shown in case B of Figure 2, if the rising edge of DLY is faster than REF, the pulse width of DN becomes wider than that of UP. The wider the DN width, the longer the delay because the V_{CTRL} goes down. Figure 2 shows two completely different results that appear despite the same conditions as the 1st $t_{VCDL} > t_{REF}$, wherein t_{VCDL} means the total delay of the VCDL, and t_{REF} is the reference time of REF. For such a condition, the designer should be aware that the PD has to output a wider UP to shorten the subsequent t_{VCDL} such as the 2nd, 3rd, 4th, and so forth, so that the final t_{VCDL} becomes equal to t_{REF}. Case A of Figure 2 shows the normal locking process as intended by a designer, and as a result, the 5th REF and 4th DLY are in phase, whereas

case B of Figure 2 shows the detailed process of falling into second harmonic locking due to the wrong operation of PD. For the section of the 1st~2nd t_{REF}, although the 1st t_{VCDL} was obviously longer than t_{REF}, the PD outputs a wider DN, and more delay was caused by the lowered V_{CTRL}. Even in the next section, the same operation is repeated and eventually the rising edges of the 5th REF and 3rd DLY coincide. This means that t_{VCDL} is equal to twice t_{REF} and is the second harmonic locking. In addition, while the PD can output a wider UP pulse despite the minimum t_{VCDL}, it can also output a wider DN despite the maximum t_{VCDL}. The former is stuck in the fastest operation, and the latter is stuck in the slowest operation. Strictly speaking, these harmonic locking and stuck-in issues are caused by the initial state of the DFFs inside the PD rather than the wrong operation of the PD, and the bigger problem is that the correct state of the DFFs cannot be guaranteed when the DLL starts up or the frequency of REF changes abruptly.

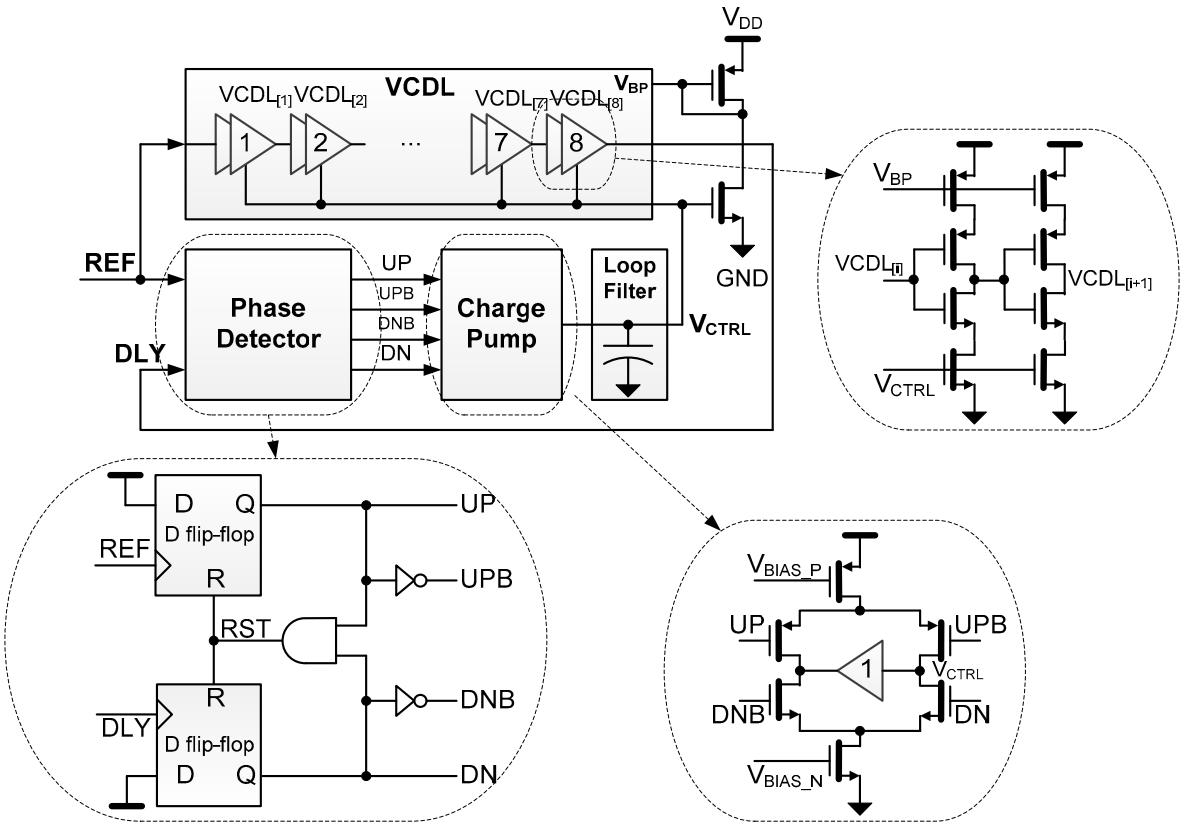

Figure 1. Basic DLL architecture.

Several studies have been conducted to solve the false locking problem caused by using this simple PD structure [2–13]. The technique in [6] using an external reset pulse makes it possible to escape from the false lock state, but does not actively respond to situations such as sudden changes in the reference signal. The DLL in [7] adopted a complicated algorithm for the false lock issue with multiphase clocks. The DLL with a wide locking range as in [9] used the proper band-selection technique, requiring an additional digital-to-analog converter and many digitally controlled delay cells. The methods using a time-to-digital converter (TDC) [12] or extra replica delay cells [13] consumed high power and required a large area.

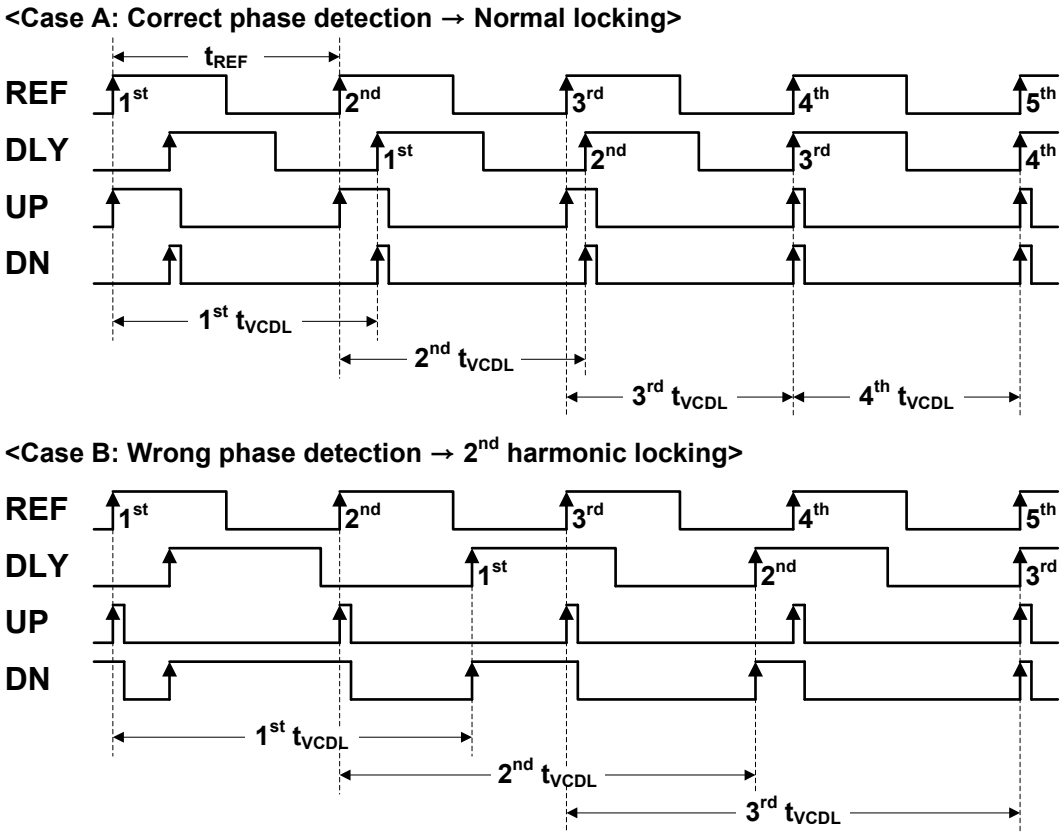

Figure 2. Two different operations of conventional PD under the same input condition as 1st $t_{VCDL} > t_{REF}$ (Case A: Correct phase detection; Case B: Wrong phase detection).

The issues of harmonic locking and becoming stuck in the fastest/slowest operation could be simultaneously solved if the new PD was able to provide information about whether t_{VCDL} is longer than t_{REF}, because all the issues stem from using an extremely simple conventional phase detector that only outputs the phase difference between DLY and REF. This study proposes the Phase Detector to Measure the Delay of VCDL (PD-MDV), to improve the existing PD. The newly proposed PD-MDV can be implemented with less complexity by adding the same number of DFFs as the VCDL unit and can provide the efficient locking time, as it rarely outputs wrong UP/DN pulses.

2. Proposed DLL with PD-MDV

A schematic of the structure of the proposed PD-MDV DLL is shown in Figure 3. For a proof of concept of the PD-MDV, conventional circuits for the charge pump and VCDL are used, as shown in Figure 1. The proposed PD-MDV consists of two parts, a shift register part and an UP/DN generation part, as shown in Figure 4. The shift register is implemented with nine DFFs, i.e., as many as the number (eight stages) of VCDL units plus 1. As the conventional PD is already configured with two DFFs, the increased number of DFFs is eight. The UP/DN generation part is composed of a DFF and few logic gates. The UP/DN generation is discussed in detail in Section 2.5. Compared to [2], the PD-MDV is much simpler. Sections 2.1–2.4 explain how the phase detector measures the delay of the VCDL. Subsequently, we explain how the proposed PD-MDV works for three cases (Sections 2.1–2.3) according to the time difference between t_{REF} and t_{VCDL}. Section 2.5 describes the characteristics of the VCDL.

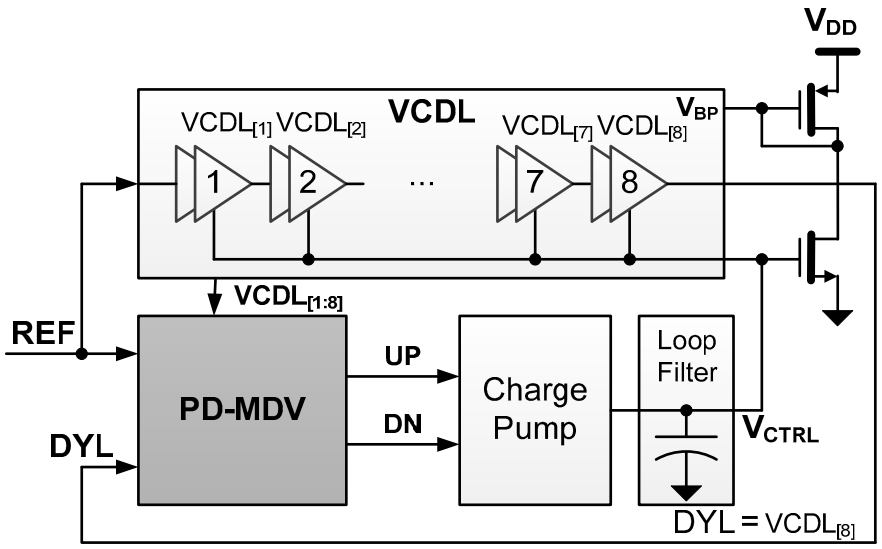

Figure 3. The structure of the proposed PD-MDV DLL.

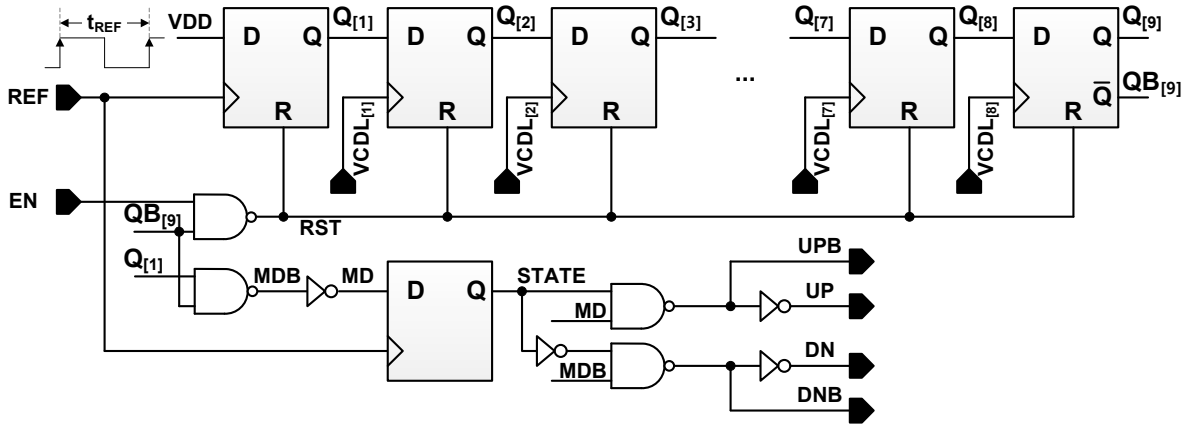

Figure 4. Proposed PD-MDV schematic.

2.1. Case 1: PD-MDV Operation with Fixed High V_{CTRL} for $t_{VCDL} < t_{REF}$

Figure 5 is a timing diagram illustrating the PD-MDV operation for $t_{VCDL} < t_{REF}$ where the *8*th output of $VCDL_{[8]}$ precedes the REF wherein $VCDL_{[i]}$ is the output of the i-th delay cell. If the rising edges of all VCDL outputs are expressed together with the rising edge of REF, $\Sigma VCDL_{[i]}$ is obtained. The total length of the gray area represents the measured delay of the VCDL and is called MD, which stands for the total delay of VCDL. The first DFF of the shift register is triggered by REF to output $Q_{[1]}$ as '1', where $Q_{[n]}$ is defined as the output of the n^{th} DFF. Subsequent DFFs are also triggered by $VCDL_{[i]}$ to sequentially output $Q_{[i+1]}$ as '1'. As the signal width of MD is conceptually defined as the time duration from the rising edge of REF to the rising edge of $VCDL_{[8]}$, the MD is implemented as the AND-gate output of ($QB_{[9]}$ and $Q_{[1]}$). As $t_{VCDL} < t_{REF}$, the wider DN signal is required, which is the same as the inversion signal of MD (MDB), and that the UP signal is not needed. The STATE is updated with the MD value at the rising edge of the REF, and its value for Case 1 is always '0' because the rising edge of the MD is the delayed version of the first rising edge of the earliest clock REF, as the sum of a DFF delay for $Q_{[1]}$ and an AND gate delay. The design of the UP/DN signal according to the STATE is explained after examining the PD-MDV operation under different conditions in Sections 2.2 and 2.3.

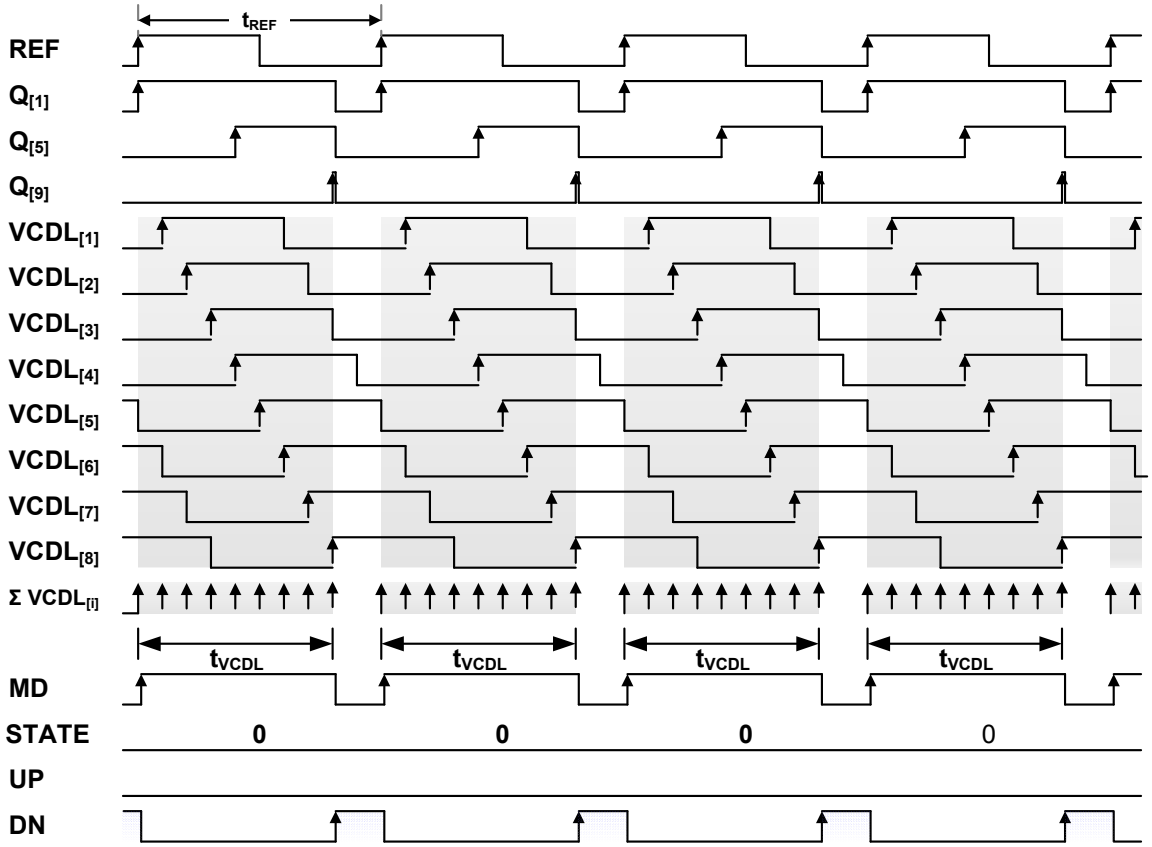

Figure 5. Timing diagram for the PD-MDV operation under the condition $t_{VCDL} < t_{REF}$.

2.2. Case 2: PD-MDV Operation with Fixed Middle V_{CTRL} for $t_{REF} < t_{VCDL} \leq 2 \cdot t_{REF}$

Figure 6 is a timing diagram for $t_{REF} < t_{VCDL} \leq 2 \cdot t_{REF}$. $\Sigma VCDL_{[i]}$, that is, the pulse width of MD is expressed as longer than t_{REF}. The desired UP signal is the remaining time minus the initial period of t_{REF} from the MD width. The STATE at the first rising edge of REF is '0'. However, at the second rising edge of the REF, t_{VCDL} is longer than t_{REF}. Thus, it becomes '1'. STATE outputs '0' and '1' alternately, and the UP signal outputs a single UP pulse every two cycles of the REF. Additionally, it should be noted that the DN signal is not needed. The difference is that the number of UP signals is reduced by half compared to the case in which the existing PD is used.

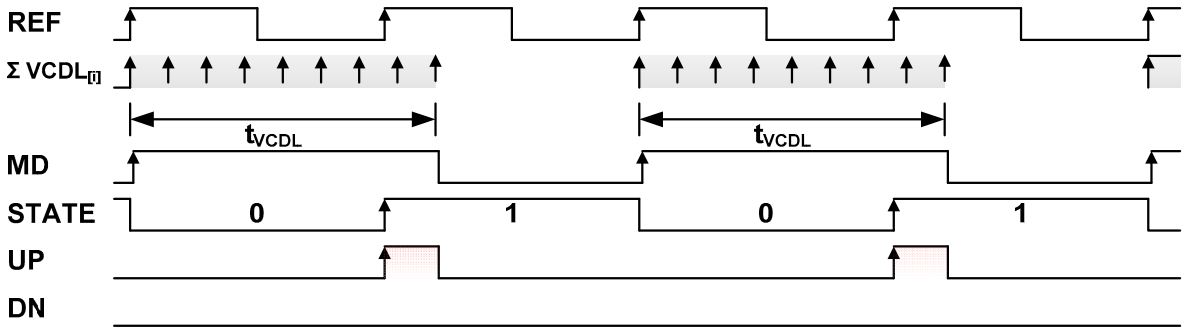

Figure 6. Timing diagram for the PD-MDV operation under the condition $t_{REF} < t_{VCDL} \leq 2 \cdot t_{REF}$.

2.3. Case 3: PD-MDV Operation with Fixed Low V_{CTRL} for $t_{VCDL} > 2 \cdot t_{REF}$

Figure 7 is a timing diagram for the case of $t_{VCDL} > 2 \cdot t_{REF}$. Compared to Figure 6, it can be seen that the pulse width of the MD is expressed longer than one cycle. The wider

UP signal is required, whereas the DN signal is not needed. Similarly, the STATE at the first rising edge of REF is '0'. However, during the second and third edges where the delay is measured, the rising edge of $VCDL_{[8]}$ still has not appeared. Therefore, MD is kept high, and STATE will repeat 011.

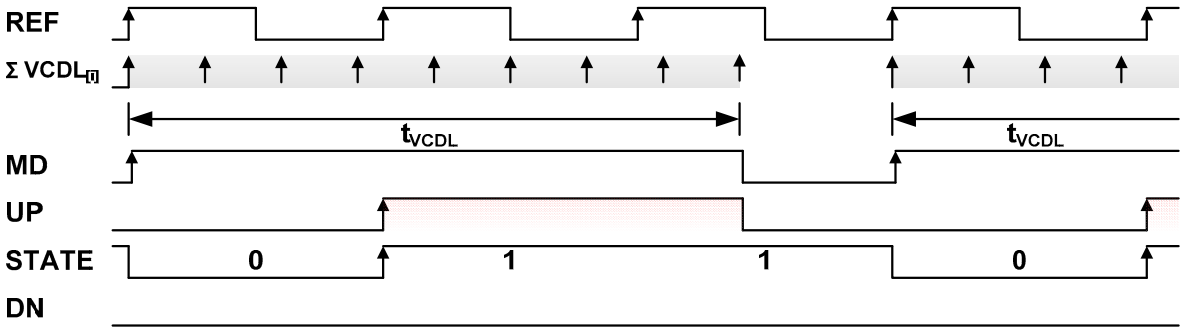

Figure 7. Timing diagram for the PD-MDV operation under the condition $t_{VCDL} > 2 \cdot t_{REF}$.

2.4. Understanding of STATE Signal

Note that only the DN is required in Case 1, and only the UP in Cases 2 and 3. The pulse width of UP and DN should be adjusted according to the measured delay, and the STATE signal plays a role in adjusting the pulse width. Table 1 summarizes the logical relationship between the UP/DN signals and the STATE signal is drawn in the timing diagram of Figures 5–7. Under the condition of STATE = '0', UP should output '0' and DN should output MDB, and under the condition of STATE = '1', UP should output MD and DN should output '0'. Therefore, the UP/DN generation part is configured as shown in Figure 4. STATE = '0' in the second row of the table means that the 1st t_{REF} period starts measuring t_{VCDL}. The delay measurement starts with the rising edge of REF. However, all other periods of t_{REF} are defined as STATE = '1'. For Case 1, as the first measurement is completed before the second rising edge, the second measurement should start on the second rising edge. Therefore, STATE is always '0'. The first '0' of '01' and '011', which are the STATE patterns of Cases 2 and 3, also means that the 1st t_{REF} period starts measuring t_{VCDL}. The timing diagrams in Figures 5–7 are drawn for the purpose of explanation under the condition that only the PD-MDV operates independently without feedback. If the proposed PD-MDV replacing the existing PD and the DLL is normally locked, UP and DN are output alternately, and STATE repeats 0 and 1 as shown in Figure 8.

Table 1. Logic table for UP/DB pulse generation.

	Case 1	**Case 2**	**Case 3**
STATE = '0'	DN = MDB UP = '0'	Same as the left	Same as the left
STATE = '1'	Nor occurred (Don't care)	DN = '0' UP = MD	Same as the left

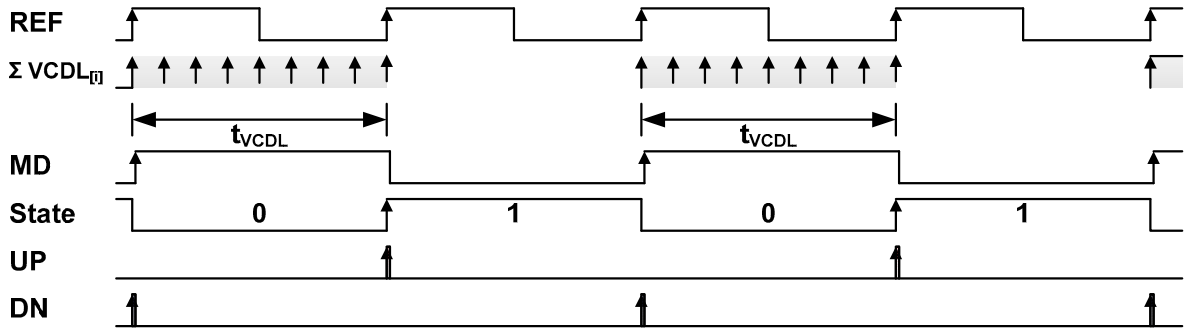

Figure 8. Timing diagram under condition of DLL locking with PD-MDV.

2.5. Design of Voltage-Controlled Delay Line

The VCDL unit is a current starved buffer [14], consisting of a total of eight stages, and is designed to operate even under slow, typical, and fast process corners, as well as under temperature variations of −55 °C to 125 °C. The voltage range of V_{CTRL} is determined by considering the frequency operating range of the DLL, which is from 20 MHz to 200 MHz for display interface applications [2,15,16]. Figure 9 shows the characteristics of the delay of the VCDL according to V_{CTRL}. The fastest corner condition on the 50 ns guideline for the 20 MHz operation is 'fast process + 125 °C'. Even under the condition of 'fast process + 125 °C', the DLL should operate with a 20 MHz clock input so that the V_{CTRL} is reduced to the lowest level ($V_{CTRL.min}$) of 0.27 V. In contrast, the slowest corner condition on the 5 ns guideline for 200 MHz operation is 'slow process + 125 °C'. Even under the condition of 'slow process + 125 °C', the DLL should operate with a 200 MHz clock input so that the V_{CTRL} increases to 0.67 V, which is the highest level ($V_{CTRL.max}$). Therefore, the output swing range of the charge pump is wide at 0.25~0.9 V.

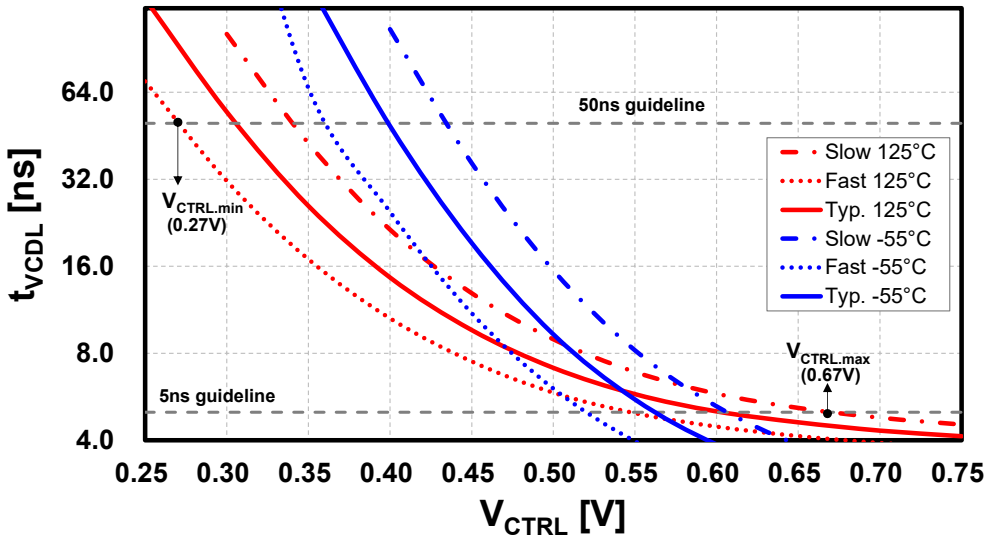

Figure 9. Characteristics of the delay of the VCDL according to V_{CTRL}, temperature, and process corner to design the output swing range of charge pump.

3. Performance Evaluations

The proposed DLL works well over the supply voltage of 1.1~1.3 V, process corners, and temperature variations. In order to consider parasitic components that cannot be adopted in the pre-layout simulation, parasitic capacitances were added to all signal nodes in consideration of the interconnected metal width and length. In addition to this, dedicated efforts such as unit cell layout and parasitic extraction were made to reflect more accurate parasitics in critical nodes. Figure 10 shows the locking behavior for 0 V initial conditions

of V_{CTRL}, causing a more extreme situation than Case 3. During locking (0~320 ns), the measured delay times of MD and UP are maintained at '1', and V_{CTRL} increases linearly to search the appropriate delay condition for locking. At about 320 ns, MD approaches the locking condition and outputs a low value for the first time. After that, V_{CTRL} reaches the locking condition, an MD signal is toggled, and V_{CTRL} is maintained nearly constant, resulting in the UP and DN signal outputted alternately. That is, the operating condition in Figure 8 has been verified by simulation. The linear rise in V_{CTRL} is evidence that the proposed technique has no abnormal operation according to the PD state, which means that the DLL with the PD-MDV is most efficiently locked. In addition, when the phase of t_{REF} is changed by 180° or when there is a sudden frequency change from 20 MHz to 200 MHz or vice versa, locking without any problem, in the same way as in Figure 10, has been verified for the PD-MDV. The proposed 1.2 V, 20~200 MHz DLL with a PD-MDV was designed using the 65 nm complementary metal-oxide-semiconductor process. The power consumption was 0.4 mW at 200 MHz. Figures of Merit (FoMs) related to energy efficiency, which is popular in processor and oscillator design and is defined as power consumption over the maximum operating frequency, were used to evaluate the DLL performance [17,18]. The FoM of the proposed DLL was 2 μW/MHz.

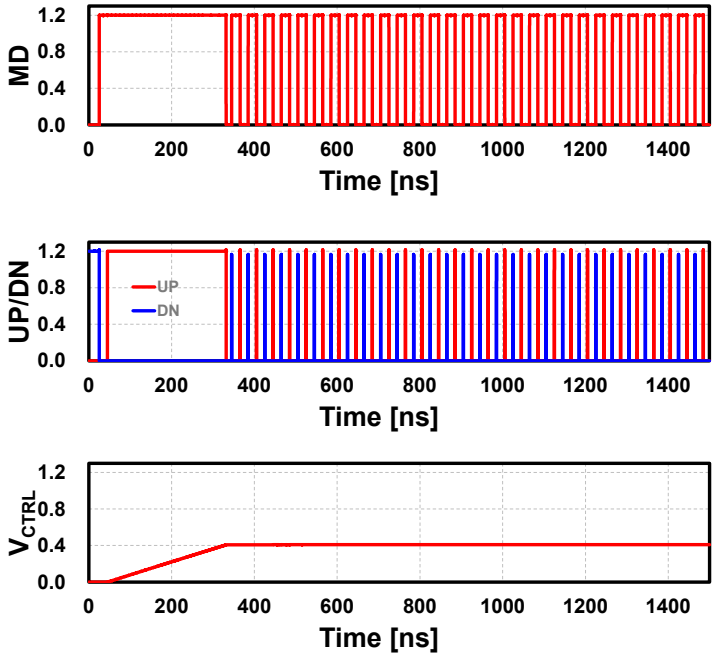

Figure 10. The locking behavior of the PD-MDV according to a 0 V V_{CTRL} initial condition at REF = 50 MHz.

Periodic jitter was measured based on a transient noise simulation. Figure 11a represents an overlapped waveform of the DLL output voltage obtained through an iterative 256-cycle transient simulation at 200 MHz after locking. The peak-to-peak jitter of 256 samples was simulated as ±5 ps, which arises from timing variation on the rising edges. In order to analyze rms and peak-to-peak jitter, the number of iterations was increased to 2500. Figure 11b shows the analyzed histogram results of the period jitter for 2500 samples. As shown in Figure 11b, the rms and peak-to-peak jitter were 3.1 ps and 22.0 ps at 200 MHz, respectively. In addition, the rms jitter at 20 MHz and 50 MHz (not shown here) was simulated as 78.8 ps and 24.2 ps, respectively. Table 2 summarizes the performance comparison with various DLLs that have solved the false locking issue or that have a similar operating frequency. The proposed structure exhibited a lower power consumption level with competitive period jitter characteristics. As a result, the proposed DLL shows one of the lowest figures-of-merit when compared with previous false-locking-free DLLs.

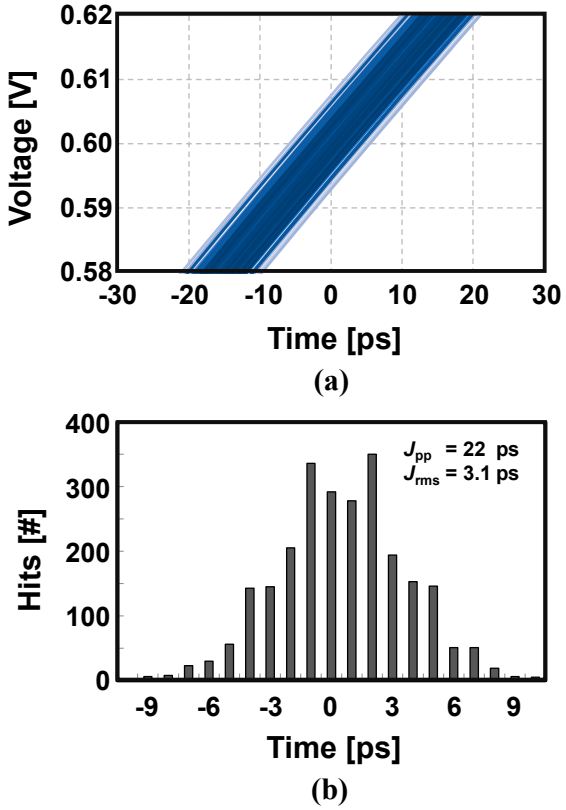

Figure 11. Jitter simulation at 200 MHz: (**a**) overlapped waveforms of 256 cycles; (**b**) histogram of 2500 samples.

Table 2. Performance Summary of the proposed PD-MDV DLL.

	[2]	[5]	[12]	[19]	[20]	This Work *
Process (nm)	150	130	250	55	180	65
Supply (V)	1.8	1.5	1.2	1.2	1.2	1.2
Freq. range (MHz)	20−135	80−450	32−320	560−800	125−875	20−200
Power Consumption (mW)	2.2 @130 MHz	26 @180 MHz	15 @320 MHz	6.92 @800 MHz	2.78 @250 MHz	0.4 @200 MHz
Efficiency FoM (μW/MHz)	16.9	125.6	46.9	8.7	11.1	2.0
Jitter RMS/Peak-to-Peak (ps) @f_{OUT}	−/192 @100 MHz	2.3/10 @180 MHz	4.4/15 @200 MHz	1.2/6.5 @800 MHz	2.1/4.4 @250 MHz	3.1/22 @200 MHz

** This work has only simulation results for proof of concept.*

4. Conclusions

As described in Sections 2.1–2.4, the PD-MDV was proposed to solve problems, such as the harmonic lock or becoming stuck in the fastest/slowest operation caused by the conventional PD. The new PD accurately measures t_{VCDL} to avoid outputting incorrect UP/DN signals. When observing the linear settling waveform of V_{CTRL}, the proposed technique contributes to the efficient locking of DLL. In contrast to previous approaches, the problems are solved in a very simplistic manner, by adding only the same number of DFFs as the delay unit. This idea was verified under various conditions, including process corners, temperature variations, start-up conditions, and abrupt changes in t_{REF}.

Author Contributions: S.-H.C. conceived the idea. S.-H.C. and Y.-K.C. co-wrote and edited the manuscript. S.-H.C. suggested the initial idea of the phase detector and designed the circuits. All authors discussed the results and commented on the manuscript. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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