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Design of a Power Regulated Circuit with Multiple LDOs for SoC Applications

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Abstract: In this paper, a power regulated circuit (PRC) is proposed for system-on-a-chip (SoC) applications. The proposed PRC is composed of a limiter, a bandgap reference (BGR), three low-dropout regulators (LDOs), and a bias generator. A high output voltage of an active rectifier is given to the limiter, which limits it to a desired supply voltage for circuits in PRC. The curvature-compensated BGR robust to process, voltage and temperature (PVT) variations are designed to provide a stable reference voltage for three LDOs. The three LDOs are implemented to generate regulated output dc voltages. The proposed PRC is designed and fabricated in 130 nm bipolar-CMOS-DMOS (BCD) technology with die area of 1.9 mm × 0.860 mm, including pads. The measurement results show that the limiter limits the input voltage of (6 V to 20 V) to 5.3 V. The BGR produces a stable reference voltage of 1.24 V with a power supply rejection ratio (PSRR) of −58.6 dB and −51.9 dB at 10 Hz and 1 kHz, respectively. The LDO_5V, LDO_3V, and LDO_1.5V generate regulated output dc voltages of 5 V, 3 V, and 1.5 V, respectively, with dc load regulations of 0.43 mV/mA, 0.70 mV/mA, and 0.28 mV/mA while delivering load currents of 300 mA, 100 mA, and 100 mA, respectively.

Keywords: BCD technology; bandgap reference; low-dropout regulators; limiter; power regulated circuit (PRC)

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1. Introduction

During the past decade, wireless power transfer (WPT) has shown unprecedented development and has emerged as one of the promising technologies, especially near field (non-radiative) for wireless charging of electric vehicles, mobile phones, wearable devices, and implanted medical devices to improve user convenience and flexibility [1–5]. Near-field technology is sub-divided into two categories: inductive and capacitive coupling techniques for short-range applications, and magnetic resonance coupling techniques for mid-range applications [6]. Wireless Power Consortium (WPC) and Power Matters Alliance (PMA) standards are based on an inductive coupling technique [7,8], while Alliance for Wireless Power (A4WP) is based on a magnetic resonance coupling technique [9]. The operating frequency for WPC/PMA standards is from 87–357 kHz, while A4WP normally operates at 6.78 MHz. In our work, power is wirelessly transferred from the transmitter to the power receiving unit through A4WP standard. The power receiving unit is composed of an active rectifier, a dc–dc converter, a successive-approximation register (SAR) analog-to-digital converter (ADC), frequency detection, a protection block, a digital block, and a power-up circuit [10]. The active rectifier converts the incoming ac voltage into dc voltage and supplies it to the dc–dc converter and PRC to regulate it for battery and sub-blocks in the power receiving unit. This regulated dc voltage from PRC is also used as the supply voltage for SAR ADC, digital logic block, bias generator, and buffer circuits [11,12]. Since PRC is the subject of this research work, we will concentrate on its suggested architecture and performance.

Due to high increasing demands for wearable/portable devices such as tablet PCs, smartphones, laptops, smart watches, and wireless handsets, the use of power management systems is becoming increasingly important for prolonging the battery life of these devices [13]. A low-dropout (LDO) regulator is an essential block of power management integrated circuits (PMICs) that provide a clean and stable supply voltage to portable devices [14,15]. The high power supply rejection ratio (PSRR), improved line and load regulations, and stability are very demanding specifications for an analog LDO. The PSRR is the measure of how many ripples are rejected or suppressed by the LDO over a wide frequency range, and is expressed as [16,17]:

$$PSRR = 20log\left(\frac{V_{out,ripple}}{V_{in,ripple}}\right) \tag{1}$$

Recently, a number of techniques have been implemented to improve the abovementioned specifications for the LDO [18–20]. These techniques either employ a feed-forward ripple cancelation path or an adaptive path to improve the performance of the LDO. Ref. [21] reports a digital LDO (DLDO) with a feed-forward controller and weight redistribution algorithm (WRA) for line regulation improvement with a transient pump circuit to reduce the undershoot. An event-driven DLDO with an adaptive linear/binary two-step search is presented in [22] to achieve a fast transient response. The adaptive linear search is offered by a two-dimensional circular shift register. A DLDO with a voltage-controlled oscillator (VCO)-based control is described in [23]. The frequencies of the two VCOs in the control loop are controlled by the output voltage and the reference level, respectively. The VCO-based control is a hybrid of analog and digital control schemes. A transient detector is used to improve the transient speed of the DLDO regulator. Similarly, bandgap reference (BGR) generates a reference (fixed) voltage regardless of supply variations, process, temperature changes and circuit loading conditions [24]. The BGR is widely used in many sub-systems such as LDO, a dc–dc converter, SAR ADC, DAC converters, and memories [25]. The bipolar junction transistor (BJT)-based BGR designs are less sensitive to process variations compared to pure-MOSFET designs [26], and can obtain accurate and scalable output [27] among all BGR topologies. There are factors that affect the accuracy of BGR, such as (a) non-linear relation between base-emitter voltage (V_{BE}) of BJT and temperature, (b) input offset voltage of operation amplifier for generation of complementary-to-absolute-temperature (CTAT) and proportional-to-absolute-temperature (PTAT) characteristics, and (c) process variations [28]. The V_{BE} of the BJT transistor has a negative temperature co-efficient (TC) (i.e.,) CTAT. The difference between base-emitter voltages of two BJT transistors that have different current densities results in positive TC (i.e.,) PTAT. The V_{BE} of BJT transistor can be written as [29].

$$V_{BE} = V_T ln\left(\frac{I_C}{I_S}\right) \tag{2}$$

where $V_T = kT/q$ is the thermal voltage, k is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge of an electron. I_C and I_S are the collector and saturation current, respectively. The CTAT of V_{BE} can be expressed as:

$$\frac{dV_{BE}}{dT} = \left(\frac{V_{BE} - (4+m)V_T - E_g/q}{T}\right) \tag{3}$$

where E_g is the bandgap energy of silicon. Similarly, PTAT due to a difference of V_{BE} of two BJT transistors operating at unequal current densities is shown as:

$$\Delta V_{BE} = V_T ln\left(\frac{nI_o}{I_S}\right) - V_T ln\left(\frac{I_o}{I_S}\right) = V_T ln(n) \tag{4}$$

By solving (3) and (4), we can develop a reference voltage that has nominally zero TC. Mathematically,

$$V_{REF} = \alpha_1 V_{BE} + \alpha_2 V_T ln(n) \tag{5}$$

where α_1 is normally equal to one, and α_2 is the ratio of the resistors used in the BGR circuit. Therefore, by choosing the optimum value of the resistors ratio and n, we can generate reference voltage with near-to-zero TC.

In this research work, a power regulated circuit (PRC) for a power receiving unit is presented for system-on-a-chip (SoC) applications. The proposed PRC provides regulated and stable dc voltages for different load conditions, and also serves as supply voltage for sub-blocks such as SAR ADC, digital blocks, bias generator, and buffer circuits in the power receiving unit. The rest of the paper is organized as follows: Section 2 illustrates the block diagram of the proposed PRC. Section 3 discusses the sub-blocks used in the proposed work. Section 4 depicts measurement results. Finally, Section 5 concludes the paper.

2. Proposed Power Regulated Circuit (PRC)

Figure 1 illustrates a block diagram of the proposed PRC used in the power receiving unit. The proposed PRC is composed of a limiter, a BGR circuit, three LDOs, and a bias generator. The active rectifier in the the power receiving unit receives ac voltage of 6.78 MHz frequency and generates a dc voltage (V_{RECT}). The limiter in the PRC limits V_{RECT} to a desired dc voltage level (V_{LIMIT}) and used as a supply voltage for BGR and three LDOs. The supply voltage of the bias generator comes from the output of LDO_3V. The BGR circuit generates a standard reference (fixed) voltage (V_{REF}), regardless of process–voltage–temperature (PVT) variations and circuit load conditions. The standard V_{REF} value lies in the range of 1.2 V to 1.25 V. This V_{REF} is then used in three LDOs and the bias generator circuit. The three LDOs, LDO_5V, LDO_3V, and LDO_1.5V, are designed for different load conditions.

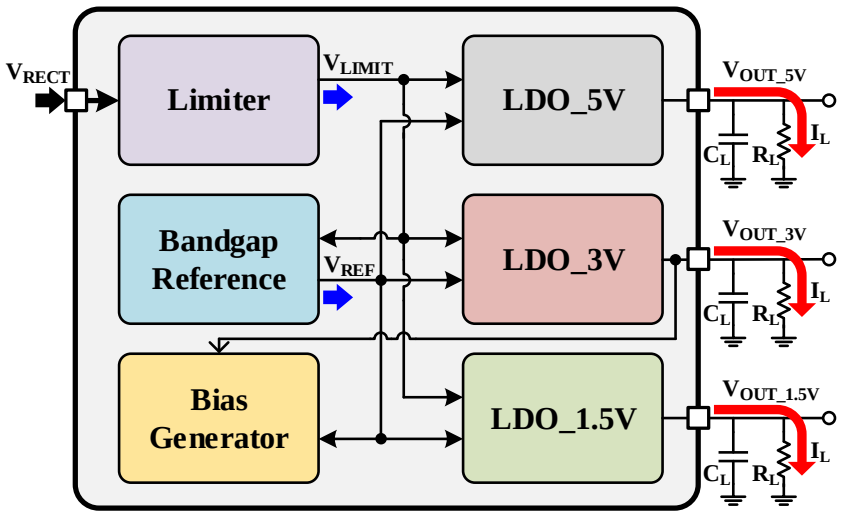

Figure 1. Block diagram of the proposed power regulated circuit (PRC).

3. Circuit Description

3.1. Limiter Design

Figure 2 shows the circuit diagram of the limiter used in the proposed PRC. The limiter circuit consists of a zener diode (D_1), high-voltage (24 V) PMOS (M_{P1} and M_{P2}), and a NMOS transistor (M_{N1}). A high-output dc voltage of an active rectifier is fed to the limiter circuit, which limits it to a desired dc voltage level for supply of other circuits such as BGR, three LDOs, and bias generator in the PRC. A bias voltage is given to the gates of M_{P1} and M_{P2} to turn them on and allows the current to flow in the circuit. An optimum gate voltage for M_{N1} is a developed courtesy resistor (R_2), zener diode (D_1), and a capacitor (C_1) to generate desired dc voltage (V_{LIMIT}) at the output, as shown in Figure 2. This limiter circuit can draw a current of 520 µA to support other blocks in the PRC.

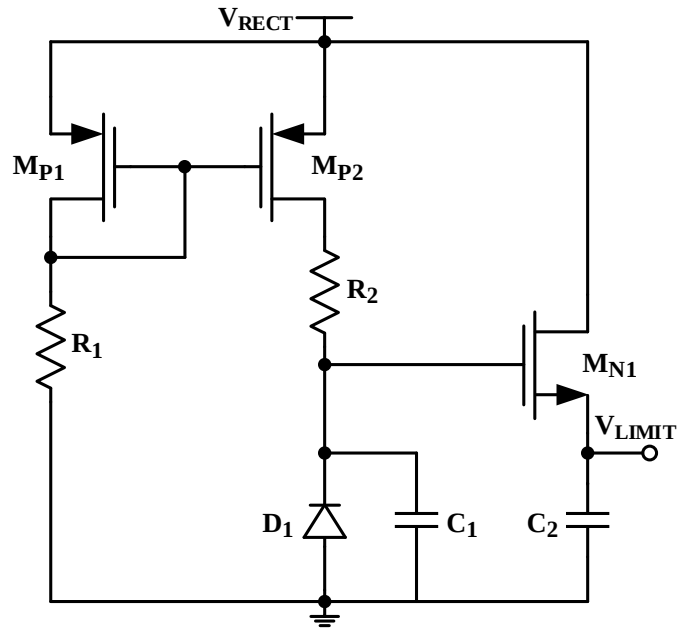

Figure 2. Circuit diagram of the proposed limiter in the PRC.

3.2. Bandgap Reference (BGR) Design

Figure 3 presents a circuit diagram of the BGR implemented in the PRC. A two-stage op-amp is used in the BGR. The op-amp adjusts the gate voltage of the PMOS transistors in order to equalize terminal voltages V_X and V_Y. In addition, the op-amp provides sufficient loop gain and an acceptable phase margin and bandwidth. The start-up circuit and op-amp provide a fast settling time to the BGR. The output voltage V_{REF} of the BGR exhibits a nominally zero TC. Performing Kirchhoff's voltage law (KVL) at V_X results in:

$$V_X = V_{BE1} \tag{6}$$

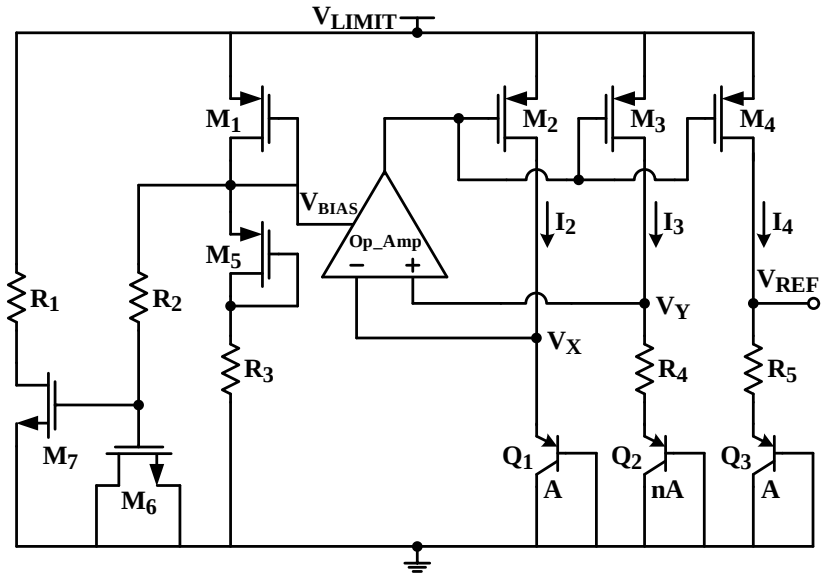

Figure 3. Circuit diagram of the proposed bandgap reference (BGR) in the PRC.

Similarly, applying KVL at V_Y results in:

$$V_Y = V_{BE2} + I_3 R_4 \tag{7}$$

Since op-amp equalizes V_X and V_Y, it can be written as:

$$I_3 = \frac{V_{BE1} - V_{BE2}}{R_4} \tag{8}$$

By putting (4) in (8), I_3 is given by:

$$I_3 = \frac{V_T ln(n)}{R_4} \tag{9}$$

Since, $I_3 = I_4$, the V_{REF} of the BGR can be written as:

$$V_{REF} = V_{BE3} + I_3 R_5 \tag{10}$$

$$V_{REF} = V_{BE3} + \left(\frac{V_T ln(n)}{R_4}\right) R_5 \tag{11}$$

Thus, V_{REF} with near-to-zero TC can be generated by finding the optimum values of n, R_4 and R_5.

3.3. Low-Dropout Regulator (LDO) Design

Figure 4 depicts a circuit diagram of the proposed LDO used in the PRC. The circuit structure for all three LDOs is the same. However, the sizes of the transistors, bias voltages, capacitors, resistors, and the PMOS pass transistor (M_P) are different for three LDOs. For instance, the width of M_P for LDO_5V, LDO_3V, and LDO_1.5V is 8 mm, 1.2 mm, and 0.8 mm, respectively, while the channel length is set to the minimum. A high open-loop gain error amplifier (EA) is used to provide an acceptable PSRR at the gate of the transistor M_G. The M_G acts as a common gate transistor between M_P and the output of the EA. The capacitor C_M provides stability to LDO by applying Miller's theorem. An NMOS transistor M_N is cascaded with M_P to improve the PSRR of the LDO. The M_N shields the M_P from power supply variations. The gate of M_N is biased using a simple RC filter, which further minimizes ripples at gate of the M_N. The open-loop gain (A_P) of M_P is given by:

$$A_P = g_P \left(\frac{R_{F1} + R_{F2}}{r_{oP}}\right) \tag{12}$$

where g_P and r_{oP} are the transconductance and output resistance of M_P, respectively. The feedback voltage (V_{FB}) can be written as:

$$V_{FB} = A \left(\frac{R_{F2}}{R_{F1} + R_{F2}}\right) \tag{13}$$

where A is the open-loop gain of EA. The closed–closed transfer function of the LDO is given by:

$$\frac{A_P}{1 + A_P V_{FB}} = \left(\frac{g_P \left(\frac{R_{F1}+R_{F2}}{r_{oP}}\right)}{1 + g_P \left(\frac{R_{F1}+R_{F2}}{r_{oP}}\right) \left(\frac{AR_{F2}}{R_{F1}+R_{F2}}\right)}\right) \tag{14}$$

If loop gain ($A_P V_{FB}$) is much higher than one, then PSRR can be related to the open loop gain as:

$$PSRR \approx \left(\frac{R_{F1} + R_{F2}}{A * R_{F2}}\right) \tag{15}$$

Thus, open-loop gain (A) and feedback resistors (R_{F1} and R_{F2}) play a critical role in the performance of the LDO.

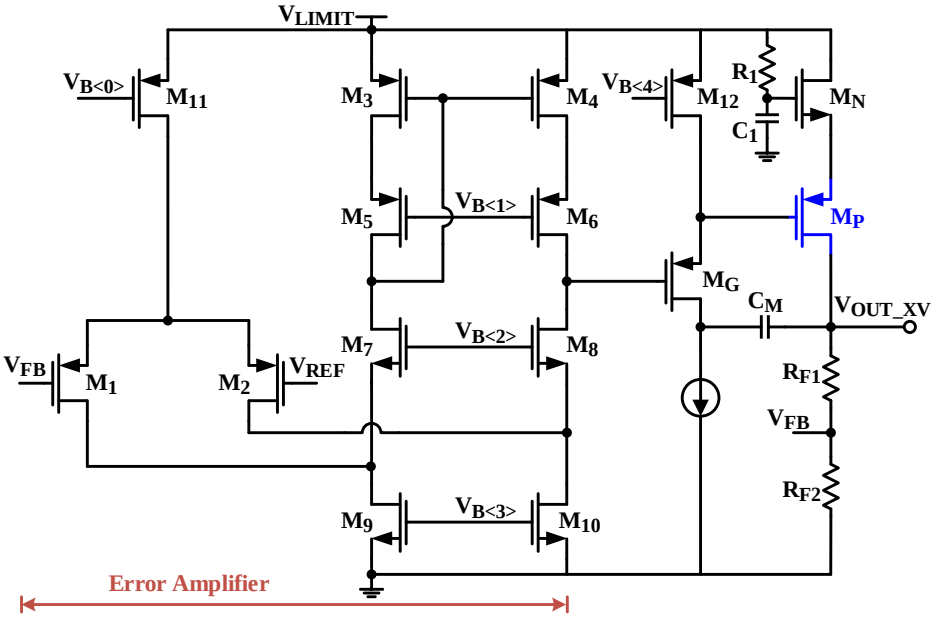

Figure 4. Circuit diagram of the proposed low-dropout regulator (LDO) in the PRC.

4. Measurement Results

Figure 5 shows the top layout pattern of the proposed PRC with a layout area of 1.9 mm × 0.860 mm, including pads. The circuit is designed and fabricated in a 130 nm BCD process.

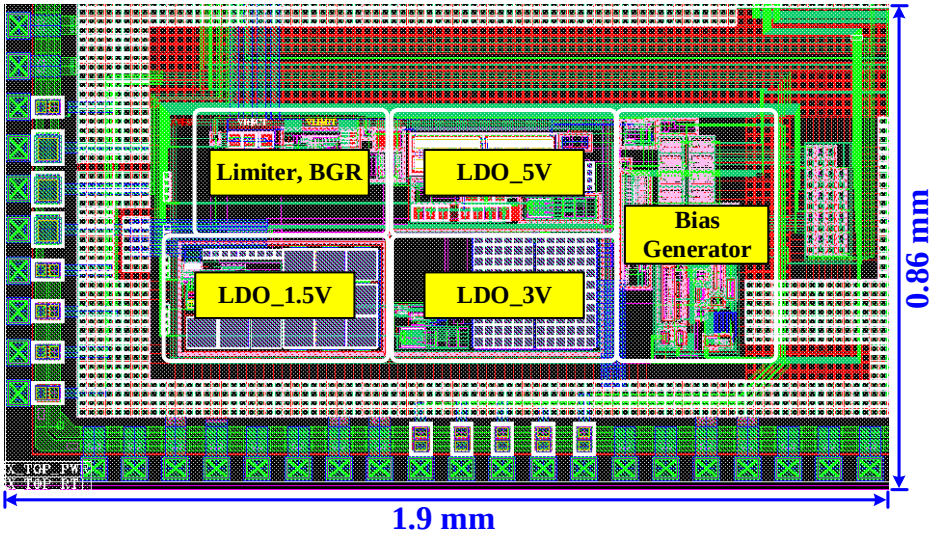

Figure 5. Top layout pattern of the proposed power regulated circuit (PRC).

Figure 6 demonstrates post layout simulation results of PRC. The supply voltage (V_{RECT} in this case) is swept from 0 to 20 V and back to 0 to check the performance of PRC. It can be seen that PRC operates normally in this supply range. The limiter produces a desired output voltage (V_{LIMIT}) of 5.3 V for this wide range of V_{RECT}. This V_{LIMIT} is used as a supply voltage for other circuits in the PRC. The BGR provides a stable reference voltage (V_{REF}) of 1.24 V. The BGR requires minimum V_{LIMIT} of 2 V. From 2 to 5.5 V, the BGR produces stable V_{REF} of 1.24 V. The LDO_5V, LDO_3V, and LDO_1.5V generate regulated output dc voltages (V_{OUT_5V}, V_{OUT_3V}, and $V_{OUT\_1.5V}$) of 5.004 V, 3.003 V, and 1.5001 V, respectively. The total current consumption of PRC is 176.4 µA.

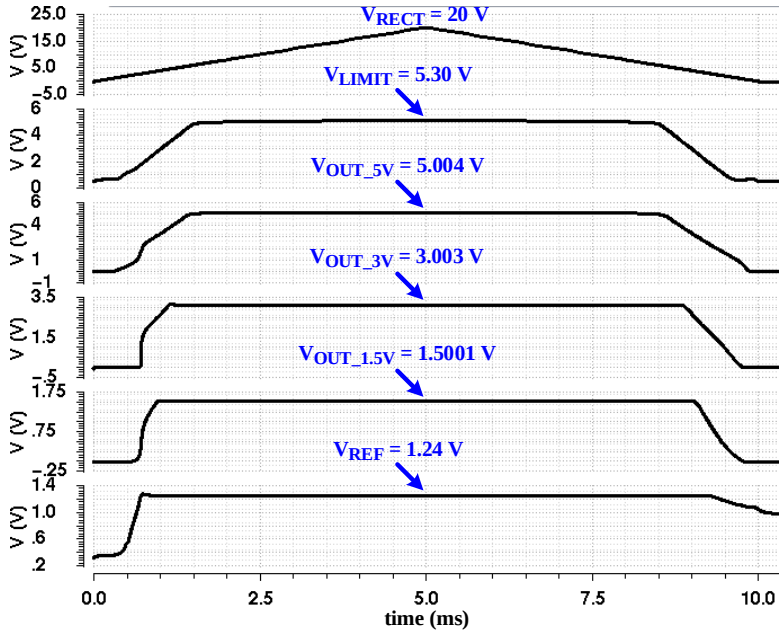

Figure 6. Top simulation results of the proposed power regulated circuit (PRC).

Figure 7 displays post-simulation results of the BGR. Figure 7a shows the result of 200 Monte Carlo runs for the BGR. The mean value of the BGR for 200 runs is 1.24 V, with standard deviation of 28.49 mV. Here, all the mismatch (including CMOS transistors, resistors, and BJT transistors) and process variations in the BGR circuit are considered. The mismatch shows a shift (left or right) in the output voltage (V_{REF}) caused by the non-idealities. Figure 7b presents V_{REF} for different corner cases (SS, TT, and FF) over a temperature range from −40 °C to 100 °C. The maximum deviation (ΔV) in V_{REF} for this temperature range is 11.7 mV, which is acceptable and satisfies TC of the BGR. The mean value of V_{REF} at 30 °C is 1.24 V. Figure 7c depicts PSRR of the BGR for different corner cases. The values of PSRR at 10 Hz frequency for SS (4.5 V, 100 °C), TT (5 V, 30 °C), and FF (5.5 V, −40 °C) are −55.7 dB, −58.6 dB, and −59.3 dB, respectively. Similarly, values of PSRR at 1 kHz for SS, TT, and FF are −49.1 dB, −51.9 dB, and −54.1 dB, respectively. This demonstrates good PSRR over a wide frequency range. Figure 7d shows a stability check of the BGR for different corner cases. The loop gain and phase margin of BGR for SS, TT, and FF conditions are (87.2 dB, 64.5°), (83.5 dB, 63.2°), and (77.1 dB, 60.5°), respectively. These results show that the proposed BGR operates well regardless of the PVT variations.

Figure 8 demonstrates measured results of LDO_5V. Figure 8a shows load transient response from 100 µA to 100 mA. The LDO_5V displays a stable settling behavior with a 1 µF output ceramic capacitor. The maximum undershoot and overshoot are 88 mV and 126 mV, respectively, with a 100 mA step load current. Similarly, Figure 8b presents a load transient response from 300 mA to 200 mA, with maximum overshoot and undershoot of 137 mV and 108 mV, respectively. Figure 8c depicts load regulation for a wide range of load current, 10 µA to 300 mA. The dc fluctuation in the output voltage is nearly 130 mV over the wide load current range, which is 2.6% of the output voltage (V_{OUT_5V} = 5 V). Figure 8d shows line regulation for input voltage range of 5.3 V to 7.1 V at 300 mA load current. The dc variation in the output voltage is 45 mV, which shows good line regulation.

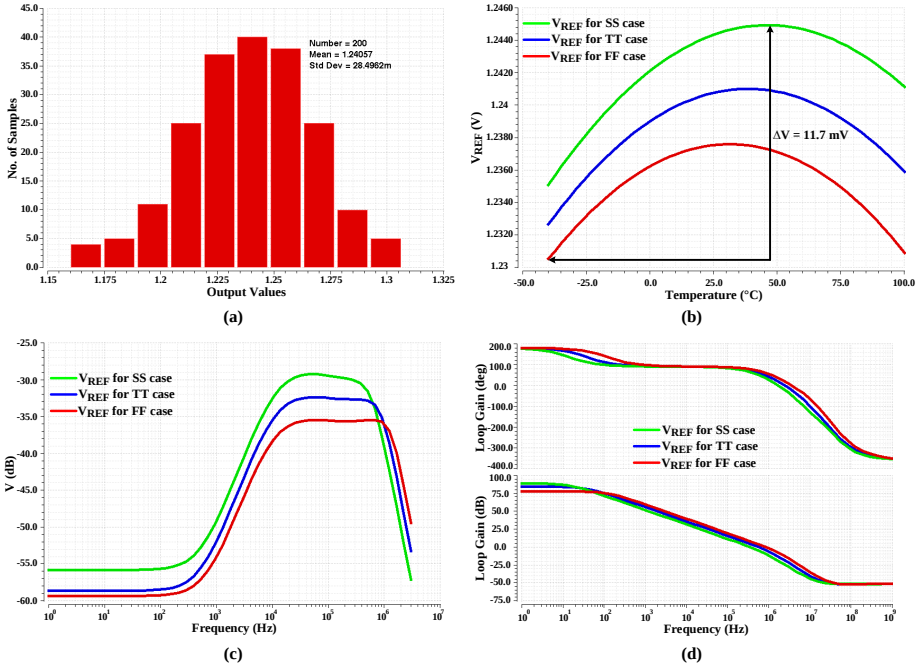

Figure 7. Post-simulation results of the proposed BGR. (**a**) Monte Carlo simulation. (**b**) Output voltage's variation over temperature range. (**c**) PSRR for different corner cases. (**d**) Stability check.

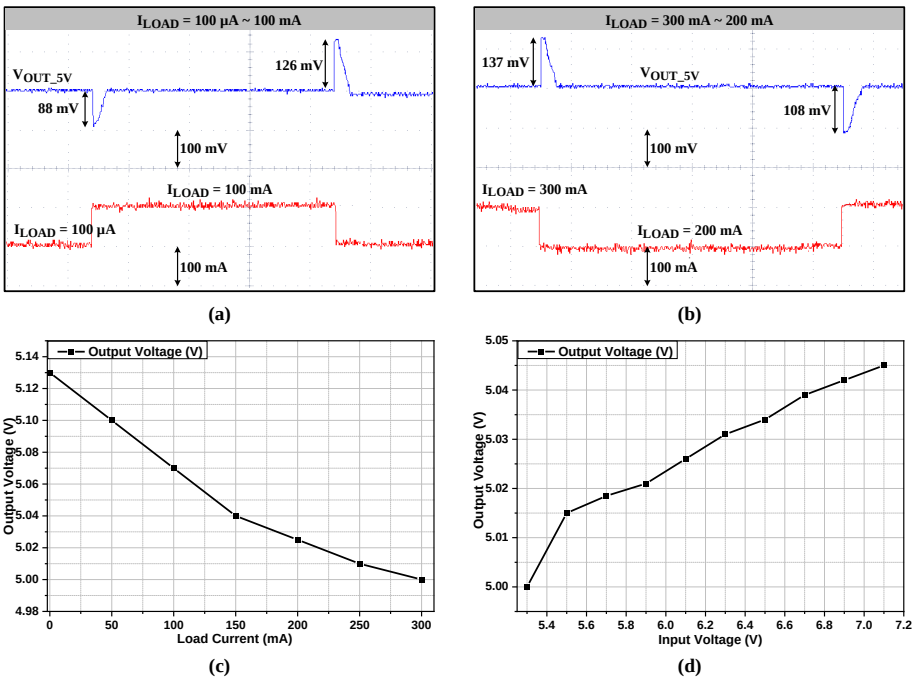

Figure 8. Measured results of LDO_5V. (**a**) Load transient response from 100 µA to 100 mA. (**b**) Load transient response from 300 mA to 200 mA. (**c**) Load regulation. (**d**) Line regulation.

Figure 9 shows measurement results of LDO_3V. Figure 9a depicts a load transient response from 100 µA to 100 mA with maximum undershoot and overshoot of 72 mV and 96 mV, respectively. Figure 9b displays load regulation for a load current ranging from 10 µA to 100 mA. The dc variation in the output voltage is around 70 mV, which is 2.34% of the output voltage (V_{OUT_3V} = 3V). Figure 9c presents line regulation at 100 mA load current for input range of 5.3 V to 6.5 V. The dc variation in output voltage for this input voltage range is 56 mV.

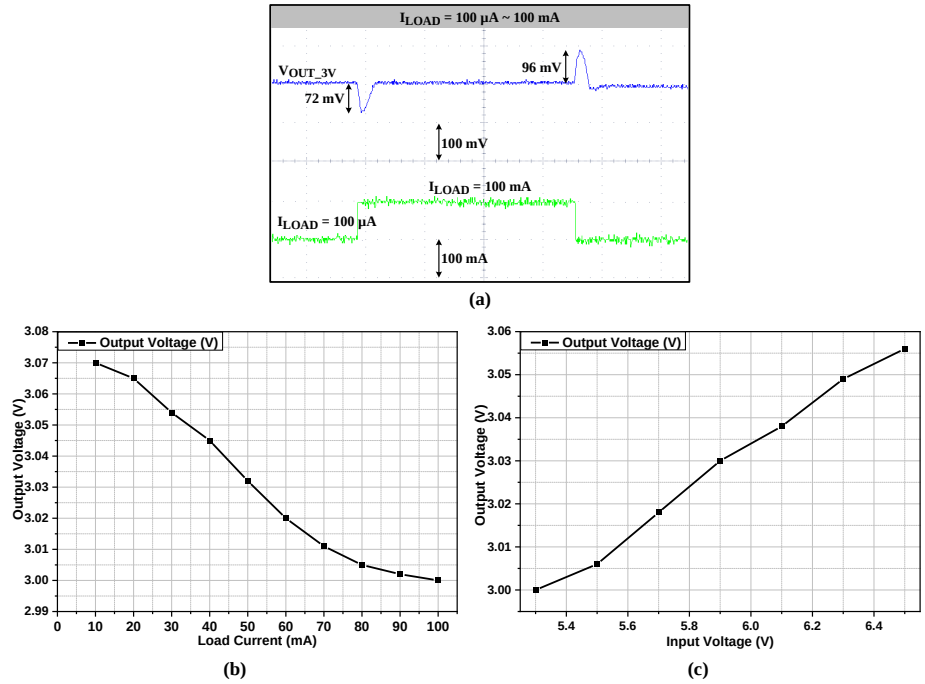

Figure 9. Measured results of LDO_3V. (**a**) Load transient response from 100 µA to 100 mA. (**b**) Load regulation. (**c**) Line regulation.

Figure 10 presents measured results of LDO_1.5V. Figure 10a shows load transient response from 100 µA to 100 mA with maximum undershoot and overshoot of 62 mV and 84 mV, respectively. Like LDO_3V, LDO_1.5V is designed for the same load current condition of 10 µA to 100 mA. Figure 10b depicts load regulation with dc variation in output voltage of around 28 mV, which is 1.86% of the output voltage ($V_{OUT\_1.5V}$ = 1.5 V). Figure 10c displays line regulation at 100 mA load with dc variation in the output voltage of around 71 mV.

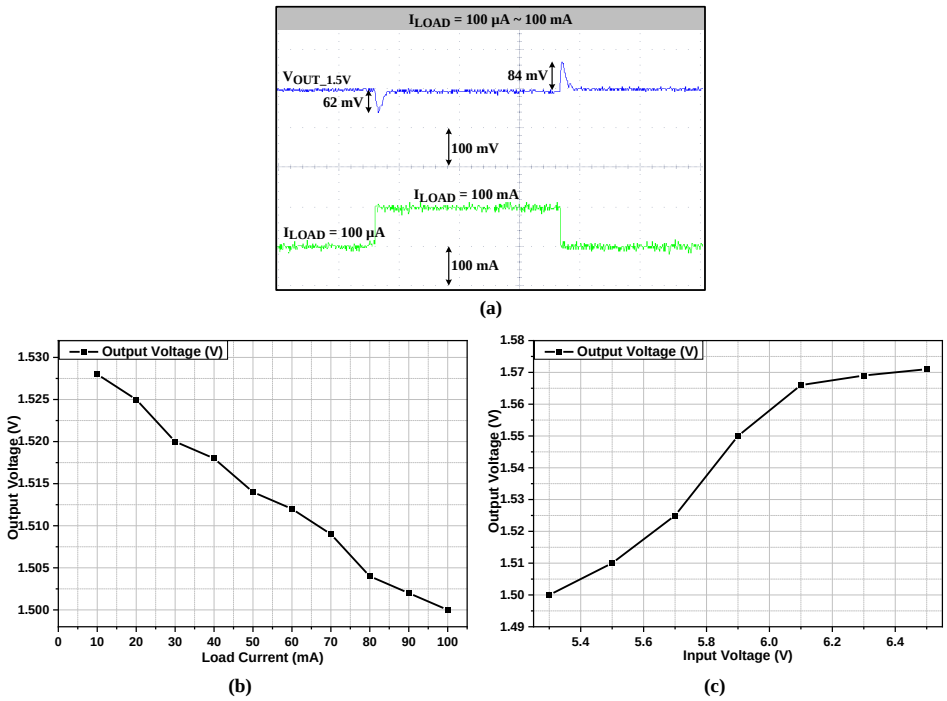

Figure 10. Measured results of LDO_1.5V. (**a**) Load transient response from 100 µA to 100 mA. (**b**) Load regulation. (**c**) Line regulation.

Since most of the research works have been carried out on either BGR or LDO, Table 1 compares the proposed LDOs with recently published works. The proposed LDOs show better performance than the reported works in terms of a wide range of load current, quiescent current, line and load regulations. However, the proposed PRC has a larger die area.

Table 1. Performance summary.

Parameters	This Work	[13]	[14]	[15]	[17]
Technology (nm)	130	180	130	180	130
Type	Analog	Analog	Analog	Analog	Digital
Internal BGR	Yes	No	No	No	No
Input Voltage (V)	5.3	1.8	1.2	1.5	0.5–1.2
Output Voltage (V)	1.24 *, 5 **, 3 ***, 1.5 ****	LDO: 1.6	LDO: 1	LDO: 1.2	LDO: 0.45–1.14
Maximum Load (mA)	300 **, 100 ***, 100 ****	50	5	100	10
Quiescent Current (µA)	38 **, 18.8 ***, 21.5 ****	55	99.04	2.4–242	24
Load Regulation (mV/mA)	0.43 **, 0.7 ***, 0.28 ****	0.14	10	0.14	10
Line Regulation (mV/V)	25 **, 46.7 ***, 59 ****	75	N/A	12.3	3.5
Undershoot (mV)	88 **, 72 ***, 62 ****	80	N/A	125	48
Overshoot (mV)	126 **, 96 ***, 84 ****	120	N/A	65	24
Load Capacitor (µF)	1	0.0001	N/A	1	0.0001
Area (mm^2)	1.634	0.14	0.00245	0.03	0.114

BGR *, LDO_5V **, LDO_3V ***, LDO_1.5V ****.

5. Conclusions

This paper presents a PRC for a power receiving unit for system-on-a-chip (SoC) applications. The proposed PRC is comprised of a limiter, a BGR, three LDOs, and a bias generator. The PRC works in such a way that the limiter limits the high output voltage of an active rectifier to the desired voltage for the power supply of BGR, three LDOs, and a bias generator. The BGR produces a stable (fixed) reference voltage for LDOs, regardless of the PVT variations. The three LDOs are designed to generate regulated output dc voltages with improved PSRR, and line and load regulation performances. The proposed PRC is designed and implemented in 130 nm BCD technology. The measurement results reveal that the limiter limits the output voltage (6 V to 20 V) of the active rectifier to 5.3 V. The BGR provides a reference voltage of 1.24 V with PSRR of −58.6 dB and −51.9 dB at 10 Hz and 1 kHz, respectively. The LDO_5V, LDO_3V, and LDO_1.5V generate regulated output dc voltages of 5 V, 3 V, and 1.5 V, respectively. These LDOs are capable of delivering 300 mA, 100 mA, and 100 mA load currents with dc load regulations of 0.43 mV/mA, 0.70 mV/mA, and 0.28 mV/mA, respectively.

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