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Digital Implementation of Harmonic and Unbalanced Load Compensation for Voltage Source Inverter to Operate in Grid Forming Microgrid

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Abstract: Voltage source inverter (VSI) is a good candidate for grid forming microgrid because it provides constant amplitude, frequency, and sinusoidal shape voltage at point of common coupling (PCC). As the microgrid is separated from utility grid, voltage quality of the PCC is easily affected by the type of load. To ensure power quality in grid operation, a three-phase VSI providing automatic voltage compensation for unbalanced or nonlinear load is presented in this paper. To maintain voltage quality at a certain level, the Fast Fourier Transform (FFT) algorithm is embedded in a proportional-resonant (PR) controller to mitigate the total harmonic distortion (THD) at PCC. In the meantime, any change of voltage magnitude that is caused by the unbalanced load could be reduced as well. To further enhance the transient response with the change of load, a predictive current (PC) controller is integrated into the PR controller. All the control strategies are implemented by digital approach. The effectiveness of proposed controls is verified through experiments on a testbed of the three-phase stand-alone system.

Keywords: Fast Fourier Transform; grid forming inverter; proportional resonant compensation; voltage source inverter (VSI)

Citation: Guo, X.-H.; Chang, C.-W.; Chang-Chien, L.-R. Digital Implementation of Harmonic and Unbalanced Load Compensation for Voltage Source Inverter to Operate in Grid Forming Microgrid. *Electronics* **2022**, *11*, 886. https://doi.org/10.3390/electronics11060886

Academic Editor: Jingyang Fang

Received: 28 November 2021
Accepted: 8 March 2022
Published: 11 March 2022

1. Introduction

The emerging technologies developed for renewable energy resources are making the microgrid operation more resilient in the distribution network. When an outage occurs at the utility grid, the microgrid could quickly switch back to the stand-alone operation for sustaining the electrical power for the loads [1].

Nowadays, DC sources, such as photovoltaic panel (PV) and battery energy storage (BES), are widely acknowledged as distributed energy resources (DERs). Since the DC source cannot directly deliver power to the AC loads, inverters are playing the key role to perform power conversion in between [2–4]. In the grid-connected mode, the voltage at the point of common coupling (PCC) is supported by the utility grid. Without the stiff voltage support by the utility grid, voltage at PCC in the stand-alone operation is heavily affected by the types of loads. The unbalanced loads would cause uneven voltage magnitude. Besides, nonlinear load could draw non-sinusoidal current and generate harmonic components in the voltage waveform. Therefore, the voltage source inverter (VSI) that operates in the grid forming microgrid should be able to maintain quality voltage at PCC [5,6].

The schematics of a three-phase three-wire six-bridge VSI is shown in Figure 1. The VSI is the most commonly used topology in the islanded microgrid operation. The merits of this topology include relatively simple control strategy, faster response speed, and low power loss. Making use of a simple control strategy could save computational resource as it is implemented by the digital micro-controller unit (MCU). Consequently, additional functions could be carried out to improve the power quality of the converter-based system. From the cost–benefit effect point of view, implementing the software control is the most

effective way for the VSI to comply with the power quality standards that were issued by ANSI, IEC, and IEEE. Therefore, this paper proposes a software implementation to improve power quality.

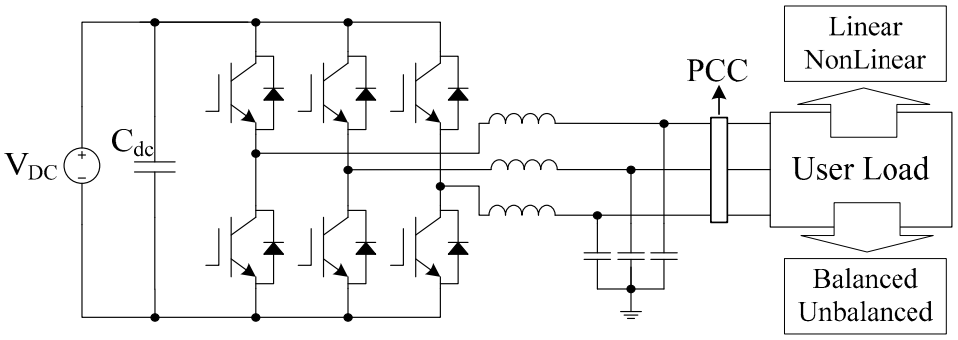


Figure 1. Schematics of the VSI within a three-phase stand-alone system.

The conventional wisdom to regulate the AC voltage is to use the proportional-integral (PI) controller for the dq transformation [7]. However, the control type does not perform well in the harmonic compensation. A numbers of control techniques were introduced to serve the harmonic compensation. Reference [8] mentioned pros and cons of various control techniques. For example, the negative sequence current component control is usually used to mitigate the uneven burdens on the phase voltage and current, i.e., the unbalanced load. It does not have the full ability to compensate the nonlinear load. The sliding mode control can be employed to acquire robust performance against the harmonics in load. However, some flaws including the chattering phenomenon in discrete implementation and the complex design issues under the transient and zero-steady-state operations [9–12]. The hysteresis current control is well known as the bang-bang type nonlinear control. The benefits of this control are of having fast dynamic performance, easy implementation with unconditioned stability. However, the uneven switching frequency leads to another problem of switching harmonics and loss. To obtain a better compensation with less switching disturbance, a weighted adaptive control combined with the hysteresis band current controller was introduced [13,14].

The operating principle of the aforementioned controls belongs to active filter (AF) type. An AF type VSI needs to generate the same harmonic components that are absorbed by the nonlinear load, so that the harmonics observed at PCC could be neutralized. Because the proportional-resonant (PR) compensation can generate the voltage component at some specific frequency, the PR compensation is right for this purpose. In addition, the decoupling of the $\alpha\beta$ axis components derived from the PR control is right for both positive- and negative-sequence compensation as the VSI is dealing with the unbalanced load condition [15]. Therefore, the PR controller is a good candidate to be further improved for better performance, easier implementation, and wider industry application.

To determine the harmonic components for the compensation, the prerequisite is to identify the harmonics of the voltage spectrum at PCC. In this paper, Fast Fourier Transform (FFT) algorithm is embedded inside the PR controller to acquire the information of voltage spectrum. Combining FFT function inside the PR controller, a turn-key voltage compensation could be realized in a stand-alone VSI for the quality voltage supply.

To realize the PR compensation, both voltage and current loops are required to give satisfactory performance. The role of the current loop is to facilitate the voltage loop compensation for a fast response. However, the signal processing and communication latency that generally exist in the digital control loop could deteriorate the dynamic response. To further improve the transient performance, this paper proposes a predictive current (PC) approach to replace the PR current controller. The testing case shows that a PR compensator combining with the predictive controller outperforms the dual PR controllers in the transient response.

The paper is organized as follows. Section 2 introduces the operating principle of PR controller to improve voltage quality under unbalanced and nonlinear loads. The deduction of FFT algorithm from discrete Fourier transform (DFT) is described in Section 3. Section 4 introduces the design flow of the PC controller that is integrated to the PR voltage control loop. Section 5 illustrates the automatic voltage compensation strategy for dealing with unbalanced and nonlinear loads. Experimental results are given in Section 6 to validate the effectiveness of the control scheme. Section 7 draws the concluding remarks.

2. Voltage Regulation for Unbalanced and Nonlinear Loads

2.1. Transfer Function of PR Controller

The traditional transfer function of the *DC* signal regulation by the PI control is shown in Equation (1)

$$G_{DC} = K_P + \frac{K_I}{s} \tag{1}$$

where K_P and K_I are the proportional and integral gains, respectively. Using the low-pass to band-pass transformation, *DC* signal controller can be transformed to *AC* signal as shown in the following form.

$$G_{AC} = G_{DC}(\frac{s^2 + {\omega_c}^2}{2s}) \tag{2}$$

The equation of the PR controller can be represented by the PI gains, where the PR controller has infinity gain at resonant frequency ω_c. However, the realization of the infinity gain of the center frequency is not feasible. We need to add a cut-off frequency ω_c to the equation [16].

$$G_{AC} = K_P + \frac{2K_R\omega_{cut}s}{s^2 + 2\omega_{cut}s + \omega^2} \tag{3}$$

2.2. Unbalanced Load Compensation

The unbalanced load is always associated with positive- and negative-sequence components. One way to solve the unbalanced load is to separately compensate these sequence signals using positive and negative sequence PI controllers as shown in Figure 2. Figure 2 shows a general solution to compensate AC power unbalance load using the positive and negative dq transformation. It is relatively complicated to realize the dq transformation because it needs a phase lock loop (PLL) to obtain the frequency information.

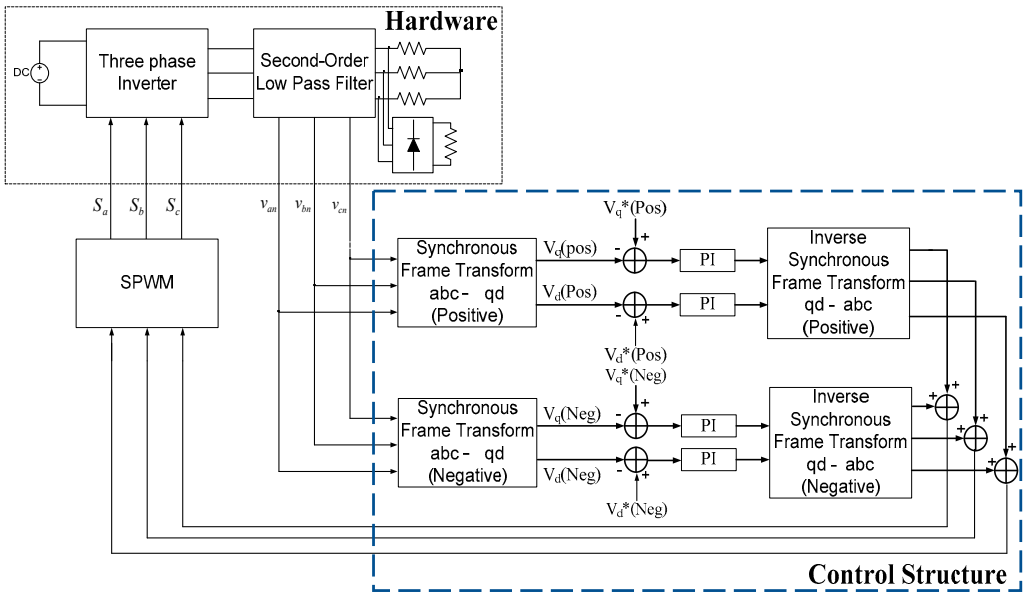


Figure 2. The conventional structure for unbalance component compensation.

To reduce the complexity, the other way to deal with the AC signal is to use universal integral equation. The concept of the universal integration of a sinusoidal signal is shown in Figure 3 [17].

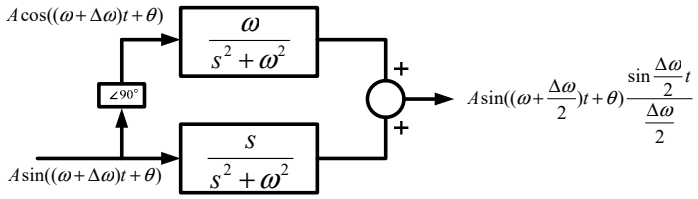


Figure 3. Universal integral equation.

Figure 4 shows the positive sequence integral equation while Δω equals to 0 by applying L'Hopital's Rule.

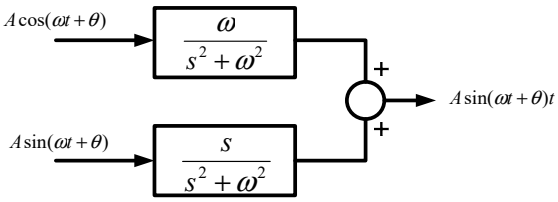


Figure 4. Positive sequence integral equation.

Likewise, Figure 5 shows the negative-sequence integral equation while Δω equals to −2ω,

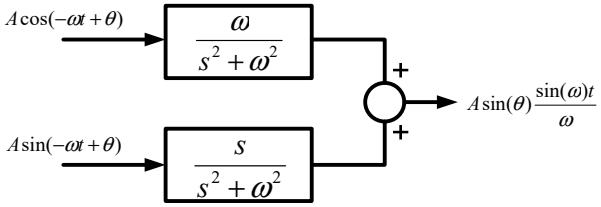


Figure 5. Negative sequence integral equation.

Define the alpha and beta axes of the system,

$$\begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} = \begin{bmatrix} A\sin(\omega t+\theta) \\ A\cos(\omega t+\theta) \end{bmatrix} \tag{4}$$

The positive- and negative-sequence integral of the alpha and beta axes are illustrated by Equations (5) and (6), which can be depicted as shown in Figures 6 and 7, respectively.

$$\begin{bmatrix} \int A\sin(\omega t+\theta)dt \\ \int A\sin(-\omega t+\theta)dt \end{bmatrix} = \begin{bmatrix} \frac{s}{s^2+\omega^2}A\sin(\omega t+\theta)+\frac{\omega}{s^2+\omega^2}A\cos(\omega t+\theta) \\ \frac{s}{s^2+\omega^2}A\sin(\omega t+\theta)-\frac{\omega}{s^2+\omega^2}A\cos(\omega t+\theta) \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} \int A\cos(\omega t+\theta)dt \\ \int A\cos(-\omega t+\theta)dt \end{bmatrix} = \begin{bmatrix} \frac{s}{s^2+\omega^2}A\cos(\omega t+\theta)-\frac{\omega}{s^2+\omega^2}A\sin(\omega t+\theta) \\ \frac{s}{s^2+\omega^2}A\cos(\omega t+\theta)+\frac{\omega}{s^2+\omega^2}A\sin(\omega t+\theta) \end{bmatrix} \tag{6}$$

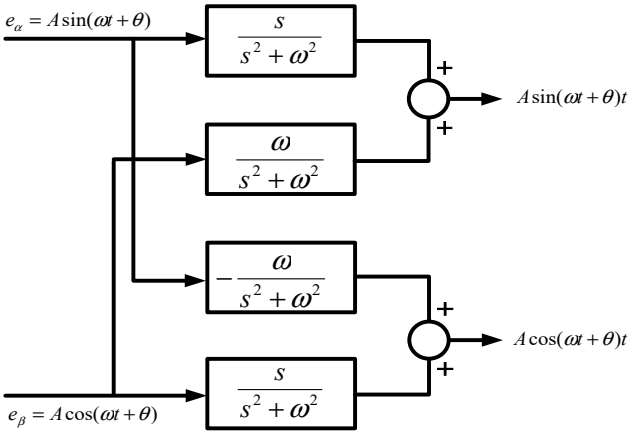


Figure 6. Positive-sequence of alpha and beta axes.

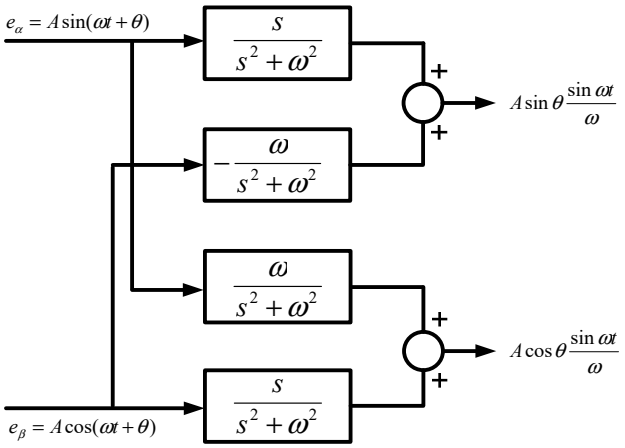


Figure 7. Negative-sequence of alpha and beta axes.

Obtaining the individual sinusoidal controller by cascading Figures 6 and 7, the controller is shown in Figure 8.

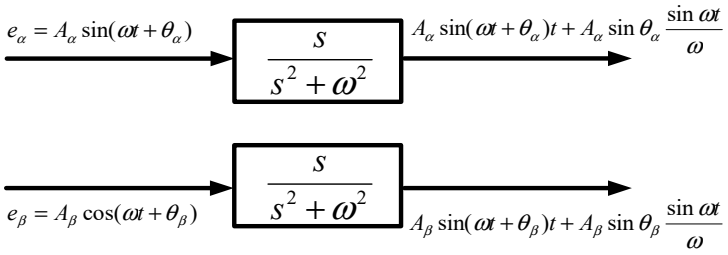


Figure 8. Integral of alpha and beta axis.

Figure 8 shows two decoupled axes and the sinusoidal controller that can compensate not only positive but also negative sequence signal at the same time. The structure of the traditional dq transformed PI control (as shown in Figure 2) can be replaced by the structure of the αβ transformed integral control (as shown in Figure 8). The control structure is much simpler.

2.3. Nonlinear Load Compensation

The nonlinear load causes the non-sinusoidal current waveform that distorts output voltage with high order harmonics. The high THDv (voltage total harmonic distortion) may reduce the life-time and efficiency of the appliances. Figure 9 shows the phenomena of the nonlinear load pollution to the in-feed current of the linear load.

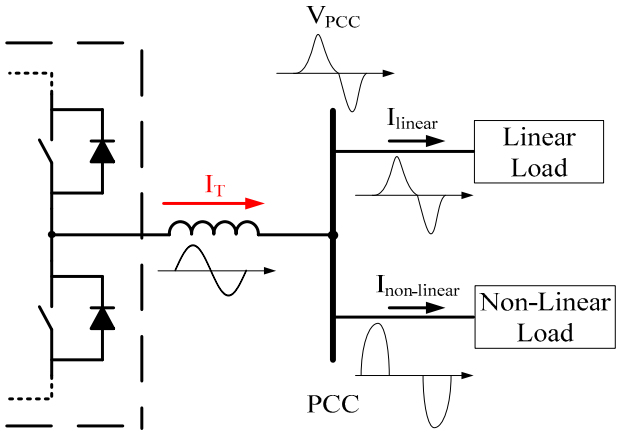


Figure 9. Current waveforms under the nonlinear load condition.

The nonlinear loads that cause higher order harmonics could be compensated by the PR controller. By setting the resonant frequency at the target frequency, PR controller can neutralize the component at that target frequency [18]. Figure 10 depicts an example of the PR controller to neutralize the fifth order harmonic component that is caused by the nonlinear load. When the PR controller is applied, the linear load would have a sinusoidal-like current in-feed that is shown in Figure 11.

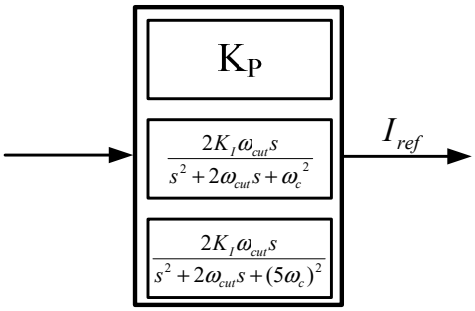


Figure 10. PR controller to neutralize the fifth order harmonic component.

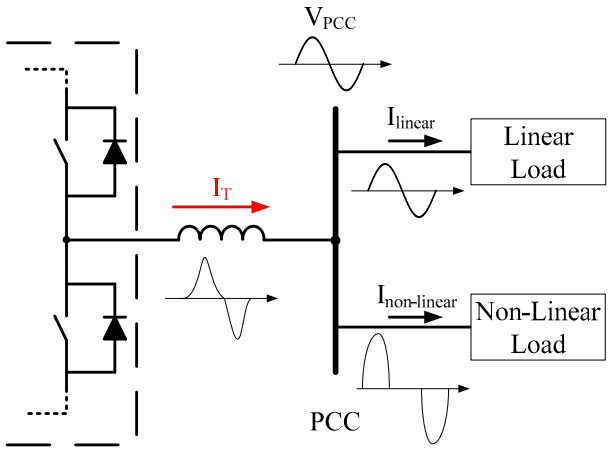


Figure 11. The current waveforms under the compensated nonlinear load condition.

2.4. Design Procedure of a Proportional and Resonant Controller

The PR controller is designed by the dual loop concept. Figure 12 shows the dual loop PR controller dealing with the aforementioned example. The transfer function and equivalent mathematical equation are expressed as follows. The voltage controller transfer function, G(s), is shown in Equation (7) where ω_o is the fundamental frequency.

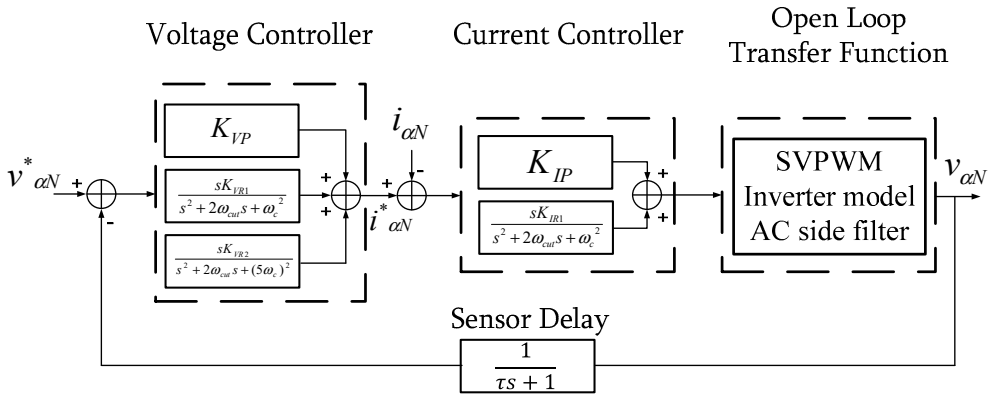


Figure 12. The dual loop PR controller block.

$$G(s) = K_{VP} + \frac{2K_{VR1}\omega_{cut1}s}{s^2 + 2\omega_{cut1}s + \omega_o^2} + \frac{2K_{VR5}\omega_{cut5}s}{s^2 + 2\omega_{cut5}s + (5\omega_o)^2} \tag{7}$$

The Current Controller Transfer Function, $H(s)$, is shown in Equation (8).

$$H(s) = K_{IP} + \frac{2K_{IR1}\omega_{cut1}s}{s^2 + 2\omega_{cut1}s + \omega_o^2} \tag{8}$$

Open loop Transfer Function, $T(s)$,

$$T(s) = \frac{0.435V_{dc}\left(\frac{1}{LC}\right)}{s^2 + \left(\frac{R_L}{L} + \frac{1}{Z_L C}\right)s + \frac{R_L}{Z_L LC}} \tag{9}$$

Sensor Delay Equivalent Transfer Function, $D(s)$,

$$D(s) = \frac{1}{\tau s + 1} \tag{10}$$

The sensor delay block is neglected for simplicity. Several inferences are made from the closed loop transfer functions.

Inference 1: Steady state error of the voltage component at the *xth* order frequency is related to the resonant coefficient of voltage controller (K_{VRx}).
Inference 2: Proportional coefficient of voltage and current controller (K_{VP}, K_{IP}) are related to the system's frequency bandwidth.
Inference 3: Resonant coefficient of current controller (K_{IRx}) is related to the response of inductor current. For example, K_{IR1} is related to transient response of the current component at fundamental frequency.
Inference 4: Resonant bandwidth of controller (ω_{cutx}) at the order of frequency order selection x is related to its transient response.

The design criteria of the PR controller are listed in the following steps according to the aforementioned inferences.

Step 1: Obtain Open Loop Transfer Function

The coefficient of the PR controller is derived from the open loop transfer function of the power stage of the inverter system. Figure 13 shows the Bode plot of the inverter model.

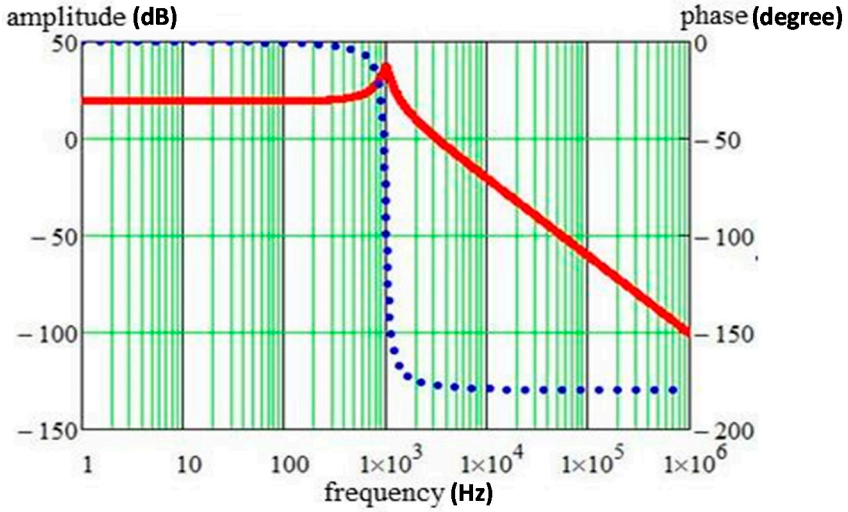
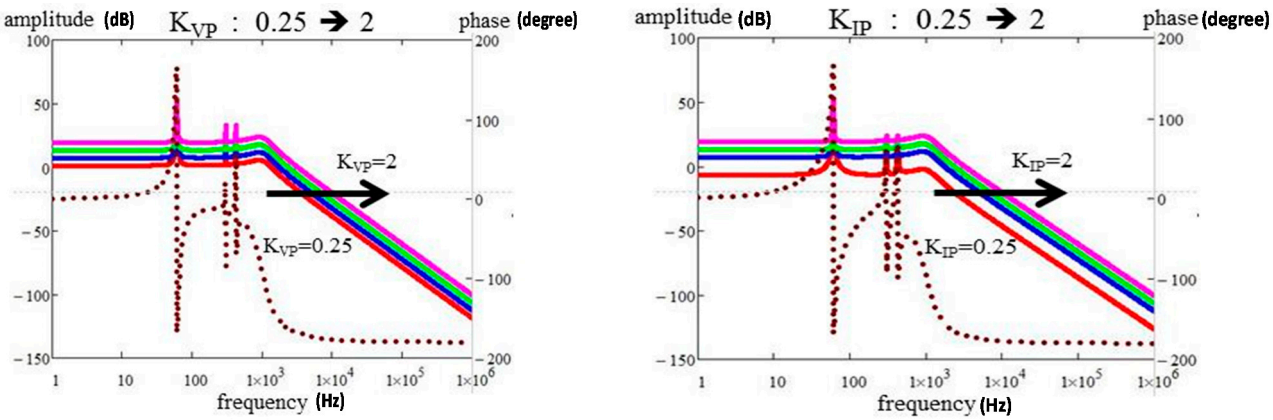


Figure 13. Bode plot of the open loop transfer function of the three-phase inverter.

Step 2: Determine System Bandwidth

Figure 14 shows that the system bandwidth is proportion to proportional coefficient in the PR controller. It is important to design the proportional coefficient in the appropriate region or system might become unstable. The upper limit of the proportional coefficient is dependent on the phase margin of the system. Assume that the phase margin should be larger than $\pi/4$, the proportional coefficients in relation to the upper bound of phase margin is shown in Equation (11).



(**a**) (**b**)

Figure 14. Variation of the proportional coefficient of the PR controller (**a**) Voltage resonant controller (**b**) Current resonant controller.

$$\pi - \tan^{-1}\left(\frac{Im[K_{VP}K_{IP}T(j\omega_{closed})]}{Re[K_{VP}K_{IP}T(j\omega_{closed})]}\right) \geq \frac{\pi}{4} \tag{11}$$

The closed loop gain is shown in Equation (12).

$$Gain_{closed\_dc} = Gain_{open\_dc} + 20\log|K_{VP}| + 20\log|K_{IP}| \tag{12}$$

The lower limit of the coefficient is to make sure that the dc gain is not lower than 0 dB. Therefore, K_{VP} and K_{IP} need to follow the rule in Equation (13).

$$K_{VP}K_{IP} \geq 10^{-\frac{Gain_{open\_dc}}{20}} \tag{13}$$

Step 3: Determine bandwidth of resonant controller, ω_{cut}

The bandwidth of individual PR controller determines the transient response of the system. Wider bandwidth performs faster transient but impacts the phase margin of the system. To ensure enough phase margin, the bound of ω_{cut} is selected according to Equation (14).

$$\pi - \left[\tan^{-1}\left(\frac{Im[G(j\omega_{cut})H(j\omega_{cut})T(j\omega_{cut})]}{Re[G(j\omega_{cut})H(j\omega_{cut})T(j\omega_{cut})]}\right)\right] \geq \frac{\pi}{4} \tag{14}$$

Step 4: Select K_{vr1} and K_{vr5} to suppress the steady state error of voltage component at specific frequency

To neutralize the higher order harmonic component in the output voltage (the fifth harmonics in this example), it is needed to focus on the target frequency component. The steady state error (*e.s.s*) of the output voltage is related to the resonant coefficient in the voltage controller. The associated relationship is illustrated by Equation (15) to Equation (18). We could obtain a lower error, *e.s.s.* from Equation (15) to Equation (16), by choosing higher gains (K_{VR1} or K_{VR5}) of the voltage resonant controller from Equation (14) to Equation (15).

$$e.s.s(j\omega_o) = |1 - a(j\omega_o)|V^*_{m1} = \left|1 - \left|\frac{P_1}{1+P_1}\right|\right|V^*_{m1} \tag{15}$$

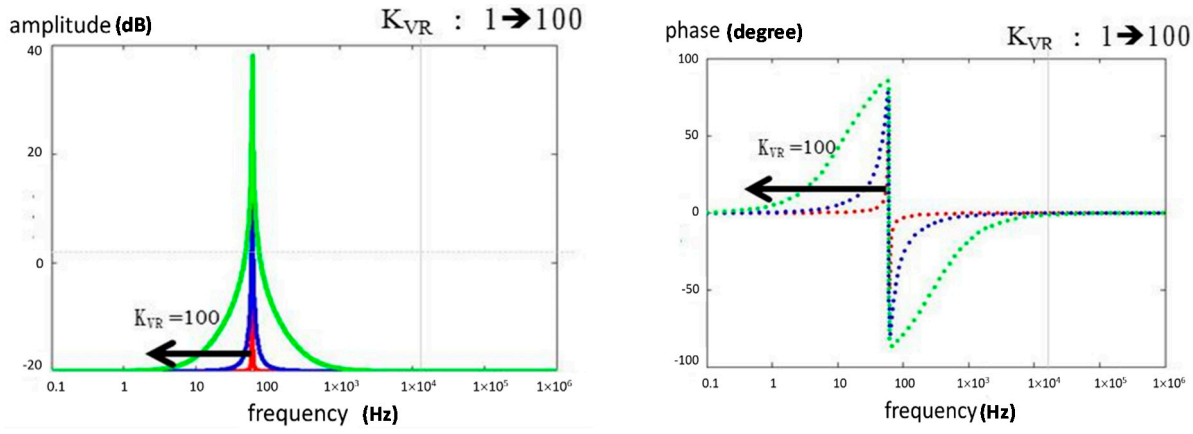
$$e.s.s(j5\omega_o) = |1 - a(j5\omega_o)|V^*_{m5} = \left|1 - \left|\frac{P_5}{1+P_5}\right|\right|V^*_{m5} \tag{16}$$

where P_1 and P_5 are

$$P_1 = \left(K_{VP} + \frac{K_{VR1}}{\omega_{cut1}}\right)\left(K_{IP} + \frac{K_{IR1}}{\omega_{cut1}}\right)\left(\frac{0.435V_{dc}\left(\frac{1}{LC}\right)}{-\omega_0^2 + \left(\frac{R_L}{C} + \frac{1}{Z_L C}\right)j\omega_0 + \frac{R_L}{Z_L LC}}\right) \tag{17}$$

$$P_5 = \left(K_{VP} + \frac{K_{VR5}}{\omega_{cut5}}\right)\left(K_{IP} + \frac{K_{IR5}}{\omega_{cut5}}\right)\left(\frac{0.435V_{dc}\left(\frac{1}{LC}\right)}{-(5\omega_o)^2 + \left(\frac{R_L}{C} + \frac{1}{Z_L C}\right)j5\omega_0 + \frac{R_L}{Z_L LC}}\right) \tag{18}$$

Figure 15a shows the steady state error reduction using a high gain coefficient K_{VR1} at 60 Hz frequency. However, K_{VR1} has its own limitation in phase margin, which is shown in Figure 15b.



(**a**) (**b**)

Figure 15. Variation of the voltage resonant coefficient K_{VR1} of the PR controller on (**a**) amplitude (**b**) phase.

Step 5: Select K_{IR} for the current controller

The current controller is usually designed to facilitate the current transient response. The higher order harmonic components shall not exist in the inductor current. For this reason, the higher order harmonic of the resonant coefficient on the PR controller is set to zero. The choice of fundamental resonant coefficient, K_{IR1}, just follows the same rule as that of the voltage resonant coefficient.

3. Fast Fourier Transform

Fourier transform converts signals from time domain to frequency domain. The transformation contains the same information as the original signal but differs in the way the signal presented. Fast Fourier Transform (FFT) is an algorithm that can simplify computation process of discrete Fourier transform (DFT). FFT can be deduced from the definition of DFT in Equation (19),

$$X[k] = \sum_{n=0}^{N-1} x[n] e^{-j\frac{2\pi}{N}nk}, k = 0, 1, 2, \ldots, (N-1) \tag{19}$$

where N represents the number of points of DFT, $x[n]$s are the input samples in time domain, and $X[k]$ represents the signal in frequency domain. The term $E^{-j\frac{2\pi}{N}nk}$ is called twiddle factor and is often represented as W_N^k.

Separating input signals into even and odd sequences as shown in Equation (20),

$$\begin{array}{c} x_{2m} = x_0, x_2, \ldots, x_{N-2}\text{: even sequence} \\ x_{2m+1} = x_1, x_3, \ldots, x_{N-1}\text{: odd sequence} \end{array} \tag{20}$$

Substitute Equation (20) into Equation (19), the DFT equation can be expressed as Equation (21)

$$\begin{aligned} X[k] &= \sum_{m=0}^{\frac{N}{2}-1} x_{2m} e^{-j\frac{2\pi}{N}(2m)k} + \sum_{m=0}^{\frac{N}{2}-1} x_{2m+1} e^{-j\frac{2\pi}{N}(2m+1)k} \\ &= \sum_{m=0}^{\frac{N}{2}-1} x_{2m} e^{-j\frac{2\pi}{\frac{N}{2}}(2m)k} + \left(e^{-j\frac{2\pi}{N}k}\right) \times \sum_{m=0}^{\frac{N}{2}-1} x_{2m+1} e^{-j\frac{2\pi}{N}(2m+1)k} \\ &= E_k + \left(W_N^k\right) \times O_k \end{aligned} \tag{21}$$

where E_k represents the even-numbered DFT and O_k represents the odd-numbered DFT. The number of points of each DFT is $\frac{N}{2}$. Due to the periodicity of DFT, $E_{k+\frac{N}{2}} = E_k = E_{k-\frac{N}{2}}$, $O_{k+\frac{N}{2}} = O_k = O_{k-\frac{N}{2}}$, the above equation is rewritten as follows.

$$X[k] = \begin{cases} E_k + \left(W_N^k\right) \times O_k, & 0 \le k \le \frac{N}{2} \\ E_{k-\frac{N}{2}} + \left(W_N^k\right) \times O_{k-\frac{N}{2}}, & \frac{N}{2} \le k \le N \end{cases} \tag{22}$$

As twiddle factor has symmetry $W_N^{k+\frac{N}{2}} = -W_N^k$ and periodicity $W_{\frac{N}{2}}^{k+\frac{N}{2}} = -W_{\frac{N}{2}}^k$, this allows us to cut the number of "twiddle factor" calculations into two. For $0 \le k \le \frac{N}{2}$ Equation (23) is obtained.

$$\begin{array}{c} X[k] = E_k + \left(W_N^k\right) \times O_k \\ X\left[k + \frac{N}{2}\right] = E_k - \left(W_N^k\right) \times O_k \end{array} \tag{23}$$

Equations (23) and (19) indicate that a DFT of length N can be decomposed into two DFTs of length $\frac{N}{2}$. This process is called Cooley–Tukey algorithm [19,20]. The decomposition process is repeated $\log_2 N$ times. Comparing the complexity of DFT which takes O(N2) operations, FFT can compute the same DFT in only O(N$\log_2 N$) operations. Using this technique, the information of voltage spectrum can be quickly obtained.

4. Predictive Current Controller

4.1. Operating Principle of the Predictive Control

The predictive controller can also be called the deadbeat controller, which is translated as "minimum beat control" or "no oscillation control". It is expected that this word can fully explain its concept. The predicted signal can be obtained through the construction and derivation of the circuit model in advance. With the feedback signal (voltage or current, etc.), the circuit model can give an expected signal before the next cycle of switching modulation [21,22]. To obtain the modulated signal in advance, the following principles must be met.

$$2f_{sw} \leq f_s \tag{24}$$

where

f_{sw}—switching frequency.
f_s—analog to digital sampling rate.

Figure 16 is shown to illustrate the operating principle, where:

$n_{th} \sim (n+2)_{th}$—modulation time stamp.
$(k-4)_{th} \sim (k+4)_{th}$—sampling time stamp.

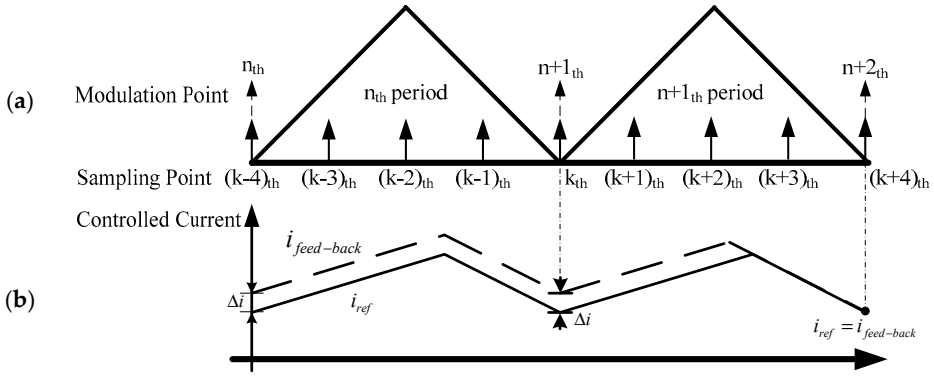


Figure 16. Predictive controller signal waveform (**a**) Digital controller built-in counter (**b**) Command current and feedback current.

Figure 16 shows that the sampling frequency used in this system is four times the switching frequency. The figure shows the process of current convergence after two cycles of modulation. It is expected that the current control mechanism can make the current in the (k + 4)th step to achieve our control objective. Before the start of the $(n + 2)_{th}$ modulation period, it is expected that the current controller can reduce the deviation (Δi) generated in the n_{th} period through the modulation action of the previous $(n + 1)_{th}$ modulation period, so that the controlled current can closely track the current command. In the next section, the PC controller model will be derived.

4.2. Modeling of the Predictive Current Control

The derivation of the current control model shall start with the derivation of the voltage–current relationship of the filtering inductor, which is shown in Figure 17 and Equation (25).

$$v_L = L\frac{di_L}{dt} \tag{25}$$

Applying the discrete signal concept, the inductor current in the next two steps can be expressed in the forms of Equations (26) and (27).

$$i_L(k+1) = \frac{v_i(k) - v_o(k)}{2L} D_n T_s + i_L(k) \tag{26}$$

$$i_L(k+2) = \frac{v_i(k+2) - v_o(k+2)}{2L}(1 - D_n)T_s + i_L(k+1) \tag{27}$$

where D_n is the duty ratio, T_S is the switching period. Within a modulation cycle, the modulation signals are the same, so the output voltage of the converter is the same.

$$v_i(n+1) = v_i(k) = v_i(k+2) \tag{28}$$

Substituting Equations (26) and (27) into Equation (28), Equation (29) is obtained.

$$v_i(n+1) = \frac{2L}{T_s}[i_L(k+2) - i_L(k)] + (1 - D_n)v_o(k+2) + D_n v_o(k) \tag{29}$$

The voltage and current variables at this time still include the future voltage and current components, the following steps are taken to carry out the predictive control:

Step 1: $i_L(k)$ should be re-formulated as follows.

$$i_L(k) = \frac{T_s}{2L}v_i(n) - \frac{T_s}{2L}(1 - D_{n,old})v_o(k-2) - \frac{T_s}{2L}D_{n,old}v_o(k) + i_L(k-2) \tag{30}$$

Step 2: Through the concept of Lagrange multiplier, the signal can be predicted in a linear way

$$v_o(k+2) = 3v_o(k-2) - 2v_o(k-4) \tag{31}$$

$$v_o(k) = 2v_o(k-2) - v_o(k-4) \tag{32}$$

Step 3: The variation of the duty cycle during the steady state period is almost 0, let

$$D_n \approx D_{n,old} \tag{33}$$

The predicted voltage variable v_i is obtained.

$$v_i(n+1) = \frac{2L}{T_s}[i_L(k+2) - i_L(k-2)] + 4v_o(k-2) - 2v_o(k-4) - v_i(n) \tag{34}$$

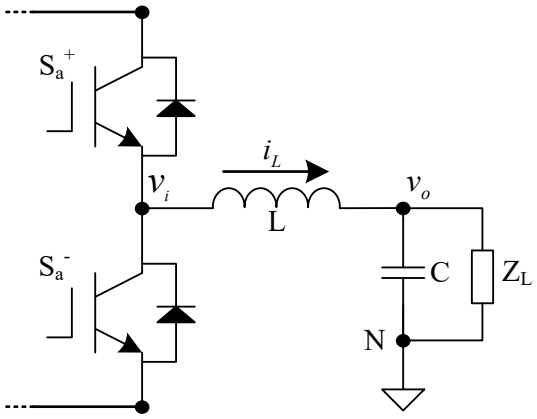


Figure 17. Circuit diagram of voltage–current relationship of the filtering inductor.

Equation (34) implies a chance to further reduce the sampling frequency from four times the switching frequency to twice the switching frequency. This way can reduce the computational burden of the signal processor but keep the same effect. The updated v_i becomes

$$v_i{}^*(n+1) = \frac{2L}{T_s}[i_L{}^*(k+1) - i_L(k-1)] + 4v_o(k-1) - 2v_o(k-2) - v_i(n) \tag{35}$$

Equation (35) shows that the next step voltage, $v_i^*(n+1)$, can be predicted from the present and past feedback signals on the right-hand side. This model can help improve the system transient response.

5. Automatic Voltage Compensation Strategy

Theoretically, any voltage harmonics at PCC can be compensated by the individual resonant controller for that specific order of frequency. However, a distorted voltage could contain harmonics with many frequency orders. It is not economical to compensate all the harmonics due to the restriction of the hardware. Under limited controller resources, only dominant voltage harmonic components are to be neutralized. Except the resonant controller tuned at fundamental frequency ω_0, two higher order voltage harmonics are considered. The design of the automatic voltage compensation is shown as follows.

Step 1: Set parameters of resonant controllers

Several sets of PR controllers that compensate specific order of the fundamental frequency are formed and saved in the DSP memory.

Step 2: Sample voltage feedback signal

Sample the feedback signal of voltage at PCC. Note that the size of FFT needs to be the power of 2, such as 256, 512, 1024, etc. If the sampling number cannot fit the size, it can insert zero-value samples to meet (zero-stuffing), but the results may be distorted and need to be adjusted.

Step 3: Execute FFT

Execute FFT of signal from Step 2 to acquire the voltage spectrum at PCC.

Step 4: Identify the major harmonic component

Calculate the amplitude of each harmonics and pick the highest two components (for example, the fifth and seventh order harmonics) as indices for the resonant controller selection.

Step 5: Choose the corresponding resonant controllers

Use the indices acquired from Step 4 to choose the resonant controllers that are set in Step 1 for that specific frequency (for example, the PR controller tuned at 300 Hz and 420 Hz).

Step 6: Integrate PC controller into the PR controller

Integrate the PC control loop into the PR control voltage loop together for voltage regulation. Figure 18 shows the Schematic diagram of the PR Controller integrating with PC Controller within a VSC.

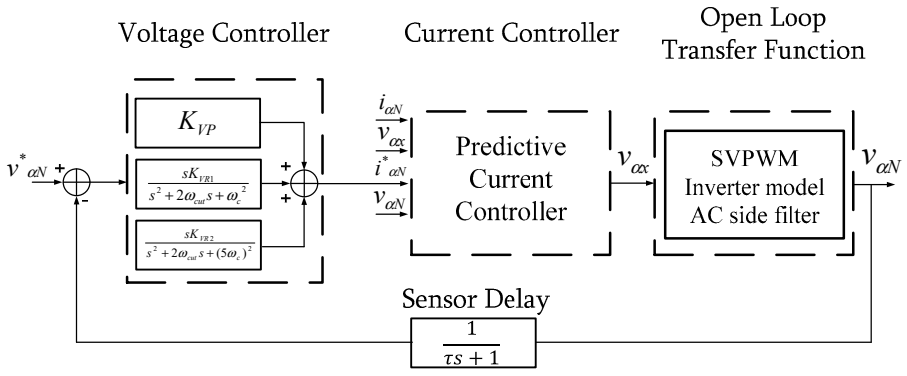


Figure 18. Schematic diagram of PR Controller with PC Controller within a VSC.

6. Experimental Results

We implemented the FFT and controllers of the three-phase stand-alone VSI using the DSP manufactured by TEXAS INSTRUMENT®. The input DC bus voltage and AC output voltage is 360 V and 110 V in RMS, respectively. The loading conditions could be nonlinear and unbalanced. Two experiments were conducted to verify the effectiveness of the automatic voltage compensation. The experimental results were measured by the power analyzer HIOKI 3390.

6.1. Unbalanced Load Test

Without grid voltage support, the three-phase line-to-line voltage of the grid forming inverter-fed AC system could be very sensitive to unbalanced loading condition. Figure 19 shows waveforms of the inverter line-to-line output voltage and line current at PCC. A single-phase load with 1142 W was connected between phase a and b. The phase c is unloaded. Figure 19 shows that the magnitudes of line current I_a and I_b are quite evident compared to that of I_c, while the three-phase line-to-line voltages remain the same. The compensated %VUR measure was 0.12%, which was far below the standard of NEMA (%VUR < 3%). This experiment verifies that three-phase line-to-line voltages still keep in balance under unbalanced loading condition.

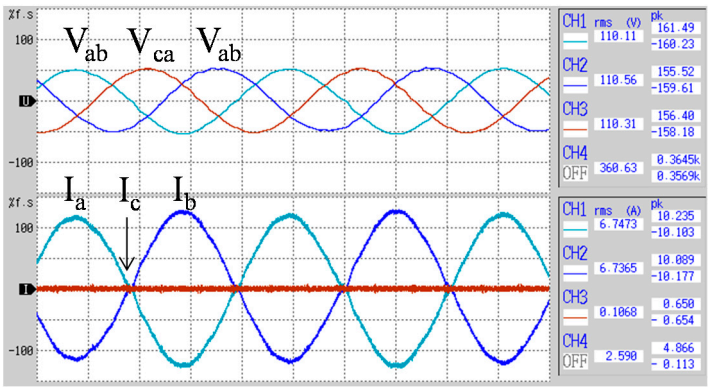


Figure 19. Waveforms of inverter output voltage and current under unbalanced load.

6.2. Unbalanced Load Plus Nonlinear Load Test

In the next test, a star connected unbalanced resistive load with a nonlinear load that consists of a 200 W three-phase full-bridge rectifier, in parallel with a 470 µF capacitor and a 100 Ω resistor were used to test the inverter. System configuration of the three-phase inverter serving the unbalanced as well as the nonlinear load is shown in Figure 20. In addition to the unbalanced condition, another test was made to evaluate the effectiveness of the proposed resonant controller in reducing the total harmonic distortion of line-to-line voltage.

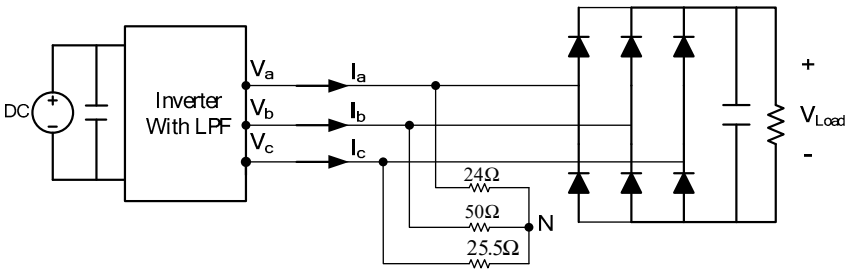
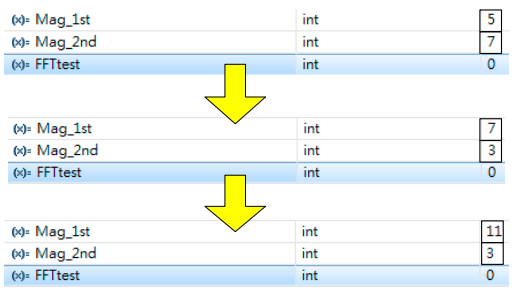


Figure 20. System configuration of the three-phase inverter serving both unbalanced and nonlinear loads.

Figure 21 shows the load test results using different resonant controller settings. The harmonics identification using different PR controllers for voltage compensation is shown in

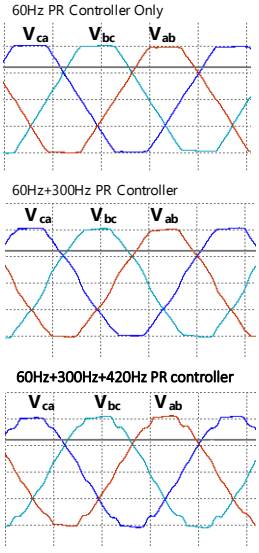
Figure 21a, where Mag_1st and Mag_2nd represent the highest two harmonics components. The subplot at the top of Figure 21a shows that the uncompensated voltage contains the fifth and seventh order harmonics in the beginning. After using the PR controller with (60 + 300 Hz) harmonics compensation, the fifth harmonics was decreased. The subplot in between of Figure 21a shows that the fifth order harmonics was no longer the highest one. The highest two harmonics became the order of seventh and third. Following that, a further compensation of the seventh harmonics was also made using the PR controller. The subplot at the bottom of Figure 21a shows that the fifth and seventh order harmonics were decreased. The highest two harmonics became the order of 11th and third. Although the highest two harmonics switched to the other order, the magnitudes were lower. Figure 21d demonstrates the voltage harmonic spectra measured from the PCC. The voltage spectrum validates the result of harmonics identification that is shown in Figure 21a. Figure 21b shows the %THDv (Voltage Total Harmonic Distortion) measured from different PR voltage compensation. The decrease from 5.84% to 2.89% proves that this control strategy can effectively improve voltage quality. The changes of voltage waveforms are shown in Figure 21c. Note that the harmonic compensation of the VSI is automatically executed. The FFT program first identified the orders of the highest two harmonic component, then the corresponding settings of the resonant controller were used to neutralize the identified harmonic components.



(**a**)

PR Controller	THDv
60 Hz	5.84%
60 + 300 Hz	3.78%
60 + 300 + 420 Hz	2.89%

(**b**)



(**c**)

(**d**)

Figure 21. Nonlinear load (three-phase full bridge rectifier) compensated by different PR controllers (**a**) harmonics identification using FFT algorithm (**b**) THDv (**c**) voltage waveforms (**d**) voltage harmonic spectra measured from power analyzer.

Table 1 shows the steady-state operating test of the dual PR and PR + PC controlled VSIs under the unbalanced and nonlinear loading condition. The PR controller that was used for both VSIs were designed to compensate 60 + 300 + 420 Hz components. The results of Table 1 show the PR + PC controlled voltage and current harmonic distortions, as well as the phase voltage unbalance rate are lower than that of the dual PR controlled VSI, which means that the power quality is better. The next section will further analyze the data and waveform measurement of the control structure with the resonant controller and the PC control.

6.3. Transient Load Test

In the transient load test, a comparison of the response speed between the dual PR controllers and a PR controller combined with the PC control was made. The initial loading

condition of this experiment was a three-phase balanced load of 200 W, then a load of 1000 W was suddenly applied to phase a.

Table 1. Measurement data of the dual PR and PR + PC controlled VSIs under the unbalanced and nonlinear loading test.

	Dual PR Controller	**PR + PC Controller**
Loading condition	25 Ω, 5 Ω, 50 Ω + 100 Ω	25 Ω, 25 Ω, 50 Ω + 100 Ω
Output voltage (V_{rms})	110.51 V_{rms}	109.75 V_{rms}
Output current (I_{rms})	2.62 A(25 Ω), 1.5 A(50 Ω)	2.61 A(25 Ω), 1.49 A(50 Ω)
%THDv (%)	4.41%	3.15%
%THDi (%)	3.54%	2.91%
%VUR (%)	0.5%	0.13%
Input power (W)	715.1 W	717.7 W
Output power (W)	557.73 W	557.03 W
Total efficiency (%)	77.99%	77.61%

Figure 22a,b are the testing result of the VSI implemented by the dual PR controllers and the PR controller combined with the PC controller, respectively. Figure 22a shows that the voltage peak momentarily decreased by about 10 V, while the current had 2A fluctuation during the transient state. The 1000 W load was instantaneously applied to make the current transient for 150 ms until it reached steady state again. Figure 22b shows that the voltage peak also momentarily decreased by about 10 V, then the voltage and current returned to steady state in just about 50 ms. There was no current fluctuation during transient state, which helped improve the system stability. The testing case shows that a PR + PC controller outperforms the dual PR controllers in the transient response.

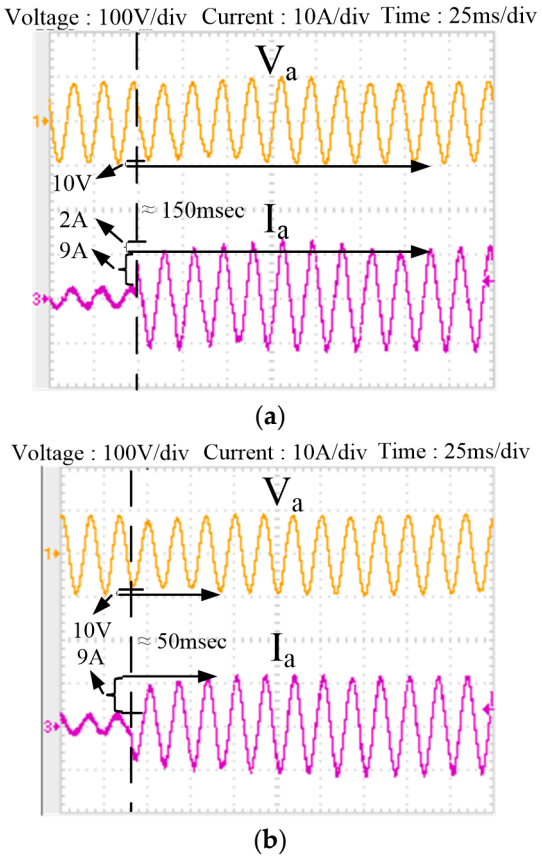


Figure 22. Voltage waveforms when the 1000 W load was instantaneously loaded to a VSI with (**a**) Dual PR controller (**b**) PR controller combined with PC controller.

7. Conclusions

This paper demonstrates a turn key solution for a VSI to compensate unbalanced and nonlinear load conditions in a grid forming microgrid. The operating principle and the design flow of the PR as well as the PC controller are illustrated in detail for the purpose of compensation on unbalanced and nonlinear load. With the embedded FFT identification technique, the PR controlled VSI can automatically neutralize the most influential harmonic components to improve the voltage quality. The PC controller can help advance current sampling inside the current control loop to minimize the digital control latency. The steady-state and transient tests were conducted to validate the effectiveness of the proposed control scheme. Testing results show that the VSI not only keeps voltage balance under unsymmetrical loading condition, but also reduces the %THDv at the PCC under nonlinear load. The PC controller can help enhance both steady-state and transient performances under the digital implementation.

Author Contributions: The conceptualization, review and editing, and funding acquisition were contributed by the project manager L.-R.C.-C. The implementation of the proposed methodology, software development and circuit performance validation were conducted by X.-H.G. and C.-W.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the ministry of science and technology of Taiwan under grant: MOST 110-3116-F-006-002-.

Acknowledgments: This research was funded by the ministry of science and technology of Taiwan under grant: MOST 110-3116-F-006-002-.

Conflicts of Interest: The authors declare no conflict of interest.

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