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Low Threshold Voltage Shift in AlGaN/GaN MIS-HEMTs on Si Substrate Using SiN_x/SiON as Composite Gate Dielectric

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Abstract: This study has demonstrated AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs) on Si substrates with a SiN_x/SiON composite gate dielectric. The threshold voltage shift in the devices was investigated. The MIS-HEMTs with the SiN_x/SiON composite gate dielectric exhibited superior threshold voltage uniformity and small threshold voltage hysteresis than the reference device with SiN_x only gate dielectric. The variation of the device threshold voltage was mainly related to trapping process by the interface states, as confirmed by band diagrams of MIS-HEMTs at different gate biases. Based on frequency-dependent capacitance measurements, interface state densities of the devices with the composite and single gate dielectrics were extracted, where the former showed much smaller interface state density. These results indicate that the SiN_x/SiON composite gate dielectric can effectively improve the device performance of GaN-based MIS-HEMTs and contribute to the development of high-performance GaN electronic devices.

Keywords: AlGaN/GaN; interface state; MIS-HEMT; SiN_x/SiON; threshold voltage

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1. Introduction

Gallium nitride (GaN) based high electron mobility transistors (HEMTs) have been widely investigated for power electronics due to their high breakdown voltage, low on-state resistance, and high switching speed [1,2]. Due to the limited availability of expensive free-standing GaN substrates, AlGaN/GaN HEMTs on cost-effective silicon (Si) substrates are the current research focus [3–5]. However, heteroepitaxially grown HEMTs are prone to the formation of traps in the buffer layer, in the channel layer, and on the surface. The existence of surface traps led to larger gate leakage current, lag of threshold voltage, breakdown voltage reduction, and other reliability issues in the HEMT devices [6,7]. In order to solve these issues induced by surface traps and improve the gate stability, an insulating dielectric material is usually inserted under the gate to form a metal-insulator-semiconductor HEMT (MIS-HEMT). The introduction of an insulating gate dielectric can effectively reduce the gate leakage current, surface state density, and improve the overall performance of the devices [8–10].

To date, many insulating gate dielectrics have been demonstrated for AlGaN/GaN MIS-HEMTs, including SiO_2 [11], SiN_x [12], SiON [13,14], Al_2O_3 [15], HfO_2 [16], ZrO_2 [17],

and BN [18]. Various deposition techniques were used to form these insulating gate dielectrics, such as plasma-enhanced chemical vapor deposition (PECVD), low-pressure chemical vapor deposition (LPCVD), in situ metal-organic chemical vapor deposition (MOCVD), and so on [19,20]. The choice of insulating gate dielectric material depends on many considerations, such as high dielectric constant, ability to form a good MIS interface with the semiconductor, high conduction band offset, compatible deposition process, stability, and cost [21,22]. Compared with conventional PECVD based insulating dielectrics, e.g., SiN_x, the LPCVD-SiN_x are deposited at higher growth temperature with fewer impurities and no plasma bombardment damage. As a result, the LPCVD-SiN_x can greatly improve the performance of the GaN-based MIS-HEMTs due to its higher film quality, higher breakdown field, and lower gate leakage [23]. However, during the high temperature deposition process of the LPCVD-SiN_x, Ga atoms in the GaN material will diffuse outward, resulting in the formation of Ga vacancies and dangling bonds on the GaN surface, which can increase the surface leakage [24]. SiON is a dielectric with a bandgap between the SiO_2 (9 eV) and SiN_x (5.3 eV) [25]. It has been reported that the PECVD-SiON can form a stable atomic structure interface with GaN and reduce the Ga dangling bonds that are terminated by N in SiON although the SiON dielectric layer alone can not overcome the gate leakage well [14,26,27]. Therefore, a composite gate dielectric based on LPCVD-SiN_x and PECVD-SiON can be solution to not only reduce the gate leakage but also solve the problem of Ga diffusion at the high deposition temperature in LPCVD.

In this work, a SiN_x/SiON composite gate dielectric for AlGaN/GaN MIS-HEMTs on Si was demonstrated for the first time, where SiON was deposited at a relatively low-temperature by PECVD followed by a high-temperature LPCVD-SiN_x. This novel composite gate dielectric layer can effectively suppress threshold voltage hysteresis, reduce gate leakage, and prevent performance degradation of the devices.

2. Materials and Methods

The MIS-HEMTs were fabricated on AlGaN/GaN epilayers grown by MOCVD on a p-type Si (111) substrate. The device structure consisted of 2 nm GaN-cap layer, 21 nm AlGaN barrier layer with 21% Al composition, 200 nm GaN channel layer, and 3.6 μm thick high-resistance GaN buffer layer. The electron mobility and sheet carrier concentration in the two-dimensional electron gas (2DEG) channel at room temperature by Hall measurements were 1793 $cm^2/V^{-1}s^{-1}$ and 1.3×10^{13} cm^{-2}, respectively.

Figure 1a shows the schematic of the MIS-HEMTs with the SiN_x/SiON (20 nm/10 nm) as a composite gate dielectric and passivation layer. The SiON was deposited by PECVD at 350 °C in SiH_4, NH_3, N_2O, and N_2 atmospheres. The SiN_x layer was deposited by LPCVD at 780 °C with an ammonia flow of 280 sccm, a SiH_2Cl_2 flow of 70 sccm, and a deposition rate of 3 nm/min. For comparison, a reference sample with only LPCVD-SiN_x of 20 nm as the gate dielectric was fabricated using the same process, as shown in Figure 1b. The relative permittivity of SiN_x and SiON are 7.5 and 5.8, respectively. The mesa isolation was realized by multi-energy fluorine ion implantation (SEN NV-GSD-HE) [28]. Ohmic contacts of Ti/Al/Ni/Au (20 nm/130 nm/50 nm/50 nm) for source and drain electrodes were fabricated by electron beam evaporation followed by rapid thermal annealing at 875 °C for 30 s in N_2 ambient. The contact resistances were 0.91–1.1 Ω·mm measured by the linear transmission line method (TLM). The gate electrode was formed by depositing Ni/Au (50 nm/150 nm) followed by annealing at 400 °C for 10 min in N_2. The gate-to-source distance (L_{gs}), gate-to-drain distance (L_{gd}), gate length (L_g), and gate width (W_g) were 2 μm, 14 μm, 2 μm, and 100 μm, respectively.

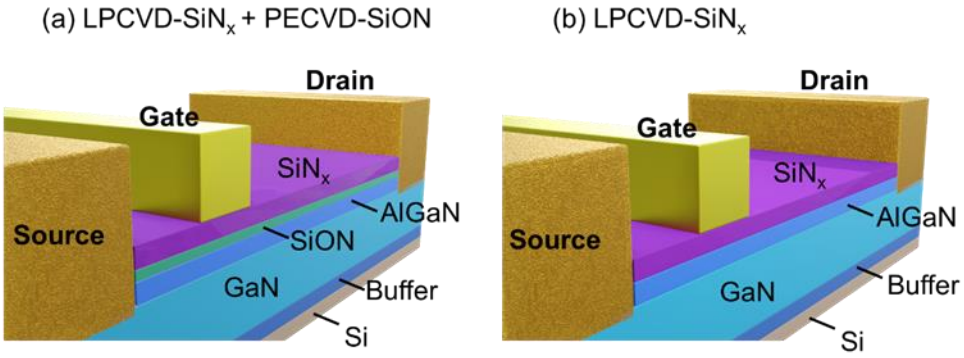

Figure 1. Schematics of MIS-HEMTs with (**a**) SiN_x/SiON and (**b**) SiN_x gate dielectric. The gate-to-source distance (L_{gs}), gate-to-drain distance (L_{gd}), gate length (L_g), and gate width (W_g) were 2 μm, 14 μm, 2 μm, and 100 μm, respectively.

3. Results and Discussion

The electrical characteristics of the MIS-HEMTs were measured by Keysight B1505A, including DC characterization, interface state, and threshold voltage (V_{th}) stability under different gate voltage sweeping ranges. The transfer characteristics of the two samples under various gate-source voltage (V_{gs}) sweep ranges are shown in Figure 2. During the sequential sweeps, the gate voltage was scanned from −15 V to a maximum gate voltage (V_{max}). To investigate the effects of the gate voltage stress, the V_{max} was changed manually for each scan from −6 V to 12 V with a step of 2 V, where the drain−source voltage (V_{ds}) was fixed at 1 V. The stress time of the V_{max} was < 1 s. With the increase in V_{max}, the V_{th} of the MIS-HEMT with SiN_x/SiON composite gate dielectric varied from −9.49 V to −8.68 V with a variation (ΔV_{th}) of 0.81 V. The V_{th} of the MIS-HEMT with SiN_x only gate dielectric varied from −5.01 V to −3.24 V with a much larger ΔV_{th} of 1.77 V. It indicates that the maximum gate voltage stress affects the following transfer curves with a positive shift of V_{th} and the SiN_x/SiON composite gate dielectric can significantly improve the V_{th} stability of the GaN MIS-HEMTs.

The V_{th} and the V_{th} hysteresis (ΔV_{th}) of MIS-HEMTs as a function of the V_{max} are summarized in Figure 2c. The ΔV_{th} was defined as the V_{th} difference between the V_{th} with a scanned V_{max} and the V_{th} with a V_{max} of −6 V. The V_{th} of the MIS-HEMT with SiN_x/SiON gate dielectric was almost constant as V_{max} changed from −4 V to 12 V, whereas there was an obvious positive shift of the V_{th} for the MIS-HEMT with SiN_x only gate dielectric. The ΔV_{th} of both kinds of MIS-HEMTs were almost 0 V as the V_{max} increased from −4 V to 4 V and increased as the V_{max} increased further. The ΔV_{th} of the MIS-HEMT with SiN_x/SiON and SiN_x only gate dielectric at V_{max} = 12 V were 0.81 V and 1.77 V, respectively. Therefore, the SiN_x/SiON composite gate dielectric can effectively improve the stability of the threshold voltage and reduce the threshold voltage hysteresis compared with SiN_x only gate dielectric. The positive shift of the V_{th} at V_{max} > 2 V indicates a trapping process of electrons by the interface states between the dielectric layer and the barrier layer, or the acceptor-like traps in the barrier layer [10,29] thereby requiring a higher V_{th} for ON-state. Figure 2d shows the comparison of the gate leakage for the two kinds of devices. Although the total thicknesses of the dielectrics are different, the devices showed almost the same gate leakage suggesting a high quality of the LPCVD-SiN_x layer as designed for reducing the gate leakage current.

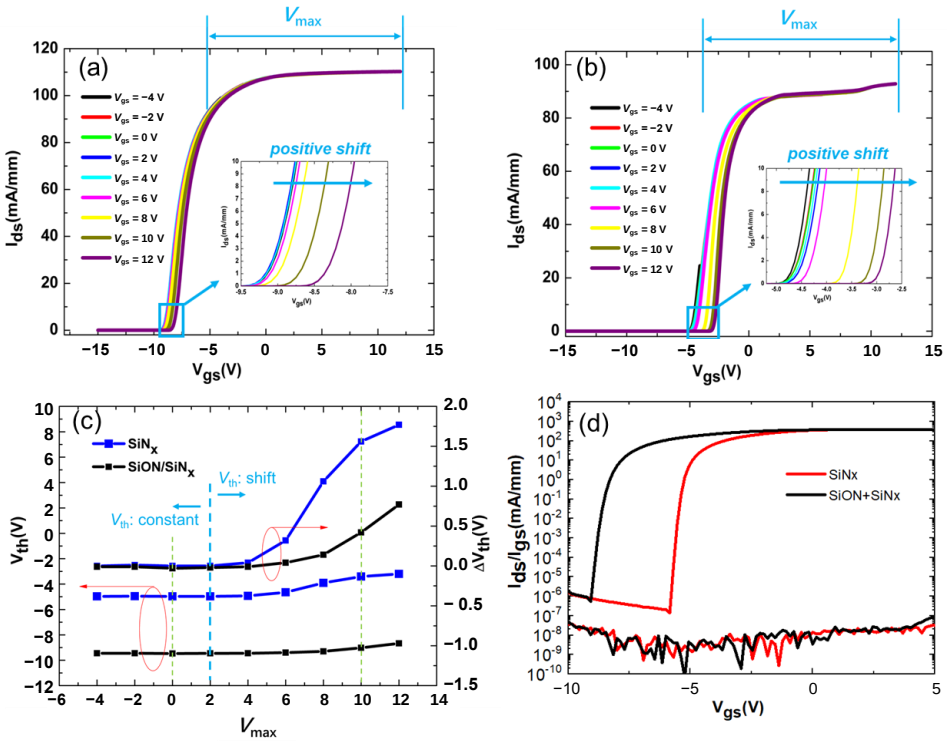

Figure 2. Transfer characteristics of AlGaN/GaN MIS-HEMTs with (**a**) SiN_x/SiON dual layers and (**b**) SiN_x layer under various gate-source voltage sweeps. (**c**) The threshold voltage (V_{th}) and the Vth hysteresis (ΔV_{th}) as a function of gate voltage stress (V_{max}). (**d**) Gate leakage comparison.

The influences of the OFF-state stress was also investigated to further compare the performance of the two kinds of devices as shown in Figure 3. The transfer curves of the MIS-HEMTs were first measured V_{max} = 10 V (shift region as shown in Figure 2c). Then, the devices were stressed by an OFF-state condition with V_{gs} of −10 V and V_{ds} = 1 V for 200 s. The transfer curves of the MIS-HEMTs after the OFF-state stress were measured with V_{max} = 10 V for comparison. The transfer curves with V_{max} = 0 V (constant region as shown in Figure 2c) are also shown in Figure 3 as references. The V_{th} of the MIS-HEMT with SiN_x/SiON composite gate dielectric exhibited a negative shift of 0.5 V, whereas the V_{th} of the MIS-HEMT with SiN_x only gate dielectric showed a negative shift of 0.62 V. The negative shift after the OFF-state stress indicates an electron releasing process from the traps to the 2DEG channel resulting in the recovery of the V_{th} [12].

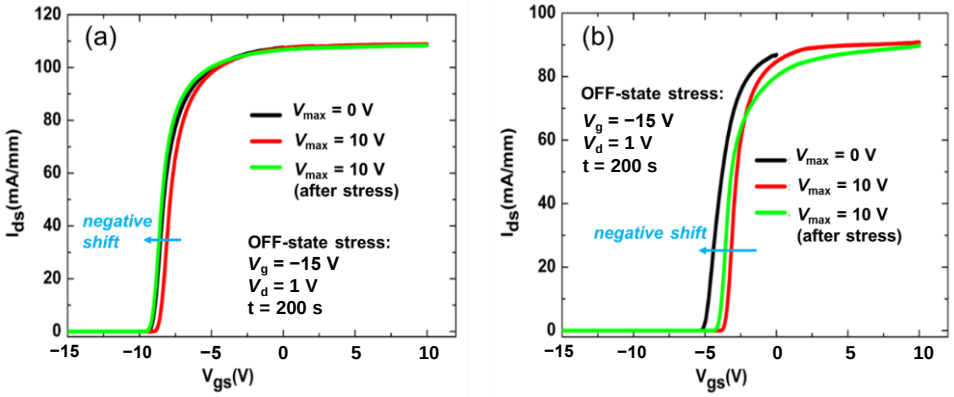

Figure 3. Transfer characteristics of the MIS-HEMTs with (**a**) SiN_x/SiON dual layers and (**b**) SiN_x layer before (black and red) and after OFF-state stress (green).

To clarify the trapping and detrapping process causing the shift of the V_{th}, the band diagrams of the MIS-HEMTs at the gate region are depicted in Figure 4 [30]. At thermal equilibrium, traps at the interface below the Fermi level are filled with electrons, whereas traps above the Fermi level are empty [19]. When $V_{gs} > V_{th}$, the Fermi level of the interface states shifts upwards resulting in more empty traps below the Fermi level. Then, the traps below the Fermi level will be filled by electrons from the channel, i.e., the electron trapping process, as shown in Figure 4a. The higher the V_{max} is applied to the gate, the more the electrons are trapped by the interface states, as shown in Figure 4b. This process causes the positive shift of the V_{th}. When the OFF-state condition or the negative gate bias is applied, the Fermi level shifts downwards resulting in the detrapping process of electrons back to the 2DEG channel, as shown in Figure 4c [31]. This process causes the negative shift of the V_{th}.

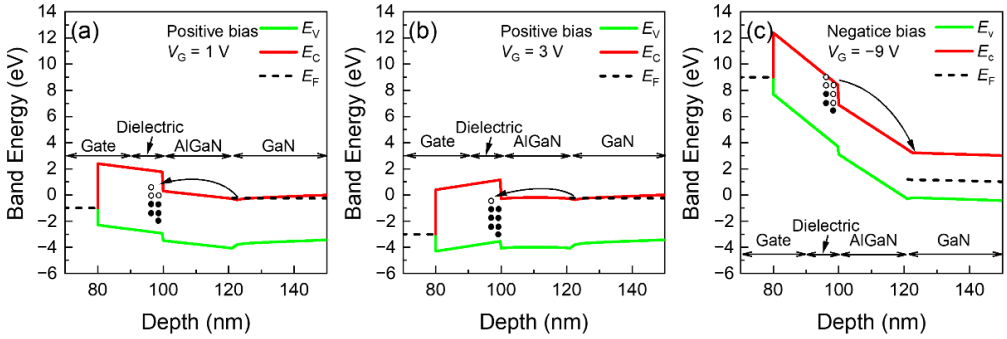

Figure 4. Schematic band diagrams of MIS-HEMTs at (**a**) positive bias (V_{max} = 1 V), (**b**) positive bias (V_{max} = 3 V), and (**c**) negative bias (V_{gs} = −9 V).

Capacitance method was used to evaluate the interface states [32]. Figure 5a,b show the C-V curves of the two kinds of MIS-HEMTs at different frequencies from 100 kHz to 1 kHz. There are two steps in the C-V curves. The first one corresponds to the 2DEG accumulation at the AlGaN/GaN interface. The second one corresponds to that at the dielectric/AlGaN interface. The interface state density can be estimated based on the frequency dispersions of the second slope onset. The detailed calculation formula can be found in [14]. The interface state density distributions as a function of energy level are presented in Figure 5c. At the energy level of 0.36 eV~0.47 eV, the interface state density of the MIS-HEMT with SiN_x/SiON composite gate dielectric was on the order of ~10^{13}, which is significantly smaller than that of the MIS-HEMT with SiN_x only. Compared with the SiN_x only dielectric, SiN_x/SiON can effectively reduce the overall interface states density, especially at deep energy levels. These results further prove that the SiN_x/SiON composite gate dielectric in this work can considerably reduce the interface state density thereby improving the electrical performance of the GaN-based MIS-HEMTs. The thicknesses of SiN_x and SiON extracted from the C-V profiles are 20.3 nm and 9.6 nm, respectively, which are consistent with the designed values. The output curves are shown in Figure 5d. The on-resistance for the MIS-HEMTs with SiN_x/SiON composite gate dielectric and SiN_x only gate dielectric is 3.12 mΩ·cm^2 and 3.4 mΩ·cm^2, respectively.

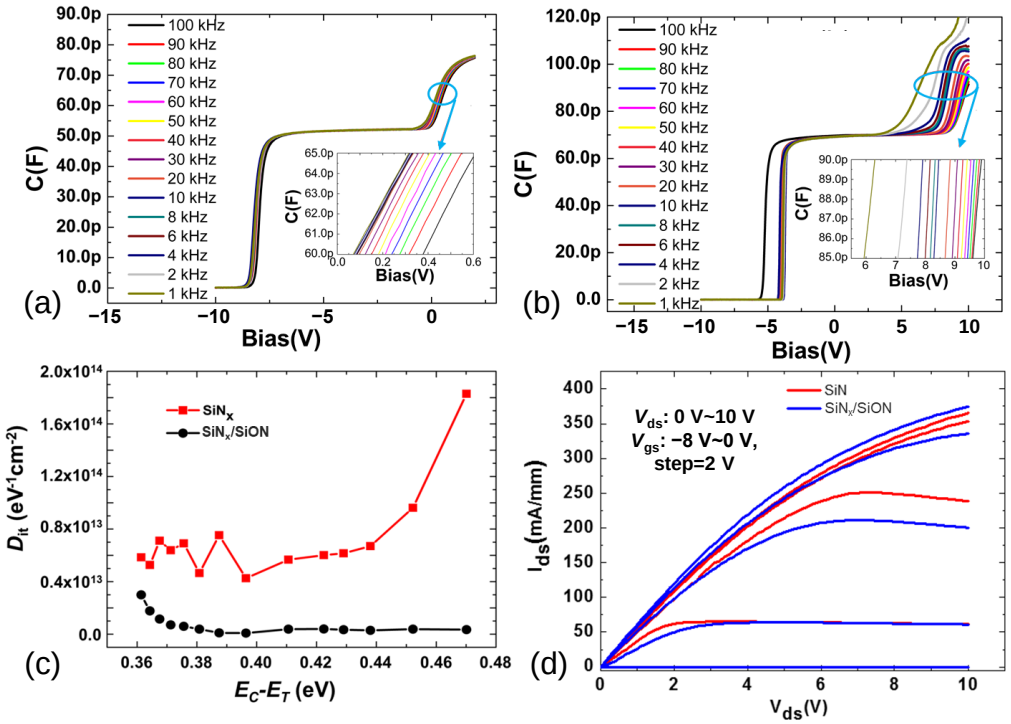

Figure 5. C-V curves of AlGaN/GaN MISHEMTs with (**a**) Si_3N_4/SiON composite gate dielectrics and (**b**) SiN_x gate dielectric. (**c**) The interface state density as a function of energy level for the AlGaN/GaN MIS-HEMTs with different gate dielectrics. (**d**) Output curves of the two kinds of devices.

4. Conclusions

AlGaN/GaN MIS-HEMTs on Si with SiN_x/SiON composite gate dielectric were demonstrated. Low-temperature PECVD-SiON can improve the contact interface between GaN and the dielectric layer, and suppress the high thermal decomposition of GaN surface during the LPCVD-SiN_x process. High-quality LPCVD-SiN_x can serve as an excellent gate dielectric to enhance device performance. Compared with the MIS-HEMT with only LPCVD-SiN_x, the device with the SiN_x/SiON composite gate dielectric showed more stable Vth and much smaller ΔVth. Frequency-dependent C-V measurements showed that the device with the composite dielectric had a significantly smaller interface state density. This work shows a route to realizing high-performance GaN-based MIS-HEMTs with a SiN_x/SiON composite gate dielectric layer.

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Data Availability Statement: The data presented in this study are available on request from the first author.

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