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Analysis of HBM Failure in 3D NAND Flash Memory

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Abstract: Electrostatic discharge (ESD) events are the main factors impacting the reliability of NAND Flash memory. The behavior of human body model (HBM) failure and the corresponding physical mechanism of 3D NAND Flash memory are investigated in this paper. A catastrophic burn-out failure during HBM zapping is first presented. Analysis shows that NMOS fingers' local heating induced by inhomogeneous substrate resistance R_{sub} and local heating induced by the drain contact and 3D stacked IC (SIC) structure lead to the failure. Therefore, a new approach is proposed to reduce local heat generation. Finally, by increasing N+ length (NPL) and introducing a novel contact strip, the silicon result shows enhanced ESD robustness.

Keywords: electrostatic discharge (ESD); human body model (HBM); transmission line pulse (TLP); technology computer aided design (TCAD); 3D NAND Flash memory

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1. Introduction

ESD testing is one of the major reliability qualifications for NAND Flash memory [1]. A common ESD event referred to as the human body model (HBM) is widely used to characterize device reliability when the charge in the human body is being transferred to the ground through integrated circuits. In addition, transmission line pulse (TLP) testing can provide reference for critical parameters in the ESD circuit [2–4]. Thus, testing with a combination of HBM and TLP is common practice [5,6]. There are some other efficient techniques that can be used for ESD robustness, such as TCAD simulation, layout modeling, and ESD device modeling [7–16], which enable quick pinpointing of design weakness and reduced development cycle and costs.

Nowadays, NAND Flash memory is widely used in mass storage applications. Three-dimensional NAND Flash memory with 3D stacked IC (SIC) [17,18] is the most viable solution for high-capacity storage and low-bit-cost non-volatile memory [19,20]. During the contact-type usage, the pins of packaged die may be exposed to ESD sources such as human fingers; hence, ESD immunity is required for NAND Flash memory. Thus, the study of ESD damage on 3D NAND Flash memory is of great significance.

In this paper, a severe HBM burn-out failure in 3D NAND Flash ESD stress is investigated. Local heating induced by inhomogeneous R_{sub}, the drain contact, and the 3D SIC structure is verified to be the cause of the ESD clamp failure. Consequently, an improvement in heat generation is proposed. Silicon analysis demonstrates the validity of process refinement.

2. ESD Clamp Device Structure

A simplified cross-sectional view of a 3D NAND Flash test chip is shown in Figure 1. Two stacking wafers are connected together by millions of bonding interface vias (BIVs) [17,18]. As shown in the figure, the ESD pad on the backside of the upper wafer is connected to

the ESD clamp circuit on the lower wafer through BIVs in between the two wafers [21–24]. During the ESD test, test voltage is applied to the metal pad on the top and discharge through the ESD clamp at the bottom.

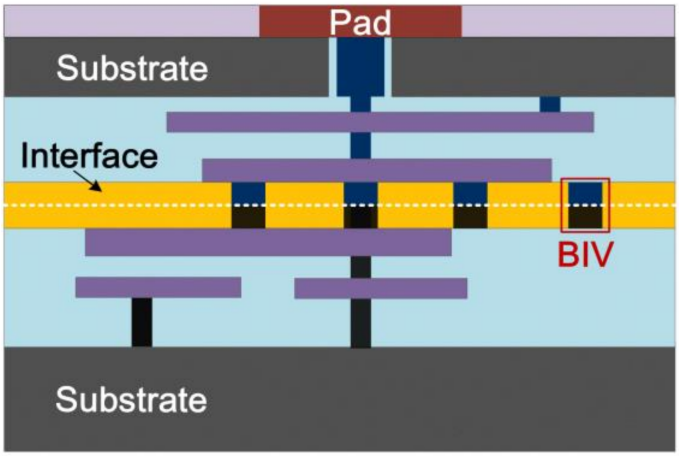

Figure 1. Cross-sectional view of 3D NAND Flash test chip.

The NMOS transistors used in the ESD clamp were fabricated with NAND technology. Figure 2 illustrates the cross-section and equivalent circuit of the HV NMOS of the ESD protection circuit in the NAND Flash test chip. N+ diffusion of the drain/source side is located inside the N-type lightly doped drain (N-LDD) area. Under the drain and source contacts (CTs), there is the silicide layer. The length from the drain contact to the N+ edge and the length from the N+ edge to the gate poly are referred to as N+ length (NPL) and N-LDD length (NLL), respectively.

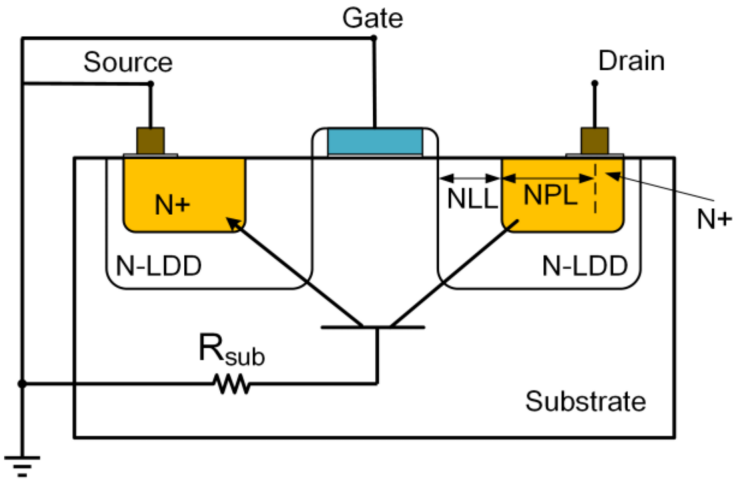

Figure 2. Cross-section of HV NMOS in ESD clamp circuit.

The simplified layout top view of the multi-finger NMOS in the ESD clamp is illustrated in Figure 3, with eight fingers shown. The multiple NMOS fingers are surrounded by a P+ guard ring, with their gate, source, and drain connected in parallel. The ground pad VSS is located at the right side of the floorplan and is outside of the P+ guard ring.

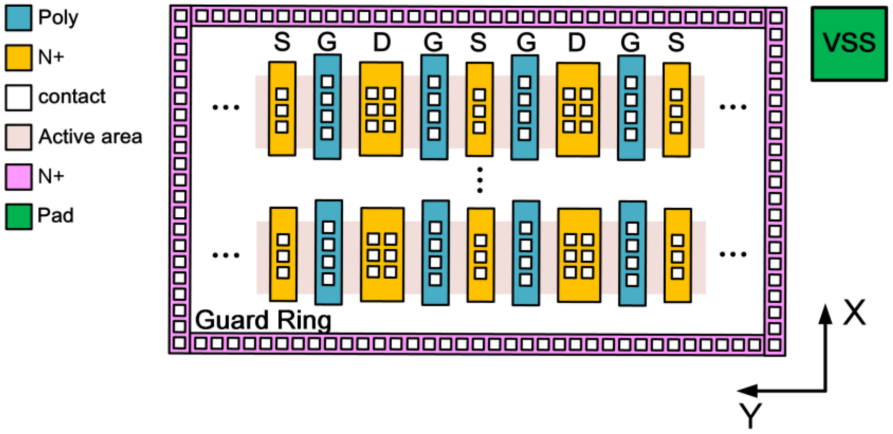

Figure 3. Layout top view for multi-finger NMOS in ESD clamp (simplified layout, N = 8).

3. HBM Testing System

In order to evaluate the ESD robustness of the NAND Flash test chip, an HBM test was performed on packaged dies. A KeyTek MK2 ESD tester was used. The HBM stress model is shown in Figure 4. The tester can provide a stepped testing voltage of up to 8 KV.

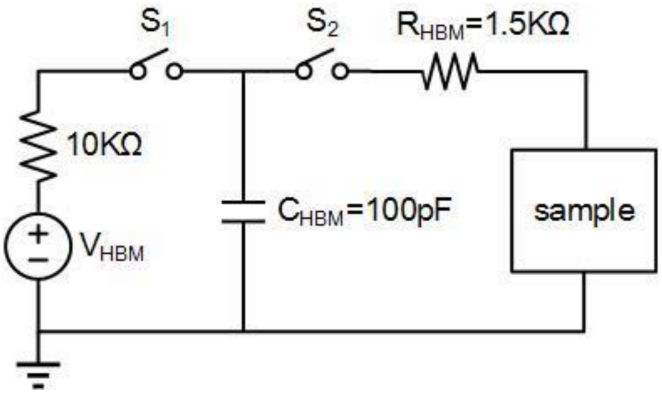

Figure 4. Schematic of a simplified HBM stress ESD model.

4. Experimental Results and Discussion

4.1. HBM Test Results

The general specification of a NAND Flash memory HBM test is 2 KV [25,26]. The testing voltage for HBM testing starts from 250 V and increases by 250 V per step. In this paper, an HBM test was performed on both a raw test chip sample and an optimized test chip sample with process splits. Failures were observed during the HBM test on the raw test chip sample. The process splits were then processed and verified through an HBM test.

Three raw test chip samples were chosen for the HBM test. As shown in Table 1, they failed at 1 KV, 1.25 KV and 1.5 KV. For each failed sample, the test voltage presented below was passed.

Table 1. HBM test results with raw test chip samples.

Sample	Failure Voltage (KV)
Sample 1	1
Sample 2	1.25
Sample 3	1.5

4.2. Failure Analysis: Multi-Finger NMOS

4.2.1. Analysis of NMOS Turn-On Nonuniformity

Failure analysis was conducted on the damaged pad of the failed 3D NAND Flash test chip after the 1 KV HBM test. Abnormal catastrophic burn-out was observed. As the SEM result shows in Figure 5, about 40% of the pad area was burned out, from the central area to the edge. This indicates that the heat generated during burn-out is tremendous.

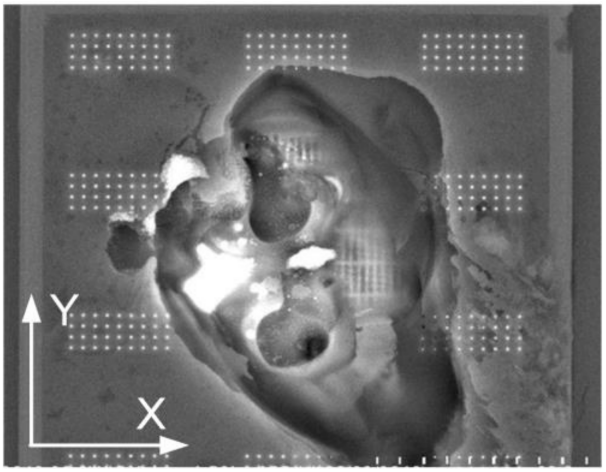

Figure 5. Burn-out damage observed with SEM of a failed 3D NAND Flash test chip sample.

The measured TLP results of the ESD clamp are illustrated in Figure 6. It can be seen that after some fingers are turned on by the pulsed voltage higher than V_{t1}, the maximum drain voltage V_D (around V_{t2}) remains below V_{t1} (V_{t1}: turn-on voltage, V_{t2}: thermal failure voltage). In addition, it can also be seen from the figure that the thermal failure current I_{t2} is much lower than the normal ampere level during ESD clamp discharges [27,28], indicating a partial turn-on of the fingers. The multiple extrapolation lines in the IV curve also suggest the different numbers of the turn-on of NMOS fingers. When V_{t2} remains below V_{t1}, the failed fingers will never turn-on before thermal failure. Hence, a problem with the nonuniform turn-on of the NMOS finger occurs. Accordingly, the ESD current mainly flows through the turned on fingers, which have limited charge and heat release ability. Once the temperature reaches the melting point of silicon and metals, thermal runaway occurs, resulting in severe device failure.

4.2.2. Analysis of Substrate Resistance

Figure 7a presents the simplified layout top view of the multi-finger NMOS with only one row of an NMOS finger shown. The marked red rectangle in Figure 7a represents the minimum repeatable NMOS finger unit whose equivalent substrate resistance network is shown in Figure 7b. Since each NMOS finger shares the drain and source with adjacent fingers, the marked finger's substrate area starts from the center of the shared drain to that of the shared source. Using technology computer-aided design (TCAD) simulation, the unit-length equivalent resistance of the substrate was obtained. By measuring the distance from the center *O* to the four sides of the rectangle, the substrate resistance network of a single NMOS finger could be illustrated in Figure 7b. The resistance from the center *O* to the VSS pad is essentially the R_{sub} of that NMOS finger.

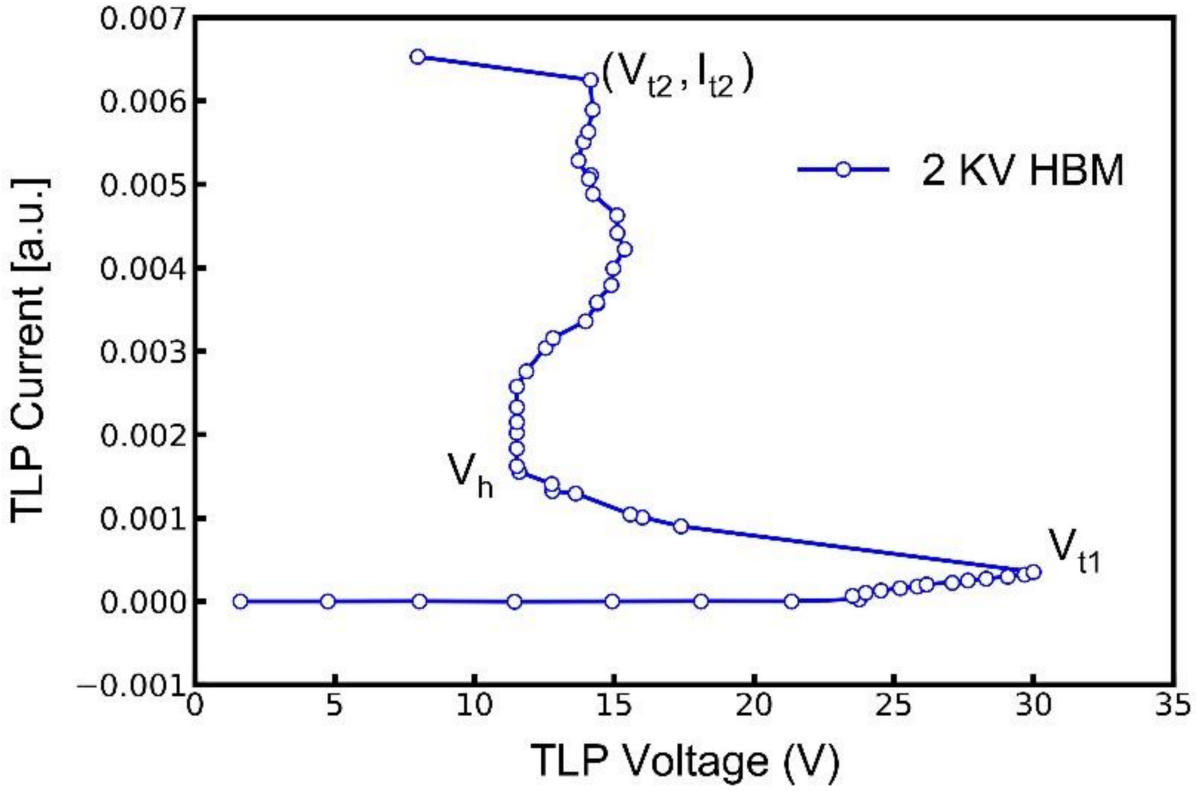

Figure 6. Measured TLP I-V curve for ESD protection circuit.

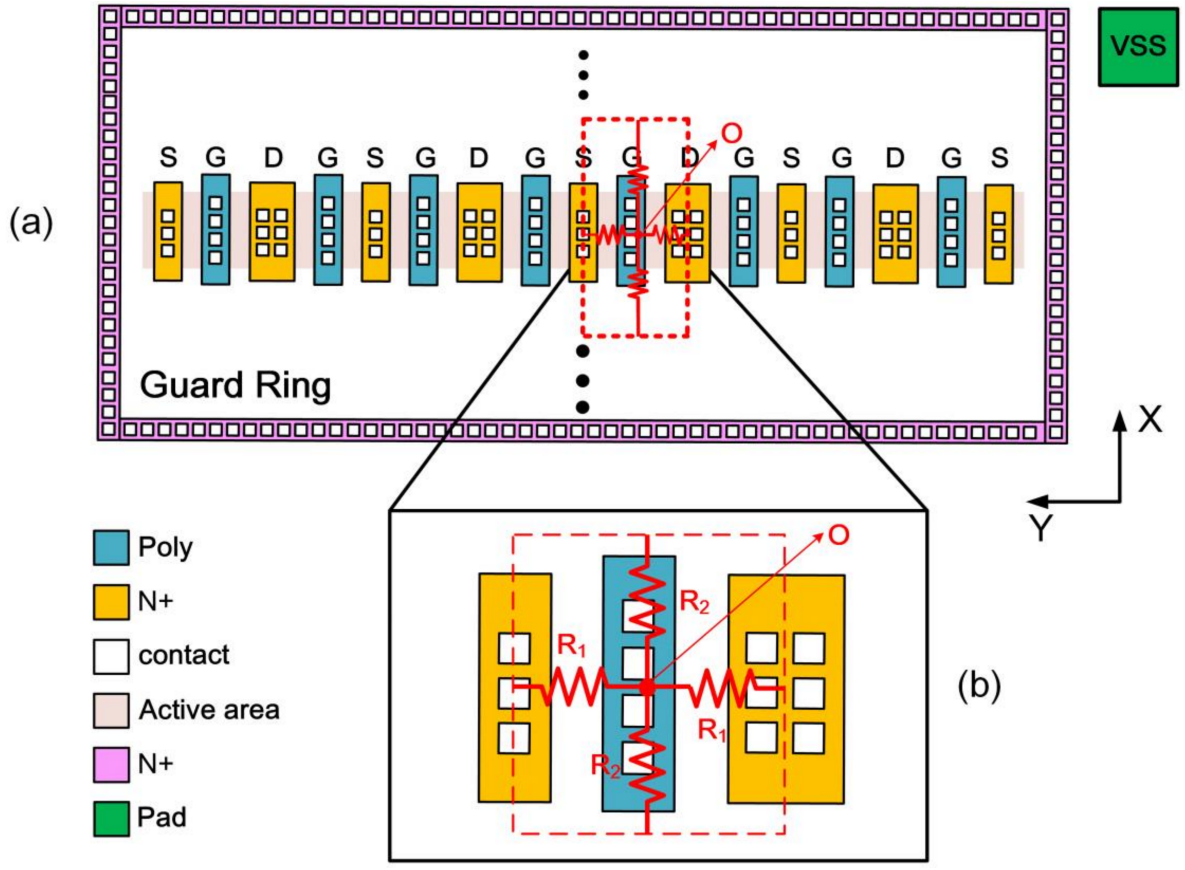

Figure 7. (**a**) Equivalent NMOS finger substrate resistance network of 8-finger example layout; (**b**) substrate resistance network for a single NMOS finger.

Figure 8 shows the multi-finger NMOS substrate resistance network. NMOS fingers are divided into edge fingers (zone A to zone H) and central fingers (zone I). All the central fingers share the same symmetrical network as shown in Figure 7b. For the edge fingers, the substrate length of the lateral side (close to the guard ring) is longer than that of the inner side due to the design rule limitation. Therefore, under the same unit-length equivalent substrate resistance, the lateral equivalent substrate resistance is larger than the inner substrate resistance. The equivalent resistance of the P+ guard ring is also presented in Figure 8. The guard ring is connected to the VSS pad in parallel with the ground bus. Similarly, the equivalent resistance can also be obtained with TCAD simulation.

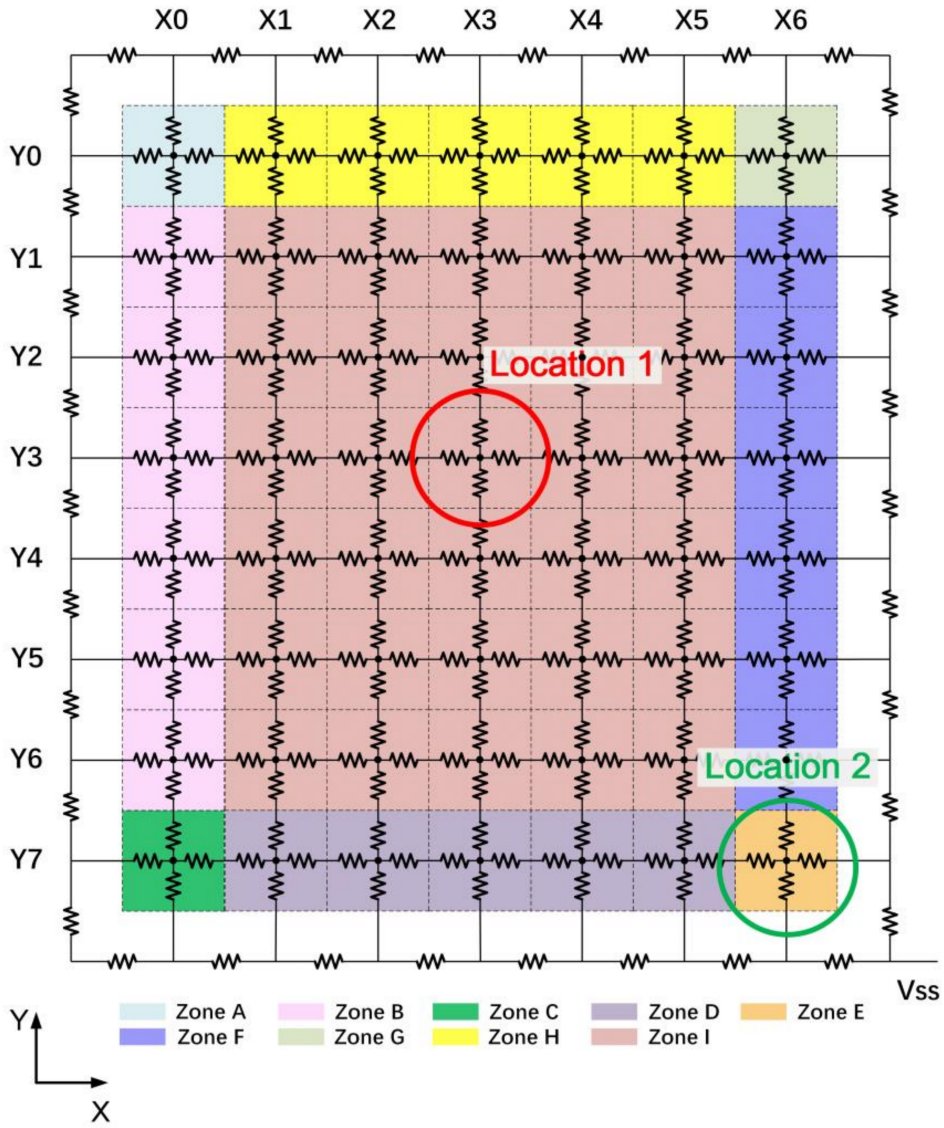

Figure 8. Multi-finger NMOS substrate resistance network in ESD clamp.

Based on the multi-finger NMOS's equivalent substrate resistance network shown in Figure 8, R_{sub} of each of the NMOS fingers is shown in Table 2. It can be seen that both the maximum R_{sub} and the maximum substrate voltage V_{sub} are found in Location 1 (X3, Y3).Near Location 1, NMOS transistors' R_{sub} values are very similar. Considering the nonuniformity of the substrate process, there could be more than one parasitic bipolar in the central area that turns on when V_D exceeds V_{t1}. When V_D remains below V_{t1}, the failed fingers remain turned-off before thermal breakdown happens. Hence, ESD current mainly flows through turned-on NMOS fingers, resulting in limited discharge current

I_{t2}. Moreover, limited contact count also impairs current spreading and heat dissipation. Therefore, local hot-spot formation in the central area raises the local temperature until the melting of silicon and metal occurs. This demonstrates that thermal failure is caused by nonuniformity in NMOS turn-on.

Table 2. NMOS finger equivalent substrate resistance by simulation (a.u.).

Y \ X	X0	X1	X2	X3	X4	X5	X6
Y0	6.11	6.03	5.94	5.84	5.72	5.59	5.47
Y1	8.57	8.97	9.05	9.02	8.90	8.66	8.13
Y2	9.19	9.82	10.06	10.08	9.95	9.61	8.87
Y3	9.37	10.10	10.39	10.45	10.32	9.94	9.15
Y4	9.30	10.04	10.35	10.42	10.30	9.93	9.15
Y5	8.97	9.65	9.91	9.97	9.88	9.57	8.86
Y6	8.19	8.65	8.80	8.83	8.77	8.58	8.10
Y7	5.52	5.52	5.52	5.51	5.49	5.45	5.41

4.3. Failure Mechanism Analysis: Drain Contact and 3D Stacking

4.3.1. Effect of Drain Contact

In the previous section, the correlation between local heating and NMOS finger turn-on nonuniformity was established using a substrate resistance network model. In addition to the burn-out marks on the ESD pad of the 3D NAND test chip shown in Figure 1, they were also found on the backside of the lower wafer.

In order to further verify the cause of the failure, focused ion beam (FIB) analysis was employed on the failed test chip. As shown in Figure 9, the FIB result exhibits cross-wafer and cross-layer burn-out, in which the upper and lower substrates are not shown. From the figure, it can be seen that the melted region involves both the upper wafer and the lower wafer [17], and device damage spreads across all metal layers and vias. Therefore, , this HBM failure not only causes large area burn-out of the pad in the horizontal direction but also induces damage from the pad down to the ESD clamp in the vertical direction. Normally, device damage in ESD failure is mainly concentrated in an area of a few micrometers within a single layer [28,29]. Such severe burn-out is extremely rare [27,30,31].

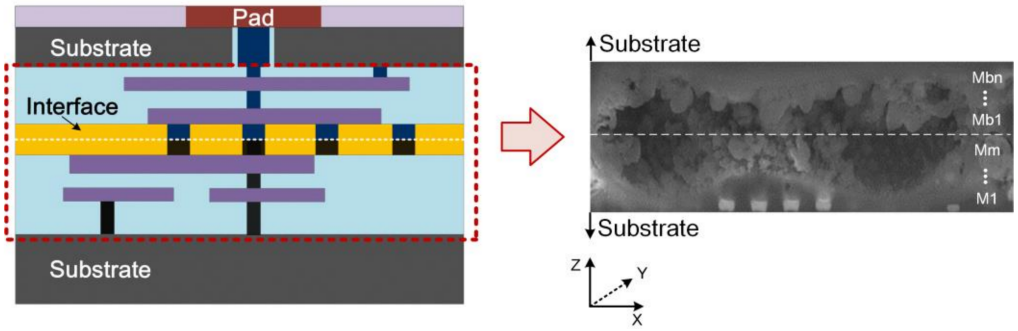

Figure 9. FIB-sectioned image of the burn-out damage.

Through further investigation, it was found that the material of the NMOS drain contact has a much higher resistivity and melting point than those of the material of metal layers and vias in the middle. Due to the NMOS finger nonuniform turn-on, the ESD current mainly flows through turned on NMOS fingers. Therefore, ESD current flows through a few drain contacts. When the current flowing through each contact exceeds its limit, local heating occurs at the drain contact. While local heating occurs at NMOS, a large quantity of heat is also generated and accumulated at the drain contact. Before

the temperature reaches the melting point of the contact, the contact keeps heating the surrounding area and metal layers. Hence, the drain contact could potentially be another heat contributor.

To further verify the effect of the drain contact, a process split with increased drain contact count was conducted in the experiment. As shown in Table 3, the ESD test results show improved ESD robustness. This proves that increasing the drain contact count can improve heat dissipation and reduce ESD failure. However, failure voltages vary from sample to sample, indicating that the ESD clamp turn-on nonuniformity issue still exists.

Table 3. HBM test results of a test chip with drain contact improvement.

Sample	Failure Voltage (KV)
Sample 1	2
Sample 2	2
Sample 3	2.5

4.3.2. Effect of 3D Stacking

In the previous section, the drain contact was validated to be the second contributor to local heating. However, the drain contact is located close to the ESD clamp and far from the ESD pad and middle metal layers. Such a severe multi-layer burn-out is still inexplicable.

As previously mentioned, the pad is connected to the ESD clamp through BIVs in the middle. Due to area and process limitations, there are limited BIVs on the discharge path, which have very high thermal resistance and generate a lot of heat. In [22], it is reported that a thermal hot spot in a 3D stack chip can cause the temperature to increase to a value that is three times higher than that in a 2D wafer. Compared with a 2D wafer, the same thermal power will cause a higher temperature in 3D stack usage. This is attributed to the weakened heat diffusion in the thinned die and the poor heat conducting adhesives used in the vertical integration, which bring in high thermal resistance. Therefore, when a hot spot forms on the ESD clamp, the temperature of the whole chip rapidly increases. Eventually, short-time large-quantity heat release occurs, resulting in cross-wafer cross-layer failure.

5. Optimization of Heat Generation

Under the ESD stress condition, the heat generated in the drain side is mainly composed of heat from the metal layers, NMOS fingers, and the drain contact. Since heat from the metal layers is design oriented, heat optimization mainly focuses on the NMOS finger and contact.

5.1. NMOS Heat Optimization

It has been demonstrated that R_{sub} is responsible for local heating. It can be noted that current mainly flows through the turned-on NMOS fingers of the burned out ESD clamp. As a result, under the same total ESD stress current, reducing each NMOS finger current by increasing the turned on NMOS finger count is effective in improving heat and ESD robustness.

During an ESD event, the electrical behavior of the NMOS transistor is determined by the parasitic lateral bipolar. With the NMOS turned off, the device IV curve will exhibit a snapback characteristic, with the drain voltage dropping from the junction breakdown voltage V_{t1} to the snapback voltage V_h. The variations in the junction profile and channel length are used to evaluate the correlation between device parameters and ESD performance. For an LDD device, the avalanche breakdown mainly occurs on the drain–substrate junction. Drain length consists of N-LDD length (NLL) and N+ length (NPL), as shown in Figure 10a.

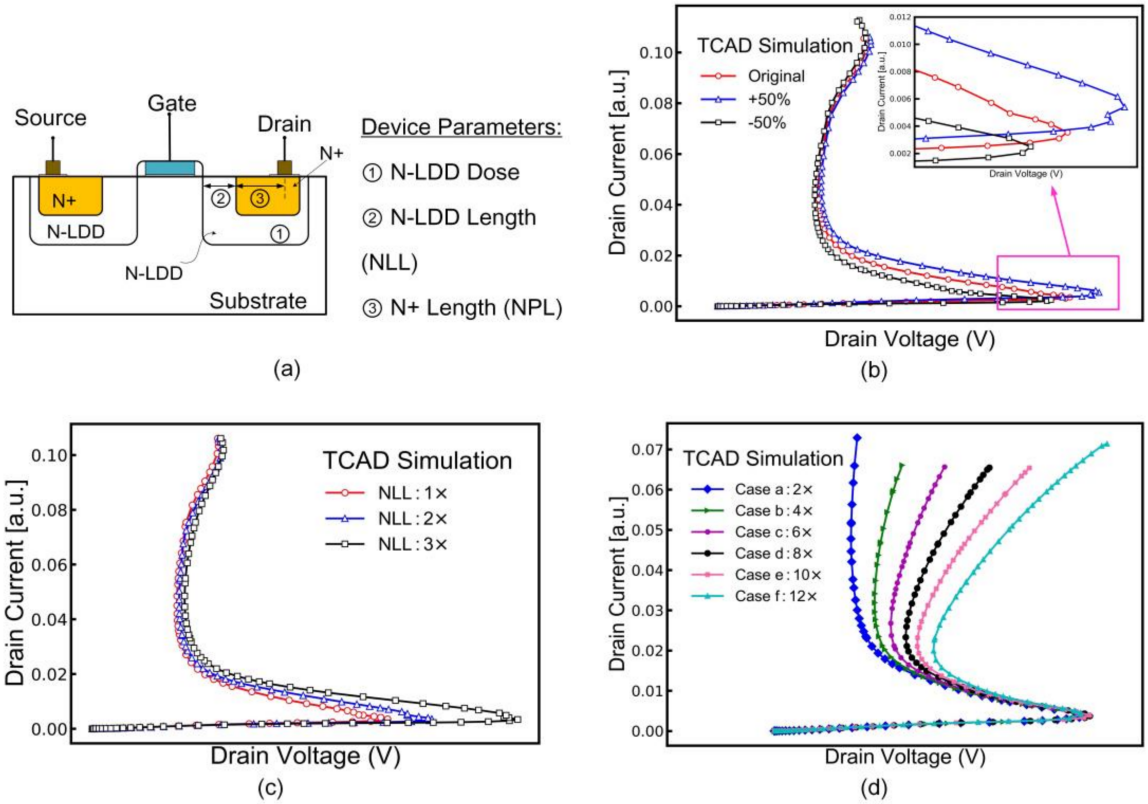

Figure 10. (**a**) Crosssection of LDD NMOS depicting various device parameters. IV curves of NMOS with varied (**b**) N−LLD dose, (**c**) NLL size, and (**d**) NPL size obtained using TCAD simulation.

The ESD performance of a single NMOS transistor with a different N-LDD dose, NLL, and NPL, as observed using TCAD simulation, is shown in Figure 10b–d. It can be seen that both the N-LDD dose and NLL have a similar influence on ESD behavior. The NMOS transistor exhibits increasing V_{t1} and unchanged V_{t2} with N-LDD dose and NLL change. On the other hand, the NMOS device exhibits increasing V_{t2} and unchanged V_{t1} with NPL change.

Figure 10b,c show the effect of the N-LDD dose and NLL on ESD performance. For the N-LDD device, avalanche breakdown occurs at the LDD–substrate junction. Electric fields exist parallel and perpendicular to the channel. The lateral electric field is weakened by the increased N-LDD dose [32]. Subsequently, it requires a higher V_D to provide sufficient I_{sub} to pull up the substrate potential to a voltage that is higher than the p–n junction turn-on voltage. In addition, the LDD device structure causes a reduction in electric-field intensity [33]. Increasing the N-LDD length would further reduce the electric-field intensity. Consequently, a higher V_D is needed to turn on the p–n junction.

Once the parasitic bipolar is switched on, the current flows from the drain to the substrate, and the N-LDD dose shows almost no influence on thermal breakdown. Furthermore, an increase in V_{t1}, as shown in Figure 10b,c, would jeopardize NMOS finger turn-on uniformity and, thus, induce thermal breakdown. Moreover, an enhanced V_{t1} could exceed the device stress voltage limitation and cause device failure even before the ESD clamp is turned on. Therefore, changing the N-LDD dose and NLL is not applicable.

Figure 10d shows the effect of NPL on ESD performance. It can be seen that when NPL increases from 2 times to 12 times the unit size, V_{t2} increases from around V_h to above V_{t1}, while V_{t1} remains unchanged.

For a triggered ESD clamp circuit, V_{t2} can be simply approximated as [34]

$$V_{t2} = V_h + I_{t2} * R_{on} \quad (1)$$

where R_{on} is on-resistance. With the increased NPL size, extra resistance R_D is introduced at the drain, as shown in Figure 11. Accordingly, we have

$$V'_{t2} = V'_h + I_{t2} * (R_D + R_{on}) \quad (2)$$

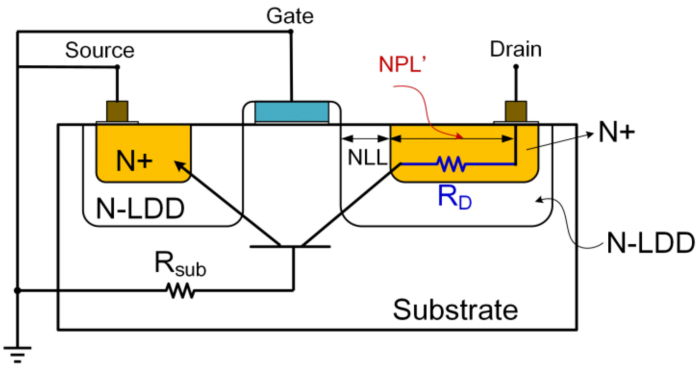

Figure 11. Cross-section of HV NMOS with extended N+ length.

For a single transistor, I_{t2} mainly depends on transistor width instead of channel length. V_h is given by the following equation:

$$V_{sb} \approx BV_{dss}(1-\alpha) \approx \frac{BVdss}{(2)^{1/n}}\left(L_{eff}/L_d\right)^{2/n} \quad (3)$$

where n is a constant, L_d is diffusion length, L_{eff} is effective channel length, and α is common base current gain [35]. Hence, both V_h and V_{t2} increase with NPL. As shown in Case f in Figure 10d, by moderately setting NPL, we can obtain a V_{t2} value that is higher than V_{t1}.

Before the drain–substrate junction is turned on, the drain has high impedance. I_{sub} is generated by the high voltage applied to the drain. Therefore, the new R_D has no influence on V_{sub} or on turn-on voltage V_{t1}.

A summary of the effect of N-LDD dose, NLL, and NPL on ESD performance is shown in Table 4. Increasing NPL size is the only effective option to improve LDD NMOS ESD robustness.

Table 4. Summary of ESD performance with different device parameters.

Device Parameter	V_{t1}	V_{t2}
N-LDD Dose	√	×
NNL	√	×
NPL	×	√

5.2. Contact Heat Reduction

According to the discussion above, besides multi-finger NMOS turn-on nonuniformity, the drain contact also contributes to the catastrophic burn-out. It is demonstrated that increasing the contact count can effectively reduce the heat generated. This is because the thermal power generated by the drain contact is directly proportional to the resistance and current flowing through it. Therefore, a novel contact strip process with no extra mask cost is introduced in this work. The total resistance of one novel contact strip decreases the column contacts to 14.9%.Therefore, contact improvements include increasing the contact column number to N times the original value and replacing the traditional contact column with a contact strip, as shown in Figure 12a–c. Assuming that N is 3, the total heat power of the drain contact is reduced to 4.97% of the original design.

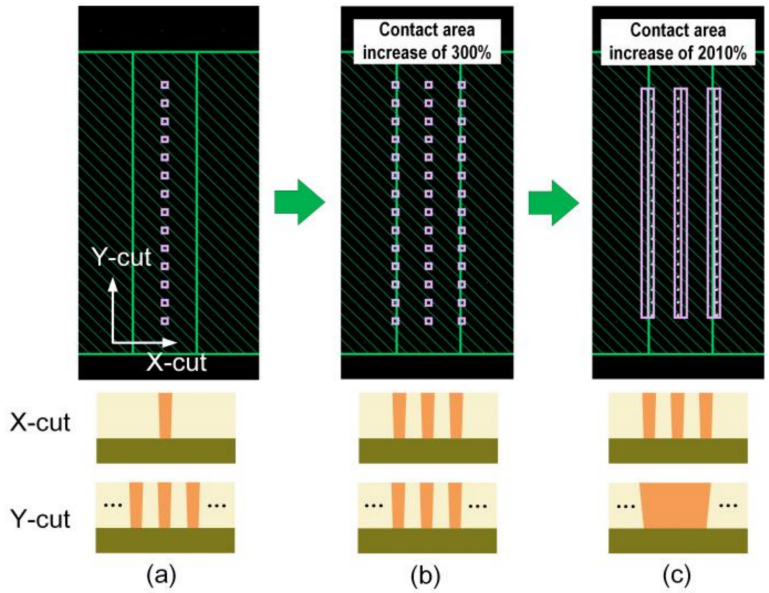

Figure 12. Contact change for dissipation improvement: (**a**) original contact count, (**b**) increased contact count (N = 3), (**c**) novel contact strip.

5.3. Silicon Results

From the many failure analyses and experimental results, process splits are used to validate the process improvement. Figure 13 shows the TLP characteristics of the multi-finger NMOS with different NPL sizes (2*M, 3*M, 4*M, 5*M, and 6*M), while NPL size in the original failed ESD clamp is M um. Compared to Case 1 and Case 2, V_{t2} exceeds V_{t1} in Case 3, Case 4, and Case 5, indicating that all the NMOS fingers turn on before thermal breakdown. However, Case 4 and Case 5 correspond to an increased on-resistance R_{on} and second breakdown trigger voltage V_{t2}, resulting in higher heat generation. Fabricated with the same material, the device dissipation ability remains the same. Thus, the power dissipation in Case 4 and Case 5 causes the temperature in the device to rise and eventually cause thermal breakdown, meaning silicon melting can occur. Therefore, the moderate V_{t2} in Case 3 is the optimal choice, which is also the only NPL size that falls between Case e and Case f in Figure 10d. The silicon verification result is in good agreement with the TCAD prediction.

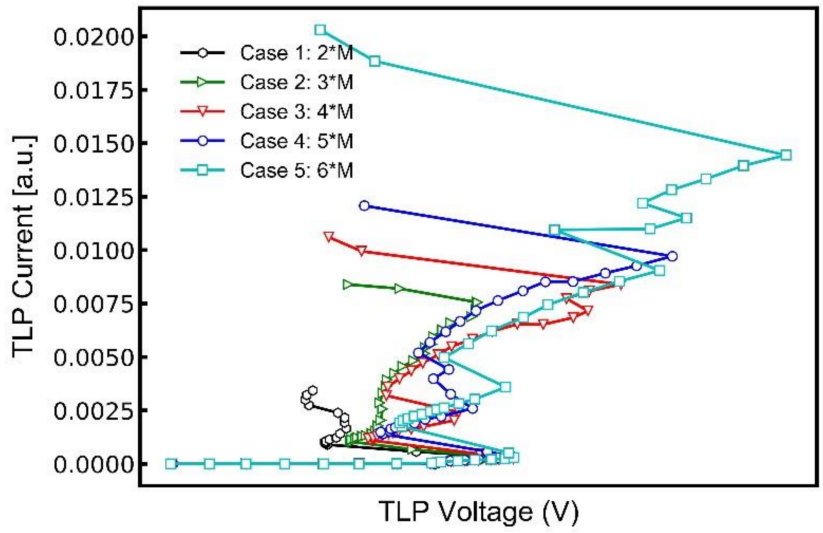

Figure 13. Measured multi-finger NMOS TLP IV curves with different NPL sizes.

From the TLP analysis above, the NPL size in Case 3, shown in Figure 13, is chosen as the final NPL size. Combined with an improved NMOS drain contact, the HBM test results are shown in Table 5. As shown in the table, the test samples exhibit good uniformity.

Table 5. HBM test results with NPL and drain contact improvement.

Sample	Failure Voltage (KV)
Sample 1#	3.5
Sample 2#	3.5
Sample 3#	3.5

6. Conclusions

In this paper, we investigated a catastrophic HBM failure in 3D NAND Flash technology. Through analysis, it was found that the NMOS turn-on nonuniformity and the local heating induced by the drain contact and 3D stack structure were the causes of the failure. The TLP measurement showed nonuniform turn-on in a multi-finger NMOS. Based on the substrate resistance network model, the distribution pattern of substrate resistance R_{sub} matched the burn-out finger location. Hence, local hot-spot formation in the early turn-on of NMOS fingers caused by R_{sub} induced thermal breakdown. In addition, due to the high melting point and high resistivity, the drain contact heated its surroundings, which produced a lot of heat. The thermal hot spot in 3D stacking resulted in a threefold increase in temperature, causing a large amount of heat to be released within a short time period. In conclusion, the increase in NPL and the introduction of a novel contact strip were demonstrated to be effective in local heat reduction. With device refinement, notable ESD immunity was attained with even higher voltage.

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Conflicts of Interest: The authors declare no conflict of interest.

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