



Article SEU Tolerance Efficiency of Multiple Layout-Hardened 28 nm DICE D Flip-Flops

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Abstract: Three layout-hardened Dual Interlocked Storage Cell (DICE) D Flip-Flops (DFFs) were designed and manufactured based on an advanced 28 nm planar technology. The systematic vertical and tilt heavy ion irradiations demonstrated that the DICE structure contributes to radiation tolerance. However, it is hard to achieve immunity from a Single Event Upset (SEU), even when a ~3-µm well isolation is utilized. The SEU mitigation of the hardened DFFs was affected by the data patterns and clock signals due to the imbalance in the number of upset nodes. When the clock signal equalled 0, no error was observed in ¹⁸¹Ta irradiation, indicating that the DICE DFFs are SEU tolerant in vertical irradiation owing to their reasonable isolation of sensitive volumes. The divergences of SEU cross-sections were enlarged by our specially designed joint change of tilt incidences for both the along-cell and cross-cell irradiation of heavy ions. The evaluations of SEU for both the vertical and tilt irradiations assist with eliminating the overestimation of SEU tolerance and guarantee the in-orbit safety of spacecraft in harsh radiation environments.

Keywords: D Flip-Flop; heavy ion; radiation hardened; Single Event Upset

1. Introduction

As a key component of digital circuits, there is wide concern about the irradiation tolerance of D Flip-Flops (DFFs) in advanced technologies in the context of the increasingly unparalleled performance requirements of space electronic systems, despite their reduced area and power consumption [1–4]. The standard Dual Interlocked Storage Cell (DICE) has been applied to DFFs in deep-submicron planar Complementary Metal Oxide Semiconductor (CMOS) technologies to achieve low Single Event Upset (SEU) rates [3,4]. However, the critical charges of SEU for DFF cells are not high, especially for the advanced nanoscale technologies [3–6]. Moreover, the heavy ion-induced charge sharing phenomenon among adjacent sensitive nodes increases the probability of upsets, making the basic hardening techniques ineffective [5,6]. Thus, it is essential to characterize the radiation tolerance and evaluate the effectiveness of hardening strategies of nanoscale circuits.

In recent years, some heavy ion irradiation results for the standard and hardened DFFs of different process nodes have been characterized, and the main SEU cross sections in the published literature are shown in Table 1 [3–6]. The heavy ion irradiation results for the 65 nm standard DFF, basic DICE DFF, and a temporal-DICE DFF are presented in Ref. [3]. The temporal-DICE DFF comprises a temporal structure for its master latch and a DICE structure for its slave latch, which is expected to be SEU hardened. However, merely the basic DICE DFF presents an enhanced radiation tolerance, indicating that the basic DICE DFF appears to be the most attractive for achieving a very high radiation hardness with the least circuit overheads in terms of area and power dissipation [3]. The different SEU cross sections of 40 nm and 28 nm DFFs are illustrated in Ref. [4]. It has been



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Copyright: © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). found that the standard 40 nm design has a larger SEU cross-section than the standard 28 nm design [4]. At the LET value of 60 MeV·cm²·mg⁻¹, the upset cross sections for the 28 nm designs are statistically identical, whereas there is still a noticeable improvement for the 40 nm capacitive hardened DFF, indicating that for the advanced technologies, using capacitance to reduce SEU cross-sections for high LET particles is unattractive [4]. The SEU cross-sections for a broad scope of parameters including the clock frequency and angle of incidence are characterized for the hardened and unhardened DFFs in 32 nm Silicon on Isolator (SOI) technology [5]. The 32 nm DICE DFF is improved in SEU tolerance, while the influence of LET values and frequency is significant. Additionally, the LET values used in Ref. [5] are not high and, therefore, cannot fully characterize the failure rates of hardened DFFs. Thus, the tilt incidence of high-LET heavy ions should be utilized to further investigate the mechanisms of SEU sensitivities, especially for the hardened DFFs. Besides, the vertical heavy ion irradiations are utilized to study the standard and hardened DFFs that employ compact (1.05 μ m) or separate (2.25 μ m) DICE structures in 22 nm SOI technology in Ref. [6]. Additionally, the enhanced SEU tolerances are verified for the DICE DFFs with either compact or separate structures [6]. Thus, the spacing of sensitive nodes is also an essential parameter that affects the SEU tolerance of DICE DFFs.

Table 1. Heavy ion irradiation results of DFFs with different process nodes of planar technologies in published Refs. [3–6]. The LET (MeV·cm²·mg⁻¹) values and the corresponding cross-sections (σ : cm²·bit⁻¹) are shown below. (Cap = capacitance; Stan. = Standard DFF without radiation hardening; T-DICE = Temporal-DICE).

	65 nm			40	nm	32 nm SOI		
Туре	Stan.	DICE	T-DICE	Stan.	Cap. (×2.5)	Stan.	DICE	
Max. LET	~48	~48	~48	~60	~60	~40	~40	
σ	$\sim 3.3 \times 10^{-6}$	$\sim 6.7 \times 10^{-8}$	$\sim 1.6 \times 10^{-6}$	$\sim 1.1 \times 10^{-8}$	$\sim 1.5 \times 10^{-8}$	$\sim 1.5 \times 10^{-10}$	$\sim 6.5 \times 10^{-11}$	
		28 nm			22 nm SOI			
Type	Stan	C_{22} ($\times 1.5$)	C_{22} (\times 3)	Stan	DICE	DICE		
туре	Start.	Cap. (×1.5)	Cap. (~3)	Stall.	(1.05 µm)	(2.25 µm)		
Max. LET	~60	~60	~60	~85	~85	~85		
σ	$\sim 4.5 \times 10^{-9}$	$\sim 4.5 \times 10^{-9}$	$\sim 4.5 \times 10^{-9}$	$\sim 7.5 \times 10^{-10}$	$\sim 5.0 \times 10^{-11}$	$\sim 5.0 \times 10^{-11}$		

Based on the discussions above, it is confirmed that the DICE hardened DFFs with multiple node spaces have not been fully investigated using systematic heavy-ion irradiations. The high-LET heavy-ion irradiations with different tilt angles are not available in the literature, but the high-LET ions are essential for verification of the SEU sensitivities and hardening effects on the circuits [6–11]. In addition, the 28 nm bulk planar devices are not well represented in the layout-hardened circuits and irradiation results, with the result that the SEU mechanisms of 28-nm planar devices are not clear [11–16]. Therefore, the characterization of 28 nm DICE hardened DFFs with different node spaces is essential to reveal the basic features of SEU sensitivities and promote the effective application of radiation hardening design for the 28 nm high-performance digital circuits and systems.

In this paper, three different DICE hardened DFFs were designed and fabricated in a 28 nm planar technology to fully characterize their SEU sensitivities. The test circuits were fabricated using a metal-gate process with a high-k gate dielectric, and isolated with shallow trench isolation (STI) technology. It is expected that the measured radiation results of the designed DFFs will provide sufficient SEU support data to guide the design of in-orbit applications. The rest of the paper is organized as follows: Section 2 details our specially designed DFFs including the layouts with hardening strategies and irradiation parameters; Section 3 presents the results for vertical and tilt irradiation of heavy ions; and in Section 4, the irradiation results are summarized and discussed in detail.

2. Circuits Design and Irradiation Setup

The DFF test chip was designed and fabricated using a commercial 28 nm planar bulk silicon process. The test structure was constructed with three chains of DICE DFFs and each chain contained 2000 cascaded DFFs. The three DFF chains had a shared data input (DI) and clock (CK), but their output ports (DOs) were separate. All the DFFs were designed with the normal DICE structure consisting of the double master latches and double slave latches as shown in Figure 1. The CK buffers employed in each DICE DFF determine the working state of the master latches or the slave latches in the DFF. When CK = 1, the dual interlocked master latches ML1 and ML2 maintain the logic value, while the slave latches SL1 and SL2 are bypassed. When CK = 0, the slave latches SL1 and SL2 maintain the logic value while the master latches ML1 and ML2 are bypassed. All the DFFs in one chain were designed with the same layout structures, but the DFFs in different chains were designed with different layout structures as shown in Figure 2. The three detailed layout structures of DFF0, DFF1 and DFF2 are shown in Figure 2a–c, respectively. The circuit structures and the basic layout of the three DFFs are identical, whereas the different node spacing of the three DFFs was designed to achieve the exact isolation of the two interlocked latches of the DICE structure. The drain regions of the off-state MOS transistors are regarded as sensitive volumes (SV). In addition, the minimum SV spacings of the two interlocked latches in DFF0, DFF1, and DFF2 were ~1.68 µm, ~1.95 µm, and ~3.00 µm, respectively. The effectiveness of DICE hardened circuits and the degree of charge sharing effects for 28 nm planar technology were evaluated directly according to the irradiation results of the different DFFs.

An SEU test system was developed to evaluate the SEU sensitivities of the different DFFs. As shown in Figure 3, the system was composed of a motherboard and a daughterboard. The DFF test chip installed on the daughterboard was controlled and monitored by the FPGA-based motherboard via a digital board-to-board I/O interface. A host computer located in the heavy-ion radiation room was connected to the FPGA via a RS-232 interface in order to control the test and record all the data. Another remote computer located outside the radiation room was connected to the host computer inside the radiation room via an ethernet link to enable the operator conduct the test.

Before the heavy-ion irradiation, the FPGA provided the input value via the DI and a 40 MHz clock signal via the CK to each chain to first initialize the stored logic value of all the DFFs. Then the clock signal CK was set to stable to place the DFFs in a static mode and fix the working latches in a DFF. After that, the heavy ions struck the DFF test chip until the fluence reached 10⁷ ions·cm⁻². Then the 40 MHz clock signal was inputted to the CK, and the logic value stored in all the DFFs was read by the FPGA, which recognized and counted all the upsets simultaneously for each chain. The upset count of each chain was reported to the host computer, and the host computer analyzed the data in real time, displayed the SEU counts, and recorded all the information.

The heavy-ion tests were conducted with the Single-Event Effect Test Terminal (SEETT) at the Heavy Ion Research Facility in Lanzhou (HIRFL) of the Chinese Academy of Sciences. The flux of ions was controlled at 10^4 ions·cm⁻²·s⁻¹. The vertical irradiation (0°-tilt) and tilt incidences (30°, 45°, and 60°) were used, and the air-layer and 8.3 µm passivation were accounted for in the calculation of the ions' energy and Linear Energy Transfer (LET) values so that the experimental heavy ions reached the SV with sufficient energy deposition. The heavy-ion irradiation conditions and parameters used in the experiments are listed in Table 2. The DFF test chips were de-capped before exposure to irradiation, and the passivation layers on the top of the chip included aluminum, copper, silicon dioxide, tungsten, and other passivation materials. The Input/Output (I/O) and core voltages of the test chip were set at 1.8 V and 0.8 V, respectively, during the irradiation. The ¹⁸¹Ta ions with a controllable 1865 MeV of energy at the surface of the sample chip were selected to receive the large-tilt incidence during irradiation, and the high-LET ¹⁸¹Ta ions were selected to receive the SEU sensitivities of the hardened circuits with isolated SVs. In addition, the X-direction (along-cell irradiation) and Y-direction (cross-cell irradiation) were classified.

Hence, a coefficient for the effective fluence (F_{eff}) of ions in SV was required for the tilt incidence, which is related to the beam fluences (F) counted by the particle detector and the cosine value of tilt angle with a vertical direction (θ).

$$F_{eff} = F \cdot \cos\theta \tag{1}$$



Figure 1. The basic structure of the hardened DFFs.



Figure 2. Layouts of (**a**) DFF0 with a minimum sensitive node at ~1.68 μ m, (**b**) DFF1 with a minimum at ~1.95 μ m (minimum well spacing), and (**c**) DFF2 with a minimum sensitive node at 3.00 μ m (well spacing).



Figure 3. Specially designed SEE testing system.

Tabl	e 2.	Inf	formation	about t	he	parameters	of ion	s and	irrac	liati	ion	condi	tions.
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Energy in SV (MeV)	LET (MeV·cm ² ·mg ^{−1})	Range in Silicon (µm)	Tilt (°) (x, y)	Data Pattern	Clock
1695.3	78.3	99.2	(0, 0)	1 & 0	1&0
1623.8	79.0	95.3	(0, 45)	1 & 0	1
1521.7	80.1	89.8	(0,60)	1 & 0	1
1668.8	78.6	97.8	(0, 30)	1 & 0	1
1623.8	79.0	95.3	(45, 45)	1 & 0	1
1623.8	79.0	95.3	(45,0)	1 & 0	1
1668.8	78.6	97.8	(30, 0)	1 & 0	1
1521.7	80.1	89.8	(60, 0)	1 & 0	1

3. Irradiation Results

The iradiation results are presented in this section. We only recorded the error events induced by a single ion; thus, the SEU cross-sections (σ) are calculated by

$$\sigma = \frac{\sum_{j} j \cdot N_{j}}{F \cdot N \cdot \cos\theta} \quad j = 1, 2, 3, \cdots$$
(2)

where *j* is the error bits of an SEU event, N_j is the number of SEU events involving j-bit errors, *F* is the beam fluences, $cos\theta$ is the cosine value of tilt angle with vertical direction, and N is the total bits of DFF. The SEU cross-sections of three DFF chains were extracted by our test system. The one-sigma error bar of SEU cross-sections was calculated for each experimental condition and noted in our following figures. The results of static SEU cross-sections with different data patterns and CK signals are shown in Figure 4. It was found that no Multiple Bit Upsets (MBU) were observed in the test, because each DFF was placed in a unique well region, and all of the DFFs in a chain were separated by over 15 µm, which is effective in preventing the charge sharing effects and MBUs. The downward-pointing arrows in Figure 4 mark the limited value of no upset events. It means that if no upset event was observed during the full irradiation procedure, the maximal SEU cross-sections $(1/(F \cdot N \cdot cos\theta))$ are marked in the figure and labeled with the downward-pointing arrows.



Figure 4. Data patterns and CK dependence of SEU cross-sections.

For CK = 0, the master latches were under the bypass state, while the logic values of slave latches was maintained. No upset was observed in vertical ¹⁸¹Ta irradiations (CK = 0), indicating that the DICE DFFs have SEU tolerance owing to their reasonable isolation of SVs. For CK = 1, the working functions of master latches and slave latches were exchanged. When both the CK and DI were equal to 1, the SEU cross-sections of DFF0, DFF1, and DFF2 were $\sim 3.2 \times 10^{-9} \text{ cm}^2/\text{bit}$, $\sim 3.6 \times 10^{-9} \text{ cm}^2/\text{bit}$, and $\sim 5.6 \times 10^{-9} \text{ cm}^2/\text{bit}$, respectively. When the CK = 1, and the DI = 0, the SEU cross-sections of DFF0, DFF1, and DFF2 were ~7.7 \times 10⁻⁹ cm²/bit, ~9.5 \times 10⁻¹⁰ cm²/bit, and <5.0 \times 10⁻¹¹ cm²/bit, respectively. The SEU cross-sections indicate that the large-area well isolation can improve the SEU tolerance of the DFFs for full 0 data, whereas for the full 1 data, the well isolation seems to slightly increase the SEU sensitivities. The measured SEU cross-sections of the two data patterns are different because the structures of the DFFs are asymmetric. The circuit-level simulations with the double-exponential model were conducted to investigate the imbalance of the SEU susceptibility of DFFs, and the results are shown in Table 3. The number of upset nodes means that the upset data of DFF was observed if the selected nodes of transistors in DFF were injected by the transient pulse with an equivalent LET value at $\sim 80 \text{ MeV} \cdot \text{cm}^2 \cdot \text{mg}^{-1}$. Based on the data in Table 3, it is clear that the number of upset nodes was significantly increased when CK = 1. This is because the DICE structure of the master latch and slave latch in DFF is asymmetric for the consideration of driving behavior. In addition, the asymmetric structure leads the SEU cross-sections of DFFs to have clock and data pattern dependency.

Table 3. Results of the double-exponential pulse injections (LET = $\sim 80 \text{ MeV} \cdot \text{cm}^2 \cdot \text{mg}^{-1}$).

	DFF0	DFF1	DFF2
Number of upset nodes ($DI = 0$, $CK = 0$)	2	2	2
Number of upset nodes (DI = 1, CK = 0)	2	2	2
Number of upset nodes (DI = 0 , CK = 1)	16	16	16
Number of upset nodes (DI = 1, $CK = 1$)	13	13	13

The systematic along-cell irradiations with $0-60^{\circ}$ changeable tilt angles as well as the cross-cell irradiations with $0-60^{\circ}$ changeable tilt angles were all conducted, and the results are shown in Figures 5 and 6. The SEU cross-sections of DFF0 presented in Figure 5a,b indicate that the SEU sensitivities of DICE DFF0 tend to increase with the increase of the tilt angles. However, the tendency for the variation of SEU cross-sections depends on

the direction of incidences and data patterns. It is obvious that the full 0 data is sensitive to both the along-cell tilts and cross-cell tilts, while the SEU cross-sections of full 1 data are not improved for the 60° cross-cell irradiation when compared with the 45° crosscell irradiation, which does not conform to the law of effective LET. In addition, a slight increase of SEU cross-sections with the increase of tilt angles for the full 1 data of the well-isolated DICE DFF1 was observed, as shown in Figure 5c,d, and the improvements of SEU cross-sections for the 60° tilt angle were not obvious compared with the 45° tilt angle. Besides, the hardening effectiveness of the full 0 data for DFF1 decreased in tilt angle irradiations. Moreover, an obvious inhibitory effect of well isolation on the SEU sensitivities was observed in the results presented in Figure 5e,f. The DICE DFF2 showed SEU immunity for the full 0 data until tilt angles over 45° , whereas the 60° cross-cell tilt incidences made the large well isolation less effective. When DI = 1, the SEU cross-sections of DFF0-2 at 60° tilt were two to three times larger than at vertical irradiation, which approximately follows the law of $1/\cos\theta$. However, when DI = 0, the SEU cross-sections of DFF0 and DFF1 at 60° tilt present orders of magnitude differences to the vertical irradiation, which may be related to the parasitic amplification effect caused by the tilt incidence.



Figure 5. Cont.



Figure 5. SEU cross-sections of DFFs vs. tilt angles: (a) X-direction for DFF0; (b) Y-direction for DFF0; (c) X-direction for DFF1; (d) Y-direction for DFF1; (e) X-direction for DFF2; (f) Y-direction for DFF2.



Figure 6. SEU cross-sections of the three DFFs (tilt angle: $X = Y = 45^{\circ}$).

The joint change of tilt angles was achieved in the irradiation experiments, and the results are shown in Figure 6. It is clear that the SEU sensitivities of DFFs depend on the data patterns. For DFF0 and DFF1, the SEU cross-sections of full 0 data were higher than that of full 1 data, whereas the data pattern dependency for DFF2 was different. Comparing the three DFFs, the SEU cross-sections for full 0 data decreased from DFF0 to DFF2, while the SEU cross-sections of along-cell and cross-cell tilt incidences had higher SEU cross-sections than the single 45° tilt incidence for all of the DFFs.

More detailed comparisons for different tilt angles and DFF chains are provided in Figure 7a,b. For full 0 data, the steady decreases of SEU cross-sections for DFF0-2 were measured, which is also consistent with the variation of the along-cell and cross-cell tilt irradiation, indicating that the well isolation was effective for full 0 data. However, for the full 1 data, the mechanisms for the SEU mitigation of well isolation are more complicated, especially for the large 60° tilt. Compared with the results in Figure 7a,b, it was found that the radiation tolerances of full 1 data are much better than the full 0 data for all of the test DFF chains, which is due to the asymmetric structure of the master latch and slave latch in DFF.



Figure 7. Comparison of SEU cross-sections under different tilt angles for (a) DI = 0 and (b) DI = 1.

4. Discussion: Hardness Assurances and Failure Analyses

The basic heavy-ion characterizations for the regular bulk planar DFFs and deepsubmicron Partially Depleted Silicon on Insulator (PDSOI) DFFs are complete, and the SEU results are reported in references [1-11]. The SEU cross-sections of conventional DFF decrease with the decrease of the technology nodes, whereas the SEU results for the DICE DFF are not consistent with the tendency for feature size shrinking [1,2,7-9]. To minimize the area of the layout, the saturated SEU cross-section of our DFF0 was nearly in the same order of magnitude as SEU cross-sections for the other DICE DFFs provided in previous work [1,2,7–11]. However, the well-isolated DFF1 and DFF2 displayed the same principle of SEU cross-sections only for the condition of full 1 data. For the full 0 data, the hardening effectiveness was much improved. In addition, the SEU sensitivities of DFF manufactured by the 130 nm bulk planar, 130 nm SOI technology, and 22 nm SOI technology have been investigated [6,10]. An approximately two orders of magnitude improvement of SOI DFF in mitigation of SEU cross-sections was verified, indicating that the SOI technology seems to have advantages to further decrease the SEU sensitivities of the nanoscale DICE DFF, and the physical separation of adjacent devices may lead to more enhancements of SEU tolerance for the nanoscale SOI process than the bulk planar process [6,17–19].

For space applications of high-performance electronic systems, the SEU sensitivities of advanced 28 nm technology must be known. Thus, the SEU sensitivities for the 28 nm radiation hardened DFFs are characterized and discussed in Section 3. It was found that the condition of CK = 1 dominated the calculated SEU cross-sections for all of the hardened DFFs, which is due to the approximate sensitive volumes that the DICE DFF cells have. Besides, it is known that the nanoscale devices have limited SEU critical charges, indicating that the charge sharing phenomenon for bulk planar technology can affect the DICE circuits with sufficient charge deposition in coupled SVs. Moreover, it should be noted that the ~3 µm well isolation in 28 nm planar technologies still cannot fully prevent the high-LET heavy ions induced SEUs. Hence, the upsets occurred in these small DFF cells should be fully evaluated before considering whether they are acceptable for space application for a certain mission. Furthermore, though the well isolation applied in DICE DFFs can reduce the SEU rates, it has limited effectiveness due to the lack of well contacts, leading the ionized charges to diffuse and affect more transistors. Therefore, simple well isolation is not a good option for DICE DFFs to further mitigate SEU sensitivities, and in the case of high SEU rates, the well contact seems essential to further mitigate the SEU cross-sections, especially for the layouts with a large spacing of well isolations.

Another interesting phenomenon we observed is that the joint change of tilts can further increase the SEU cross-sections of the hardened circuits, and the mechanisms of

SEU sensitivities for the hardened circuits are related to the actual projective spaces and spaces of SV pairs under different heavy-ion irradiation conditions, as shown in Figure 8. The direction of irradiation with the tilt of $X = Y = 45^{\circ}$ shows shorter spacing of the transistors than the individual tilt of $X = 45^{\circ}$ or $Y = 45^{\circ}$, meaning that more serious SEU sensitivity will be observed under the $X = Y = 45^{\circ}$ conditions. It is clear that the tilt incidence of high-LET heavy ions can have a more serious influence, especially for the redundancy hardened circuits. Therefore, considering the 4π -distributed high-energy heavy ions in space environments, the evaluation of SEU for both the vertical and tilt irradiations of high-LET ions is necessary to eliminate the overestimation of SEU tolerance and guarantee the in-orbit safety of spacecraft in harsh radiation environments.



Figure 8. Diagrams for the equivalent projective shapes and spaces of SV pairs under diverse heavyion tilt incidences. (a) vertical irradiation, (b) $Y = 45^{\circ}$ tilt, (c) $X = 45^{\circ}$ tilt, and (d) $X = Y = 45^{\circ}$ tilt.

5. Conclusions

In this paper, the SEU performances of different DICE DFFs fabricated with an advanced 28 nm planar technology are presented. The proportions of SEU cross-sections for the different irradiation conditions are distinguished and classified. The different clock dependency is related to the unbalanced structure of master latch and slave latch in DFFs, which can be explained by a greater than six times difference in the number of upset nodes. The DICE DFF2 is SEU immune for the full 0 data until tilt angles over 45°, whereas the 60° tilt incidences make the ~3-µm well isolation less effective. The abundant testing stresses combined with diverse layout structures indicate that the SEU immunity is hard to achieve for the 28 nm planar technology. Though the area consumption of the well isolation is non-negligible, the improvements of SEU tolerance are not obvious. In addition, the joint changes of tilts (X = Y = 45°) improve the SEU sensitivity of the hardened DFFs, which needs full consideration for the space application of hardening circuits due to the existence of long-range high-LET heavy ions in space environments. The heavy-ion evaluations are useful for the related integrated circuits and provide data to support the radiation hardening design of 28 nm technology.

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