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Current Collapse Conduction Losses Minimization in GaN Based PMSM Drive

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Abstract: The ever-increasing demands on the efficiency and power density of power electronics converters lead to the replacement of traditional silicon-based components with new structures. One of the promising technologies represents devices based on Gallium-Nitride (GaN). Compared to silicon transistors, GaN semiconductor switches offer superior performance in high-frequency converters, since their fast switching process significantly decreases the switching losses. However, when used in hard-switched converters such as voltage-source inverters (VSI) for motor control applications, GaN transistors increase the power dissipated due to the current conduction. The loss increase is caused by the current-collapse phenomenon, which increases the dynamic drain-source resistance of the device shortly after the turn-on. This disadvantage makes it hard for GaN converters to compete with other technologies in electric drives. Therefore, this paper offers a purely software-based solution to mitigate the negative consequences of the current-collapse phenomenon. The proposed method is based on the minimum pulse length optimization of the classical 7-segment space-vector modulation (SVM) and is verified within a field-oriented control (FOC) of a three-phase permanent magnet synchronous motor (PMSM) supplied by a two-level GaN VSI. The compensation in the control algorithm utilizes an offline measured look-up table dependent on the machine input power.

Keywords: GaN; frequency converter; current-collapse; loss optimization; PMSM

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1. Introduction

Due to emerging legislation and growing societal demands in many countries worldwide, the requirements for the efficiency of electrical equipment are constantly increasing. This trend is also driven by the ongoing boom in electromobility, where it is essential to achieve a high power density of the onboard and offboard electronic components. Therefore, in the field of power electronics and electric drives, significant effort is put into developing more efficient and compact devices and converters.

The design of small and highly efficient power converters for electric motors demands wide bandgap semiconductors such as those based on Silicon Carbide (SiC) and Gallium Nitride (GaN). Due to a significant reduction in switching losses, GaN-based transistors offer superior performance in high-frequency hard-switched converters than silicon transistors [1,2]. For these advantages, they are also starting to be used in electrical drives [3]. On the other hand, GaN devices also bring a few problems and challenges to the converter design and control stage. One of them is a current-collapse phenomenon that increases the conduction losses of power converters [4].

By the current-collapse, we mean resistance variations of the conductivity channel shortly after the transistor has been turned on [5]. This variation is caused by trapped charges at the gate electrode of the GaN transistor structure in the off-state [6]. The amount of trapped charge is then dependent mainly on the DC-link voltage as reported in [7] for p-doped GaN. In hard-switched converters, this phenomenon increases total losses

approximately two times, meaning that the converter heatsink system needs to be designed for double the dissipated power than what corresponds to the datasheet parameters. This disadvantage often leads to the deployment of GaN transistors in small and low-power applications rather than electric drives (which are dominated by hard-switched converters) [8,9].

Various papers try to model the current-collapse in GaN structure [10,11] to better comprehend its behavior with respect to the operating conditions, such as the transistor blocking voltage [12]. The phenomenon is also being extensively measured on various structures too [13,14]. There are also current-collapse-free GaN transistors under development [15–17]. However, presently available GaN devices still exhibit the deteriorated behavior caused by the increased on-state resistance. For instance, the current-collapse of the common GS66516 transistor, which is also utilized in this paper, was thoroughly investigated in [18].

Several approaches to reducing the losses caused by the current-collapse phenomenon have been proposed in the literature. Most solutions are based on hardware (HW) modification, with the most significant being the utilization of soft switching [19]. However, this technique complicates the converter circuit and usually doubles the number of transistors and inductors [20].

Generally, when speaking about specific problems connected with power electronic converters, software-based solutions are always preferred over hardware ones, since hardware solutions complicate the resulting circuitry and increase the cost and volume of the converter. Therefore, this paper strives to present a simple approach that mitigates the current-collapse losses of hard-switched three-phase two-level voltage-source GaN inverters (VSI). The solution is based on the author's static measurements [21] and utilizes the classical 7-segment space-vector pulse-width modulation (SVPWM) modified to omit short gate pulses when the reference vector approaches the voltage limit. The presented control algorithm operates with optimum modulation based on an offline measured look-up table (LUT) over the whole power range of the drive. The proposed method is suitable mainly for basic control strategies that do not need the knowledge of the stator voltage vector within the control algorithm (e.g., position sensor-based control with the direct transformation of the measured currents) since it brings voltage distortion at high modulation index values. The presented approach is validated within a field-oriented control (FOC) of a 0.5 kW permanent magnet synchronous motor (PMSM) drive fed by GaN VSI.

2. Theoretical Analysis

The three-phase VSI in Figure 1. is a hard-switched type of converter. Each time one transistor in one leg is turned on and the other is turned off, a blocking voltage equal to the DC-link voltage is present across the non-conducting transistor.

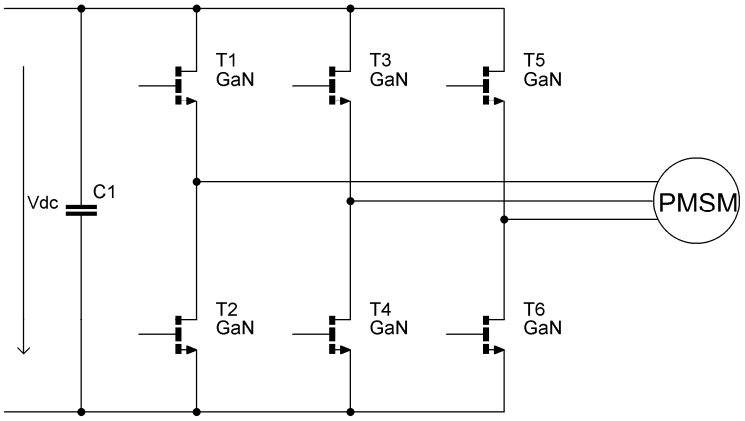

Figure 1. Three-phase two-level GaN voltage-source inverter.

Due to this type of operation (i.e., switching during "high" blocking voltage), the GaN transistor suffers from the current-collapse phenomenon, which causes higher state resistance right after each turn-on process [12]. The resistance increase depends on the blocking voltage, current polarity, and gate pulse length [13]. The behavior of dynamic on-state resistance R_{DSon} with respect to blocking voltage V_{DS} and time is illustrated in Figure 2.

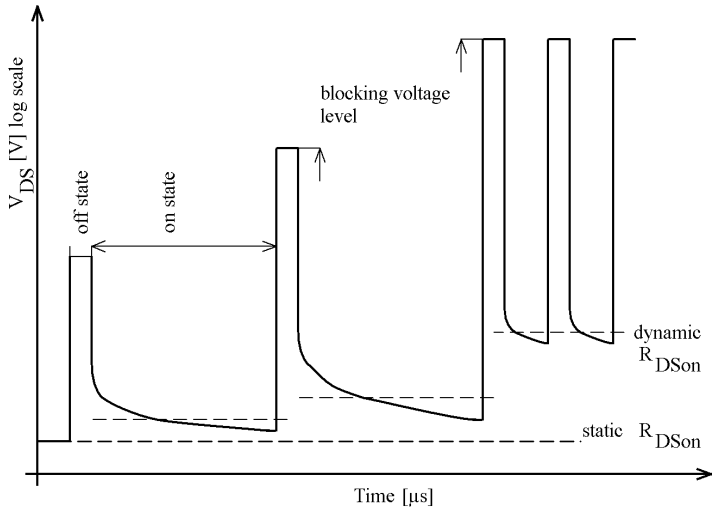

Figure 2. Current-collapse effect on on-state resistance.

In Figure 2, the transistor is turned on at the beginning with the static R_{DSon} value. After the transistor is turned off and a blocking voltage of a certain level for a certain amount of time is applied across the transistor, the following turn-on process increases the dynamic R_{DSon} because of the trapped charges around the gate that lead to the channel resistance increase. The resistance stays at a relatively high value until the parasitic charge is depleted. The dynamic R_{DSon} is then dependent on the blocking voltage level to which the transistor structure is exposed. The situation is illustrated within the second pulse in Figure 2. When the turn-on duration is short, there is not enough time for the trapped charges to be removed, and dynamic R_{DSon} becomes significantly higher as shown by the last two pulses in Figure 2. The most significant part of the additional resistance is the channel's resistance, which is based on the volt-ampere characteristic of the transistor. Concerning the channel's current i_{ch}, it is usually expressed in the literature as [8]

$$i_{ch} = g_m(V_{GS} - V_{th}) \tag{1}$$

where g_m is the device transconductance, V_{GS} applied gate voltage from the driver, and V_{th} the threshold voltage. During the current-collapse, both g_m and V_{th} are affected when the structure is exposed to a higher blocking voltage before the turn-on process. The transconductance is decreased, and the gate threshold is biased to a higher value. As a consequence, the transistor acts as it would receive a gate pulse of an insufficient voltage level (i.e., as it would work in a linear mode).

The contribution of the R_{DSon} resistance to the conduction losses can then be analytically expressed as

$$P_{cond} = R_{DSon} \cdot i_{DS}^2, \tag{2}$$

$$P_{cond} = \frac{1}{T} \sum_{i=0}^{N} R_{DSon(i)} \cdot i_{DS(i)}^2 \cdot t_{on(i)}, \tag{3}$$

where T is switching period, N number of pulses per period, $R_{DSon(i)}$ on-state resistance during the pulse, $i_{DS(i)}$ current through the transistor, $t_{on(i)}$ the turn-on time for which the power losses are calculated.

The problems, their causes, and the possible solutions connected with the current-collapse phenomenon are described briefly in Figure 3. Soft switching is a very effective method for decreasing the conduction losses; however, it requires additional hardware to be added to the converter, approximately doubling the resulting number of transistors. The blocking voltage regulation can also mitigate the effect of current-collapse. However, it requires the possibility of changing the VSI DC-link voltage value, which may result in the presence of an additional converter. This technique is sometimes used to decrease motor losses when the drive works with variable load and under variable speed conditions [22].

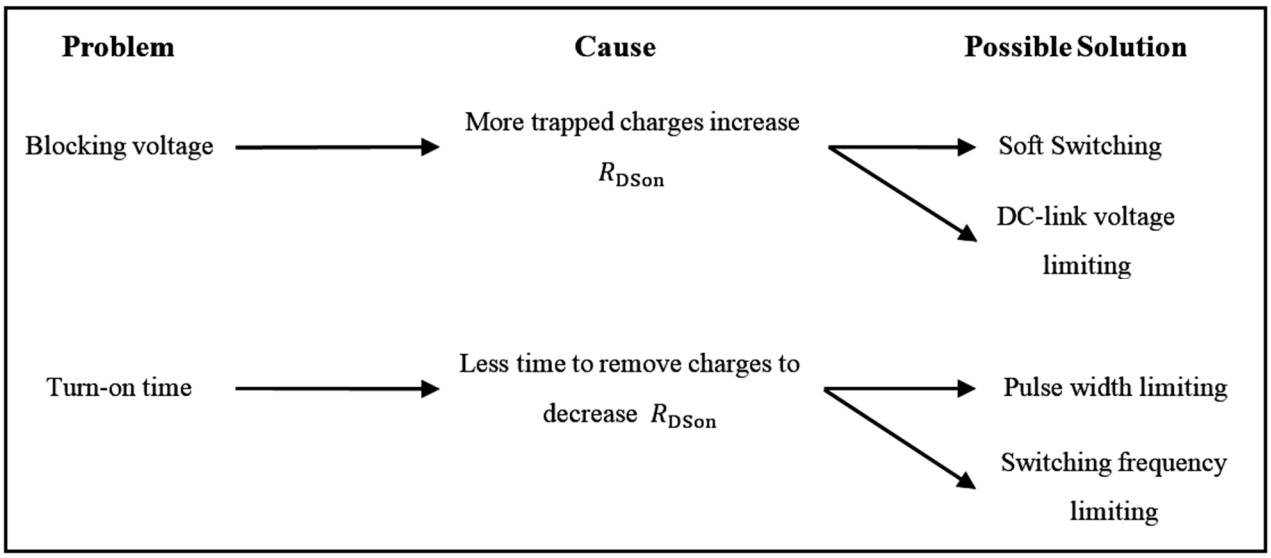

Figure 3. Problems connected with current-collapse, their causes, and possible solutions.

Decreasing the switching frequency is often used in medium- and high-power silicon-based converters to minimize the switching losses. However, in the case of GaN converters, it is generally desirable to keep the switching frequency constant and as high as possible to fully utilize the potential of the GaN devices (i.e., benefits such as easy filtering and smoothing of the motor current waveform by the motor leakage inductance) [23].

Following the above analysis, the motivation is to avoid the converter topology modification and the reduction of the switching frequency. Therefore, the solution that will be described in more detail in the following sections is purely software-based and utilizes the modification of the SVPWM pattern along with the omission of short pulses.

2.1. Space-Vector Modulation with Minimum Pulse Limitation

SVPWM is a popular modulation strategy that is extensively used in the field of electric drives. In a linear mode, it maximizes the DC-link voltage utilization, i.e., increases the modulation index compared to other modulation types while keeping undistorted sinusoidal waveforms of the motor line-to-line voltages [24]. Mathematically, the modulation can be written as

$$v_A > v_B > v_C \quad \text{or} \quad v_C > v_B > v_A \begin{cases} d_A = \dfrac{(v_A - v_C)}{2v_{DC}} \\ d_B = \dfrac{(2v_B - v_A - v_C)}{2v_{DC}} \\ d_C = \dfrac{(v_C - v_A)}{2v_{DC}} \end{cases}, \tag{4}$$

$$v_B > v_A > v_C \quad \text{or} \quad v_C > v_A > v_B \begin{cases} d_A = \dfrac{(2v_A - v_B - v_C)}{2v_{DC}} \\ d_B = \dfrac{(v_B - v_C)}{2v_{DC}} \\ d_C = \dfrac{(v_C - v_B)}{2v_{DC}} \end{cases}, \tag{5}$$

$$v_A > v_C > v_B \quad \text{or} \quad v_B > v_C > v_A \begin{cases} d_A = \dfrac{(v_A - v_B)}{2v_{DC}} \\ d_B = \dfrac{(v_B - v_A)}{2v_{DC}} \\ d_C = \dfrac{(2v_C - v_A - v_B)}{2v_{DC}} \end{cases}, \tag{6}$$

where d_A, d_B, d_C are modulator output duty cycles (i.e., the values that are compared with the triangular carrier signal) and v_A, v_B, v_C are the three-phase voltages demanded by the superior control system, and v_{DC} is the DC-link voltage. Figure 4a shows the duty cycle d_A, d_B, d_C of each inverter leg including the sinusoidal output $d_A - d_B$ which represents the relative output voltage between phases A and B.

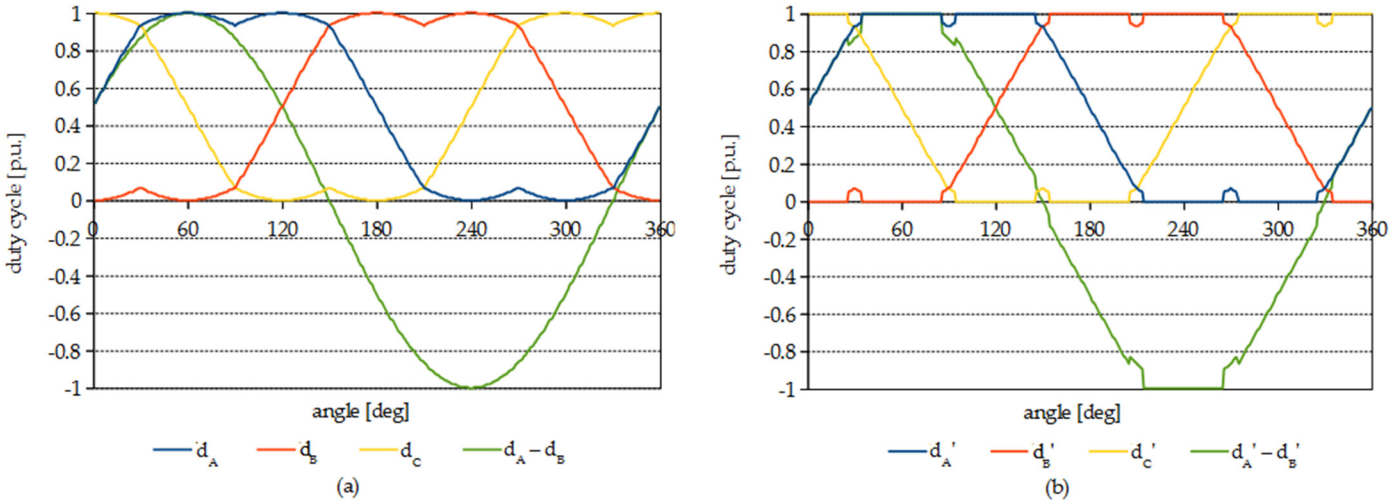

Figure 4. SVPWM modulation (**a**) linear mode and (**b**) deformed modulation with 5% pulse limitation.

For the reduction of the current-collapse conduction losses, the SVPWM is modified to exclude short pulses of given time duration. The situation is depicted in Figure 4, which shows the duty cycle waveforms in a linear mode (Figure 4a) and with the 5% percent pulse limitation (Figure 4b).

The duty cycle is equally limited in all the output phases. Depending on the limiting value d_{limit}, the modulation is adjusted as

$$d'_x = \begin{cases} d_x & \dots \text{ if } \quad d_x > d_{limit} \\ 0 & \dots \text{ if } \quad d_x < d_{limit} \\ 1 & \dots \text{ if } \quad (1 - d_x) < d_{limit} \end{cases} \qquad x = A, B, C. \tag{7}$$

Unfortunately, the technique of short pulse reduction results in the deformation of the motor voltage. The voltage vector deformation is shown in Figure 5a for the case of a stationary $\alpha\beta$ reference frame and in Figure 5b for the case of a synchronous dq reference frame. However, because only the basic sensored FOC is considered, the current controllers compensate for this distortion by adjusting the reference d and q-axis components.

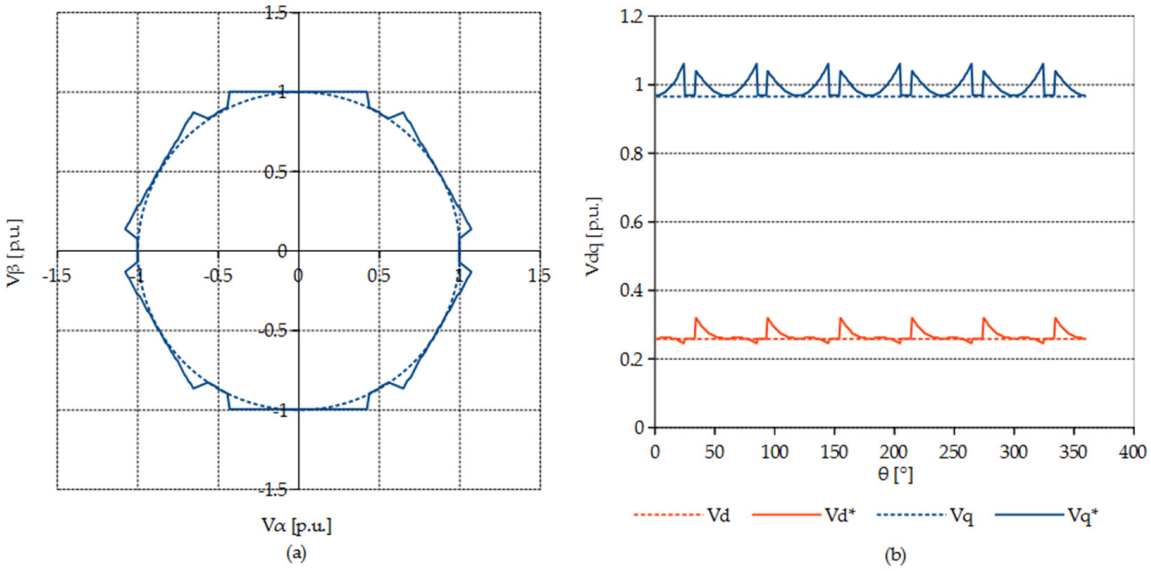

Figure 5. Deformation of the voltage vector caused by the pulse length limiting set to 5% of the duty cycle at a load angle of 15°; the reference voltage components are denoted by an asterisk. (**a**) stationary $\alpha\beta$ reference frame; (**b**) synchronous dq reference frame.

2.2. Drive Losses Analysis

If the power balance of the DC-link voltage source is neglected, the total drive losses can be divided into converter and motor losses. Limiting the minimum pulse length decreases the losses caused by the current-collapse and increases the motor losses. The increase in motor losses is caused mainly by the additional iron losses since the voltage distortion introduces the current distortion, leading to distorted flux density distribution in the machine core [25]. Therefore, the aim is to find an optimum minimum pulse length that mitigates the negative influence of current-collapse and, at the same time, does not significantly increase the machine losses. The situation is depicted in Figure 6.

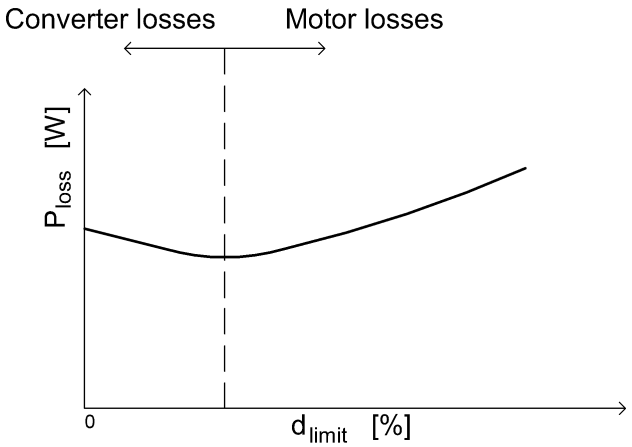

Figure 6. Electric drive loss (P_{loss}) distribution based on the limiting duty cycle d_{limit}.

2.3. PMSM Control Strategy

The block diagram of the PMSM control scheme used within the experimental part is depicted in Figure 7. The scheme is based on the traditional FOC, where the machine torque is controlled by the q-axis and the machine flux by the d-axis current component. The transformation angle between the stationary $\alpha\beta$ and the synchronous dq system attached to the rotor permanent magnet is measured using an incremental encoder. Also, strictly for measuring purposes, a speed controller superior to the q-axis current controller is

implemented. The speed controller is also used to calculate the *d*-axis current reference in the field-weakening region according to the strategy presented in [26]. In the base-speed region, the *d*-axis current reference is set to zero which is not explicitly shown in Figure 7 (the machine is a surface-mounted magnet type).

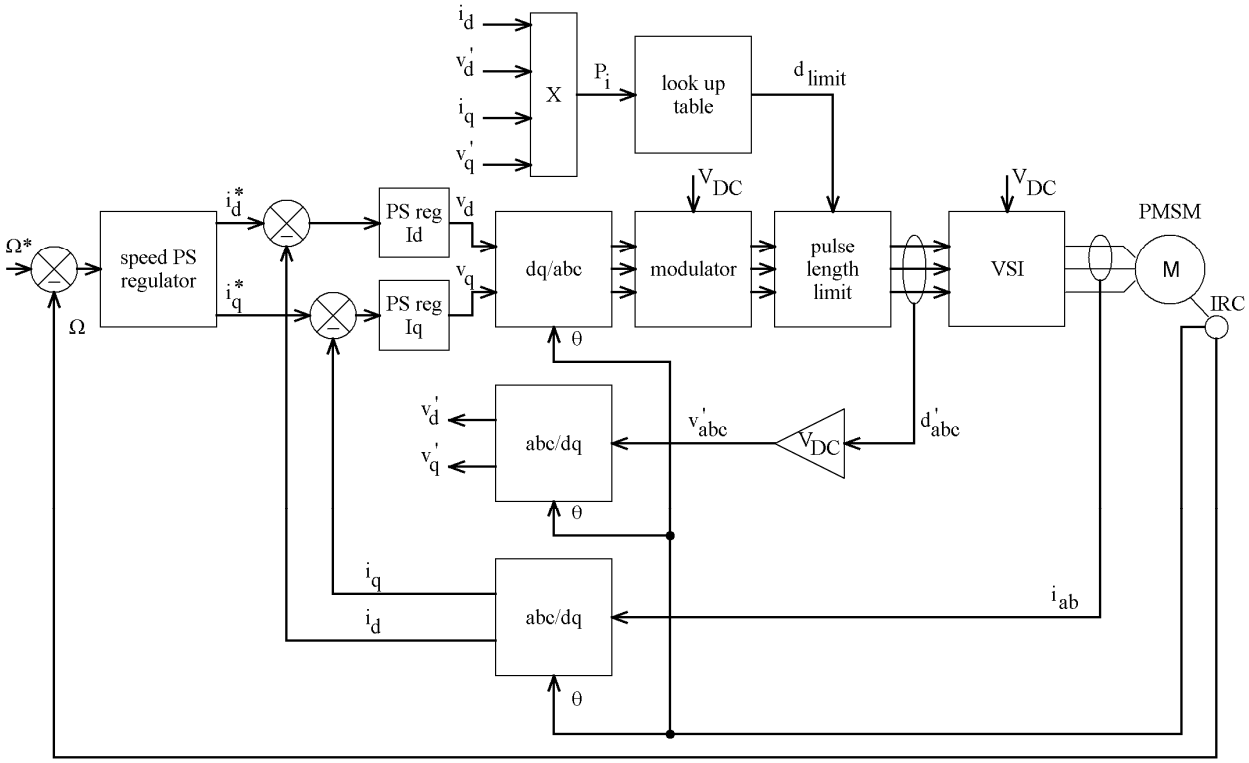

Figure 7. PMSM control scheme with added LUT-based pulse length limitation block. The values modified by the pulse-limiting algorithm are primed.

The reference voltage vector demanded by the current controllers is transformed into the three-phase system and fed to the modulator. The modulator output then enters the pulse-limiting block. The limiting value is derived from a LUT based on motor active power, calculated as

$$P = \frac{3}{2}\left(i_d \cdot v_d + i_q \cdot v_q\right), \tag{8}$$

where i_d and i_q are the *d*- and *q*-axis stator current vector components, respectively, and u_d and u_q are the *d*- and *q*-axis stator voltage vector components, respectively. The LUT is experimentally measured with respect to the machine input power, since increased mechanical power on the shaft means increased motor speed and, therefore, higher supply voltage (i.e., higher modulation index) with shorter gate pulses. Thus, in Figure 7, the voltage components reconstructed from the adjusted duty cycles are used for the motor input power calculation since, due to the voltage distortion introduced by the proposed method, the outputs from the current controllers differ from the actual voltage applied to the motor terminals.

3. Experimental Results

A picture of the experimental setup is shown in Figure 8. The workplace consists of a custom GaN VSI, two identical mechanically coupled PMSMs, a regulated DC supply, and a resistive bank used for the PMSM generator loading.

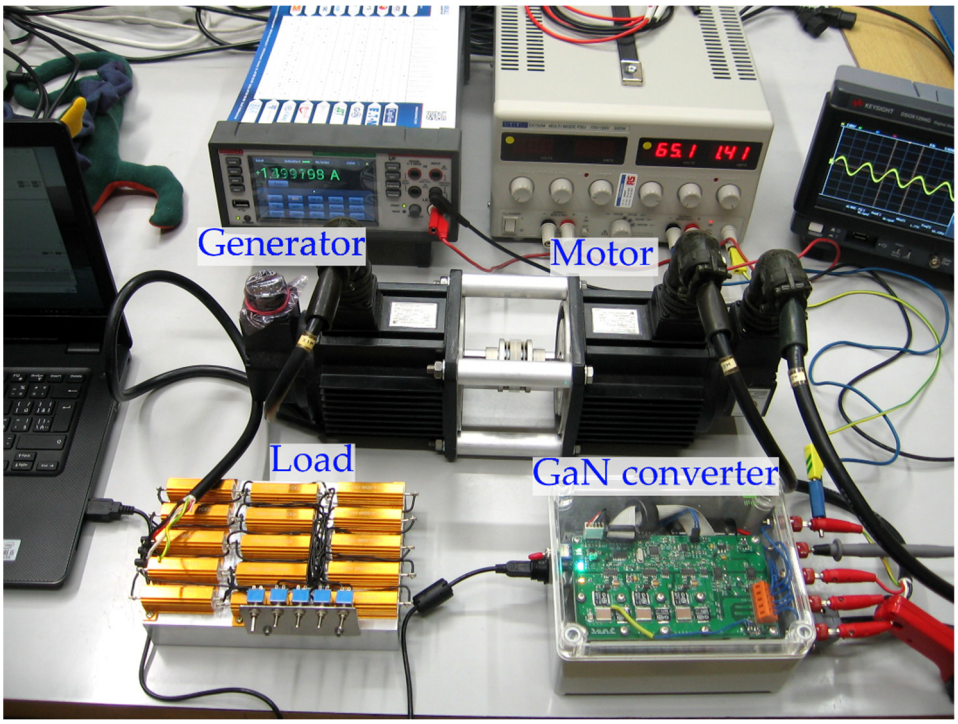

Figure 8. Experimental workplace.

3.1. Experimental Setup

Figure 9 shows a simplified block diagram of the experimental setup. The VSI is based on six GS66516B GaN transistors with Si8275 isolated half-bridge drivers. Machine phase current is measured by two TMCS1100 isolated hall-effect current transducers designed to operate with low DC offset with an internal compensation circuit. The utilized controller is ARM Cortex M4 MCU STM32F334 is equipped with an HRTIM peripheral—a 16-bit timer with up to 217 ps resolution available for the duty cycle adjustment. The VSI operates at a switching frequency of 100 kHz. Data are sampled, and the control algorithm is calculated at 25 kHz.

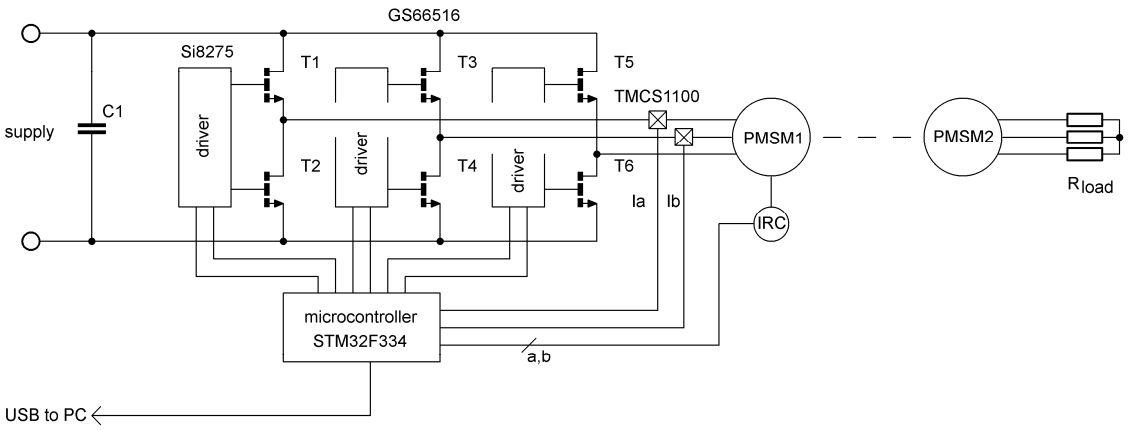

Figure 9. Simplified schematic diagram of the experimental setup.

A 500 W four-pole PMSM with an incremental encoder for the rotor position measurement is connected directly to the VSI. The motor is coupled to a second identical machine loaded by variable resistors, which serves as a load. The motor and generator nameplate data and model parameters are listed in Table 1.

Table 1. Motor and generator/brake parameters.

Motor/Generator	
Type	USAREM-05CFJ11
RPM	3000
Power [W]	500
Max voltage [V]	200
Max current [A]	3.6
Stator resistance [Ω]	1.63
d-axis inductance [mH]	10.3
q-axis inductance [mH]	10.9

3.2. Pulse Length Limiting

Figure 10 shows the waveforms of the reference duty cycles and resulting machine phase currents for multiple values of pulse limitation. The nominal duty cycle of 100% is considered a theoretical maximum in a linear modulation region. The pulse limitation process leads to the distortion of the reference duty cycle, which then contributes to the voltage vector trajectory distortion, as shown earlier in Figure 5. For high values of pulse limitation, the duty cycle practically approaches a trapezoidal waveform. However, since the switching frequency is very high, the voltage distortion only slightly contributes to the current distortion.

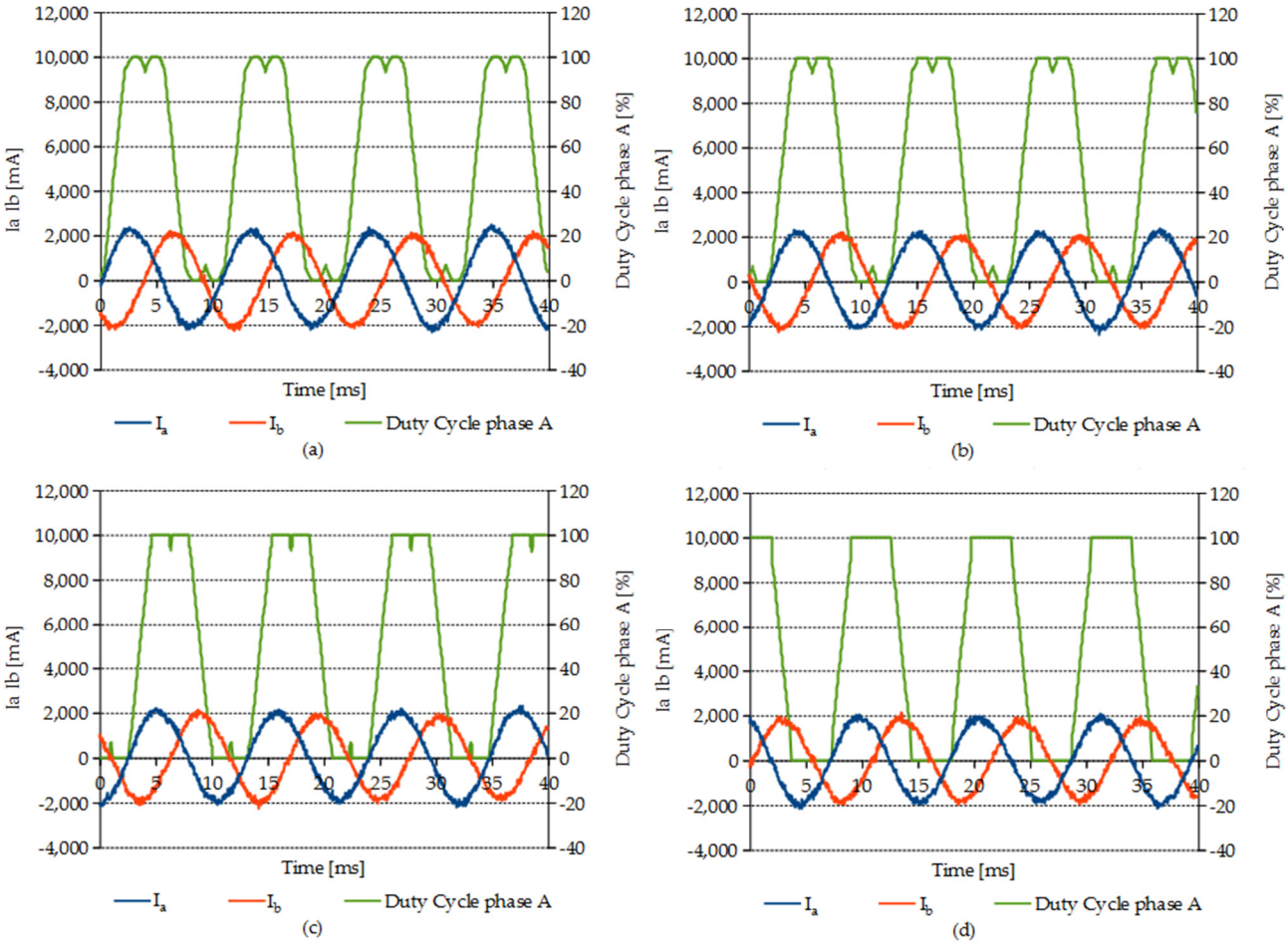

Figure 10. Modulation with: (**a**) no pulse length limited, (**b**) with limiting value 5%, (**c**) with limiting value 10%, and (**d**) with limiting value 20% of the nominal duty cycle. Measured during 2000 RPM speed, 100 V DC-link voltage, and load resistance $R_{\text{load}} = 100\,\Omega$; I_{a} and I_{b} denote the current in phases "a" and "b", respectively.

3.3. Current-Collapse Losses Minimization

Because the DC-link voltage is kept at a constant value of 100 V by the regulated DC supply, the current drawn from the DC source directly contributes to the power consumption. Therefore, the DC-link input current was measured for multiple drive-operating points and pulse-limiting values to assess the energy saved by the proposed method. Since both the PMSMs (motor and generator) are manufactured as servo drives, 100 V supply voltage was chosen with respect to the mechanical limits of the system so the PMSM drive could work in the base-speed region as well in the field-weakening region within its nominal RPM.

The recorded data are depicted in Figure 11. Figure 11a,b shows measurements for a motoring operation in the base-speed region. Figure 11c then corresponds to the field-weakening region. As expected, the DC-link current increases with the motor speed and lower load resistance.

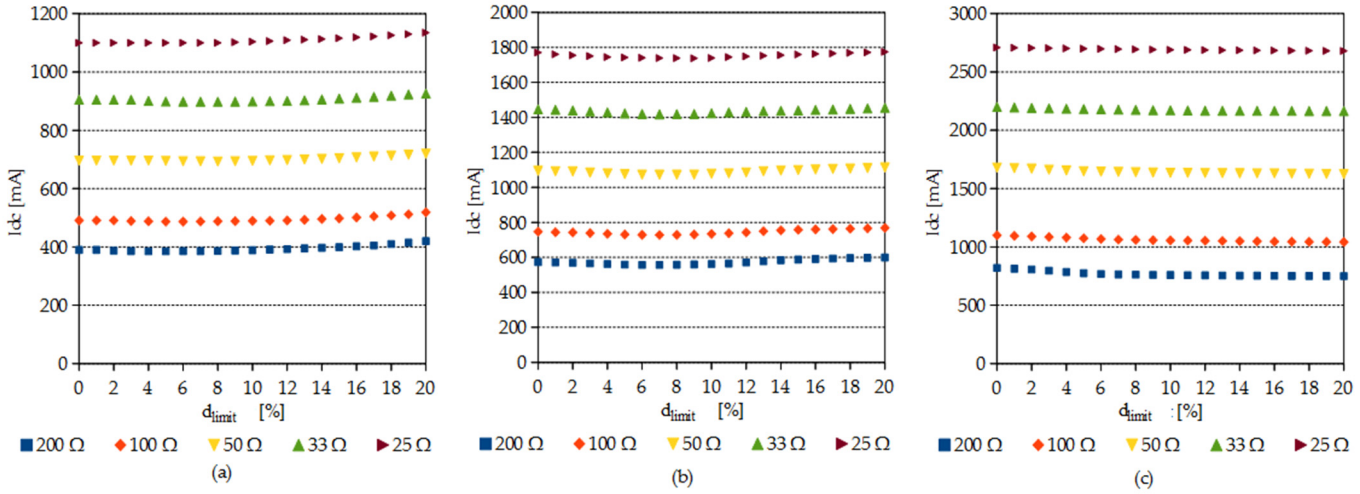

Figure 11. Input DC-link current measured at different load at (**a**) 1500 RPM, (**b**) 2000 RPM, and (**c**) 2500 RPM; I_{dc} denotes the input DC-link current.

To give a better insight into the shape of the measured waveforms and the minima's position, Figure 12 is converted into a per-unit system. The base value is different for each reference speed and corresponds to the DC-link current drawn without pulse limitation. The results are then shown in Figure 12.

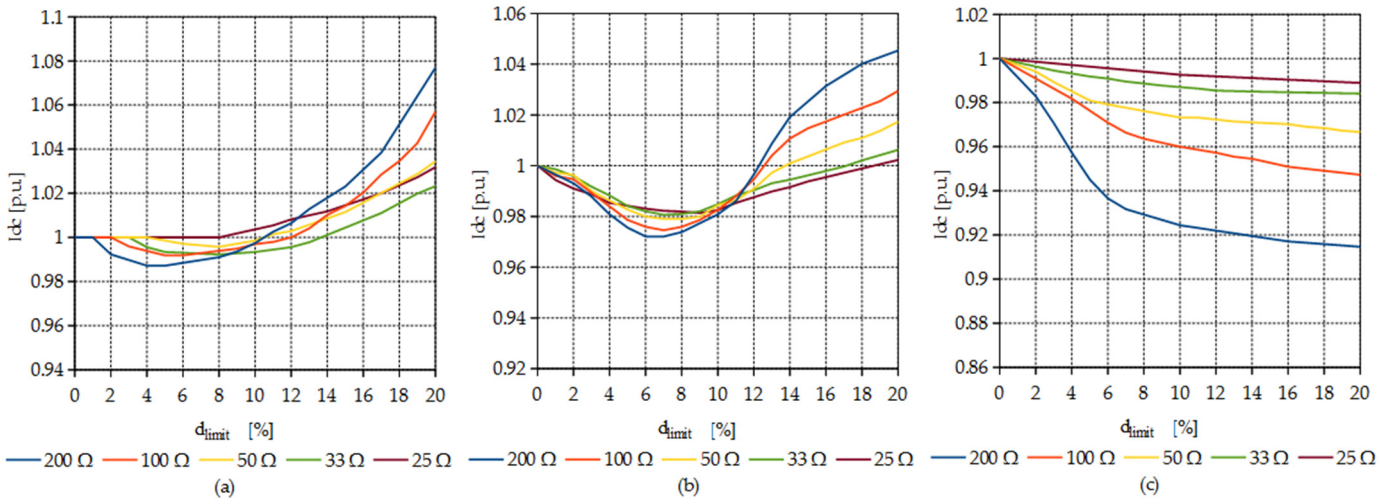

Figure 12. Relative input DC-link current measured at different load at (**a**) 1500 RPM, (**b**) 2000 RPM, and (**c**) 2500 RPM; I_{dc} denotes the input DC-link current.

In Figure 12a, the motor load is low, resulting in a significant increase in the drive losses when the pulse length limit greater than 10% is applied. Because the output power is also low, the decrease in converter losses is lower than the increase in motor losses due to the current distortion. Figure 12b shows that a more pronounced local minimum exists in the DC-link current for a specific pulse-length limit at higher speeds, since the voltage margin of the inverter decreases (more voltage is needed to counter the back-electromotive force) and, therefore, the reference voltage vector moves closer to the hexagon boundary.

In Figure 12c, the machine is operated in a field-weakening region. In this case, the local minima do not exist in the DC-link current waveforms. The cause of this behavior is that the modulation index, which is increased due to the pulse-length limiting, lowers the d-axis current, which results in a decrease in motor phase RMS current value. The reduction of stator ohmic losses in the field-weakening region is more significant than the core losses; therefore, the curves have a continuously decreasing tendency.

Overall, it can be stated that the proposed method is most effective when the reference speed approaches the boundary between the base-speed and field-weakening region and the load is low. The relative decrease in the consumed power is 2 to 3% in such a case. For lower speed, the maximum power savings are around 1% in the case of a low-load operation and are almost negligible for a high-load operation. Finally, it can be stated that the method lacks effectivity in the field-weakening region since, here, the local minima practically do not exist. The curves have a continuously descending tendency, but the decrease in current consumption, as explained above, is not caused by the mitigation of the current-collapse phenomenon.

As a final stage of the experiments, a LUT was determined for a variable inverter output power. During this measurement, the motor was running at 2000 RPM, and the load was varied in steps from 10% to 100% of the nominal torque. Again, the GaN VSI was supplied by 100 V DC. The results are depicted in Figure 13. It has been found that the discrete measured values can be relatively accurately fitted to a polynomial function in the form

$$y = ax^3 - b\,x^2 + cx, \tag{9}$$

where a, b, and c are parameters to be determined. The fitting process was done using Wolfram Mathematica, and the found values are $a = 8.102$, $b = 24.74$, and $c = 28.79$. Therefore, since the calculation of (9) is not too computationally demanding for the real-time control, the analytical expression has been used in the control algorithm for the current-collapse loss mitigation instead of the LUT that is indicated in Figure 7. The resulting compensation function is given by the formula

$$d_{\text{limit}} = 28.79\,P - 24.74\,P^2 + 8.102\,P^3 \tag{10}$$

where P is the per-unit inverter output power calculated from (5) with the base value equal to the motor input power when the speed is set to 2000 RPM, and the machine is loaded by its nominal torque. The new value of d_{limit} is updated every 100 ms since the calculated power needs to be averaged. Furthermore, it has been experimentally found that a lower update period could affect the stability of the current control loops.

A direct comparison of the measured input DC-link current for operating points corresponding to minima in Figure 12 for 1500 RPM and 2000 RPM is presented in Table 2.

The data compares the DC-link current consumption for the case of non-limited and limited duty-cycle. The drive losses are decreased on average by 2% at 2000 RPM, which can be seen as a "nominal speed" for the utilized DC-link voltage value. At 1500 RPM, the loss decrease is not significant because the converter operates with a reference voltage vector that is relatively far from the voltage hexagon boundary.

To visualize the proposed method's merits directly, infrared (IR) camera pictures of the inverter were taken. The reference machine speed was set to 2000 RPM, and the load resistance for the PMSM generator was selected as 25 Ω. As a prerequisite for the measurement, the drive was running for some time with the compensation function (Equation (10))

enabled until the temperature stabilized. Then, the compensation function was disabled, and once the temperature stabilized again, Figure 14a was taken.

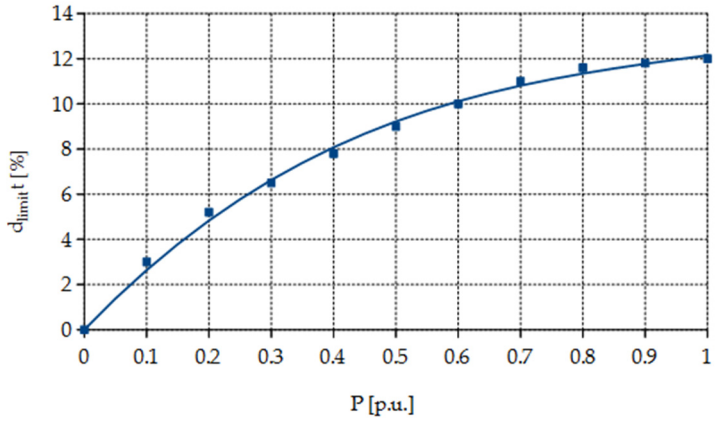

Figure 13. Third-order polynomial function fitted to the measured data (limiting duty-cycle d_{limit} as a function of the inverter output power P in per-units).

Table 2. DC-link current measurement.

Speed	Load	DC-Link Current [A]		Loss Decreased
RPM	**Ω**	**Limit = 0**	**Look Up Table**	**%**
1500	200	0.4020	0.3990	0.75
	100	0.5051	0.5030	0.42
	50	0.7162	0.7120	0.59
	33	0.9225	0.9170	0.60
2000	200	0.5730	0.5570	2.87
	100	0.7470	0.7280	2.61
	50	1.095	1.072	2.15
	33	1.446	1.418	1.97
	25	1.771	1.738	1.90

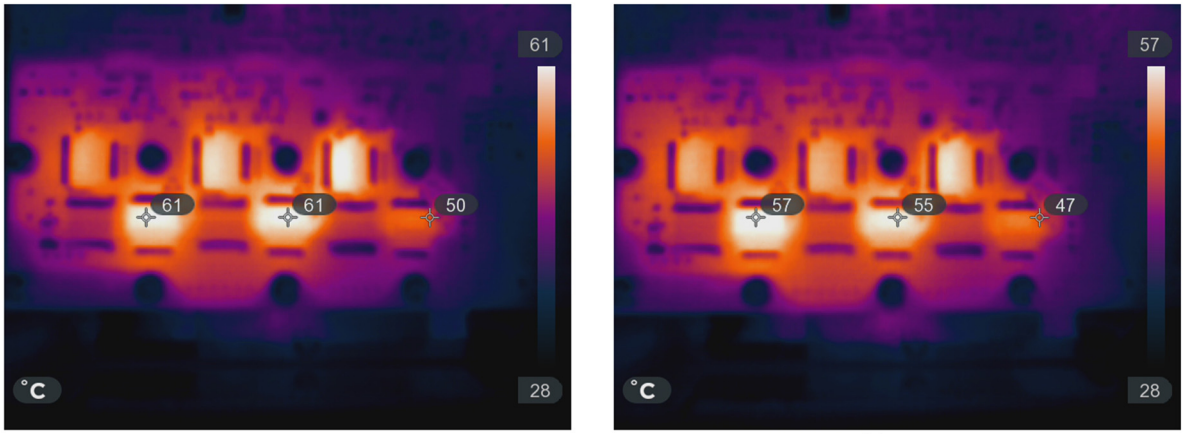

Figure 14. Infrared camera measurement at 2000 RPM and $R_{\text{load}} = 25\ \Omega$ (**a**) without pulse length limitation and (**b**) with pulse length limitation.

After that, the compensation function was enabled again, and after reaching a thermal steady-state, Figure 14b was taken. It can be seen that the steady-state temperature of the hottest point on the inverter dropped by 6 °C when the proposed method of the current-collapse loss minimization was applied. Figure 15 then shows the converter board in detail.

The GaN transistors are cooled using vias through the board with the heatsink mounted on the bottom side.

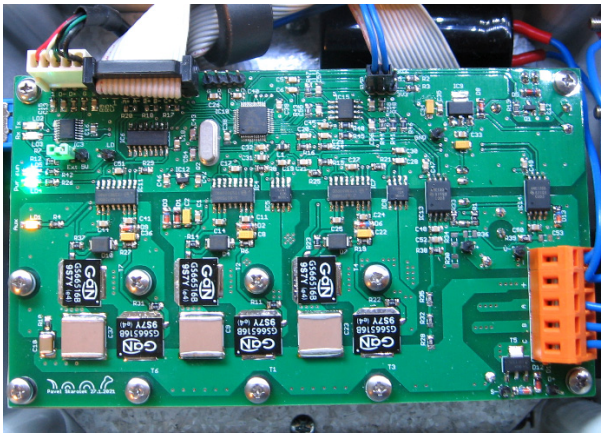

Figure 15. Detail of the inverter board.

4. Discussion

In this paper, GaN-based converter losses caused by the current-collapse phenomenon and their mitigation, respectively, were investigated. It was explained that the additional losses are caused by increased dynamic on-state resistance, which depends on the pulse length in the utilized modulation strategy. Following this, the SVPWM of a three-phase VSI driving a PMSM in a basic FOC loop was adjusted by limiting the minimum pulse for the GaN gate drivers. It was found that the modulated voltage distorted by the pulse length limiting lowers the current-collapse losses and, at the same time, causes additional machine losses because current distortion is introduced. Since both the converter and motor losses depend on the duty cycle limit value, optimal minimum pulse length corresponding to minimum consumed power for a given steady-state operating point can be determined. Moreover, it was experimentally observed that the optimum limiting duty cycle value depends on the converter input power. Therefore, a compensation function was implemented within the motor control algorithm to set the duty cycle limit with respect to the actual VSI input power calculated from the motor currents and voltages.

The amount of saved power was indirectly assessed by measuring the DC-link input current to the VSI driving a PMSM at a given speed into a variable load. The consumed DC-link current of a "clean" SVPWM (i.e., duty cycle limit set to zero) was compared to the input current corresponding to multiple duty cycle limiting values. The loss decrease thanks to the pulse length limiting was found to be dependent on the motor operating point. At low speed, the loss decrease is small due to relatively low reference voltage vector magnitude, which causes the pulse length limiting technique to be inefficient. When the motor operates in the field-weakening region at high speeds by setting a negative d-axis current, there is no local minimum corresponding to the optimal limiting duty cycle. Therefore, the method is not effective during field weakening.

A significant loss decrease was observed around a "nominal speed" for a given DC-link voltage where the reference voltage vector within the SVPWM approaches the voltage hexagon boundaries. Since this operating point is typical for PMSM deployed in non-traction applications such as pumps or servo drives, the authors believe that the proposed method could significantly decrease the power consumption for specific drives used in industry or household applications. Furthermore, another advantage of the presented method is that it is purely software-based and can be easily implemented into the control algorithm using a simple LUT or computationally undemanding analytical function.

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