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Analysis of Series-Parallel (SP) Compensation Topologies for Constant Voltage/Constant Current Output in Capacitive Power Transfer System

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Abstract: This paper analyzed the four series-parallel (SP) compensation topologies to achieve constant current (CC) and voltage (CV) output characteristics and zero phase angle (ZPA) input conditions with fewer compensation components in the capacitive power transfer (CPT) system. There are three main contributions. Firstly, the universal methodology of SP compensation topologies was constructed to achieve CC, CV output, and ZPA conditions. Secondly, four specific SP compensation topologies were investigated and summarized, including double-sided LC, double-sided CL, CL−LC, and LC−CL topologies. Their input–output characteristics are provided, and system efficiency is analyzed. Thirdly, the CL−LC and LC−CL topologies were proposed to realize ZPA conditions under CC and CV output without any external regulating circuit. A CV output LC−CL experiment prototype was implemented to validate the theoretical analysis.

Keywords: capacitive power transfer (CPT); compensation topology; zero phase angle; constant voltage/current output

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1. Introduction

Wireless power transfer (WPT) technology utilizing different energy carriers to transfer electric power without physical contact has been a research hotspot recently due to its advantages of flexibility and safety [1–4]. Inductive power transfer (IPT) and capacitive power transfer (CPT) technologies are two main effective methods among WPT systems to deliver power wirelessly [5]. IPT system using high−frequency magnetic fields to transfer power has been employed in miscellaneous applications, such as biomedical implants [6,7], wireless charging for consumer electronics (CE) [8], electric vehicles (EVs) [9–12], and unmanned aerial vehicles (UAVs) [13,14]. As a result of the high−frequency magnetic fields generated around the coupler structure in the IPT system, undesirable eddy current loss would be induced in the metallic conductors shown around the IPT system [15]. In addition, the IPT system usually adopts a coupler structure consisting of the expensive Litz wire and ferrite core, increasing the system's costs and weight [16,17]. Unlike IPT technology, a CPT system using electrical fields as an energy carrier has the advantages of low eddy current loss, lightweight, and good tolerance to metal disturbance [18]. Therefore, the CPT system is more suitable for metal environmental and lightweight applications.

A CPT system usually consists of a power electronic converter, coupler structure, and compensation topologies [19]. The converter (high-frequency inverter and rectifier) supplies the AC signal to compensation topologies. It converts the alternating current to DC load. The coupler structure realizes the wireless power transfer by generating high-frequency electric fields between the transmitting and receiving plates. A capacitive coupler structure would induce significant reactive power in the CPT system, degrading the power transfer capability [20–22]. Therefore, the compensation topologies play an essential role in eliminating the reactive power induced by the capacitive coupler [23–26]. For most charging

applications, the output characteristics of constant current (CC) and constant voltage (CV) are significant targets to extend battery life and ensure stable charging, which can also be achieved by appropriate selections of compensation topologies [27]. Furthermore, the parameters design of the compensation circuit can not only adjust the output voltage and current gain but also optimize the system efficiency [28].

Currently, the research on compensation topologies in the CPT system can be divided into basic compensated circuits and high-order compensated circuits [29–40]. The basic compensated circuits are composed of series (S) compensation, parallel (P) compensation, and series-parallel (SP) compensation, as shown in Figure 1. As the coupled capacitances of the coupler structure in the CPT system are usually the pF-level, the compensation inductors in the series compensated circuit would be large and heavy [29]. In addition, the structure of the parallel compensated circuit limited the port voltage on coupler plates, which imposed restrictions on transfer power [30]. Hence, the SP compensation and high-order compensation topologies are preferred by researchers [33–39]. Lu et al. proposed double-sided LCLC [29], double-sided CLLC [34], and double-sided LCL compensation topologies [30] to reduce the resonant inductance and increase the port voltage on the plates. At the same time, the plenty of external compensation components increased the system's complexity. They made the CPT system lose its advantages of lightness. Then, as one of the SP compensation topologies, the double-sided LC compensation circuit was proposed to achieve CC and CV output with only four external compensation components (half the number of double-sided LCCL topologies). However, when the parameters of double-sided LC are designed to achieve CV output, the zero phase angle (ZPA) condition between the input driving current and driving voltage cannot be realized, which would degrade the power transfer capability.

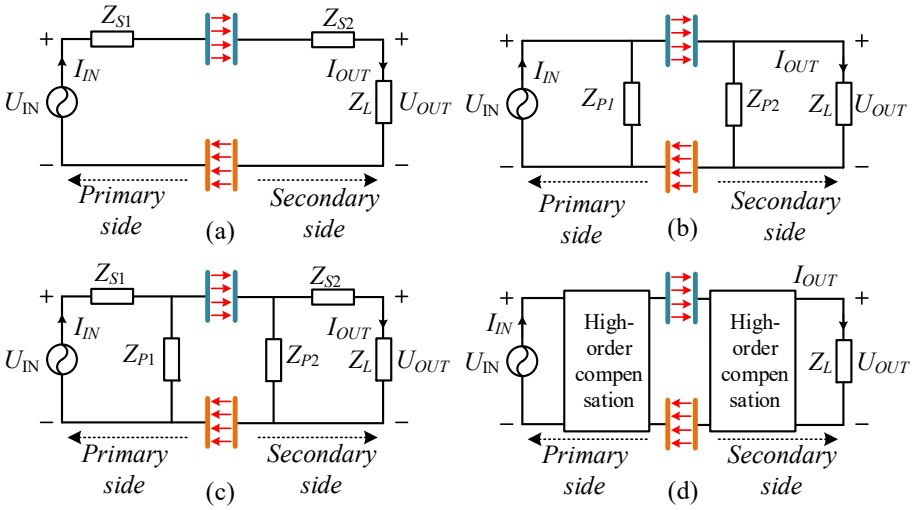


Figure 1. Compensation topologies in the CPT system. (**a**) Series compensation. (**b**) Parallel compensation. (**c**) Series-Parallel compensation. (**d**) High-order compensation.

This paper analyzed the four SP compensation topologies to achieve CC and CV output characteristics and ZPA input conditions with fewer compensation components in the CPT system. There are three main contributions. Firstly, the universal methodology of SP compensation topologies was constructed to achieve CC, CV output, and ZPA conditions. Secondly, four specific SP compensation topologies were investigated and summarized, including double-sided LC, double-sided CL, CL−LC, and LC−CL topologies. Their input–output characteristics are provided, and system efficiency is analyzed. Thirdly, the CL−LC and LC−CL topologies were proposed to realize ZPA conditions under CC and CV output without any external regulating circuit. A CV output LC−CL experiment prototype was implemented to validate the theoretical analysis.

2. Modeling of SP—Based CPT Topology

2.1. The Capacitive Coupler Structure

The most widely used coupler structure in the CPT system is shown in Figure 2, which is formed by two pairs of metal plates (P1, P2, P3, P4) stacked by each other with no contact. The distance d between P1 and P3 or P2 and P4 is the so−called transmission distance. Coupling capacitors Cij (i, j = 1, 2, 3, 4) are formed between plates Pi and Pj (i, j = 1, 2, 3, 4), which can be calculated as expressed in Equation (1):

$$C = \frac{\varepsilon_r S}{4\pi k d} \tag{1}$$

where ε_r represents the relative dielectric constant, S is the coupling area of coupler plates, and k represents the electrostatic constant. Therefore, Figure 3a shows the full-capacitor model of the four-plate capacitive structure and the equivalent induced current source model is shown in Figure 3b. The relationships of port voltage V_1, V_2, and current I_1, I_2 are expressed as follows.

$$\begin{cases} I_1 = j\omega C_1 V_1 - j\omega C_M V_2 \\ I_2 = j\omega C_2 V_2 - j\omega C_M V_1 \end{cases} \tag{2}$$

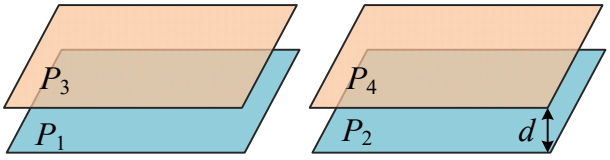


Figure 2. Classic four-plate capacitive coupler structure.

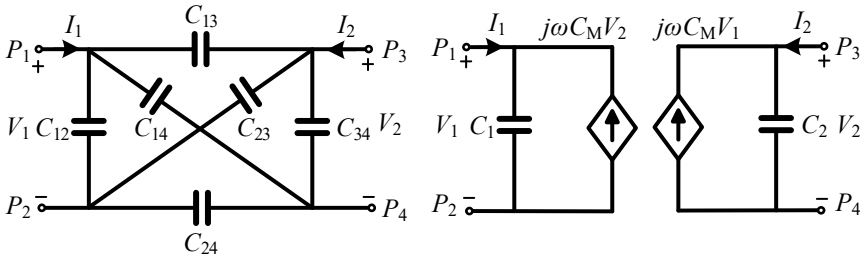


Figure 3. The modeling of capacitive coupler structure. (**a**) Full-capacitor model. (**b**) Induced current source model.

According to Equation (2), the simplified π-type and T-type models of the four-plate structure are presented in Figure 4, where the capacitance value satisfied the expressions shown in Equations (3) and (4):

$$\begin{cases} C_M = \frac{C_{13}C_{24} - C_{14}C_{23}}{C_{13}+C_{23}+C_{14}+C_{24}} \\ C_1 = C_{12} + \frac{(C_{13}+C_{14})(C_{23}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}} \\ C_2 = C_{34} + \frac{(C_{13}+C_{23})(C_{14}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}} \end{cases} \tag{3}$$

$$\begin{cases} C_a = \frac{C_{e1}C_{e2}+C_{e1}C_M+C_{e2}C_M}{C_{e2}} \\ C_b = \frac{C_{e1}C_{e2}+C_{e1}C_M+C_{e2}C_M}{C_{e1}} \\ C_c = \frac{C_{e1}C_{e2}+C_{e1}C_M+C_{e2}C_M}{C_M} \end{cases} . \tag{4}$$

where $C_{e1} = C_1 - C_M$, $C_{e2} = C_2 - C_M$. This paper only introduced the classical four-plate capacitive structure due to space constraints. Other structures are not included, such as six−plates, matrixed plates, etc.

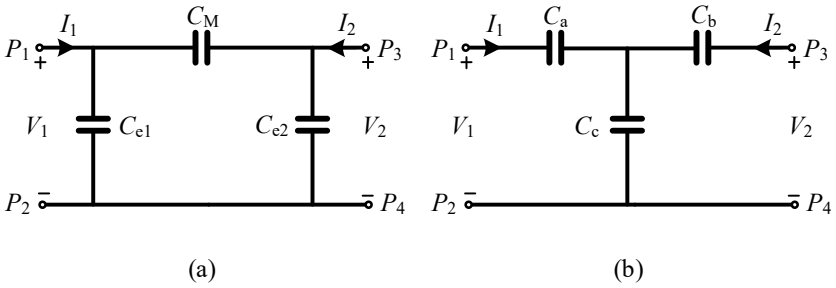


Figure 4. Simplified coupler structure. (**a**) π-type model. (**b**) T-type model.

2.2. The SP Compensation Topologies

The SP compensation topology in the CPT system is shown in Figure 5, where U_{IN} represents the output AC voltage of the high-frequency inverter, and Z_L is the input impedance of the rectifier. It should be mentioned that Z_L is resistive when the parasitic impedances of the rectifier are neglected, and the load can be considered as resistance. Z_{S1} and Z_{S2} represent the series compensation elements of the primary and secondary sides, respectively. The paralleled compensation elements of the primary and secondary sides are named Z_{P1} and Z_{P2}.

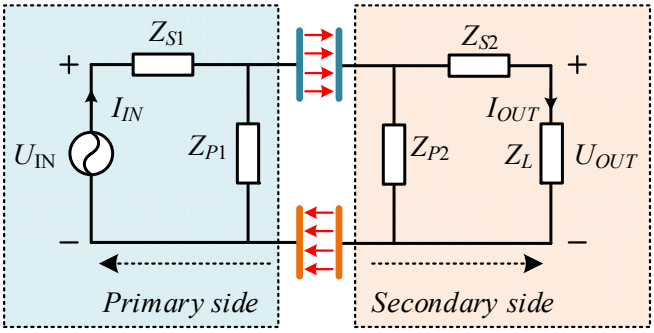


Figure 5. The SP compensation topology in the CPT system.

When U_{IN} is designed to be constant, the input source is considered a constant voltage source. The equivalent circuit is shown in Figure 6 by substituting the π-type model of the coupler structure into the SP compensation topology CPT system. Z'_{P1} and Z'_{P2} are composed of the self−capacitance $(C_1 - C_M)$ and Z_{P1} as well as $(C_2 - C_M)$ and Z_{P2}, respectively, which satisfy the expressions as follows.

$$\begin{cases} Z'_{P1} = \frac{Z_{P1}}{Z_{P1} j\omega (C_1 - C_M) + 1} \\ Z'_{P2} = \frac{Z_{P2}}{Z_{P2} j\omega (C_2 - C_M) + 1} \end{cases} \tag{5}$$

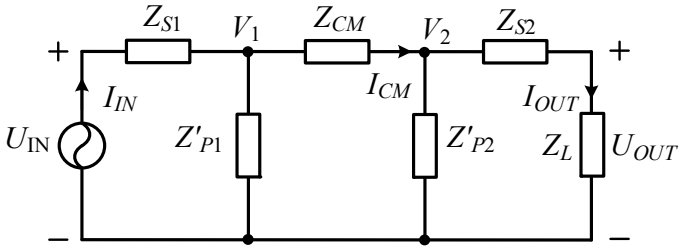


Figure 6. The SP compensation topology with the π-type model of coupler structure.

According to Kirchhoff's law, the SP circuit can be expressed as

$$\begin{bmatrix} U_{IN} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & 0 \\ Z_{21} & Z_{22} & Z_{23} \\ 0 & Z_{32} & Z_{33} \end{bmatrix} \cdot \begin{bmatrix} I_{IN} \\ I_{CM} \\ I_{OUT} \end{bmatrix} \tag{6}$$

where $Z_{11} = Z_{S1} + Z'_{P1}$, $Z_{12} = -Z'_{P1}$, $Z_{21} = -Z'_{P1}$, $Z_{22} = Z'_{P1} + Z'_{P2} + Z_{CM}$, $Z_{23} = -Z'_{P2}$, $Z_{32} = -Z'_{P2}$, $Z_{33} = Z'_{P2} + Z_{S2} + Z_L$. The output voltage U_{OUT} and output current I_{OUT} can be calculated according to Equation (6), which can be written as

$$\begin{cases} U_{OUT} = -\frac{U_{IN} Z_{12} Z_{23} Z_L}{(Z'_{P2}+Z_{S2}+Z_L)(Z_{12}^2 - Z_{11}Z_{22}) + Z_{11}Z_{23}^2} \\ I_{OUT} = -\frac{U_{IN} Z_{12} Z_{23}}{(Z'_{P2}+Z_{S2}+Z_L)(Z_{12}^2 - Z_{11}Z_{22}) + Z_{11}Z_{23}^2} \end{cases} \tag{7}$$

To achieve CC output characteristics, the following conditions need to be satisfied.

$$\begin{gathered} Z_{12}^2 - Z_{11}Z_{22} = 0 \\ \Rightarrow Z'_{P1} + Z_{S1} // (Z_{CM} + Z'_{P2}) = 0 \end{gathered} \tag{8}$$

Then, the input impedance Z_{IN} and the output current I_{OUT} can be derived as

$$\begin{cases} Z_{IN} = \frac{Z_{11} Z_{23}^2}{Z_{23}^2 - Z_{22} Z_{33}} \\ I_{OUT} = \frac{U_{IN} Z_{12}}{Z_{11} Z_{23}} \end{cases} \tag{9}$$

The condition to achieve CV output characteristics is expressed as follows

$$(Z'_{P2} + Z_{S2})(Z_{12}^2 - Z_{11}Z_{22}) + Z_{11}Z_{23}^2 = 0 \tag{10}$$

The following condition Equation (11) can be obtained to achieve CV output by simplifying Equation (10).

$$\begin{cases} Z_{S1} + Z'_{P1} = 0 \\ Z_{S2} + Z'_{P2} = 0 \end{cases} \tag{11}$$

The input impedance Z_{IN} and the output voltage U_{OUT} can also be calculated as

$$\begin{cases} Z_{IN} = Z_{11} + \frac{Z_{33} Z_{12}^2}{Z_{23}^2 - Z_{22} Z_{33}} \\ U_{OUT} = \frac{U_{IN} Z_{12} Z_{23}}{Z_{12}^2 - Z_{11} Z_{22}} \end{cases} \tag{12}$$

When the inverter's output current is constant, the CC or CV output condition can also be derived according to the above theory. The compensation parameters to achieve CC output should satisfy the following equation:

$$Z_{22} = 0 \Rightarrow Z'_{P1} + Z_{CM} + Z'_{P2} = 0 \tag{13}$$

The current gain can be calculated as

$$G_I = \left| \frac{I_{OUT}}{I_{IN}} \right| = \left| \frac{Z'_{P1}}{Z'_{P2}} \right| = \left| \frac{Z_{12}}{Z_{23}} \right| \tag{14}$$

Then, the input impedance Z_{IN} can be derived as

$$Z_{IN} = Z_{11} + G_I^2 Z_{33} \tag{15}$$

The condition to achieve CV output characteristics with a constant current input source can be deduced based on the reciprocity of CC output with a constant voltage input source, which is presented as follows.

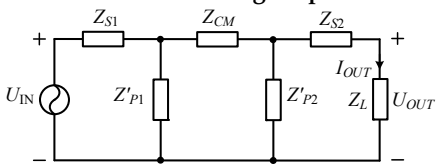
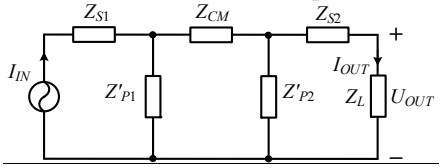
$$\begin{array}{c} Z_{23}^2 - (Z_{33} - Z_L)Z_{22} = 0 \\ \Rightarrow Z'_{P2} + Z_{S2}//(Z_{CM} + Z'_{P1}) = 0 \end{array} \tag{16}$$

Similarly, the output voltage U_{OUT} and the input impedance Z_{IN} can be derived as

$$\begin{cases} U_{OUT} = \frac{Z'_{P1}(Z_{S2}+Z'_{P2})}{Z'_{P2}} I_{IN} \\ Z_{IN} = -\frac{Z'^2_{P1}(Z_{S2}+Z'_{P2})}{Z_L Z_{22}} + Z_{S1} + \frac{Z'_{P1}(Z_{CM}+Z'_{P2})}{Z_{22}} \end{cases} \tag{17}$$

To explicitly demonstrate the output characteristics of SP compensation topologies, we have concluded the above theories in Table 1. Table 1 shows the conditions for realizing CC output or CV output of the CPT system based on the SP compensation network when the input source is a constant current source or a constant voltage source, and the expression of system current or voltage gain under corresponding conditions. The following section will analyze the specific SP-based compensation topology. As most application scenarios adopted the voltage−driven inverter, and the circuit characteristics of SP compensation with constant current input are similar to that of constant voltage input, the circuit analysis of the constant current input source is not included in this paper.

Table 1. Comparison of SP-based compensation topologies.

		Constant Voltage Input	**Constant Current Input**
			
CC Output	Condition	$Z_{12}^2 - Z_{11}Z_{22} = 0$ $\Rightarrow Z'_{P1} + Z_{S1}//(Z_{CM} + Z'_{P2}) = 0$	$Z_{22} = 0$ $\Rightarrow Z'_{P1} + Z_{CM} + Z'_{P2} = 0$
	Output Gain	$I_{OUT} = \frac{U_{IN}Z_{12}}{Z_{11}Z_{23}}$	$G_I = \left\lvert \frac{I_{OUT}}{I_{IN}} \right\rvert = \left\lvert \frac{Z'_{P1}}{Z'_{P2}} \right\rvert = \left\lvert \frac{Z_{12}}{Z_{23}} \right\rvert$
	Input Impedance	$Z_{IN} = \frac{Z_{11}Z_{23}^2}{Z_{23}^2 - Z_{22}Z_{33}}$	$Z_{IN} = Z_{11} + G_I^2 Z_{33}$
CV Output	Condition	$\begin{cases} Z_{S1} + Z'_{P1} = 0 \\ Z_{S2} + Z'_{P2} = 0 \end{cases}$	$Z_{23}^2 - (Z_{33} - Z_L)Z_{22} = 0$ $\Rightarrow Z'_{P2} + Z_{S2}//(Z_{CM} + Z'_{P1}) = 0$
	Output Gain	$U_{OUT} = \frac{U_{IN}Z_{12}Z_{23}}{Z_{12}^2 - Z_{11}Z_{22}}$	$U_{OUT} = \frac{Z'_{P1}(Z_{S2}+Z'_{P2})}{Z'_{P2}} I_{IN}$
	Input Impedance	$Z_{IN} = Z_{11} + \frac{Z_{33}Z_{12}^2}{Z_{23}^2 - Z_{22}Z_{33}}$	$Z_{IN} = -\frac{Z'^2_{P1}(Z_{S2}+Z'_{P2})}{Z_L Z_{22}} + Z_{S1} + \frac{Z'_{P1}(Z_{CM}+Z'_{P2})}{Z_{22}}$

3. Circuit Analysis of Specific SP Topology

3.1. Double-Sided LC Compensation Topology

Figure 7 shows the double-sided LC compensation topology with the π-type model of capacitive coupler structure, where L_{S1} and L_{S2} are the series compensation inductors and C_{P1} and C_{P2} are the paralleled compensation capacitors. Generally, large capacitance C_{P1} and C_{P2} are paralleled on the coupler structure to eliminate the impact of variation of C_{e1} and C_{e2}. To achieve CC output characteristics, the derivation in Equation (8) can be rewritten as

$$\omega^2 L_{S1} = \frac{C'_{P2} + C_M}{C'_{P1}C'_{P2} + C'_{P1}C_M + C'_{P2}C_M} \tag{18}$$

where $C'_{P1} = C_{P1} + C_{e1}$, $C'_{P2} = C_{P2} + C_{e2}$. Then, the output current can be calculated as

$$I_{OUT} = -j\omega \frac{C'_{P1}C'_{P2} + C'_{P1}C_M + C'_{P2}C_M}{C_M} U_{IN} \tag{19}$$

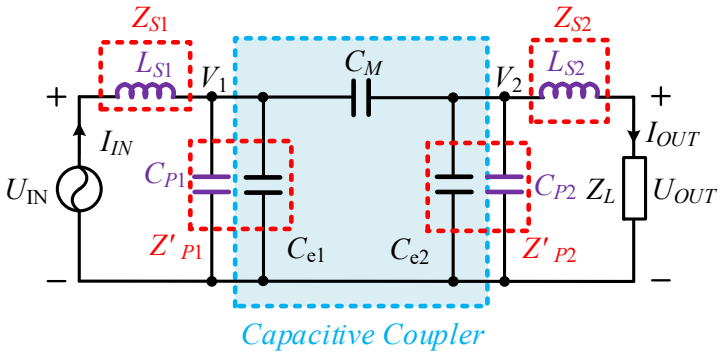


Figure 7. Double-sided LC compensation topology with π-type coupler model.

The input impedance Z_{IN} of double-sided LC compensation with CC output characteristics can be calculated through Equation (9), and the condition to achieve ZPA operation is derived as

$$\omega^2 L_{S2} = \frac{C'_{P1} + C_M}{C'_{P1}C'_{P2} + C'_{P1}C_M + C'_{P2}C_M} \tag{20}$$

Similarly, the condition to achieve CV output characteristics can be derived through Equation (10), which is expressed as

$$\begin{cases} \omega^2 L_{S1} = \frac{1}{C_{P1}+C_{e1}} \\ \omega^2 L_{S2} = \frac{1}{C_{P2}+C_{e2}} \end{cases} \tag{21}$$

The voltage gain of double-sided LC compensation topology is presented as follows.

$$G_V = -\frac{C_{P1} + C_{e1}}{C_{P2} + C_{e2}} \tag{22}$$

The input impedance Z_{IN} of double-sided LC compensation with CV output characteristics can also be calculated as

$$Z_{IN} = \frac{1}{G_V^2/Z_L - j\omega C'_{P1}(C'_{P1}/C_M + C'_{P1}/C'_{P2} + 1)} \tag{23}$$

As the result of $C'_{P1}/C_M + C'_{P1}/C'_{P2} + 1 > 0$, there is always an imaginary part in Z_{IN}, which means the ZPA operation cannot be achieved with CV output characteristics.

3.2. Double-Sided CL Compensation Topology

The double-sided CL compensation topology is presented in Figure 8, where compensation inductors L_{P1} and L_{P2} are paralleled on the coupler structure, and compensation capacitors C_{S1} and C_{S2} are series with the coupler structure. Z'_{P1} and Z'_{P2} are composed of L_{P1} and C_{e1}, L_{P2} and C_{e2} in parallel, respectively. Z_{S1} and Z_{S2} represent the capacitive reactance of C_{S1} and C_{S2}. To achieve CC output characteristics, the derivation in Equation (8) can be rewritten as

$$\begin{cases} \omega^2 L_{P1} = \frac{C_{e2}}{C_{S1}C_{e2}+C_{e1}C_{e2}+C_{e1}C_M+C_{e2}C_M} \\ \omega^2 L_{P2} = \frac{C_{e1}}{C_{e1}C_{e2}+C_{e1}C_M+C_{e2}C_M} \end{cases} \tag{24}$$

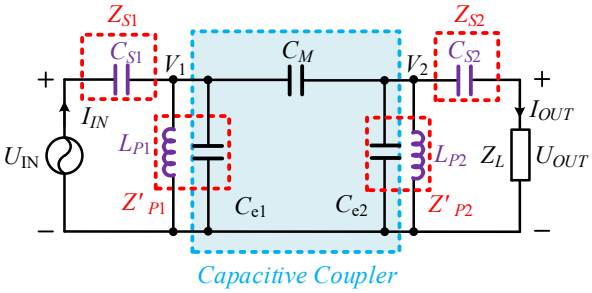


Figure 8. Double-sided CL compensation topology with π-type coupler model.

When the compensation elements satisfy the expression in Equation (24), the output current can be calculated as

$$I_{OUT} = -j\omega \frac{C_{S1}C_{e2}}{C_{e1}} U_{IN} \tag{25}$$

Then the input impedance Z_{IN} can be deduced as

$$Z_{IN} = \frac{1}{j\omega(C_c + C_b - \frac{C_b}{\omega^2 L_{P2} C_{S2}}) + \frac{C_b}{L_{P2}} Z_L} \tag{26}$$

where the expression C_b and C_c is shown in Equation (4). ZPA operation condition of double-sided CL compensation topology can be achieved when the reactive part of Z_{IN} is eliminated. Hence the following equation is derived from Equation (24).

$$C_{S2} = \frac{C_b^2}{C_c + C_b} \tag{27}$$

Same with the previous analysis, to achieve CV output characteristics, the compensation elements should satisfy the condition as

$$\begin{cases} \omega^2 L_{P1} = \frac{C_{e2}}{C_{S1}C_{e2} + C_{e1}C_{e2} + C_{e1}C_M + C_{e2}C_M} \\ \omega^2 L_{P2} = \frac{C_{e1}}{C_{S1}C_{e1} + C_{e1}C_{e2} + C_{e1}C_M + C_{e2}C_M} \end{cases} \tag{28}$$

The voltage gain G_V is given by

$$G_V = \frac{C_{S1}C_{e2}}{C_{S2}C_{e1}} \tag{29}$$

The input impedance Z_{IN} with CV output characteristics is deduced by

$$Z_{IN} = \frac{-1/\omega^2 C_{S1}^2}{1 + (\frac{C_{e2}}{C_{e1}})^2 (1 - \frac{1}{\omega^2 C_{S2}^2 Z_L}) - j\frac{C_c}{\omega C_a^2}} \tag{30}$$

where C_a is expressed in Equation (4), as C_c is not equal to zero, the input impedance consists of the real and imaginary parts. Therefore, the ZPA cannot be realized under the CV mode of double-sided CL compensation topology.

3.3. CL−LC Compensation Topology

The CL−LC compensation topology with π-type coupler model is presented in Figure 9, C_{S1}, and L_{S2} represent the series compensation capacitor on the primary side and the inductor on the secondary side, respectively. L_{P1} and C_{P2} are the compensation inductor and capacitor paralleled in the primary and secondary ports of the coupler structure, respectively. To simplify the analysis, the π-type coupler model is transferred to the T-type circuit, as shown in Figure 10.

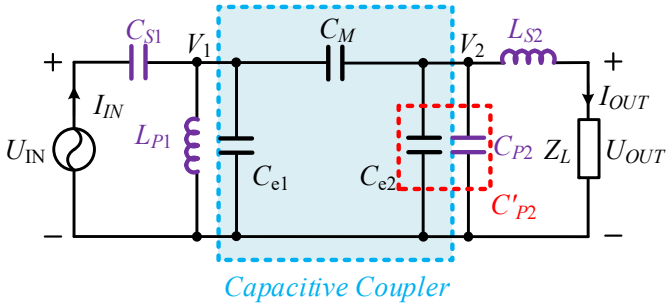


Figure 9. CL−LC compensation topology with π-type coupler model.

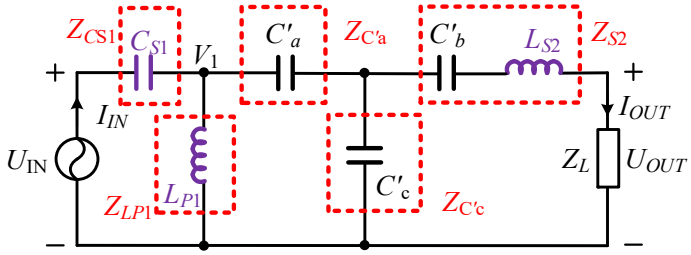


Figure 10. CL−LC compensation topology with T-type coupler model.

As shown in Figure 10, the impedances corresponding with Figure 5 are circled by a red box. Then, the Z_{11}, Z_{12}, Z_{22} of Figure 10 can be rewritten as

$$\begin{cases} Z_{11} = \frac{1}{j\omega C_{S1}} + j\omega L_{P1} \\ Z_{12} = -j\omega L_{P1} \\ Z_{22} = \frac{1}{j\omega C'_a} + \frac{1}{j\omega C'_c} + j\omega L_{P1} \end{cases} \tag{31}$$

The values of C'_a, C'_b, and C'_c are given by

$$\begin{cases} C'_a = \frac{C_{e1}C'_{P2}+C_{e1}C_M+C'_{P2}C_M}{C'_{P2}} \\ C'_b = \frac{C_{e1}C'_{P2}+C_{e1}C_M+C'_{P2}C_M}{C_{e1}} \\ C'_c = \frac{C_{e1}C'_{P2}+C_{e1}C_M+C'_{P2}C_M}{C_M} \end{cases} . \tag{32}$$

where $C'_{P2} = C_{e2} + C_{P2}$. Therefore, the CC mode of CL−LC compensation topology is derived as

$$\omega^2 L_{P1} = \frac{(\frac{1}{C'_a} + \frac{1}{C'_c})\frac{1}{C_{S1}}}{\frac{1}{C'_a} + \frac{1}{C'_c} + \frac{1}{C_{S1}}} \tag{33}$$

The expression of Equation (33) can be simplified as $Z_{LP1} = (Z_{C'a} + Z_{C'c})//Z_{CS1}$, where $Z_{LP1} = j\omega L_{P1}$, $Z_{C'a} = j\omega C'_a$, $Z_{C'c} = j\omega C'_c$, $Z_{CS1} = j\omega C_{S1}$. The output current I_{OUT} under CC output characteristics is given by

$$I_{OUT} = -j\omega(1 + \frac{C'_c}{C'_a})U_{IN} \tag{34}$$

The condition to achieve ZPA of CL−LC topology with CC output can be deduced by

$$\omega^2 L_{P2} = \frac{1}{C'_b} + \frac{1}{C'_c} - \frac{C'_a C'_c}{C'_a + C'_c}(1 + \frac{C'_a C'_c}{(C'_a + C'_c)C_{S1}}) \tag{35}$$

Then the input impedance Z_{IN} is expressed by

$$Z_{IN} = \frac{C'_a C'_c}{Z_L C_{S1}(C'_a + C'_c)} \tag{36}$$

According to Equation (10), the condition to achieve CV output characteristics of CL−LC topology is calculated as

$$\begin{cases} \omega^2 L_{P1} = \frac{1}{C_{S1}} = \frac{1}{C'_a} + \frac{1}{C'_c} \\ \omega^2 L_{S2} = \frac{1}{C'_b} + \frac{1}{C'_c} \end{cases} \tag{37}$$

The voltage gain G_V is given by

$$G_V = \frac{C_{S1}}{C'_c} \tag{38}$$

The input impedance Z_{IN} is given by

$$Z_{IN} = \omega^4 C_c^2 L_{P1}^2 Z_L \tag{39}$$

It can be concluded from Equations (36) and (39) that the ZPA operation condition can be achieved under arbitrary resistance value of Z_L in CC or CV mode of CL−LC compensation topology.

3.4. LC−CL Compensation Topology

The LC−CL compensation topology with the π-type equivalent circuit of the capacitive coupler structure is shown in Figure 11. L_{S1} and C_{S2} represent the series compensation inductor and capacitor, respectively. C_{P1} and L_{P2} represent the paralleled compensation capacitor and inductor, respectively. Similar to the analysis of CL−LC topology, the LC−CL compensation topology with a T-type coupler model is shown in Figure 12, where C'_a, C'_b, and C'_c is given by

$$\begin{cases} C'_a = \frac{C'_{P1}C_{e2} + C'_{P1}C_M + C_{e2}C_M}{C_{e2}} \\ C'_b = \frac{C'_{P1}C_{e2} + C'_{P1}C_M + C_{e2}C_M}{C'_{P1}} \\ C'_c = \frac{C'_{P1}C_{e2} + C'_{P1}C_M + C_{e2}C_M}{C_M} \end{cases}. \tag{40}$$

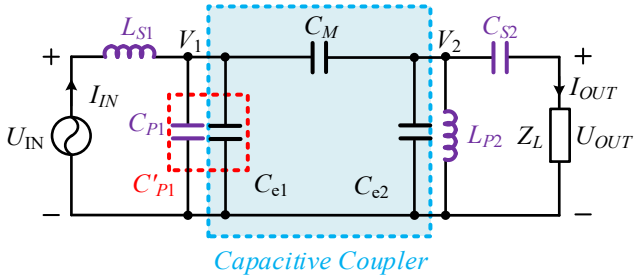


Figure 11. LC−CL compensation topology with π-type coupler model.

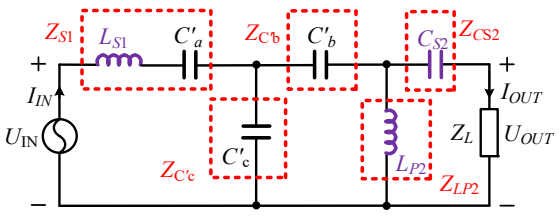


Figure 12. LC−CL compensation topology with T-type coupler model.

The condition to achieve CC output, as shown in Equation (8) can be rewritten as

$$Z_{C_c'}^2 - \left(Z_{S1} + Z_{C_c'}\right)\left(Z_{C_c'} + Z_{C_b'} + Z_{LP2}\right) = 0 \tag{41}$$

By solving Equation (41), the compensation elements to realize CC output can be derived as

$$\begin{cases} \omega^2 L_{S1} = \frac{1}{C_a'} \\ \omega^2 L_{P2} = \frac{1}{C_b'} \end{cases} \tag{42}$$

Then the output current I_{OUT} is deduced by

$$I_{OUT} = j\frac{U_{IN}}{\omega L_{P2}} \tag{43}$$

The input impedance Z_{IN} under CC output condition is calculated as

$$Z_{IN} = \frac{1}{(\omega C_b')^2 Z_L + j[\omega C_b'(1 - \frac{C_b'}{C_{S2}}) + \omega C_c']} \tag{44}$$

It can be seen that the input impedance consists of an imaginary and a real part. Therefore, the following expression can be derived to achieve ZPA operation with CC output characteristics.

$$\begin{aligned} &\omega C_b'(1 - \tfrac{C_b'}{C_{S2}}) + \omega C_c' = 0 \\ &\Rightarrow C_{S2} = \tfrac{C_b'^2}{C_b' + C_c'} \end{aligned} \tag{45}$$

According to Equation (10), the CV output condition can be deduced as

$$\begin{cases} \omega^2 L_{S1} = \frac{1}{C_a'} + \frac{1}{C_c'} \\ \omega^2 L_{P2} = \frac{1}{C_{S2}} \end{cases} \tag{46}$$

Then the voltage gain G_V is derived as

$$G_V = \frac{C_c'}{C_{S2}} \tag{47}$$

When the compensation inductor L_{P2} satisfies (48), the ZPA operation can be achieved, and the input impedance ZPA is given in Equation (48).

$$\begin{cases} \omega^2 L_{P2} = \frac{1}{C_b'} + \frac{1}{C_c'} \\ Z_{IN} = \frac{Z_L}{\omega^4 C_c'^2 L_{P2}^2} \end{cases} \tag{48}$$

The comparison of each SP-based CPT compensation topology has been listed in Tables 2 and 3, which show output characteristics, ZPA condition, and compensation conditions to achieve CC or CV output, respectively. To sum up, it can be concluded that all four basic SP compensation topologies can realize the CC and CV output characteristics through properly designing compensation parameters. However, the double-sided LC and double-sided CL topologies cannot realize the ZPA condition when designed to achieve CV output. On the contrary, the CL−LC and LC−CL topologies can achieve ZPA conditions on both the CC output and CV output. Therefore, the following analysis concentrates on the CL−LC and LC−CL topologies due to their advantages of good input characteristics.

Table 2. Comparison of SP-based compensation topologies to achieve CC output.

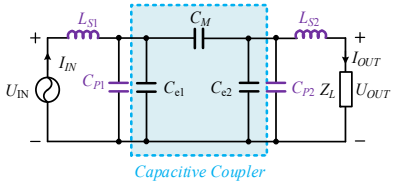
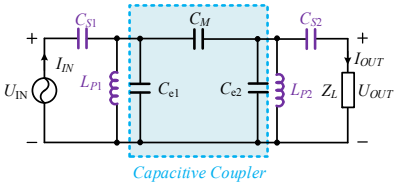
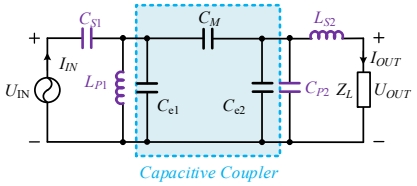
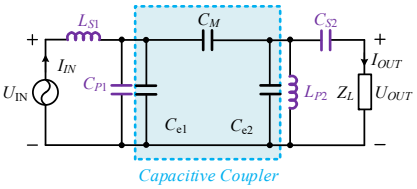
Compensation Topologies	CC Output	
	Conditions	**Output Current**
 Double-sided LC compensation topology	$\omega^2 L_{S1} = \frac{C'_{P2}+C_M}{C'_{P1}C'_{P2}+C'_{P1}C_M+C'_{P2}C_M}$ ZPA can be achieved with the condition: $\omega^2 L_{S2} = \frac{C'_{P1}+C_M}{C'_{P1}C'_{P2}+C'_{P1}C_M+C'_{P2}C_M}$	$I_{OUT} = -j\omega\frac{C'_{P1}C'_{P2}+C'_{P1}C_M+C'_{P2}C_M}{C_M}U_{IN}$ Where $C'_{P1} = C_{P1}+C_{e1}, C'_{P2} = C_{P2}+C_{e2}$
 Double-sided CL compensation topology	$\begin{cases}\omega^2 L_{P1} = \frac{C_{e2}}{C_{S1}C_{e2}+C_{e1}C_{e2}+C_{e1}C_M+C_{e2}C_M} \\ \omega^2 L_{P2} = \frac{C_{e1}}{C_{e1}C_{e2}+C_{e1}C_M+C_{e2}C_M}\end{cases}$ ZPA can be achieved with the condition: $C_{S2} = \frac{C_b^2}{C_c+C_b}$ $Z_{IN} = \frac{L_{P2}}{C_b Z_L}$	$I_{OUT} = -j\omega\frac{C_{S1}C_{e2}}{C_{e1}}U_{IN}$ Where $\begin{cases} C_b = \frac{C_{e1}C_{e2}+C_{e1}C_M+C_{e2}C_M}{C_{e1}} \\ C_c = \frac{C_{e1}C_{e2}+C_{e1}C_M+C_{e2}C_M}{C_M}\end{cases}$
 CL−LC compensation topology	$\omega^2 L_{P1} = \frac{(\frac{1}{C'_a}+\frac{1}{C'_c})\frac{1}{C_{S1}}}{\frac{1}{C'_a}+\frac{1}{C'_c}+\frac{1}{C_{S1}}}$ ZPA can be achieved with the condition: $\omega^2 L_{S2} = \frac{1}{C'_b}+\frac{1}{C'_c}-\frac{C'_a C'_c}{C'_a+C'_c}(1+\frac{C'_a C'_c}{(C'_a+C'_c)C_{S1}})$ $Z_{IN} = \frac{C'_a C'_c}{Z_L C_{S1}(C'_a+C'_c)}$	$I_{OUT} = -j\omega(1+\frac{C'_c}{C'_a})U_{IN}$ Where $\begin{cases} C'_a = \frac{C_{e1}C'_{P2}+C_{e1}C_M+C'_{P2}C_M}{C'_{P2}} \\ C'_b = \frac{C_{e1}C'_{P2}+C_{e1}C_M+C'_{P2}C_M}{C_{e1}} \\ C'_c = \frac{C_{e1}C'_{P2}+C_{e1}C_M+C'_{P2}C_M}{C_M}\end{cases}$ and $C'_{P2} = C_{P2}+C_{e2}$
 LC−CL compensation topology	$\begin{cases}\omega^2 L_{S1} = \frac{1}{C'_a} \\ \omega^2 L_{P2} = \frac{1}{C'_b}\end{cases}$ ZPA can be achieved with the condition: $C_{S2} = \frac{{C'_b}^2}{C'_b+C'_c}$ $Z_{IN} = \frac{1}{(\omega C'_b)^2 Z_L}$	$I_{OUT} = j\frac{U_{IN}}{\omega L_{P2}}$ Where $\begin{cases} C'_a = \frac{C'_{P1}C_{e2}+C'_{P1}C_M+C_{e2}C_M}{C_{e2}} \\ C'_b = \frac{C'_{P1}C_{e2}+C'_{P1}C_M+C_{e2}C_M}{C'_{P1}} \\ C'_c = \frac{C'_{P1}C_{e2}+C'_{P1}C_M+C_{e2}C_M}{C_M}\end{cases}$ and $C'_{P1} = C_{P1}+C_{e1}$

Table 3. Comparison of SP-based compensation topologies to achieve CV output.

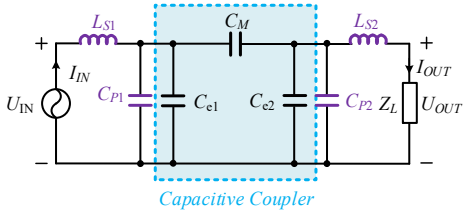
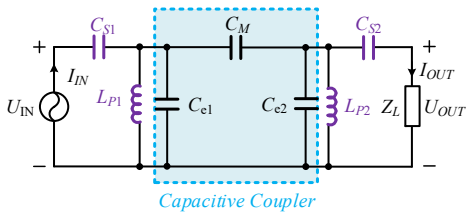
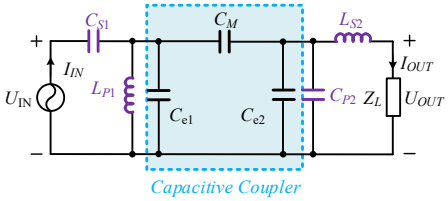
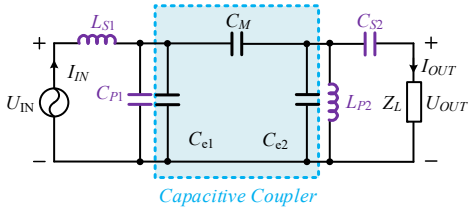
Compensation Topologies	CV Output	
	Conditions	**Voltage Gain**
 Double-sided LC compensation topology	$\begin{cases}\omega^2 L_{S1} = \frac{1}{C_{P1}+C_{e1}} \\ \omega^2 L_{S2} = \frac{1}{C_{P2}+C_{e2}}\end{cases}$ ZPA cannot be achieved $Z_{IN} = \frac{1}{G_V^2/Z_L - j\omega C'_{P1}(C'_{P1}/C_M+C'_{P1}/C'_{P2}+1)}$	$G_V = -\frac{C_{P1}+C_{e1}}{C_{P2}+C_{e2}}$ Where $C'_{P1} = C_{P1}+C_{e1}, C'_{P2} = C_{P2}+C_{e2}$
 Double-sided CL compensation topology	$\begin{cases}\omega^2 L_{P1} = \frac{C_{e2}}{C_{S1}C_{e2}+C_{e1}C_{e2}+C_{e1}C_M+C_{e2}C_M} \\ \omega^2 L_{P2} = \frac{C_{e1}}{C_{S1}C_{e1}+C_{e1}C_{e2}+C_{e1}C_M+C_{e2}C_M}\end{cases}$ ZPA cannot be achieved $Z_{IN} = \frac{-1/\omega^2 C_{S1}^2}{1+(\frac{C_{e2}}{C_{e1}})^2(1-\frac{1}{\omega^2 C_{S2}^2 Z_L})-j\frac{C_c}{\omega C_a^2}}$	$G_V = \frac{C_{S1}C_{e2}}{C_{S2}C_{e1}}$ Where $\begin{cases} C_a = \frac{C_{e1}C_{e2}+C_{e1}C_M+C_{e2}C_M}{C_{e2}} \\ C_b = \frac{C_{e1}C_{e2}+C_{e1}C_M+C_{e2}C_M}{C_{e1}} \\ C_c = \frac{C_{e1}C_{e2}+C_{e1}C_M+C_{e2}C_M}{C_M}\end{cases}$

Table 3. *Cont.*

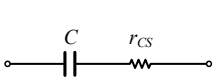
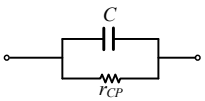
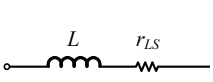
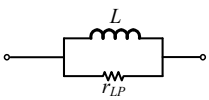
Compensation Topologies	CV Output: Conditions	CV Output: Voltage Gain
 CL−LC compensation topology	$\begin{cases} \omega^2 L_{P1} = \frac{1}{C_{S1}} = \frac{1}{C'_a} + \frac{1}{C'_c} \\ \omega^2 L_{S2} = \frac{1}{C'_b} + \frac{1}{C'_c} \end{cases}$ ZPA can be achieved $Z_{IN} = \omega^4 C'^2_c L^2_{P1} Z_L$	$G_V = \frac{C_{S1}}{C'_c}$ Where $\begin{cases} C'_a = \frac{C_{e1}C'_{P2}+C_{e1}C_M+C'_{P2}C_M}{C'_{P2}} \\ C'_b = \frac{C_{e1}C'_{P2}+C_{e1}C_M+C'_{P2}C_M}{C_{e1}} \\ C'_c = \frac{C_{e1}C'_{P2}+C_{e1}C_M+C'_{P2}C_M}{C_M} \end{cases}$ and $C'_{P2} = C_{P2} + C_{e2}$
 LC−CL compensation topology	$\begin{cases} \omega^2 L_{S1} = \frac{1}{C'_a} + \frac{1}{C'_c} \\ \omega^2 L_{P2} = \frac{1}{C_{S2}} \end{cases}$ ZPA can be achieved with the condition: $\begin{cases} \omega^2 L_{P2} = \frac{1}{C'_b} + \frac{1}{C'_c} \\ Z_{IN} = \frac{Z_L}{\omega^4 C'^2_c L^2_{P2}} \end{cases}$	$G_V = \frac{C'_c}{C_{S2}}$ Where $\begin{cases} C'_a = \frac{C_{e1}C'_{P2}+C_{e1}C_M+C'_{P2}C_M}{C'_{P2}} \\ C'_b = \frac{C_{e1}C'_{P2}+C_{e1}C_M+C'_{P2}C_M}{C_{e1}} \\ C'_c = \frac{C_{e1}C'_{P2}+C_{e1}C_M+C'_{P2}C_M}{C_M} \end{cases}$ and $C'_{P2} = C_{P2} + C_{e2}$

4. Efficiency Analysis of SP-Based CPT Topology

The circuit simplified models of passive components with parasitic resistance are presented in Table 4 [39], where r_{CS} and r_{LS} are the series resistance, r_{CP} and r_{LP} are the paralleled resistance, Q_C and Q_L represent the quality factor of compensation capacitors and inductors, respectively. To simplify the efficiency calculation, the circuit model of parasitic resistance should be appropriately adopted according to the specified compensation topology. Figure 13 shows the four basic SP compensation topologies considering the parasitic resistance of passive components. The system efficiency of double-sided LC and double-sided CL compensation topology can be expressed as

$$\begin{cases} \eta|_{LCLC} = \dfrac{|I_{OUT}|^2 Z_L}{|I_{OUT}|^2 Z_L + |I_{OUT}|^2 r_{LS2} + |I_{IN}|^2 r_{LS1} + \frac{|V_1|^2}{r_{CP1}} + \frac{|V_2|^2}{r_{CP2}}} \\ \eta|_{CLCL} = \dfrac{|I_{OUT}|^2 Z_L}{|I_{OUT}|^2 Z_L + |I_{OUT}|^2 r_{CS2} + |I_{IN}|^2 r_{CS1} + \frac{|V_1|^2}{r_{LP1}} + \frac{|V_2|^2}{r_{LP2}}} \end{cases} \tag{49}$$

Table 4. Circuit Models Of Capacitor And Inductor With Parasitic Resistance.

	Capacitor		Inductor	
Circuit model				
Parasitic resistance	$r_{CS} = 1/(\omega C \cdot Q_C)$	$r_{CP} = Q_C/(\omega C)$	$r_{LS} = (\omega L)/Q_L$	$r_{LP} = \omega L \cdot Q_L$

The system efficiency of CL−LC and LC−CL topology can be expressed as

$$\begin{cases} \eta|_{CLLC} = \dfrac{|I_{OUT}|^2 Z_L}{|I_{OUT}|^2 Z_L + |I_{OUT}|^2 r_{LS2} + |I_{IN}|^2 r_{CS1} + |I_{LP1}|^2 r_{LP1} + \frac{|V_2|^2}{r_{CP2}}} \\ \eta|_{LCCL} = \dfrac{|I_{OUT}|^2 Z_L}{|I_{OUT}|^2 Z_L + |I_{OUT}|^2 r_{CS2} + |I_{IN}|^2 r_{LS1} + |I_{LP2}|^2 r_{LP2} + \frac{|V_1|^2}{r_{CP1}}} \end{cases} \tag{50}$$

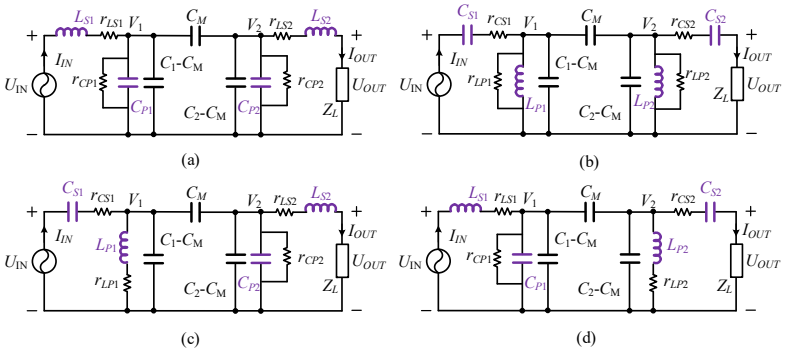


Figure 13. SP-based CPT topology considering the parasitic resistance. (**a**) Double-sided LC compensation, (**b**) double-sided CL compensation, (**c**) CL−LC compensation, (**d**) LC−CL compensation.

The system efficiency of four SP-based compensation topologies can be derived from Equations (49) and (50). Taking the LCCL compensation topology as an example, its AC−AC efficiency is calculated as

$$\eta|_{LCCL} = \frac{1}{1 + Z_L\left(\frac{\omega C_{P1}}{Q_C G_V^2} + \frac{\omega C_{S2}}{Q_L}\right) + \frac{1}{Z_L}\left(\frac{G_V^2}{\omega C'_a Q_L} + \frac{G_V^2 C_{P1}}{C'^2_a Q_C} + \frac{Q_L + Q_C}{\omega C_{S2} Q_L Q_C}\right)} \tag{51}$$

where G_V is equal to C_c/C_{S2}, and C'_a, C'_c are expressed in (40). As shown in Equation (51), when the quality factor and impedance of passive elements are fixed, the efficiency of LCCL topology is decided by the load resistance Z_L and system operation frequency ω. Hence, the maximum system efficiency can be derived as

$$\eta|_{LCCL\_max} = \frac{1}{1 + 2\sqrt{\left(\frac{\omega C_{P1}}{Q_C G_V^2} + \frac{\omega C_{S2}}{Q_L}\right)\left(\frac{G_V^2}{\omega C'_a Q_L} + \frac{G_V^2 C_{P1}}{C'^2_a Q_C} + \frac{Q_L + Q_C}{\omega C_{S2} Q_L Q_C}\right)}} \tag{52}$$

The optimum load resistance to achieve the maximum system efficiency is calculated as follows.

$$Z_L = \sqrt{\frac{\left(\frac{G_V^2}{\omega C'_a Q_L} + \frac{G_V^2 C_{P1}}{C'^2_a Q_C} + \frac{Q_L + Q_C}{\omega C_{S2} Q_L Q_C}\right)}{\left(\frac{\omega C_{P1}}{Q_C G_V^2} + \frac{\omega C_{S2}}{Q_L}\right)}} \tag{53}$$

Figure 14 illustrates the system efficiency curves against the variations of load resistance for four SP compensation topologies. The output voltages of the four topologies are designed to be the same. The voltage gains of CLLC and LCCL are 0.2 and 5, respectively. It can be seen that the system efficiency of CLLC topology is the highest among the load variations, which is due to the CLLC topology in CV mode equivalent to the buck converter, leading to the smallest loop current under the same power level. Each compensation topology has an optimum load resistance to achieve the highest system efficiency. The optimum load resistance can be adjusted according to the application requirements.

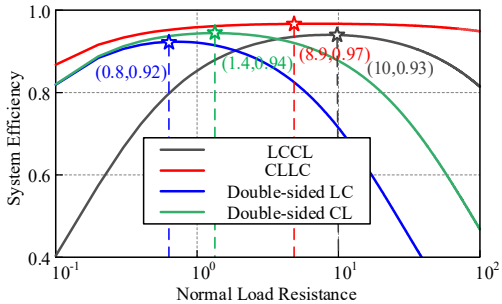


Figure 14. System efficiency versus load resistance variations.

5. Experimental Verification

5.1. Experimental Prototype

To verify the proposed theory, an experimental prototype of the CPT system with LCCL compensation topology is built up, as shown in Figure 15. The coupler structure consists of four 300 mm × 300 mm aluminum plates. The transfer distance is set to 5 mm. The switching devices of the full−bridge inverter adopted C2M0160120D MOSFETS, and the MSC020SDA120B−ND diodes were used in the full−bridge rectifier. In order to eliminate the undesirable magnetic loss of ferrite in the traditional inductor, the compensation inductors in the experiment adopted the air−core inductor constructed by PVC tubes wounding with Litz wire. To reduce the size of inductors, the switching frequency of MOSFETS was set to 1 MHz. The system parameters are listed in Table 5.

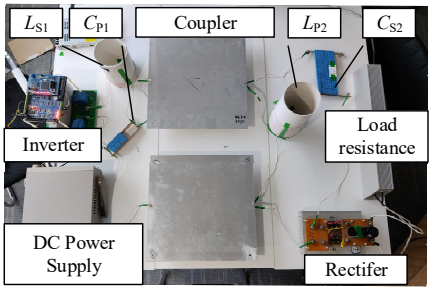


Figure 15. Experimental prototype of CPT system with LCCL compensation topology.

Table 5. Experimental Parameters.

Symbol	Value
U_{dc}/V	20
R_L/Ω	100
f/MHz	1
C_M/pF	114.8
C_{P1}/nF	1
C_{S2}/pF	202.1
L_{S1}/μH	25.28
L_{P2}/μH	125.3

5.2. Experimental Results

When the voltage gain of the LCCL compensation CPT system is designed to 5, the experimental AC waveforms of U_{IN}, I_{IN}, U_{OUT}, and I_{OUT} are shown in Figure 16. The value of U_{IN}, I_{IN}, U_{OUT}, and I_{OUT} is 18.7 V, 4.49 A, 90.8 V, and 0.89 A, respectively. The phase difference between the input voltage and the input current is close to zero degrees, and it can be concluded that the ZPA operation of LCCL topology to achieve CV output is achieved without an extra compensation circuit. As the parasitic resistances of compensation components exist, the measured voltage gain with 100 Ω load resistance is 4.52.

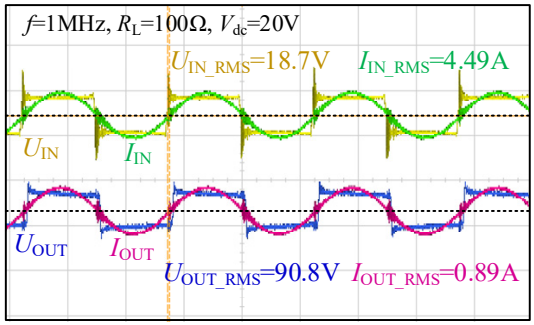


Figure 16. Experimental waveforms of U_{IN}, I_{IN}, U_{OUT}, and I_{OUT}.

To verify the constant output voltage characteristics, the output voltage gains are measured with load resistance changing from 100 Ω to 20 Ω. The measured results and simulated results are illustrated in Figure 17. The simulated results are conducted in MATLAB/SIMULINK models. When the load resistance increases to 5 times itself, the voltage gain changes from 4.54 to 4.90 in simulation models. While in practice, due to the impact of the parasitic resistance of passive components, the voltage gain increased from 3.95 (79 V) to 4.54 (90.8 V), spaces missing, and the rate of voltage change reached 12.9%. The voltage drop can be reduced in practical applications by adopting compensation elements with more minor resistance and more accurate passive components.

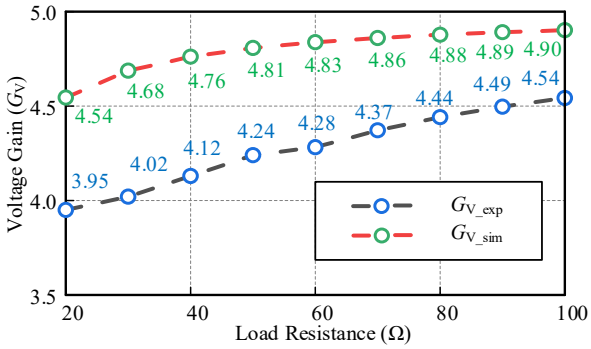


Figure 17. The output voltage against the load resistance variations.

Figure 18 shows the measured system efficiency and output power with changing load resistance. As the output voltage is independent of load resistance, the output power decreased from 334 W to 78 W with load resistance changed from 20 Ω to 100 Ω. Since the losses of the inverter, rectifier, and capacitive coupler are not considered in the calculation of system theoretical efficiency, the system experimental efficiency is obviously lower than the system theoretical efficiency. The system efficiency increased with the increasing load resistance, which is consistent with theoretical analysis. Therefore, the double-sided LC compensation CPT system preferred the heavy load situation. The maximum system efficiency when load resistance changes from 20 Ω to 100 Ω can reach 89% and the system efficiency can be lifted further by using compensation elements with high−quality factors.

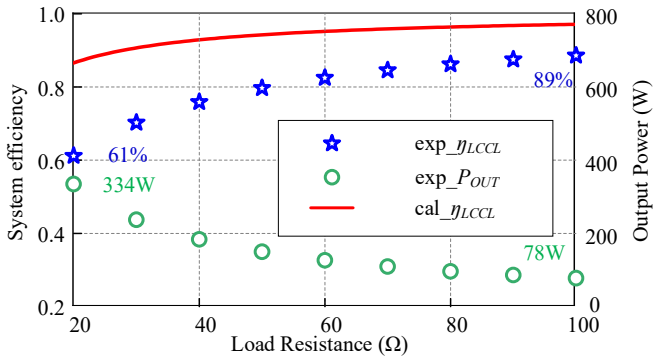


Figure 18. Measured efficiency and output power.

6. Conclusions

This paper analyzed the SP compensation topologies in the CPT system to achieve CC/CV output characteristics and ZPA input conditions. The T/Π circuit models of the coupler structure were adopted to simplify the regular SP compensation circuit, and the input–output characteristics of four specific SP compensation topologies were derived, respectively. Under CC output conditions, four specific topologies can achieve ZPA input property. In contrast, only CLLC and LCCL topologies can realize the ZPA input when designed to achieve CV output. The system efficiency calculation methodologies were

given and analyzed. The experimental verification was carried out, and the ZPA condition and load−independent output characteristics were verified.

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