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Design of a GaAs-Based Ka-Band Low Noise Amplifier MMIC with Gain Flatness Enhancement

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Abstract: This paper presents a GaAs-based Ka-band low noise amplifier (LNA) with gain flatness enhancement. Active device optimization and inductive degeneration techniques were employed to obtain a low noise figure (NF) and good input/output return loss. In order to achieve a flat gain response over a wide bandwidth, the stagger tuning technique was utilized. The proposed LNA was implemented by 0.15 μm GaAs pHEMT process, and the chip area is only 1.5 × 0.9 mm^2. Measurement results show that the presented LNA exhibits a small signal gain of 21.5 ± 0.3 dB, and the NF of the LNA is less than 2.2 dB from 32 to 40 GHz at room temperature.

Keywords: LNA; Ka band; GaAs; monolithic microwave integrated circuit

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1. Introduction

The number of wireless devices, along with the amount of data, has increased dramatically over the last two decades, necessitating wireless systems with greater communication capacity and higher data rates. However, radio spectrum resources for wireless communication are scarce, and radio frequency (RF) bands have been densely allocated for various commercial and military applications. There is a growing interest in millimeter-wave wireless systems. "Ka-band" refers to electromagnetic waves in the frequency range of 26.5–40 GHz. The millimeter wave frequency bands used for 5G communication are mostly in Ka-band, such as 28, 37, and 39 GHz in the United States, 26 GHz in Europe, and 26 GHz and 40 GHz in China [1]. In addition, satellite communication systems [2] and passive millimeter wave imaging [3–5] also operate in Ka-band.

The low noise amplifier is the first active module of the receiver, and its performance is directly related to the receiver's dynamic range and sensitivity. Low noise amplifiers are expected to have extremely low noise figures, high gain, good input and output return loss, low power consumption, and good linearity [6]. However, gain flatness is often an overlooked indicator. Good gain flatness can ensure that the signal has an approximate amplification degree in the band and relax the requirements for the dynamic range of the analog–digital converter (ADC) [7], so it has notable research significance.

Several circuit topologies for broadband low-noise amplifiers have been reported, such as distributed amplifiers, shunt feedback amplifiers, and filter-matching network amplifiers. Distributed amplifiers [8,9] can achieve wide bandwidth with low input and output return loss but at the expense of power consumption and area. The feedback amplifier [10,11] can expand the amplifier's bandwidth, but it tends to degrade the noise performance; the filter-matching network amplifier [12] can achieve broadband frequency response, but excessive passive components increase the loss of input matching, deteriorating the noise figure. Ref. [13] demonstrated a wide bandwidth, low noise amplifier with source degeneration and resistive feedback that achieved a gain greater than 25 dB but with poor gain flatness.

A 32–50 GHz low noise amplifier has a gain of 28 dB but a noise figure of 2.8 dB [14]. The LNA in Reference [15] exhibits a gain flatness of 1.2 dB and NF of 2.2–2.6 dB, but its gain is limited. Reference [16] presented a low noise amplifier using resistive and inductive feedback techniques that achieved a gain of 19.8 dB and a gain flatness of 0.8 dB, but it did not show the measurement data of the noise figure. The gain flatness of the low-noise amplifier can be further improved while maintaining high gain, a low noise figure, low power consumption, and a small chip area.

In this paper, we propose a compact gain flatness enhancement wide-band low noise amplifier. To achieve simultaneous input and noise matching, the inductive degeneration technique is employed, and the stagger tuning technique is used to improve gain flatness. The designed LNA was implemented through a 0.15 µm GaAs pHEMT process. The measurement results show that the proposed LNA achieves a gain of 21.5 dB with a gain flatness of ±0.3 dB. The measured noise figure at room temperature is below 2.2 dB from 32 to 40 GHz. The LNA draws 17 mA from a 3.3 V power supply. The designed LNA realizes the organic combination of low noise figure, high gain, good gain flatness, low power consumption, and small chip area.

The paper is organized as follows: Section 2 introduces the design methodology of the circuit in detail, including active device optimization, inductive degradation technology, and stagger tuning technique. The experimental results and performance comparison table with the state-of-the-art mm-wave wideband LNAs are presented in Section 3. Finally, the paper is concluded in Section 4.

2. Circuit Design

A three-stage common-source cascade topology is utilized in this design, as can be seen in Figure 1. Inductive degeneration [17] is utilized in the first stage in order to achieve simultaneous input and noise matching [18]. The stagger tuning technique is employed to achieve flat gain. The first stage uses a 4 × 25 µm CPW transistor for low noise figure, and the second and third stages use a 2 × 50 µm MS transistor for high gain.

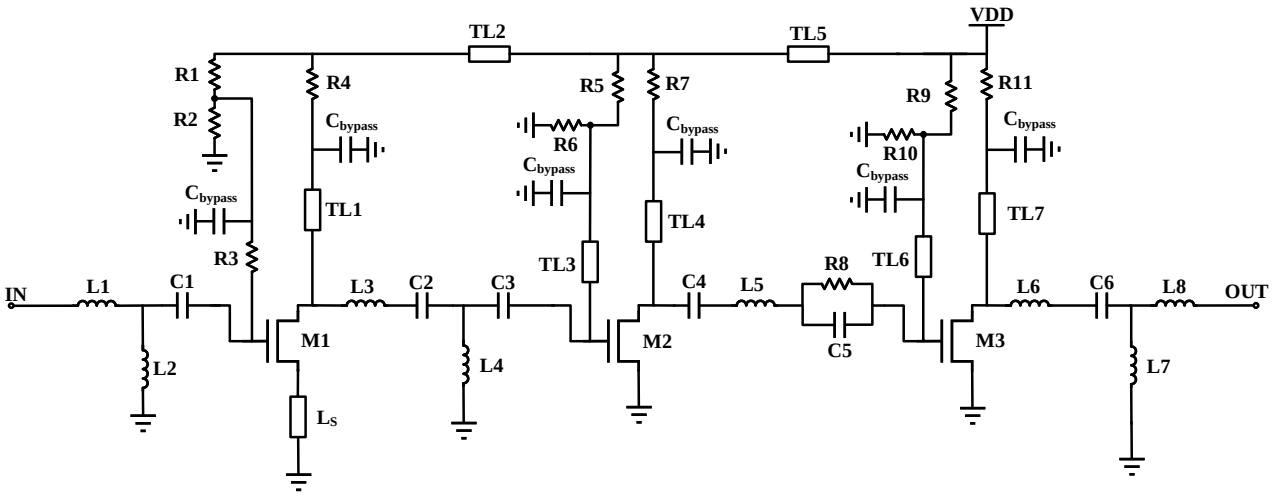

Figure 1. Schematic view of the proposed LNA.

For ease of use, the proposed LNA is powered by a single power supply. A resistor divider network and a large resistor or a quarter-wavelength transmission line comprise the biasing network. R6 is a large resistor with a resistance value of 10 kΩ which serves as a DC choke in a wide frequency range. Bypass capacitors are added to the gate bias and drain bias of each stage in order to filter out interference signals from power supplies, substrates, etc. R4, R7, and R11 are small resistors with a resistance value of 5 Ω, reducing signals' cross talk between amplifier stages and improving circuit stability.

In the input matching design, although the high-order LC network can be used to achieve broadband matching, excessive components will increase the insertion loss of the matching network and further deteriorate the noise. Therefore, in this design, simple T-type matching is adopted, in which C1 serves as a DC blocker.

2.1. Active Device Optimization

To a large extent, the performance of the transistor determines the upper limit of the LNA's performance; thus, it is critical to select the appropriate transistor type, bias point, and size. For low-noise amplifiers, the most critical indicators are noise figure and gain. Correspondingly, the minimum noise figure (NF_{min}) and the maximum available gain (max available gain, MAG) can be used to evaluate the performance of transistors.

The adopted 0.15 µm GaAs pHEMT process provides two types of transistors. One has no back holes on the source terminal and is called a coplanar waveguide (CPW) transistor; the other has back holes on both sides of the source terminal and is called a microstrip (MS) transistor. The two types of transistors are simulated and compared in detail.

First, NF_{min} and MAG under different values of V_{GS} are simulated in order to determine the optimal bias point. In the simulation, V_{DD} is fixed at 3.3 V, which is the power supply voltage of this design; the frequency is determined to be 36 GHz. V_{GS} is swept from 0.25 V to 0.85 V, and the step size is set to 0.05 V. Figure 2 depicts the simulation results.

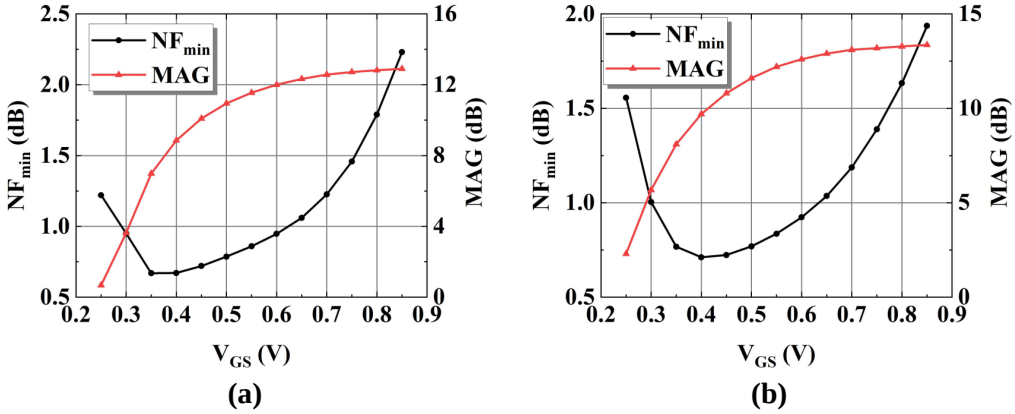

Figure 2. Simulated NF_{min} and MAG of a 4 × 25 µm (**a**) CPW; (**b**) MS transistor versus different values of V_{GS}.

The simulation results show that as V_{GS} increases, NF_{min} decreases and then increases, and there exists an optimal bias voltage V_{GS0}, which minimizes the NF_{min}. In contrast, MAG increases rapidly with V_{GS} increase, and then the magnitude of the increase slows down, indicating a monotonous increasing trend overall. It can be seen from Figure 2a that for the CPW transistor, NF_{min} reaches a minimum value when V_{GS} is around 0.4 V, but its MAG is relatively low. After carefully considering the noise figure and gain characteristics, V_{GS} is set to 0.45 V. Similarly, the MS transistor exhibits the same law, with V_{GS} set to 0.45 V as the bias point.

After determining the optimal bias point, the NF_{min} and MAG of various-size transistors were simulated. Figure 3 depicts the simulated result.

Figure 3 indicates that: (1) For the same transistor type, the NF_{min} of 4× 25 µm is lower than that of 2 × 50 µm, owing to the smaller gate parasitic resistance of the multi-finger transistor, thereby reducing the noise caused by resistance. In addition, the MAG of 4 × 25 µm is also lower than that of 2 × 50 µm. (2) For transistors of the same size, the NF_{min} of the CPW transistor and the MS transistor are almost equal, but the MAG of the MS transistor is higher than that of the CPW transistor.

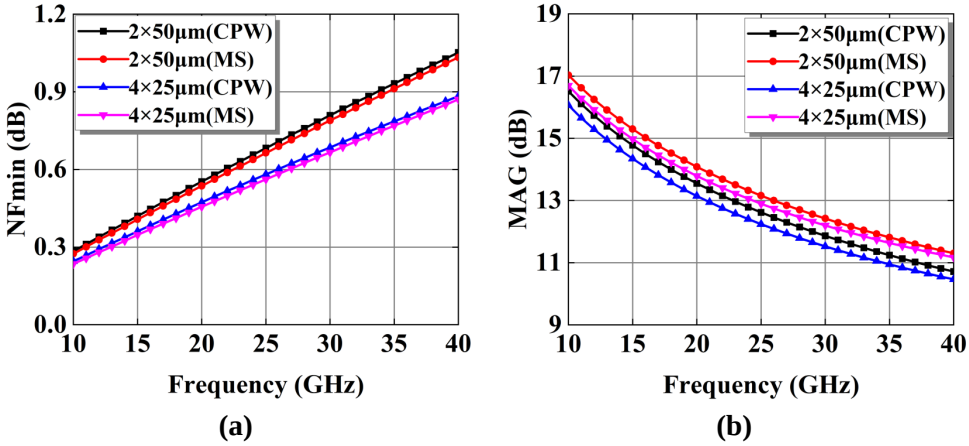

Figure 3. The simulated (**a**) NF_{min}; (**b**) MAG for transistor of different sizes (2 × 50 µm CPW, 2× 50 µm MS, 4 × 25 µm CPW, 4 × 25 µm MS).

The transistor type, bias point, and size are determined based on the above simulation results. Since the first stage employs the inductive degeneration technique, a 4 × 25 µm CPW transistor is used in the first stage to achieve a lower noise figure. The second and the third stages use a 2 × 50 µm MS transistor to meet the gain requirement.

2.2. Inductive Degeneration

The inductive degeneration technique is widely used in the design of low-noise amplifiers [19]. By connecting an inductor in series with the source terminal of the transistor, the input impedance is derived as

$$Z_{in}(s) = \frac{1}{sC_{gs}} + s(L_G + L_S) + \frac{g_m L_S}{C_{gs}} \quad (1)$$

where L_G and L_S are the series gate and degenerated inductances, respectively. C_{gs} is the gate-to-source capacitance [20]. As shown in Equation (1), the real part of the input impedance is $g_m L_S/C_{gs}$, and it is frequency independent. The L_S reduces the distance between the optimal noise impedance point and the maximum gain impedance point.

The optimal noise impedance point Z_{opt} and the maximal gain impedance point Z_{mag} are defined as follows:

$$Z_{opt}(s) = R_{opt} + j * X_{opt} \quad (2)$$

$$Z_{mag}(s) = R_{mag} + j * X_{mag} \quad (3)$$

A new parameter D is defined here to characterize the distance between two impedance points, Z_{opt} and Z_{mag}, and the definition formula for D is shown in Equation (4).

$$D = \sqrt{(R_{mag} - R_{opt})^2 + (X_{mag} - X_{opt})^2} \quad (4)$$

The L_S in Figure 1 is implemented by a short microstrip line. The variation curve of D is simulated for various source microstrip line lengths'. As shown in Figure 4, D decreases monotonically as the length of source microstrip line increases, implying that the inductive degeneration technique makes it easier to achieve both noise and input matching.

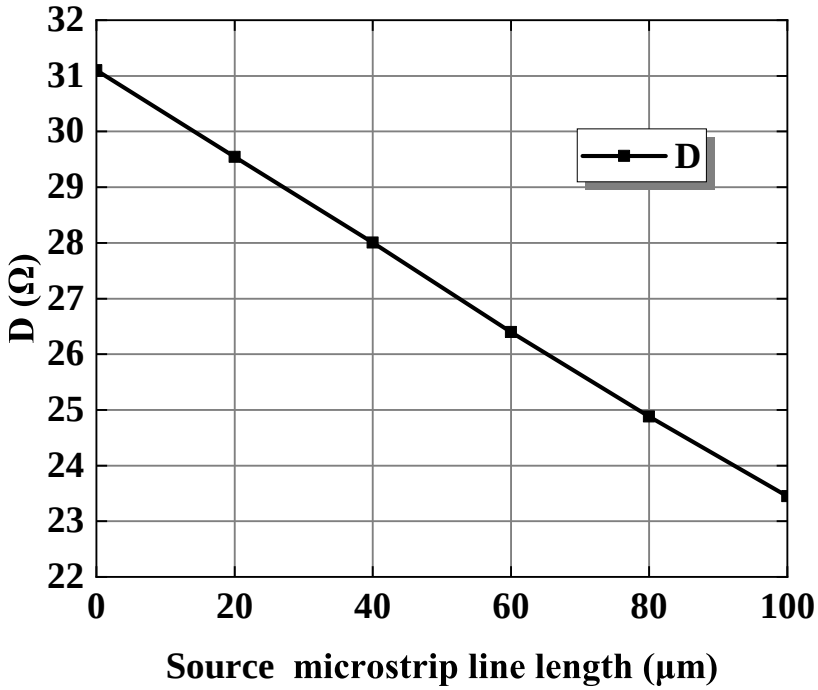

Figure 4. Simulated D versus different values of the source microstrip line length.

Adding L_S will not worsen the noise, but it can bring the distance between the two impedance points closer, allowing for simultaneous input and noise matching. However, L_S cannot be increased arbitrarily, as the increase of Ł$_S$ lowers the gain. As a result, the value of L_S should take into account two factors. Figure 5 depicts the simulated NF$_{min}$ and MAG at various source microstrip line lengths. NF$_{min}$ decreased slightly as L_S increased, but MAG decreased rapidly. Considering that the first stage should still maintain a specific gain, the source microstrip line length is determined to be 60 μm.

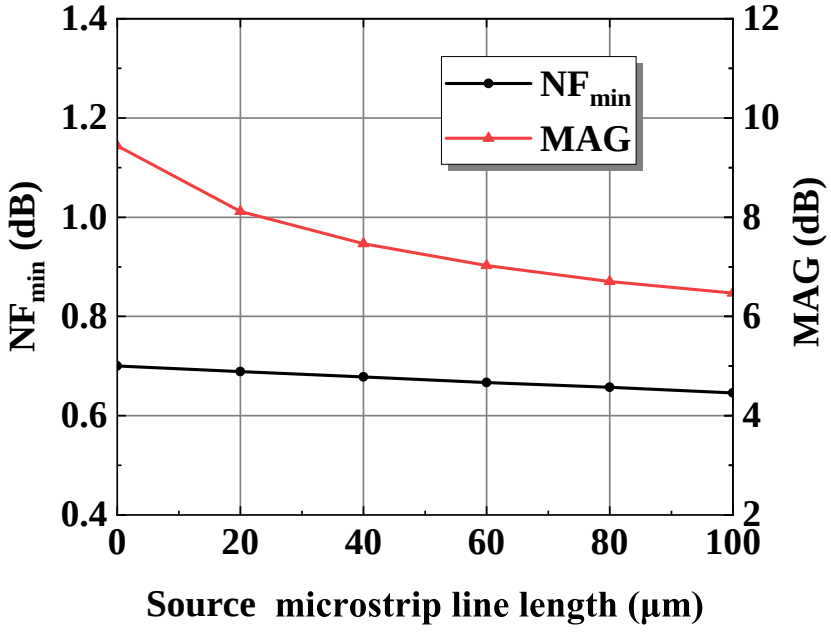

Figure 5. Simulated NF$_{min}$ and MAG versus various values of source microstrip line length.

2.3. Gain Flatness Enhancement

For broadband and flat gain, the stagger tuning technique was adopted. The basic idea of stagger tuning is to distribute the center frequencies of different amplifier stages

at various frequency points so that a flat frequency response can be obtained [21]. In this design, the gain peak frequencies of each stage are set at two different frequency points f_1 and f_2, as shown in Figure 6. Compared with the amplifier that distributes the gain peak at multiple frequency points, the amplifier that distributes the peak gain at two frequency points can maximize the gain, bandwidth, and noise figures within the target band [22]. The peak gain frequency of the first and third stages is designed to be around 29 GHz, and the peak gain frequency of the second stage is 39 GHz. Therefore, the proposed LNA obtains a flat gain response from 32 to 40 GHz.

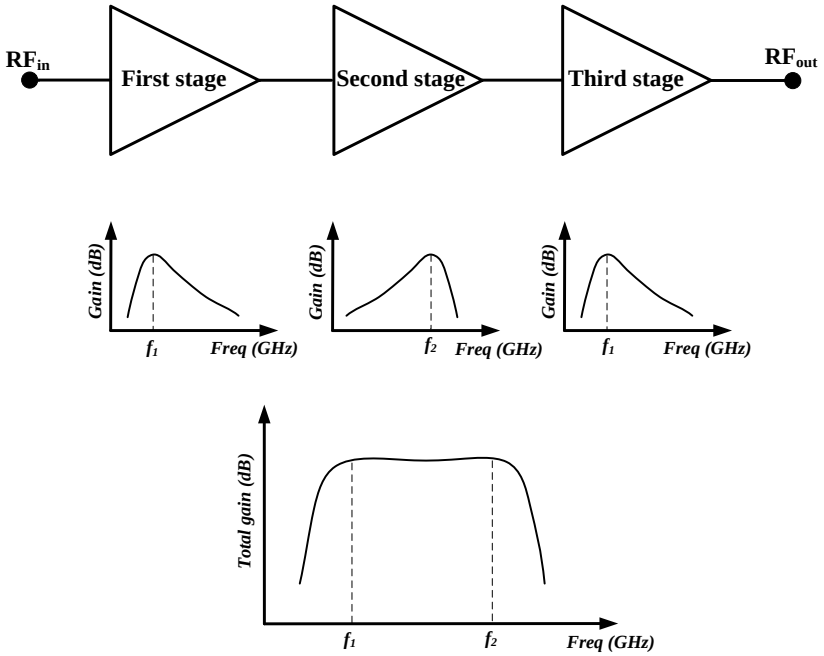

Figure 6. Block diagram of the stagger tuning technique.

2.3.1. Gain Analysis of the First Stage

The output matching network of the first stage, which includes C_2, C_3, L_3, and L_4, primarily determines the resonant frequency of the amplifier's first stage. C_{in2} represents all the second-stage transistor gate capacitances, including C_{gs2}, Miller equivalent capacitance, and other parasitic capacitances. C_{ds1} is the parasitic capacitance of M_1, assuming that the drain-to-source resistance is infinite. The small-signal equivalent model of the first stage is shown in Figure 7, where Z_1 represents the impedance seen from node A to the second stage. Z_1 can be calculated as follows:

$$\begin{aligned} Z_1(s) &= sL_3 + \frac{1}{sC_2} + sL_4 || (\frac{1}{sC_3} + \frac{1}{sC_{in2}}) \\ &= \frac{s^4 L_4 C_3 C_{in2} C_2 L_3 + s^2 [C_2 (C_{in2} + C_3)(L_3 + L_4) + L_4 C_{in2} C_3] + C_{in2} + C_3}{s^3 L_4 C_3 C_{in2} C_2 + sC_2 (C_{in2} + C_3)} \end{aligned} \tag{5}$$

The gain of the source-degenerated common-source amplifier A_{v1}(s) is

$$A_{v1}(s) \approx -\frac{g_{m1}}{1 + g_{m1} * sL_S} * (Z_1(s) || \frac{1}{sC_{ds1}}) \tag{6}$$

where g_{m1} is the transconductance of the first stage's transistor and L_S is the source degenerated inductance. Equation (5) shows that Z_1(s) has three poles p_{11}, p_{12}, and p_{13}, respectively.

$$p_{11} = 0 \tag{7}$$

$$p_{12,13} = \pm j\sqrt{\frac{C_{in2} + C_3}{L_4 C_3 C_{in2}}} \tag{8}$$

As the transistor size and bias point are determined, C_{in2} and C_{ds1} are also determined. The frequency of the first-stage amplifier's gain peak can be modified by adjusting the L_3, L_4, C_2, and C_3, especially for L_4 and C_3. After careful design and optimization, it is finally determined that L_4 is 0.16 nH and C_3 is 0.24 pF.

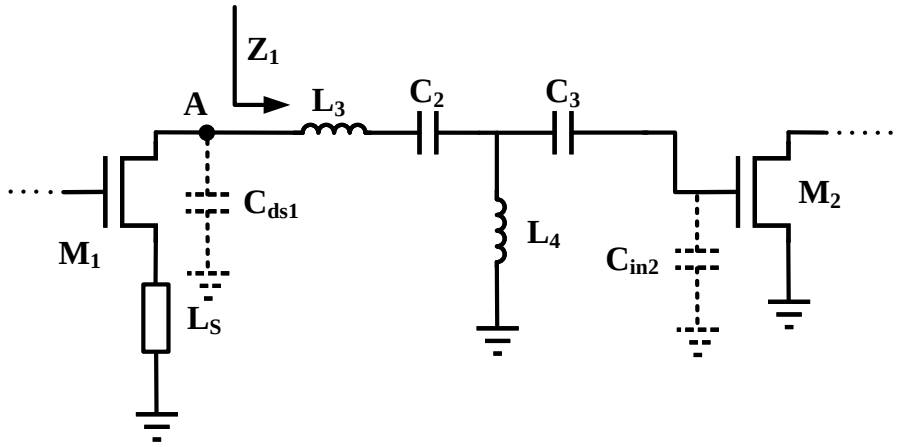

Figure 7. Small-signal equivalent model of the first stage.

2.3.2. Gain Analysis of the Second Stage

Similarly, the gain of the second stage is determined by the output matching network of the second stage. Figure 8 depicts the small-signal equivalent model of the second stage of the proposed LNA. R_8 and C_5 form a parallel RC network to improve the stability of the circuit. Since the parallel network is between the second and third stage, it does not degrade the noise figure. C_{in3} represents the sum of C_{gs3} of the transistor of the third stage, the Miller equivalent capacitance, and other parasitic capacitances. Z_2 denotes the impedance seen from node B to the third stage, and Z_2 can be calculated as:

$$\begin{aligned} Z_2(s) &= \frac{1}{sC_4} + sL_5 + \frac{1}{sC_{in3}} + R_8 || \frac{1}{sC_5} \\ &= \frac{s^3 C_5 R_8 C_{in3} L_5 C_4 + s^2 C_{in3} L_5 C_4 + sR_8(C_5 C_{in3} + C_4 C_5 + C_4 C_{in3}) + C_4 + C_{in3}}{s^2 C_5 R_8 C_{in3} C_4 + sC_4 C_{in3}} \end{aligned} \tag{9}$$

The gain of the second-stage amplifier A_{v2}(s) is:

$$A_{v2}(s) = -g_{m2} * (Z_2(s) || \frac{1}{sC_{ds2}}) \tag{10}$$

where g_{m2} is the transconductance of the second-stage transistor. C_{ds2} is the parasitic capacitance of M_2, neglect the drain-to-source resistance. Z_2(s) has two poles p_{21} and p_{22}, respectively.

$$p_{21} = 0 \tag{11}$$

$$p_{22} = -\frac{1}{C_5 R_8} \tag{12}$$

The frequency distribution of the gain peak of the second-stage amplifier can be adjusted by changing the values of L_5, C_4, and C_5. Simulations were performed to obtain the appropriate value of components. When L_5 is 80 pH, C_4 is 0.67 pF, and C_5 is 0.35 pF, the frequency response of the second stage, as shown in Figure 9, is realized.

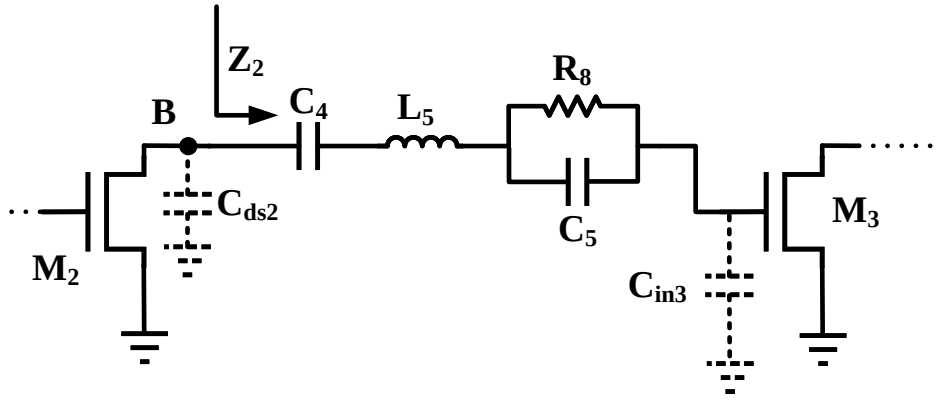

Figure 8. Small-signal equivalent model of the second stage.

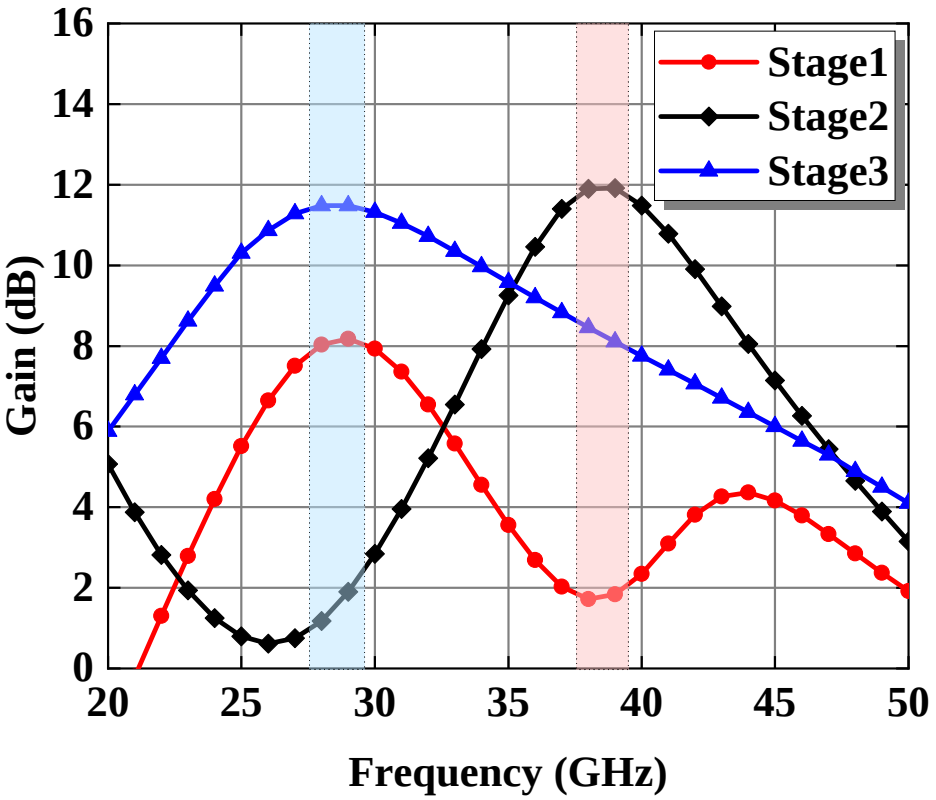

Figure 9. Simulated gain of each stage.

2.3.3. Gain Analysis of the Third Stage

Figure 10 shows a small-signal equivalent model of the third stage of the proposed LNA. R_L is the load impedance, and its value is 50 Ω. The impedance seen from node C to the output terminal Z_3 can be calculated as:

$$\begin{aligned} Z_3(s) &= sL_6 + \frac{1}{sC_6} + sL_7 \| (sL_8 + R_L) \\ &= \frac{s^3C_6(L_6L_7 + L_6L_8 + L_7L_8) + s^2C_6R_L(L_6 + L_7) + s(L_7 + L_8) + R_L}{s^2C_6(L_7 + L_8) + sC_6R_L} \end{aligned} \tag{13}$$

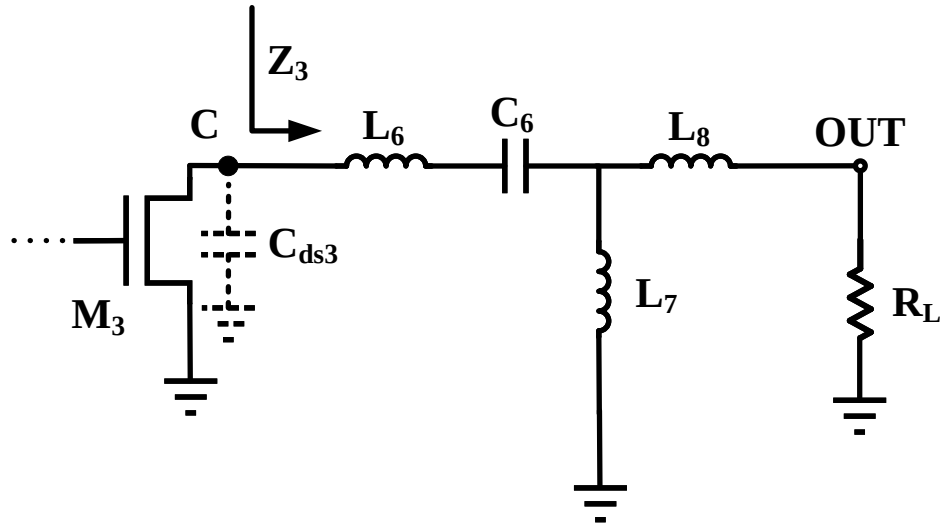

Figure 10. Small-signal equivalent model of the third stage.

Gain of the third-stage amplifier A_{v3}(s) is:

$$A_{v3}(s) = -g_{m3} * (Z_3(s)||\frac{1}{sC_{ds3}}) \tag{14}$$

In Equation (14), g_{m3} is the transconductance of the third-stage transistor. C_{ds3} is the parasitic capacitance of M_3; the drain-to-source resistance is also neglected. Z_3(s) has two pole p_{31} and p_{32}:

$$p_{31} = 0 \tag{15}$$

$$p_{32} = -\frac{R_L}{L_7 + L_8} \tag{16}$$

The frequency distribution of the gain peak of the third-stage amplifier can be adjusted by changing the values of L_6, L_7, L_8, and C_6. The peak gain of the third stage is distributed at 29 GHz, achieving a wide-band and flat gain together with the first two stages. Through simulation, it is determined that L_6, L_7, and L_8 are 0.18 nH, 0.4 nH, and 0.04 nH, respectively. The parasitic inductance of the back hole is also considered, and C_6 is 0.25 pF.

Based on the above analysis, the value of each component is determined. Figure 9 shows each stage's simulated power gain. Through careful design, the peak gains of the first and third stages are distributed at 29 GHz, and the peak gain of the second stage is distributed at 39 GHz. The proposed LNA achieves a very flat gain in the target frequency band owing to the dual-frequency stagger tuning technique.

3. Experimental Results

The Ka-band LNA was implemented in a 0.15 μm GaAs pHEMT technology with a substrate thickness of 100 μm. Figure 11 shows the micrograph of the chip, and it has a total area of 1.5 × 0.9 mm^2, including all the test pads. The LNA draws 17 mA from the supply at a V_{DD} of 3.3 V.

Figure 12 shows the measured and simulated S-parameters of the proposed Ka-band LNA with flat gain. It exhibits a typical small signal gain of 21.5 dB, and its gain flatness reaches ±0.3 dB in the frequency range of 32 to 40 GHz. There are slight differences between the simulated and measured results of S11 and S22, mainly manifested as frequency shift. Among them, S11 shifts about 2 GHz towards the high-frequency end, and S22 shifts about 3 GHz towards the high-frequency end, which is mainly caused by process fluctuations and parasitic factors. In addition, the reduction of the Q value also deteriorates S11, mainly because the simulator underestimates the parasitic resistance of components (transmission line, capacitor).

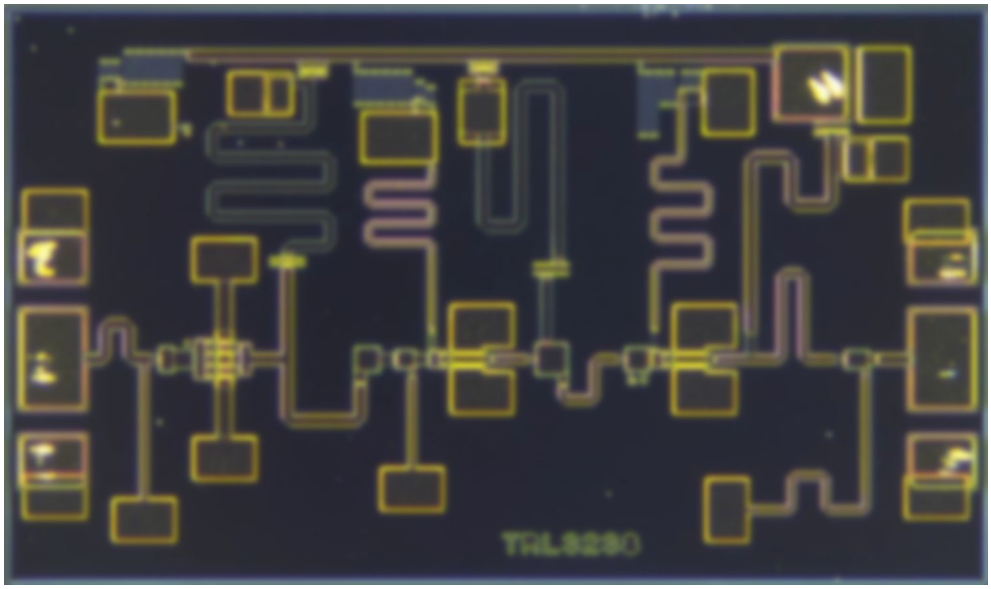

Figure 11. Micrograph of the chip.

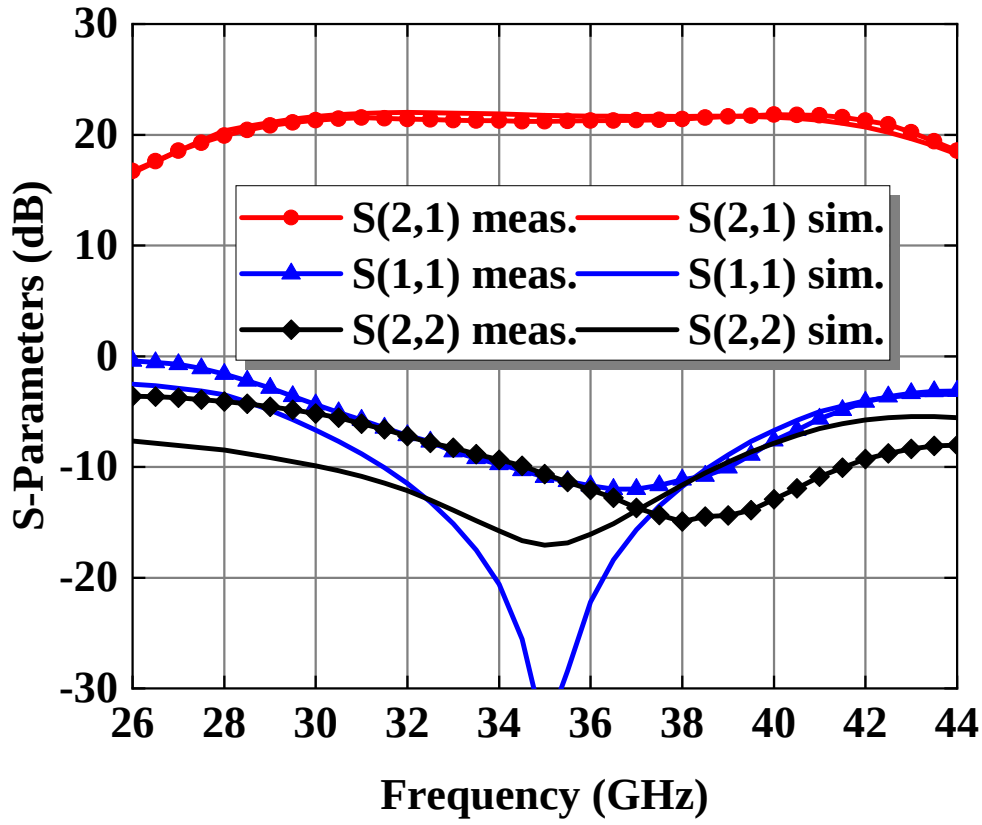

Figure 12. Simulated and measured S-parameters of the design.

The measured and simulated noise figure are given in Figure 13. The LNA achieves NF of 2–2.2 dB from 32 to 40 GHz. The output 1dB compression point (OP1dB) was measured in order to verify the linearity of the LNA, as shown in Figure 14. The LNA achieves an OP1dB of 4–12 dBm from 32 to 40 GHz, achieving high linearity with limited power consumption. The performance of the proposed wideband LNA is summarized and compared with the state-of-the-art mm-wave wideband LNAs in Table 1.

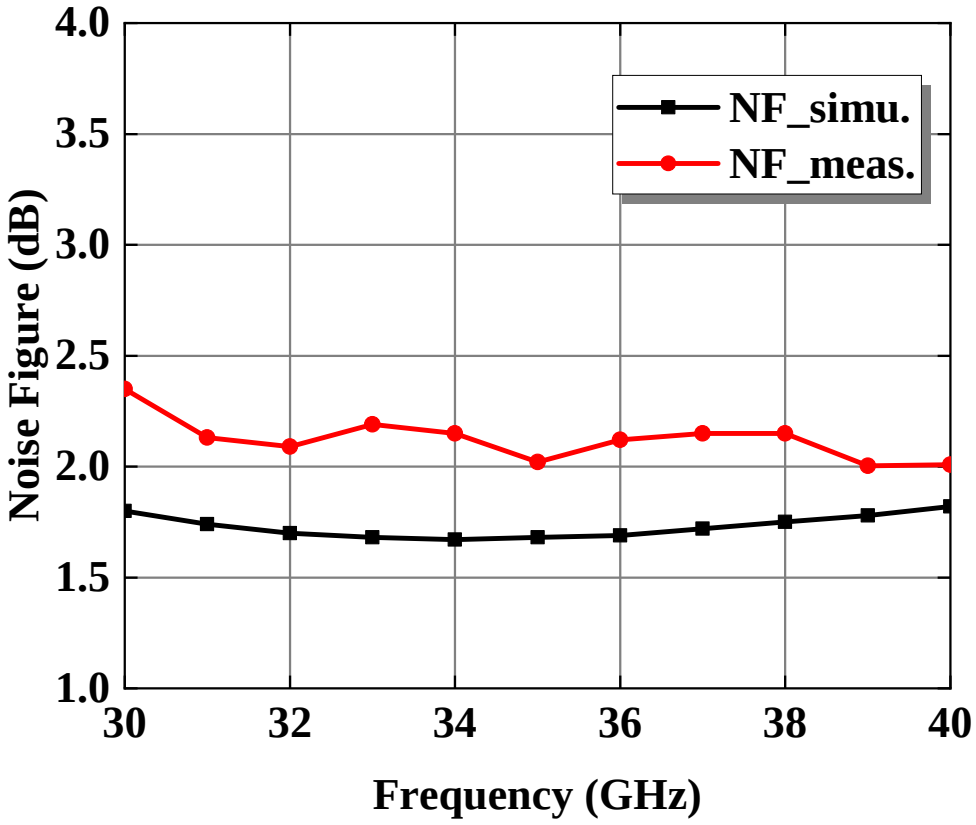

Figure 13. Simulated and measured noise figure.

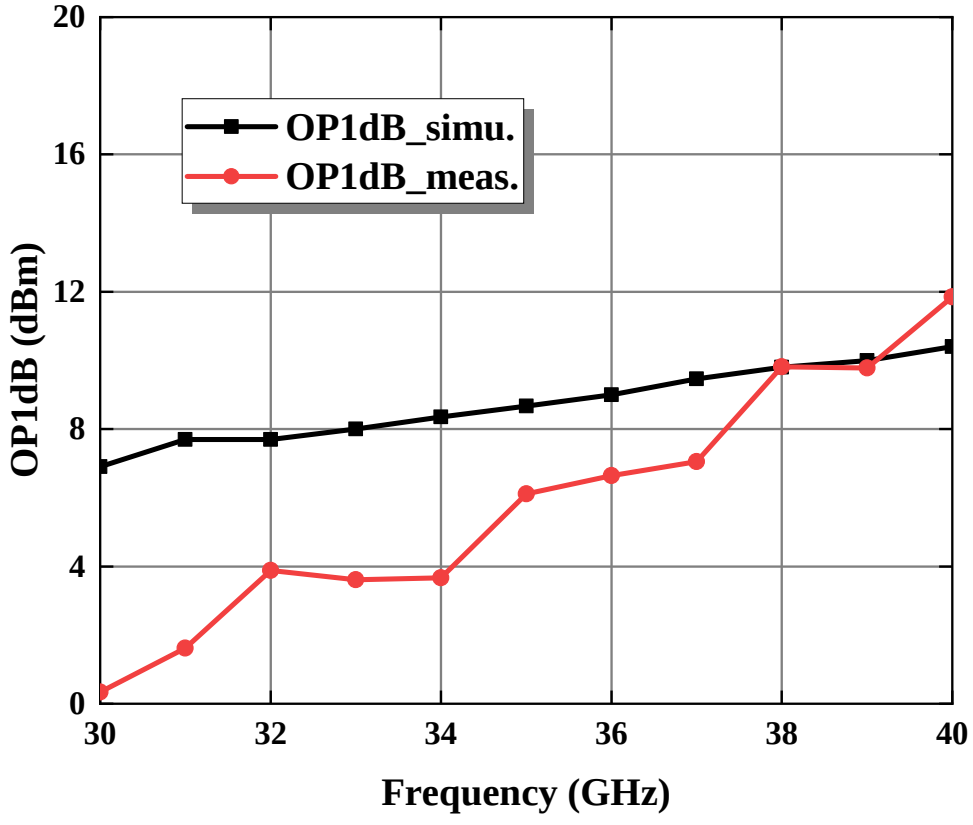

Figure 14. Simulated and measured output 1 dB compression point.

Table 1. Performance of broadband multistage LNAs.

Reference	This Work	[23]	[24]	[25]	[26]	[27]
Process	0.15-μm GaAs pHEMT	0.15-μm InGaAs pHEMT	0.15-μm GaAs pHEMT	0.15-μm GaAs pHEMT	0.15-μm GaAs pHEMT	0.1-μm GaAs pHEMT
Frequency (GHz)	32–40	29–43	25–40	22.5–34	28.5–50.5	18–43
Gain (dB)	21.5	14.2	20	22.5	23	21.6
Gain flatness (dB)	±0.3	NA	±1.5	±1.2	±1.5	±1.5
NF (dB)	2.2	2–3.3	2.8	3–4.5	3.8	1.8–2.7
Area (mm^2)	1.5 × 0.9	0.65 × 0.72	2.5 × 1.2	2.5 × 1	2 × 1.5	2 × 1
Power (mW)	56	38	230	36	62.6	140

4. Conclusions

A compact, low-power-consumption Ka-band LNA with gain flatness enhancement in a 0.15 μm GaAs pHEMT technology has been presented. The inductive degeneration technique was employed in order to achieve simultaneous input and noise matching. To enhance the gain flatness, the LNA adopts the stagger tuning technique. By distributing the peak gains at two different frequency points, a wide band and flat gain was obtained. The proposed LNA exhibits ±0.3 dB gain variation while maintaining a high gain of 21.5 dB. The noise figure is lower than 2.2 dB from 32 to 40 GHz. Moreover, it occupies only 1.5 × 0.9 mm^2 and consumes a DC power of 56 mW.

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