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Design of a Wide-Range and High-Precision Analog Front-End Circuit for Multi-Parameter Sensors

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Abstract: This article presents a wide-range and high-precision analog front-end circuit for multi-parameter sensors that can handle sensor outputs of different types (R, C, V). A rail-to-rail baseline compensation method has been proposed, which further incorporates a fine offset elimination of 0.6 mV/step. Additionally, self-zeroing and correlated double-sampling techniques are integrated to reduce low-frequency noise and offset, prevent sensor signal saturation, and enhance the precision of the analog front-end circuit. By incorporating variable components in the sensor signal acquisition circuit and integrating them with the baseline compensation circuit, the applicability range of the sensor has been expanded (R: 7 Ω–1.7 MΩ, C: 50 fF–35 pF, V: 0.05–1.7 V). Test results show all interface circuits exhibit significant total conversion gains (C: 45 mV/fF, R: 14.5 mV/Ω, V: 144 V/V), achieving high precision. Meanwhile, a coefficient of determination (R^2) greater than 0.998 indicates high conversion linearity of the circuit.

Keywords: sensor analog front-end; signal conditioning circuit; universality; switched-capacitor level shifter; offset cancellation

Citation: Yang, Y.; Li, Z.; Liu, M.; Liu, W.; Li, Z.; Hou, Y.; Liu, X.; Wang, X.; Liu, Y. Design of a Wide-Range and High-Precision Analog Front-End Circuit for Multi-Parameter Sensors. *Electronics* **2023**, *12*, 2962. https://doi.org/10.3390/electronics12132962

Academic Editor: Djuradj Budimir

Received: 7 June 2023
Revised: 30 June 2023
Accepted: 30 June 2023
Published: 5 July 2023

1. Introduction

With the rapid development of the internet of things, electronic systems centered around sensors have found wide applications in various domains such as environmental monitoring [1], healthcare [2], and smart cities [3]. The analog front-end circuit plays a vital role in sensor application systems, serving as a bridge between sensors and digital systems. It converts signals from various types of sensors (resistive/capacitive/voltage/current) [4,5] into voltage signals, which are then amplified and transmitted [6,7]. In the quest for developing sensor application systems, numerous configurations have been employed for the analog front-end circuit. Most of these configurations are tailored for specific sensors, designed to meet a limited set of requirements precisely to achieve high performance. However, as the number of emerging sensor types rapidly increases, the development time and costs of dedicated sensor-specific analog front-end circuits have significantly escalated. Therefore, the design of a versatile analog front-end circuit capable of accommodating multiple sensor types is highly necessary.

Designing a universally applicable analog front-end circuit poses two crucial challenges. Firstly, sensor signals exhibit extremely weak variations. For instance, recently proposed sensors made of flexible materials such as liquid metal demonstrate their potential for detecting human motion through wearable resistive strain sensors, where the change

in resistance is less than 1 Ω when the finger bends [8]. Similarly, the output voltage of the wearable tactile sensor varies by only a few millivolts with changes in contact force [9]. Furthermore, an all-flexible tactile sensor described in [10] has a capacitance range of 9.3 pF–13 pF, with a minimum capacitance variation of 0.4 pF. Therefore, the analog front-end circuit needs to possess high conversion gain and precision while maintaining a wide range of applicability. However, existing general-purpose electronic interface approaches have certain drawbacks. The analog front-end circuit described in [11] provides a wide range of 350 pF for capacitive sensors but suffers from low precision due to a detection step of 20 pF. The analog front-end circuit in [12] has a limited detection range of 0.5–4.5 kΩ for resistive sensors. The resistive sensor measurement circuit proposed in [13] achieves a wide range of 20 kΩ–1.1 MΩ. However, it comes at the cost of high power consumption, amounting to 195 mW. Moreover, the analog front-end circuit presented in [14] can be used for both resistive and capacitive sensors but incurs a high power consumption of 2.88 mW under high-precision mode.

Secondly, due to the diverse sensor types, the baseline values of the acquired electrical signals differ significantly, which can lead to amplifier saturation and signal loss. Therefore, wide-range compensation of the baseline is necessary. Traditional sensor baseline compensation methods, such as the one proposed in [15], utilize variable resistance structures as reference resistors and determine the compensation value through negative feedback loops. However, the limited nonlinear range of operational amplifiers severely restricts the compensation range (5–110 kΩ). In [16], a method based on the current compensation technique is proposed, which includes a current self-compensator and an improved current steering digital-to-analog converter (DAC). This approach offers lower power consumption, but the compensable range is limited to only 100 mV. The method proposed in [17] uses a capacitor array to compensate for baseline voltage. The maximum compensation range achievable with a 3 V power supply voltage is limited to ±350 mV, indicating a relatively small compensation range. These methods are customized for specific sensor types and are inefficient when applied to a universal analog front-end circuit. Another proposed method, in [18], incorporates a digital filtering structure into the amplifier section, which exhibits universality. However, it is greatly influenced by the common-mode range of the input stage bias, making it challenging to achieve considering process, voltage, and temperature variations.

In summary, the existing analog front-end circuits are primarily tailored for specific sensors, neglecting the simultaneous consideration of detection range and precision [19–22]. The baseline compensation circuits are relatively limited and offer a narrow range of compensation [23]. Therefore, this paper proposes the design of a universal analog front-end circuit that achieves a wide compensation range for rail-to-rail voltage. It offers a wide measurement range and high precision, making it suitable for multiple types of sensors. The design is based on a switchable capacitor structure that is relatively universal and easy to implement. The main sections of this article are as follows: Section 2 introduces the proposed sensor analog front-end and its working principles. Section 3 includes the test results and discussions. Section 4 presents the conclusion.

2. Circuit Implementation

Figure 1 illustrates the overall system diagram of the proposed sensor interface analog front-end circuit in this article. The sensor signal acquisition circuit consists of capacitance, resistance, and voltage signal acquisition circuits. The corresponding acquisition method is selected based on the type of sensor, and an initial signal is controlled to be connected to the subsequent circuitry using switches. The acquired voltage signal is processed in the baseline compensation circuit, where a comparator, digital calibration circuit, and DAC are used to position the small signal around the mid-rail. The difference between the sensor signal and the mid-rail voltage represents the signal variation of the sensor. Since the digital calibration circuit introduces an error equal to the DAC resolution due to the level shift controlled by the DAC, an offset cancellation circuit is required to balance the input

differential signal and further reduce the offset to a negligible level. Finally, the signal amplification circuit amplifies the processed analog signal for subsequent analog-to-digital conversion. The waveform of the entire signal processing process is shown in Figure 2.

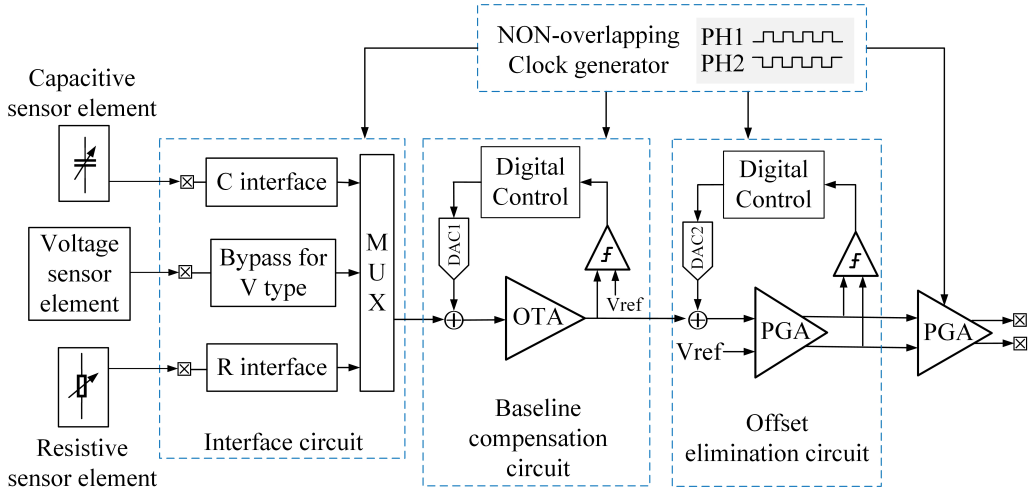


Figure 1. Overall diagram of the proposed system.

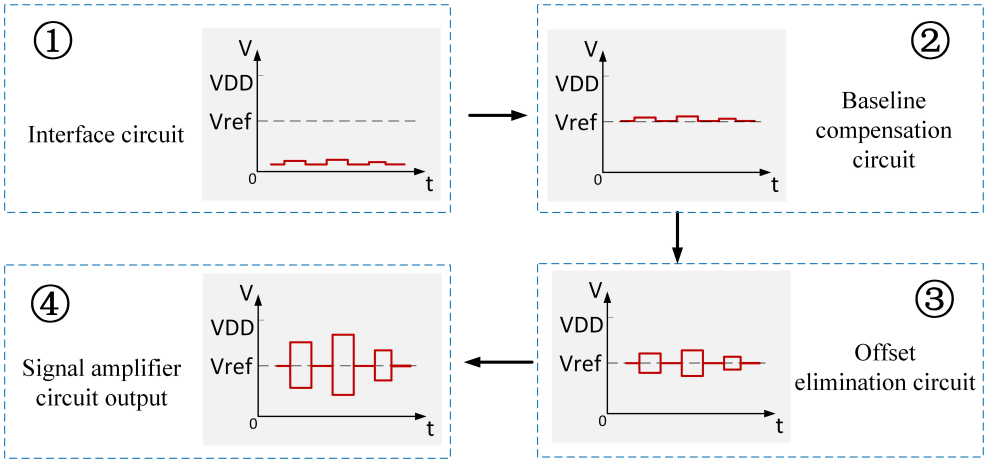


Figure 2. Waveforms during signal processing.

The baseline compensation and offset elimination are accomplished with digital circuit assistance and remain unchanged until a new reset signal arrives. Given that most sensor applications such as temperature, pressure, humidity, etc., exhibit gradual signal changes that can be regarded as direct current (DC) quantities, this persistence is reasonable. Throughout the entire implementation process, we have employed classic complementary metal oxide semiconductor (CMOS) switches and ensured that the values of the capacitors used are not too small (>0.9 pF) to mitigate charge injection and clock feedthrough effects.

2.1. Sensor Interface Circuit

The capacitance-type interface selects a switched-capacitor integrator structure, as this structure possesses a higher degree of conversion linearity, fewer parasitic effects, and a greater conversion gain than a capacitance-frequency converter or bridge circuit [24]. As shown in Figure 3, the circuit operates under the two-phase clock, proportionally transforming the capacitance of the sensor, C_{sen}, into the sampled voltage, V_{out}. During the PH1 phase, C_f is reset, and a charge, $Q_{sen} = (V_{DD} - V_{ref})C_{sen}$, is sampled in C_{sen}, while a charge, $Q_{ref} = -V_{ref}\ C_{ref}$, is sampled in C_{ref}. During the PH2 phase, a charge, $Q_{sen} = -V_{ref}\ C_{sen}$, is sampled in C_{sen}, and a charge, $Q_{ref} = (V_{DD} - V_{ref})C_{ref}$, is sampled in

C_{ref}, with conservation of charge at the inverting input node of the amplifier. The difference of the two-phase sampled charges is transmitted in C_f, resulting in the output voltage.

$$V_{out} = V_{ref} + \frac{\left(C_{sen} - C_{ref}\right) \times V_{DD}}{C_f} \tag{1}$$

From the above formula, the value of C_{sen} can be deduced.

$$C_{sen} = -\frac{C_f}{V_{ref}} \times V_{out} + C_f + C_{ref} \tag{2}$$

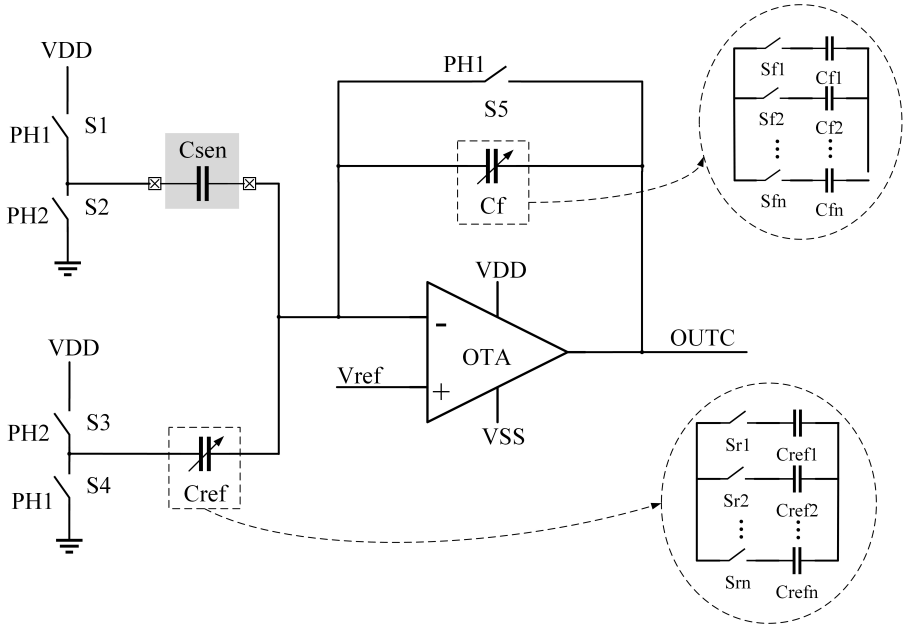


Figure 3. Capacitive sensor acquisition circuit.

In substituting values into Equation (2), the permitted output voltage range $V_{out} = [V_{min}, V_{max}]$ can be obtained when given values of C_f and C_{ref}. By designing C_f and C_{ref} as variables, appropriate values can be selected according to the current requirement, thereby expanding the capacitance range that can be sensed by the circuit.

The operational transconductance amplifier (OTA) in the circuit utilizes a classic seven-transistor structure, as illustrated in Figure 4.

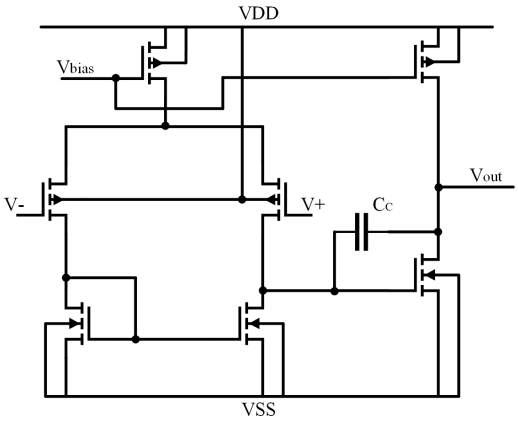


Figure 4. Acquisition circuit of resistance sensor.

For the resistance-type sensor interface, we employed a variable current source with sufficiently high output impedance, as depicted in Figure 5, injecting current into the under-test resistance-type sensor and the resulting measurement voltage value is OUTR = IR_{sen}.

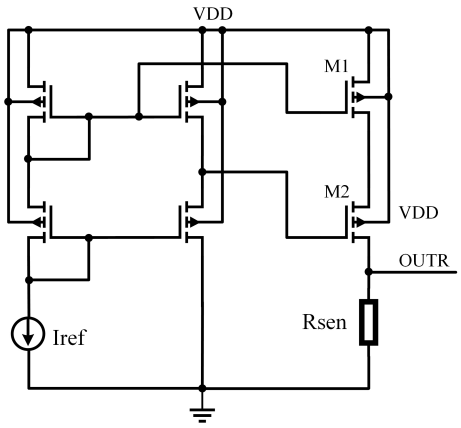


Figure 5. Acquisition circuit of resistance sensor.

The reference current source (I_{ref}) adopts a self-biased configuration, robust against the power voltage and temperature, and the output impedance is enhanced by cascode current mirrors [25]. The widths of M1, M2, and the cascode current mirrors control the current injected into the sensor.

RC sensors are first converted into voltage signals by the corresponding interface circuit, and the subsequent signal acquisition circuit in Figure 1 can directly handle the voltage signals. Thus, voltage-type signals can directly be connected to the parallel capacitance group of the baseline compensation circuit.

It is important to note that parasitic capacitance in the input can degrade the noise performance, especially during the output acquisition of RC-type sensors [26,27]. In the case of V-type sensor output acquisition, the impact of the input parasitic capacitance on the noise performance is negligible [26].

2.2. Baseline Compensation Circuit

This article employs a pre-compensation approach, utilizing a common compensation circuit for the output of various types of sensors, thus being more efficient in terms of area and cost. It consists of a comparator, selector, an 8-bit counter, an 8-bit memory, a 6–64 bit encoder, a 2–4 bit encoder, a 6-bit DAC, four parallel capacitors, and an operational amplifier. The circuit is controlled by two non-overlapping clock phases PH1 and PH2.

The level shifter based on switch capacitors can change the voltage level simply using serial capacitors. Furthermore, this structure is not impacted by the threshold voltage requirements of traditional level shifters [28]. The level shifter utilized in this article connects to four parallel capacitors via a DAC, positioning variously distributed sensor signals to the mid-rail voltage. The DAC is based on RC interpolation [29], and the interpolated parallel capacitor groups also serve as level-shifting capacitors. Figure 6 shows the overall structure and detailed process of the level shifter. During the PH1 phase, the 6-bit R-DAC charges four capacitors, and the level of the switch-controlled connection is V_H or V_L. V_H is the analog output value of the 6-bit DAC, and V_L is one resolution smaller than V_H. During the PH2 phase, the four capacitors are paralleled, leading to a 2-bit interpolation between V_H and V_L, thus realizing a total of 8-bit DAC. The level on the paralleled capacitor group is

$$V_{DAC} = V_L + \frac{n}{4}(V_H - V_L), (n = 0, 1, 2, 3) \quad (3)$$

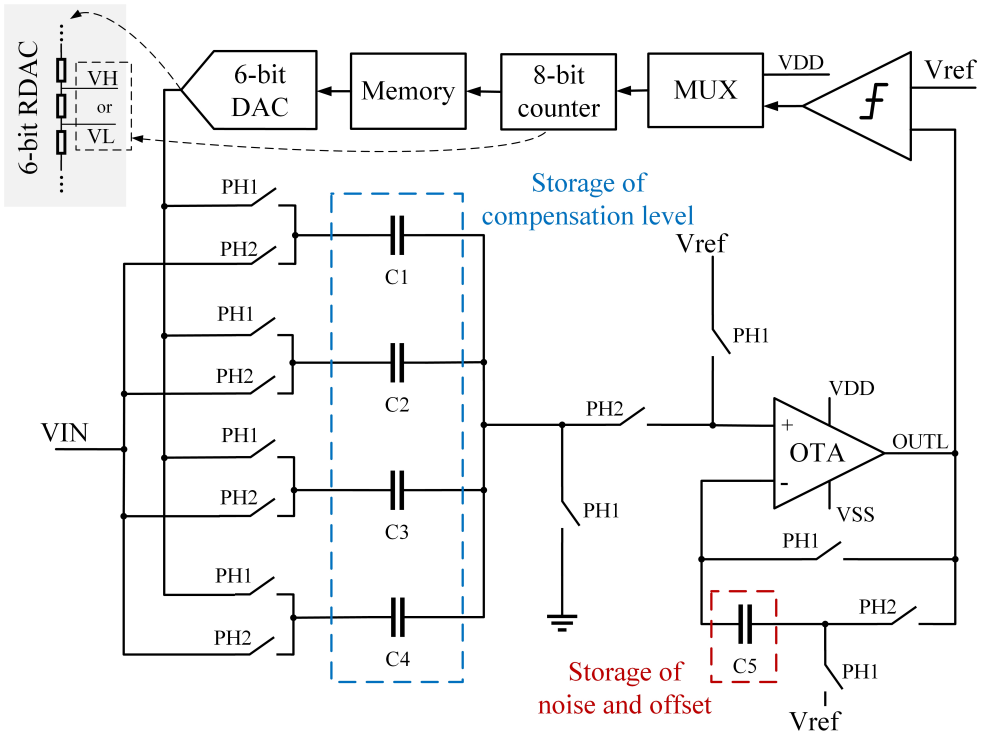


Figure 6. The implementation of a baseline compensation circuit.

Through the aforementioned process, the four paralleled capacitors can be charged to the full scale of an 8-bit DAC.

By connecting four capacitors in parallel and placing them in series at the input end, a level shift from 0 to the range of V_{DD} can be achieved. This shifted level, OUTL, is compared to the mid-rail level, V_{ref}, by the comparator. If OUTL is greater than V_{ref}, the counter begins counting and records the value in the memory while the DAC outputs the corresponding analog quantity onto the capacitor group. This process is repeated until OUTL is equal to V_{ref}, at which point the counter ceases counting and saves the current count value in the memory. The DAC output remains at the current analog quantity, completing the operation of shifting the sensor level to the mid-rail level. The direction of the level shift, either upward or downward, is determined by the charging direction of the capacitors by V_{DAC}. The amplifier section employs self-zeroing technology, where noise is sampled in the feedback capacitor in PH1 and nullified in PH2 to produce the output.

It should be noted that the noise and offset of the comparator in this circuit have a significant impact on the effectiveness of the baseline compensation. Therefore, a low-pass filter can be added at the input stage of the comparator to avoid errors in comparison results caused by rising-edge spikes. Additionally, the use of positive channel metal oxide semiconductor (PMOS) input pairs with large gate areas reduces offset and flickering noise in both the amplifier and comparator.

2.3. Offset Elimination Circuit

The level-shifting capacitor is charged using an 8-bit DAC, which limits the minimum voltage step that the level shifter can achieve. In this article, a 1.8 V power supply voltage is used, corresponding to a resolution of 7 mV for the 8-bit DAC. This means that even though the level shifter positions the signal near the mid-rail voltage, there may still be a relatively large offset of the effective signal. This amount still does not allow the amplifier to have a large gain. Therefore, to attain a greater gain while avoiding saturation, a more precise offset elimination is necessary.

We adopted a balancing technique to perform delicate offset compensation using a low-resolution DAC. As depicted in Figure 7, a 6-bit R-DAC is connected to the capacitor C_4, whose capacitance is less than the total capacitance at the right-side summing node, C_{total}. Due to the voltage division between C_1 and C_{total}, the output of the DAC influences the output level of the amplifier. The comparator checks whether the differential output level of the amplifier is balanced. If not, the counter is controlled to increase, elevating the output of the DAC until the differential output level is balanced, thus improving the resolution.

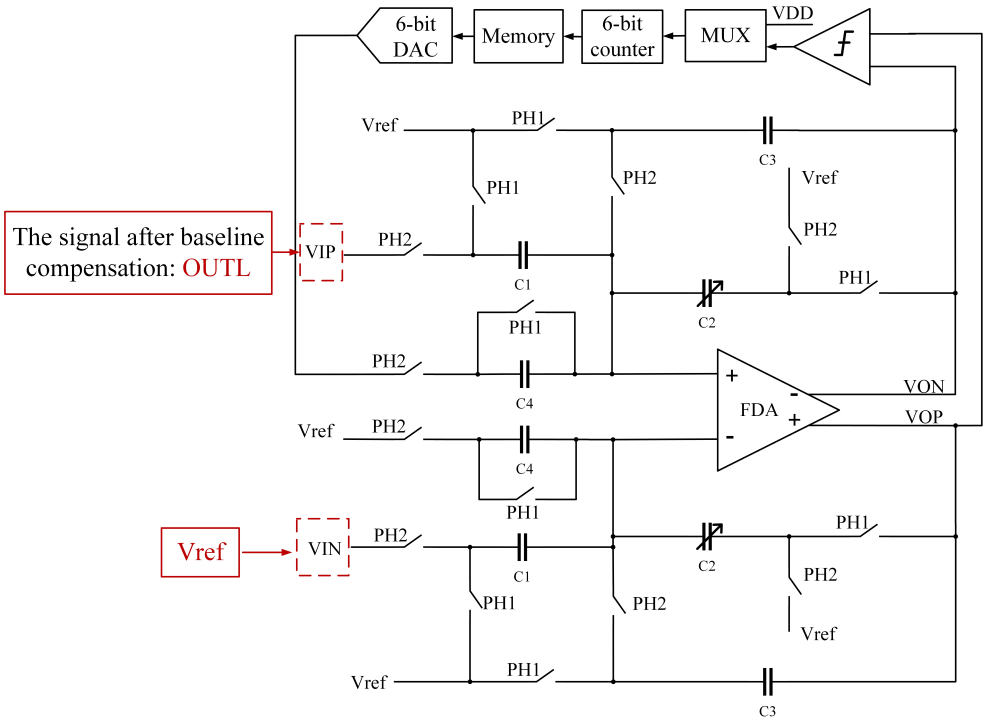


Figure 7. The implementation of an offset elimination circuit.

The structure of the offset cancellation circuit in two phases is depicted in Figure 8. The capacitor C_4 stores the DAC output voltage during the PH1 phase and discharges its charge during the PH2 phase. All capacitors are charged and discharged in two phases, satisfying the principle of charge conservation [30]. The input and output of the circuit can be decomposed into a differential mode signal and common mode signal, represented by the input voltages V_{Icm} and V_{Id}, and the output voltages V_{Ocm} and V_{Od}, respectively. Let V_X denote the ideal voltage at the input terminals of the operational amplifier at nodes A and B. First, let us analyze the charge on the capacitors in the PH1 phase, which can be expressed as

$$Q_{1A}(PH1) = C_1(V_{Icm} + V_{Id} - V_X(PH1)) \quad (4)$$
$$Q_{2A}(PH1) = C_2(V_X(PH1) - V_{ref}) \quad (5)$$
$$Q_{3A}(PH1) = C_3(V_{Ocm} + V_{Od}(PH1) - V_X(PH1)) \quad (6)$$
$$Q_{4A}(PH1) = C_4(V_{ref} - V_X(PH1)) \quad (7)$$

and, respectively,

$$Q_{1B}(PH1) = C_1(V_{Icm} - V_{Id} - V_X(PH1)) \quad (8)$$
$$Q_{2B}(PH1) = C_2(V_X(PH1) - V_{ref}) \quad (9)$$
$$Q_{3B}(PH1) = C_3(V_{Ocm} - V_{Od}(PH1) - V_X(PH1)) \quad (10)$$
$$Q_{4B}(PH1) = C_4(V_{DAC} - V_X(PH1)) \quad (11)$$

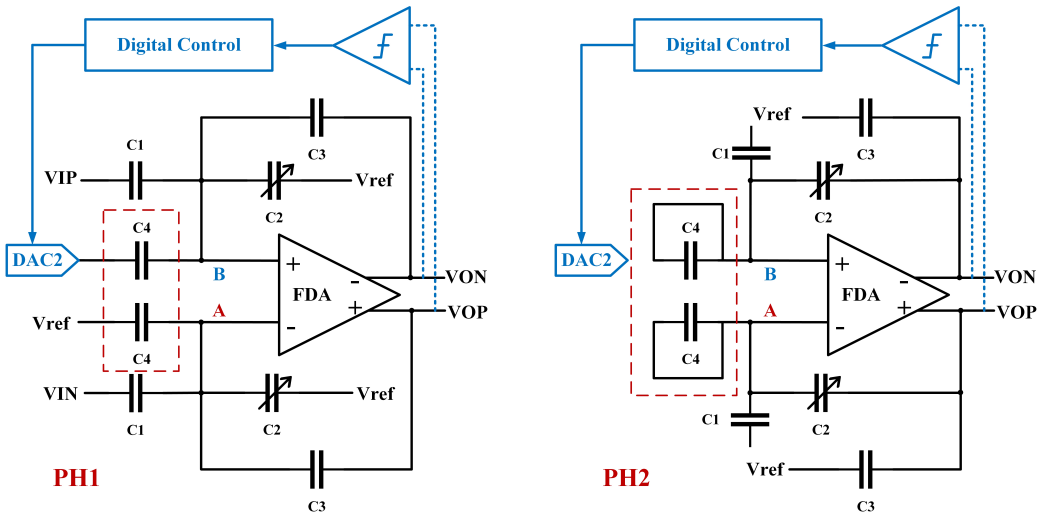


Figure 8. Offset cancellation circuit operating in two phases.

The charge on each capacitor in the PH2 phase

$$Q_{1A}(PH2) = C_1(V_{ref} - V_X(PH2)) \tag{12}$$
$$Q_{2A}(PH2) = C_2(V_X(PH2) - V_{Ocm} - V_Od(PH2)) \tag{13}$$
$$Q_{3A}(PH2) = C_3(V_{Ocm} + V_{Od}(PH2) - V_{ref}) \tag{14}$$
$$Q_{4A}(PH2) = 0 \tag{15}$$

and, respectively,

$$Q_{1B}(PH2) = C_1(V_{ref} - V_X(PH2)) \tag{16}$$
$$Q_{2B}(PH2) = C_2(V_X(PH2) - V_{Ocm} + V_Od(PH2)) \tag{17}$$
$$Q_{3B}(PH2) = C_3(V_{Ocm} - V_{Od}(PH2) - V_{ref}) \tag{18}$$
$$Q_{4B}(PH2) = 0 \tag{19}$$

When analyzing charge transfer, the polarity of the capacitors must also be considered. The polarities of all of the capacitors are shown in Figure 8. In both phases, nodes A and B, which are connected to the input of the operational amplifier, are assumed to have no current flowing through them, as the MOS transistors at the input stage act as high-impedance nodes. Based on the analysis above, it can be concluded that the total charge at nodes A and B remains constant.

When the phase changes from PH1 to PH2, node A remains connected to C_1, C_2, C_4, and the input terminal of the amplifier. The total charge stored in C_1, C_2, and C_4 remains constant, hence $\Delta Q_{1A} + \Delta Q_{4A} = \Delta Q_{2A}$. Similarly, at node B, we have $\Delta Q_{1B} + \Delta Q_{4B} = \Delta Q_{2B}$.

When the phase changes from PH2 to PH1, node A is connected to C_1, C_2, C_3, C_4, and the input terminal of the amplifier. The total charge stored on all capacitors remains constant. Based on the above analysis, it is evident that the charge on C_1, C_2, and C_4 remains constant, thus the charge on C_3 is constant, $\Delta Q_{3A} = 0$. Similarly, $\Delta Q_{3B} = 0$.

The aforementioned charge transfer process can be represented by the following equations:

$$Q_{1A}(PH1) - Q_{1A}(PH2) + Q_{4A}(PH1) - Q_{4A}(PH2) = Q_{2A}(PH1) - Q_{2A}(PH2) \tag{20}$$
$$Q_{1B}(PH1) - Q_{1B}(PH2) + Q_{4B}(PH1) - Q_{4B}(PH2) = Q_{2B}(PH1) - Q_{2B}(PH2) \tag{21}$$
$$Q_{3A}(PH1) - Q_{3A}(PH2) = 0 \tag{22}$$
$$Q_{3B}(PH1) - Q_{3B}(PH2) = 0 \tag{23}$$

By substituting Equations (4)–(19) into Equations (20)–(23), we can obtain

$$V_{od} = \frac{C_4}{2C_1} \cdot (V_{\text{dac}} - V_{\text{ref}}) + \frac{C_1}{C_2} \cdot V_{Id} \tag{24}$$

Based on the chosen values of the capacitors, the offset adjustment step is determined to be 0.6 mV, which corresponds to 1/47 of the 6-bit DAC resolution. Through this approach, the offset is effectively eliminated.

2.4. Signal Amplification Circuit

After compensating for baseline and eliminating the offset, the small signals located around the mid-rail voltage meet the signal requirements at the input end of the operational amplifier. The detection precision of the interface circuit can be improved and the signal will not be saturated and distorted by selecting the proper amplification factor. Hence, the amplifier circuit adopts a variable gain amplifier, using a tunable capacitance array to control the amplification factor of the circuit. The amplification factor is controlled by a switch array, as shown in Figure 9, where C_1 is 10.8 pF and C_2 ranges from 0.9 pF to 10.8 pF.

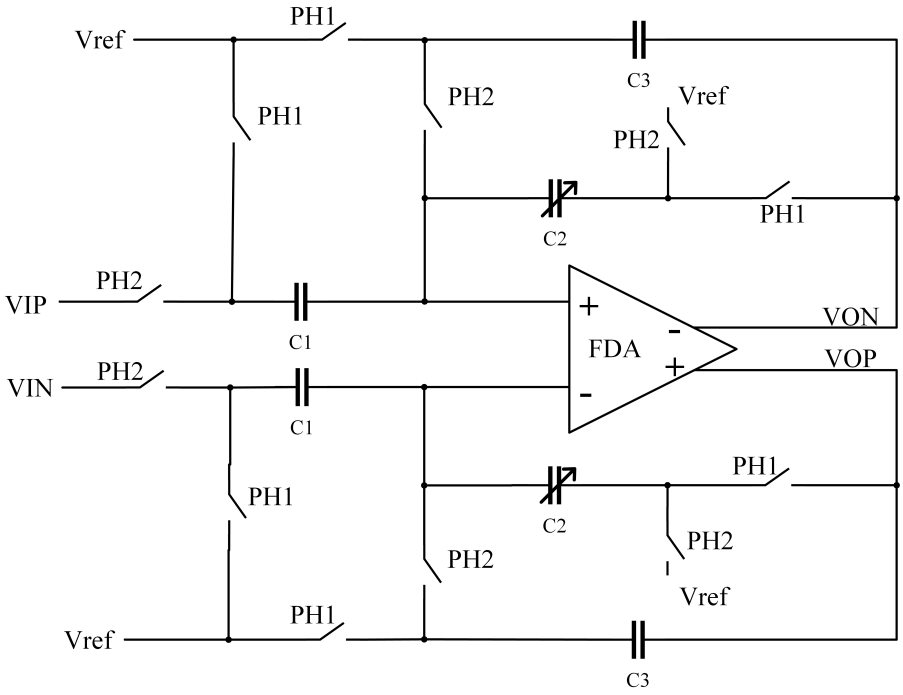


Figure 9. Signal amplification circuit.

The amplifiers used in the offset cancellation circuit and signal amplification circuit are universal amplifiers for all C-V/R-V conversion sensor signals and direct voltage input interfaces. We use a fully differential amplifier (FDA) because it can suppress common mode noise such as 60 Hz power frequency interference and has a larger output swing range under the same gain conditions compared to single-ended output structures. The FDA is a two-stage amplifier, with the first stage utilizing a folded cascode amplifier configuration and the second stage being a common-source amplifier, as illustrated in Figure 10. In addition, related correlated double sampling (CDS) technology can be used in the FDA to greatly reduce the flicker noise and mismatch of the amplifier.

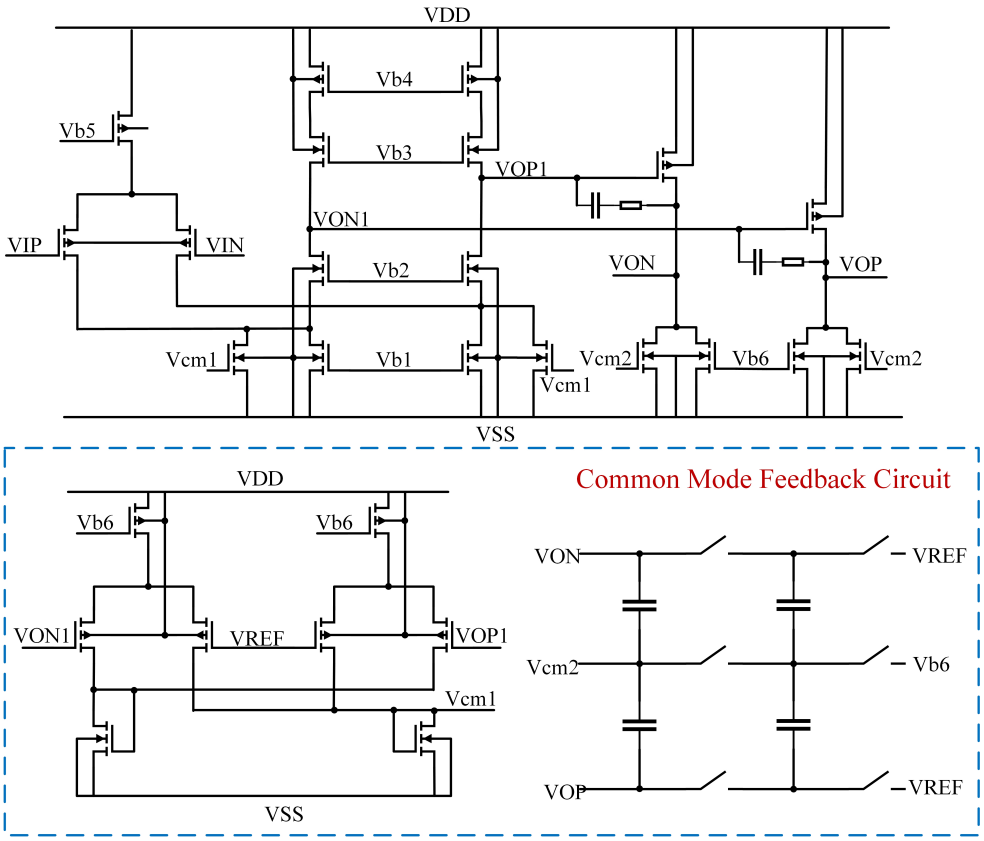


Figure 10. Circuit structure diagram of the FDA.

The circuit structure of the signal amplification circuit in two phases is shown in Figure 11, where (a) represents the input sampling phase PH1, (b) represents the amplification phase PH2, and V_{OS} represents the offset and noise effectively present at the input terminals. The circuit structure is similar to that described in Section 2.3, and the analysis of charge transfer has already been discussed.

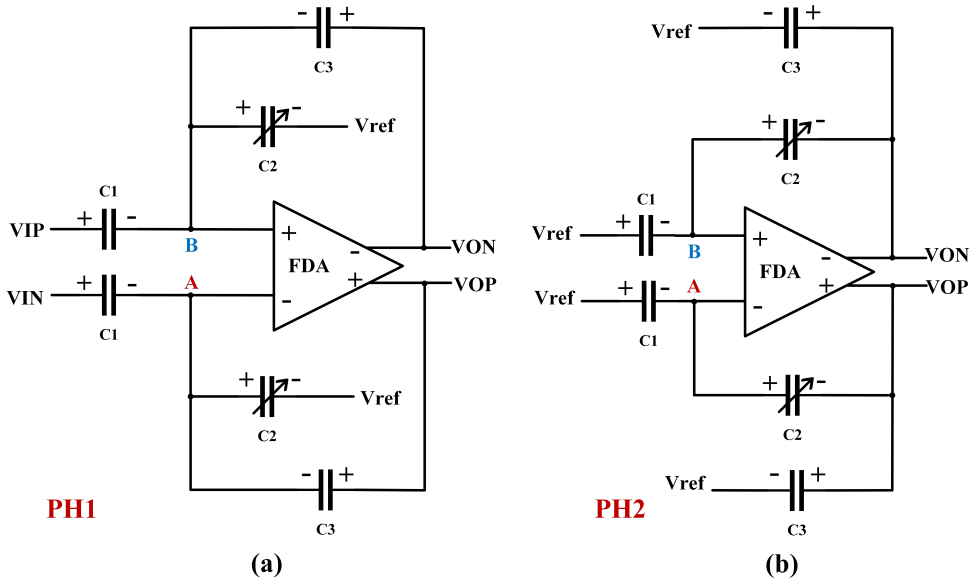


Figure 11. Signal amplification circuit operating in two phases.

In this section, we take into account the amplifier's offset and noise. By considering the voltage at nodes A and B as $V_X \pm V_{OS}/2$, and substituting it into Equations (4)–(19), we can obtain

$$\begin{aligned} &C_1(V_{Icm} + V_{Id} - V_X(PH1) - V_{OS}/2 - V_{ref} + V_X(PH2) + V_{OS}/2) \\ &= C_2(V_X(PH1) + V_{OS}/2 - V_{ref} - V_X(PH2) - V_{OS}/2 + V_{Ocm} + V_O d(PH2)) \end{aligned} \quad (25)$$

$$\begin{aligned} &C_1(V_{Icm} - V_{Id} - V_X(PH1) + V_{OS}/2 - V_{ref} + V_X(PH2) - V_{OS}/2) \\ &= C_2(V_X(PH1) - V_{OS}/2 - V_{ref} - V_X(PH2) + V_{OS}/2 + V_{Ocm} - V_O d(PH2)) \end{aligned} \quad (26)$$

By analyzing Equations (25) and (26), it can be observed that the offset and noise V_{OS} of the operational amplifier is canceled at the output terminal. By subtracting Equation (26) from Equation (25), we can obtain the relationship between the output voltage and the input voltage as $V_{Od} = \frac{C_1}{C_2} \cdot V_{Id}$.

Transient simulations were conducted on the circuit before and after applying CDS technology, and the resulting noise power spectral density is depicted in Figure 12. It can be observed that the low-frequency noise is significantly suppressed. Through Monte Carlo simulations, it was determined that the offset of the operational amplifier has a 3σ value of 7.8 mV. To simulate the offset, a DC signal of 7.8 mV was applied at one of the input terminals of the amplifier. After applying CDS and conducting transient simulations, the offset at the output terminal of the op-amp was found to be 0.18 mV. These simulation results validate the previous analysis.

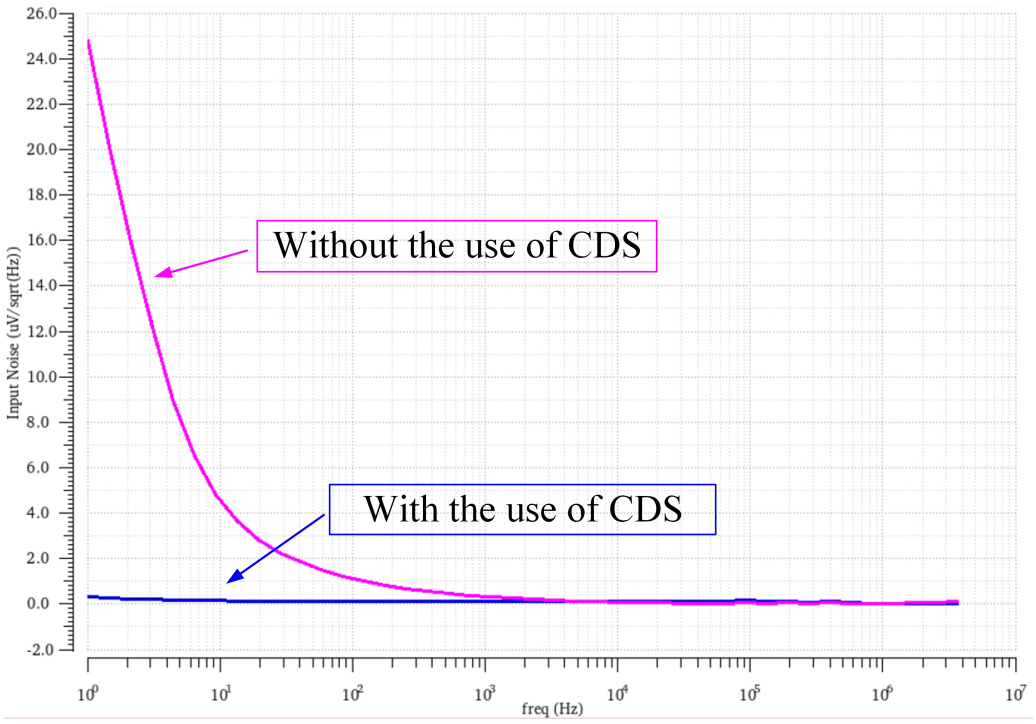


Figure 12. Power spectra of noise with and without CDS.

3. Measurement Result

Transient simulations were performed on the circuit under SS, TT, and FF process corners at temperatures of −40 °C, 25 °C, and 85 °C, respectively. Standard capacitors, resistors, and voltage sources were used as the sensors. The overall functionality of the circuit under three different measurement modes is simulated and illustrated in Figures 13–15. The waveforms on the graph represent the output differential signal of the final stage differential amplifier corresponding to capacitance values of 18.5 pF, 19.5 pF, and 20.06 pF, resistance values of 7 Ω, 7.15 Ω, and 7.3 Ω, and voltage values of 300 mV, 290 mV, 280 mV, 270 mV,

and 260 mV. It can be observed that the circuit exhibits favorable process and temperature characteristics.

The chip presented in this article is manufactured using a 0.18 µm CMOS process, with a total effective area of 0.9 mm^2, and consumes approximately 600 µA of current. A photograph of the chip's interface is shown in Figure 16. By utilizing the same analog front-end circuit to process signals instead of using the R/C/V sensor interface circuits to handle them individually, a 42% reduction in current consumption can be achieved, reducing it from 1040 µA to 600 µA, as the current consumption of a core amplifier is approximately 110 µA.

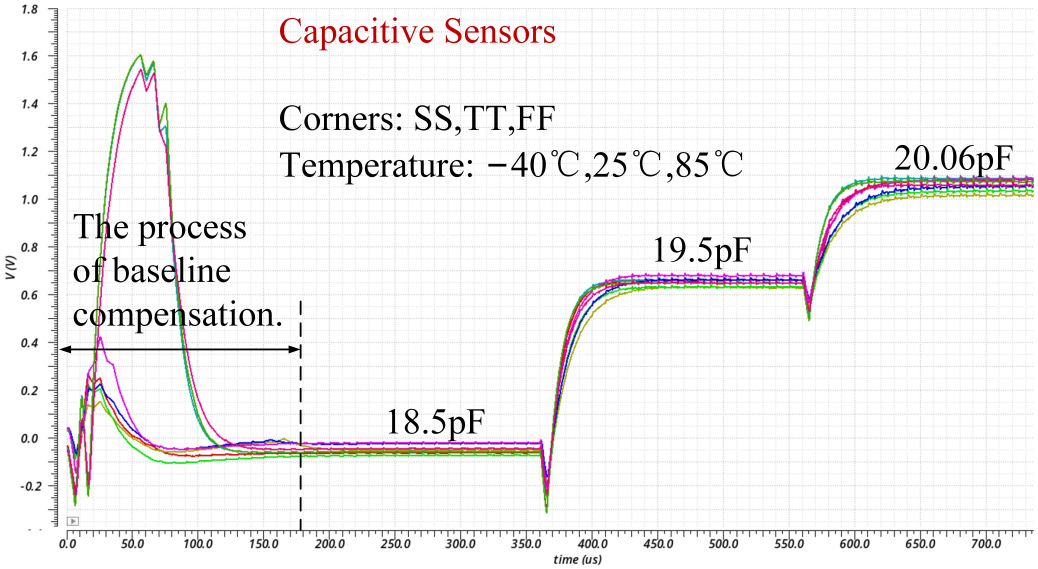


Figure 13. Transient simulation results for capacitive sensors.

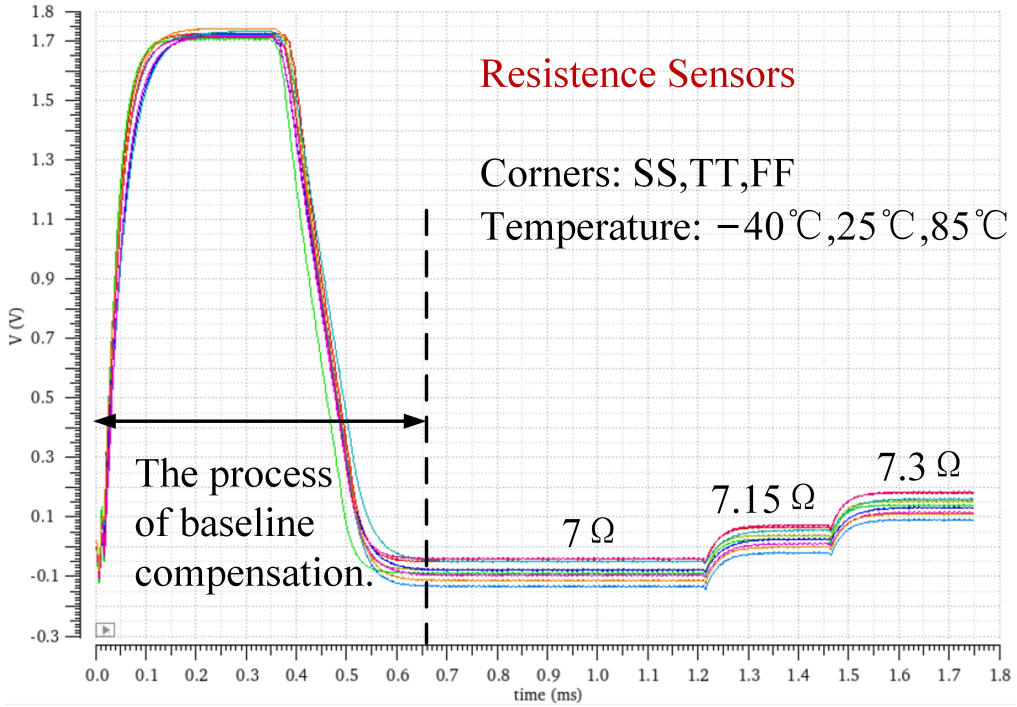


Figure 14. Transient simulation results for resistance sensors.

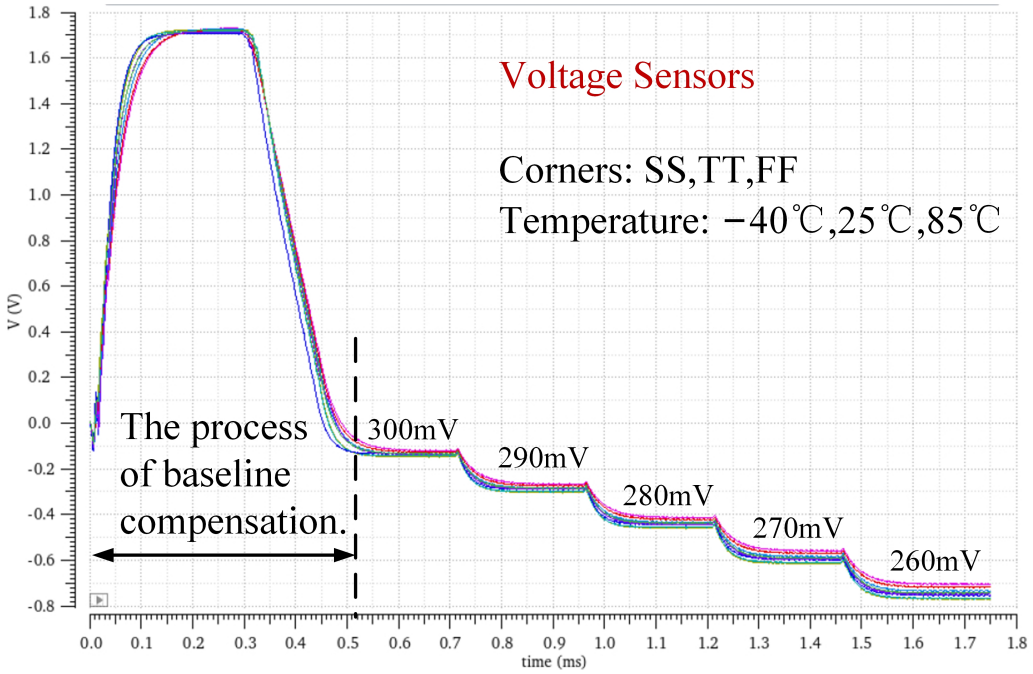


Figure 15. Transient simulation results for voltage-type sensors.

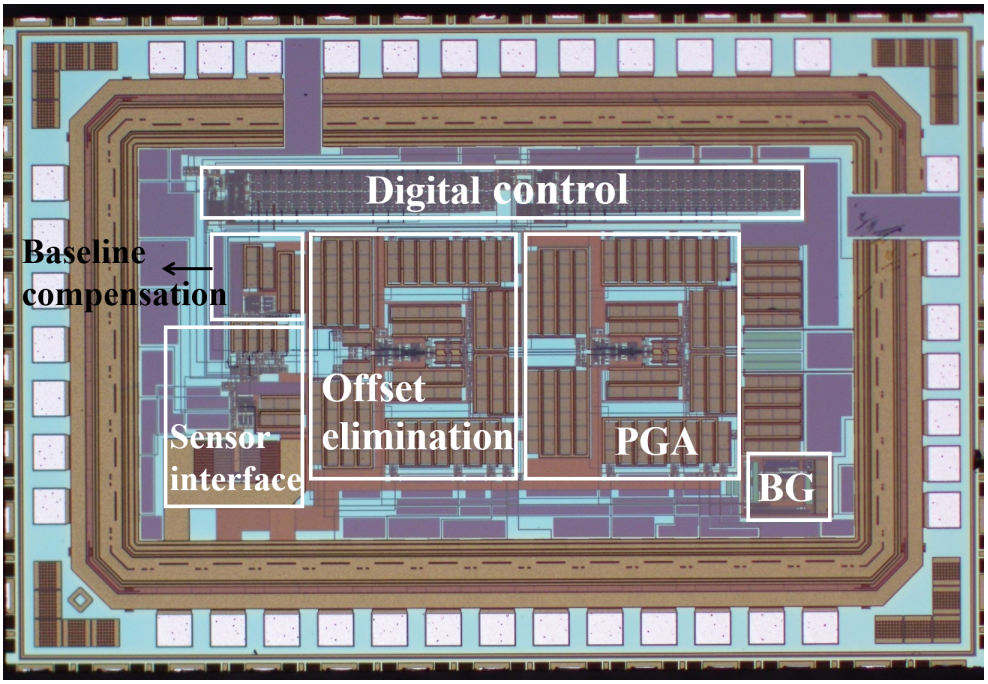


Figure 16. Microphotograph of designed analog front-end.

The environment of the test and the photo of the test printed circuit board (PCB) are shown in Figure 17. Standard capacitors and resistors are placed on the PCB board to simulate the variations of the sensor. An oscilloscope is used to observe the waveforms at various output points of the circuit system. A DC power supply provides a power voltage of 1.8 V, while a signal generator generates a 100 kHz square wave clock signal.

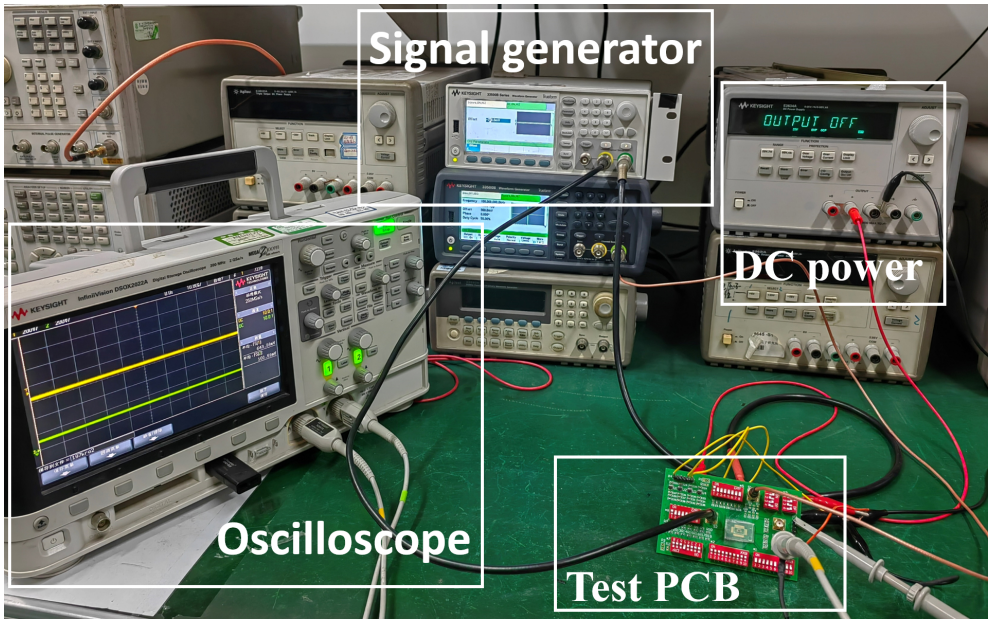


Figure 17. Demonstration of analog front-end circuit measurement.

The signal collected from any type of sensor is transformed into a voltage signal distributed within a range from 0 to V_{DD}. This voltage signal may fall within the nonlinear region of the amplifier, which is undesirable. Compensating for the initial baseline of a resistance-type sensor can solve this issue. In Figure 18, the oscilloscope trace shows how the initial signal of about 650 mV is compensated to the reference level of 800 mV. Upon completion of voltage compensation, it can be observed that the difference between the compensated voltage level and the mid-rail voltage level is less than the resolution of the 8-bit DAC, thereby ensuring that the baseline signal remains within the operating range of the amplifier.

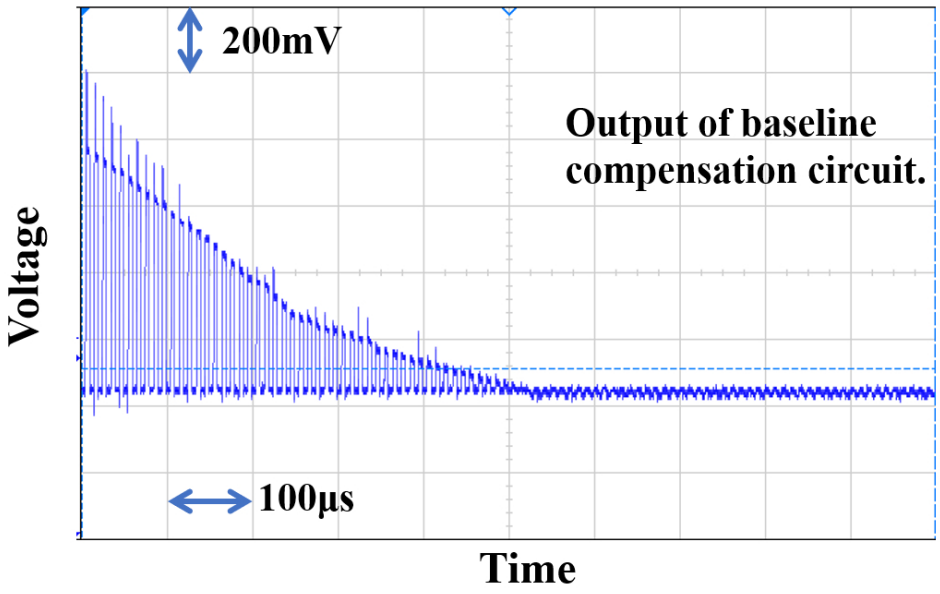


Figure 18. The processes of baseline compensation.

We measured the transient response of R/C/V-type sensors for both input and output, and due to the complexity of characterizing actual sensor circuits with real performance, standard resistors and capacitors were utilized as test components. Figure 19a showcases

the voltage signals corresponding to capacitances of 16.8 pF, 18 pF, 18.7 pF, 19.4 pF, and 20.1 pF as collected by the interface circuit, and Figure 19b displays the differential output resulting from the processing of the aforementioned signals by the chip. Similarly, Figure 19c presents the voltage signals collected by the interface circuit for resistances of 1.5 kΩ, 2.1 kΩ, 2.7 kΩ, 3.3 kΩ, and Figure 19d displays the differential output following processing by the chip. The signals processed by the analog front-end circuit render the sensor changes more discernible and significantly enhance the capability to resist noise interference. The accuracy of the chip proposed in this article, tested for R/C/V, respectively, is 1 Ω, 0.5 pF, and 1 mV, which is advantageous for cases where the electrical quantity change of the sensor is minimal.

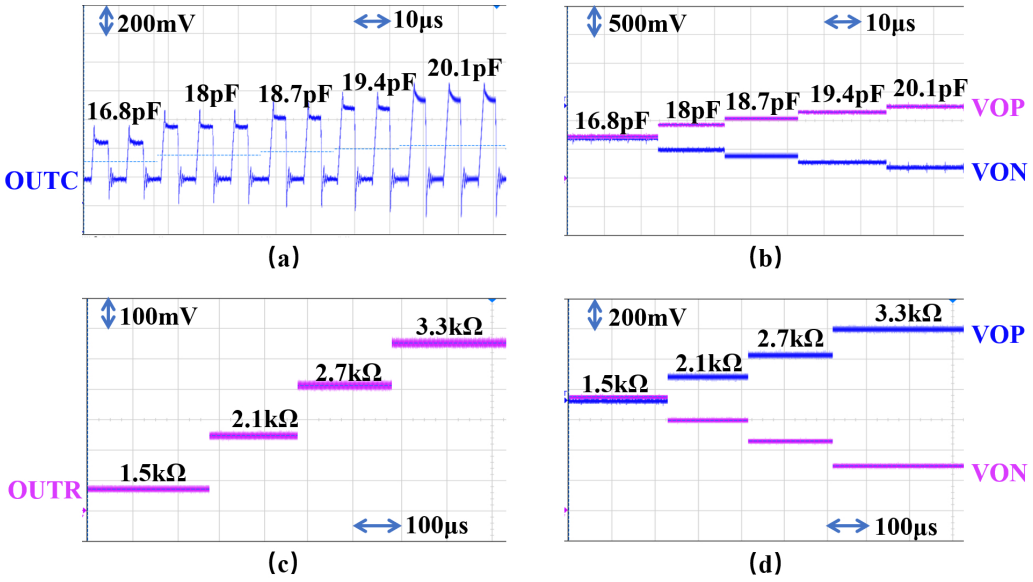
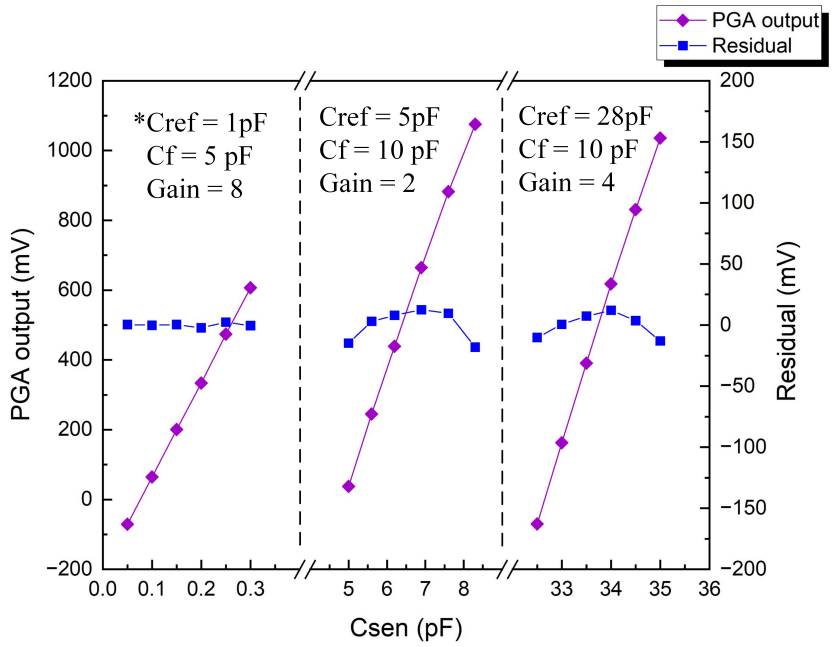


Figure 19. Sensor output acquisition waveforms of (**a**) C_{sen} and (**c**) R_{sen}. Signal amplification circuit output waveforms of (**b**) C_{sen} and (**d**) R_{sen}.

The performance of the sensor can be evaluated through linearity, and the analog front-end circuit used for the sensor should also possess adequate linearity. We use the coefficient of determination (R^2) to evaluate the linearity and calculate the root mean square error (RMSE). Figure 20 illustrates the C-V conversion characteristics of the analog front-end circuit, where selecting appropriate reference capacitance, feedback capacitance, and gain allows for the measurement of capacitive-type sensors within different ranges. Based on the results depicted in Figure 20, the calculated conversion gain for a gain of 2 is determined to be 0.32 mV/fF. The R^2 is 0.9988 and the RMSE is 1.201%. Figure 21 displays the R-V conversion characteristics of the analog front-end circuit, where choosing suitable injection current and gain enables the measurement of resistive-type sensors within different ranges. Based on the results depicted in Figure 21, the calculated conversion gain for a gain of 96 is determined to be 9.7 mV/Ω. The R^2 is 0.9996 and the RMSE is 0.950%. Figure 22 showcases the V-V conversion characteristics of the analog front-end circuit, where selecting the appropriate gain allows for the measurement of voltage-type sensors within different ranges. Based on the results depicted in Figure 22, the R^2 is 0.9999 and the RMSE is 0.678%.

For R^2, all interface circuits in this study have a conversion linearity greater than 0.998, with capacitive interfaces having the worst performance due to factors such as charge transfer and external interference. The conversion linearity is mostly below 1% based on RMSE. The test results indicate that the circuit proposed in this article exhibits exceptional performance in converting high linearity sensors and has achieved a high degree of accuracy.

Table 1 summarizes the performance of the sensor interface described in this article and compares it with previously published capacitive, resistive, and voltage sensor interfaces. The system presented in this article implements a more comprehensive set of features with a smaller area and lower power consumption.



*The curve on the left side of the graph represents the simulated results for capacitances ranging from 50 fF to 300 fF, due to the current test limitations.

Figure 20. Measured acquisition results and relative error in C_{sen}.

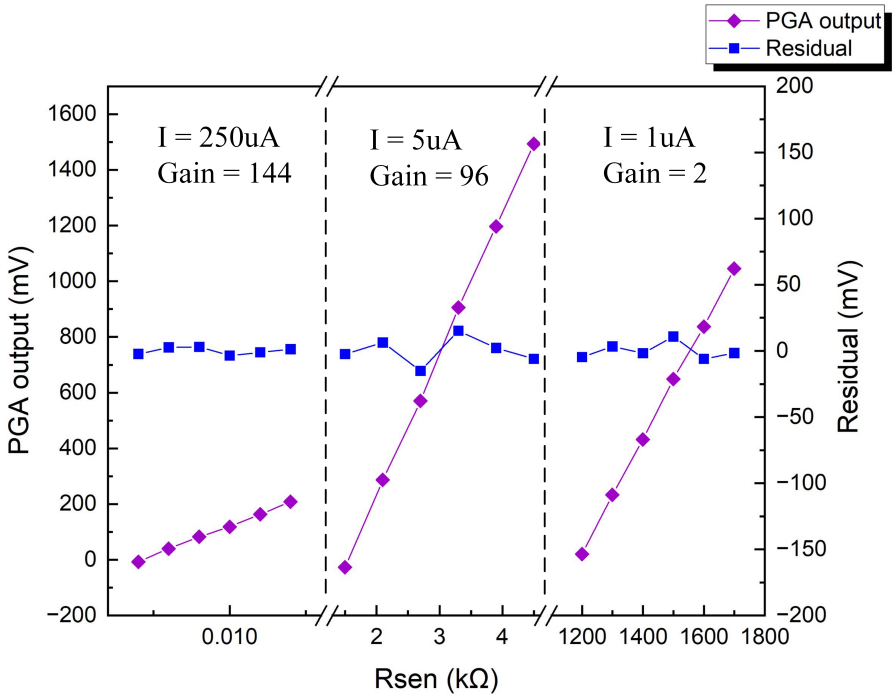


Figure 21. Measured acquisition results and relative error in R_{sen}.

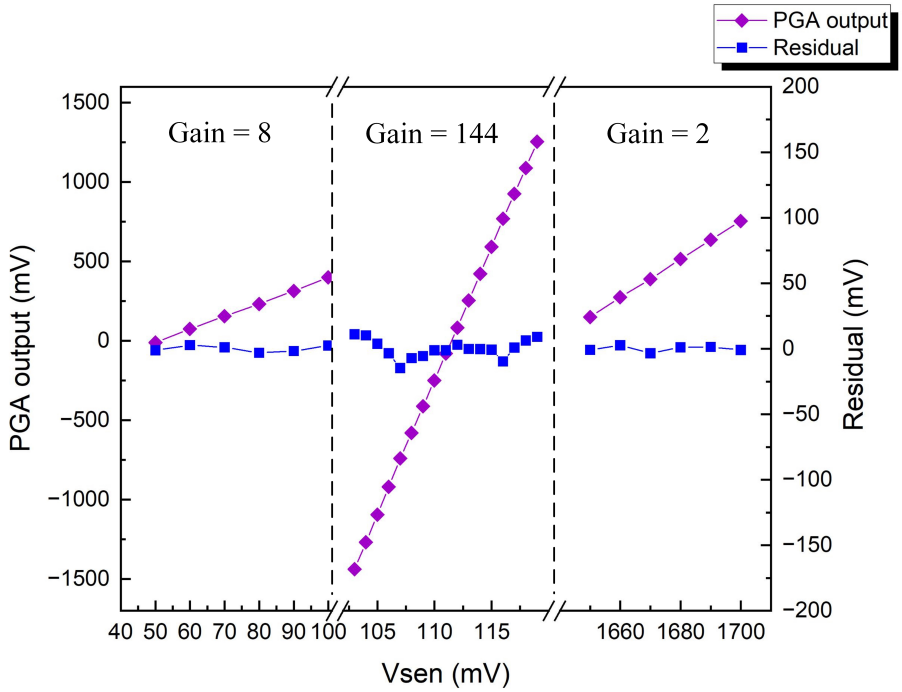


Figure 22. Measured acquisition results and relative error in V_{sen}.

Table 1. Performance summary and comparison.

	[14]	[31]	[32]	**This Work**
Sensor output type	R/C	R/C/V/I	R/C/V/I	R/C/V
Technology (μm)	0.18	0.18	0.18	0.18
Supply voltage (V)	1.8	1.8	5	1.8
Sensor range	R: 800 Ω–930 kΩ C: 400 fF–15 pF V: N/R I: N/R	R: 0.4 Ω–400 Ω C: 2 pF V: 70 mV I: 1.65 μA	R: 9.2 kΩ–10 MΩ C: 33 fF–37 pF V: 1.1 mV–0.72 V I: 16 nA–20 μA	R: 7 Ω–1.7 MΩ C: 50 fF–35 pF V: 0.05 V–1.7 V I: N/R
Power cons. (mW)	8.5	2.54	1.1	1.08
Die area (mm^2)	5.8	9.61	2.56	0.9

4. Conclusions

This article presents a versatile and high-precision analog front-end circuit for R/C/V sensors, which is suitable for multi-parameter sensors requiring high conversion gain and linearity. By utilizing the baseline compensation and offset elimination circuits, the acquisition signals of various sensor types can be processed with minimal distortion and maximum gain, allowing for better adaptability to diverse sensors with a wide range of applications. By integrating self-zeroing and correlated double-sampling techniques, the circuit successfully mitigates low-frequency noise, offset, and sensor signal saturation, enhancing overall precision. The test results indicate that all interface circuits exhibit significant total conversion gains (C: 45 mV/fF, R: 14.5 mV/Ω, and V: 144 v/v) and high linearity with R^2 values greater than 0.998. The proposed integrated circuit is implemented using 0.18 μm CMOS technology and has an effective area of 0.9 mm^2.

Author Contributions: Conceptualization, Y.Y., Z.L. (Zheng Li) and Y.L.; methodology, Y.Y. and Y.L.; software, Y.Y., Z.L. (Zheng Li), X.L. and Y.L.; validation, Y.Y., Z.L. (Zheng Li) and X.W.; formal analysis, Y.Y., Z.L. (Zheng Li) and Y.L.; investigation, Y.Y., M.L., W.L. and Z.L. (Zhenming Li); resources, Y.L.; writing—original draft preparation, Y.Y.; writing—review and editing, Y.Y., Y.H. and Y.L.; supervision, Y.L.; project administration, Y.L., Y.H. and X.L.; funding acquisition, M.L., W.L. and Z.L. (Zhenming Li). All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the Science and Technology Program from State Grid Corporation of China, grant number 5700-202155453A-0-0-00.

Data Availability Statement: No new data were created or analyzed in this study. Data sharing is not applicable to this article.

Acknowledgments: This work was supported by the Science and Technology Program from State Grid Corporation of China: "Development of flexible liquid metal based micro-sensor with anti-electromagnetic interference ability for power engineering applications".

Conflicts of Interest: The authors declare no conflict of interest.

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