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A Low Jitter, Wideband Clock Generator for Multi-Protocol Data Communications Applications

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Abstract: This paper presents a charge-pump phase-locked loop (PLL) frequency-synthesizer-based low-jitter wideband clock generator for multi-protocol data communications applications. Automatic frequency calibration (AFC) using linear variable time window technology and modified multi-modulus dividers (MMD) based on sub-multi-modulus dividers (SMMD) are developed for faster locking, lower jitter, and implementation of multi-protocol data communications applications. The clock generator is fabricated in 0.18 µm CMOS technology. The measured division ratio of the multi-modulus divider ranges from 1.875 to 25, and the output frequency is 46.875~625 MHz. The lock time does not exceed 30 µs, while jitter is less than 500 fs.

Keywords: clock generator; multi-modulus divider; automatic frequency calibration; low jitter

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1. Introduction

The quality and speed of data communication in fiber optic communication, image transmission, and serial communication depend significantly on clock performance, while the clock is the major bottleneck. Different applications, including SONET, Ethernet, and HDTV, require various levels of jitter, number of output channels, and frequency range [1–3]. Research shows that optimization of the loop adaptive tuning mechanism is the paramount factor for multi-protocol compatible clocks [4,5]. For massive MHz telecom services, reasonably designed AFC and MMD are necessary.

With a relatively faster calibration speed and simpler structure, the binary frequency search algorithm has been widely used in AFCs. Various methods have been devised to reduce lock time. Direct frequency error detection and calibration using multiphase [6] or multiplied reference clock [7] are introduced to reduce the comparison time. From a lock-time perspective, AFC based on time-to-digital converter (TDC) counting can reduce the counting period and improve the locking speed significantly, but this method is mainly used in all digital phase-locked loops (ADPLL). Many AFC techniques have also been proposed in [8–10]. In order to strengthen the applicability of the clock generator by increasing the loop divider ratio, methods such as compressing the reference clock frequency range and expanding the divider ratio of MMD can be implemented. Prior research generally confirms that the division ratio extension is invariably achieved by improving two dimensions of integer or fractional-N division accuracy [11,12]. While the MMD is composed of the pre-scalers and the counters expand the logic control bit width of the counter, the consumption of hardware cannot be ignored.

A low-jitter wideband clock generator with loop adaptive tuning architecture featuring an AFC with linear variable time window (LVTW) technology and improved MMD is developed in this article. This technology allows for higher lock accuracy with reduced time consumption by linearly changing the number of reference clock counting cycles.

Additionally, the clock generator introduces an improved MMD design, which includes SMMD. These SMMDs provide dynamic feedback divider ratios for AFC, simplifying the frequency division operation of the MMD.

The contribution of this proposal lies in its ability to achieve a reasonable compromise between wider bandwidth, lower phase noise, and faster locking ability in clock generation for multi-protocol data communications applications. Since the digital circuitry in a conventional charge pump phase-locked loop is on the low side, it is reasonable to consume additional hardware resources in exchange for an increase in locking speed. Meanwhile, the optimization of the algorithm provides another optimization idea for the development of AFC. The measurement results demonstrate the effectiveness of the proposed approach and its potential to significantly improve the performance of clock generators in the field.

2. MMD-Based Loop Adaptive Architecture

As shown in Figure 1, the clock generator comprises a phase/frequency detector (PFD), a charge pump (CP), a loop filter, a voltage-controlled oscillator (VCO), an AFC with LVTW, and an MMD.

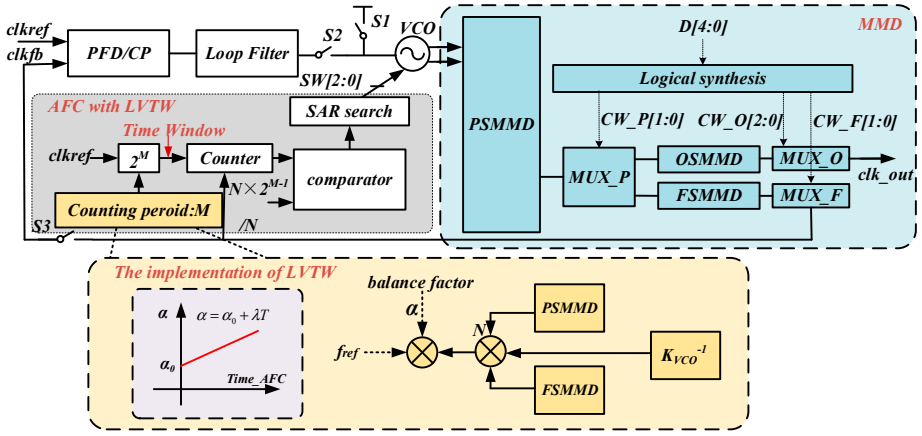

Figure 1. Block diagram of the proposed clock generator.

Due to the large initial hopping in the successive approximation (SAR) search algorithm, the accuracy required at the beginning of frequency calibration is not high. A scaling factor, λ, is introduced to linearly decrease the clock counting time according to the number of clock counting, which is summarized as AFC with LVTW technology. The MMD is implemented by three fixed divider ratios cascaded SMMDs. The division ratio is configured by the logical control word D [4:0] to control the related data selector.

The AFC and MMD parts are the core of the adaptive module, and the architecture details are provided in the following subsections.

2.1. Fast AFC with LVTW

The working mechanism of the proposed AFC is shown in Figure 2. Traditionally, clock generators have used fixed counting time for the reference clock in the AFC process. This means that the counting period remains constant, which can result in longer lock times and limited frequency resolution. The counting period is adjusted by linearly changing the number of reference clock counting cycles. By doing so, it reduces the lock time while still ensuring accurate frequency resolution. This is a significant improvement over traditional AFC techniques, as it allows for faster locking and better performance.

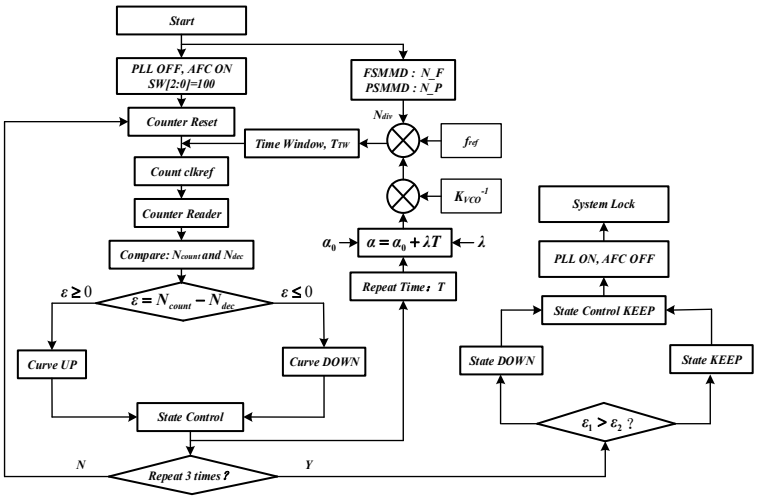

Figure 2. State diagram of the proposed AFC with LVTW.

The PLL is disconnected before the AFC starts, the control voltage of the VCO, V_{ctrl}, is set to half the supply voltage, and SW [2:0] is initialized to 100. After all registers have been reset, LVTW is introduced into the AFC process to dynamically change the counting time of the time window, which is different from the regular AFC operation. The output signal of VCO is counted in a variable time window, and the counting value is compared with the target. The curve is adjusted downwards when $\varepsilon \geq 0$ and upwards when $\varepsilon < 0$. This series of operations is designed to ensure that the most suitable tuning curve can be selected. While the AFC operation is finished, the AFC loop will be disconnected and returned to the PLL.

The implementation of LVTW is shown in Figure 3. During all the counting cycles, the total counting time of AFC consumed by the counter is $T_{total} = B\left(M/f_{ref} + \Delta T_{delay}\right)$. ΔT_{delay} is the interval time between two adjacent time windows, M is the number of counting periods, and B is the number of bits of the AFC output control words. In order to distinguish two adjacent frequency points of the VCO, Δf_{VCO}. Increasing M or decreasing the feedback frequency division ratio, N_{div}, has the same effect on improving AFC frequency resolution. In order to balance the influence of M and N_{div} on Δf_{VCO}, a balance factor, α, is introduced. So M is as follows, while K_{VCO} refers to the tuning gain of the VCO.

$$M \geq \alpha \frac{N_{div}}{K_{VCO}} f_{ref} \tag{1}$$

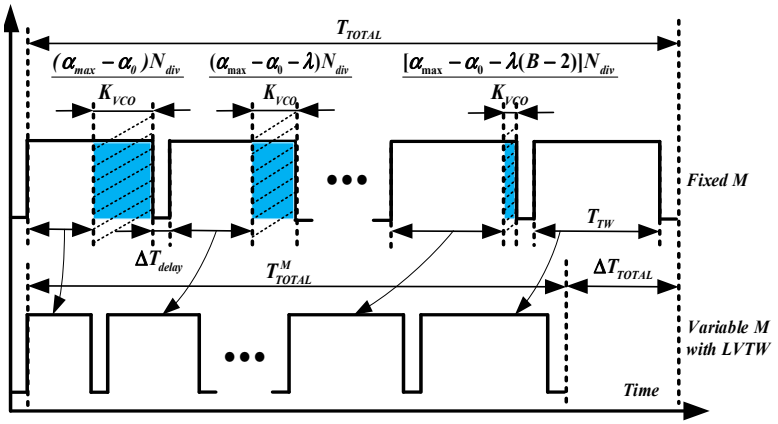

Figure 3. The implementation of the proposed LVTW.

In the PLL with conventional AFC, α is set to a fixed value to obtain a fixed M [13]. The LVTW technology constructs M by introducing a scaling factor, λ, which is strongly correlated with the number of AFC control bits, thus adjusting the counting time of the VCO feedback clock. M is

$$M = \frac{[\alpha_0 + \lambda(T-1)]N_{div,min}}{K_{VCO}} f_{ref},\ T \in [1, B] \tag{2}$$

where T is the T-th counting cycle currently being executed by the AFC. $N_{div,min}$ is the minimum feedback divider ratio, and $\lambda = (\alpha_{max} - \alpha_0)/(B-1)$.

Compared to the case of fixed M in each cycle, the feedback clock counting time for the proposed operation is shorter. As the number of counting cycles increases, T_{TW} keeps getting longer. However, the frequency resolution is not affected by this process. Due to the large initial hopping amplitude of the SAR search algorithm [14], it is not necessary that Δf_{AFC} approaches the limit of the frequency resolution required by the system (corresponding to $\alpha = \alpha_{max}$). When the AFC output control bit is close to the target frequency, Δf_{AFC} is required to be more accurate, and M should be increased appropriately to improve the frequency search accuracy. Based on LVTW technology, the reduced counting time is

$$\Delta T_{total} = \frac{N_{div,min}}{K_{VCO}}[B(\alpha_{max} - \alpha_0) - \frac{\lambda B(B-1)}{2}] \tag{3}$$

If ΔT_{delay} is ignored, the percentage of time reduction, PTR, is

$$PTR = \frac{1}{2}[1 - \frac{\alpha_0}{\alpha_{max}}] \tag{4}$$

α_{max} corresponds to the minimum resolution requirement and cannot be changed arbitrarily. The percentage of lock time reduction can be adjusted by choosing the value of α_0. In the case of $\alpha_{max} = 4$, $\alpha_0 = 2$, it can be calculated from Equation (4) that the locking time can be compressed by up to 25% using the LVTW technology.

2.2. MMD Based on Adaptive Tunning

The working mechanism of the MMD plays a crucial role in enhancing the system's performance [15]. The MMD is implemented by the cooperation of SMMDs, which are built in with several relatively fixed divider ratios. The external 5-bit control signal selects the division ratio of these three independent SMMDs and then combines them with the expected division ratio of the system. Compared to traditional methods, the proposed MMD-based architecture offers several improvements. It allows for a wider range of division ratios, enabling the clock generator to cover a broader frequency range. The improved MMD also reduces hardware consumption, making the clock generator more efficient and cost-effective.

As shown in Figure 4, SMMDs are implemented by cascading 2/3 division units of latches based on current mode logic [15]. A retimer consisting of flip-flops and buffers is adopted to mitigate clock jitter accumulation and minimize the delay time in the feedback chain of the divider [16]. The retimer is based on a phase interpolator (PI). It could retime received data with input jitter and noise in order to export clean waveforms. The feedback clock signal in the SMMDs no longer passes through the multi-input AND gates of the 2~N-1 stages and feeds the last-stage clock signal to the first-stage multi-input AND gate AND_1 directly.

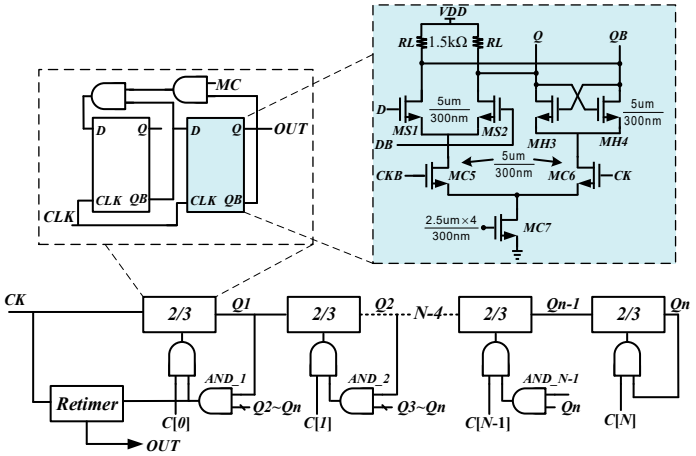

Figure 4. Schematic of SMMD and 2/3 divider.

The SMMDs are composed of pre sub-multi-modulus divider (PSMMD), feedback sub-multi-modulus divider (FSMMD), and output sub-multi-modulus divider (OSMMD), which are equipped with several relatively fixed divider ratios. CW_P [1:0] and CW_O [1:0], derived from MUX_P (multiplexer for PSMMD) and MUX_O (multiplexer for OSMMD), are generated via the logic synthesis of D [1:0]. The logic synthesis process of D [1:0] is shown in Figure 5. The division ratios of PSMMD and FSMMD are configured by CW_P [1:0] and CW_O [1:0] to dynamically reduce the current error between the clock counting number and the desired number. Meanwhile, MUX_F (multiplexer for FSMMD) is controlled by D [4:2] to configure the division ratios of the OSMMD directly. The division relationship between D [4:0] and SMMD is shown in Table 1.

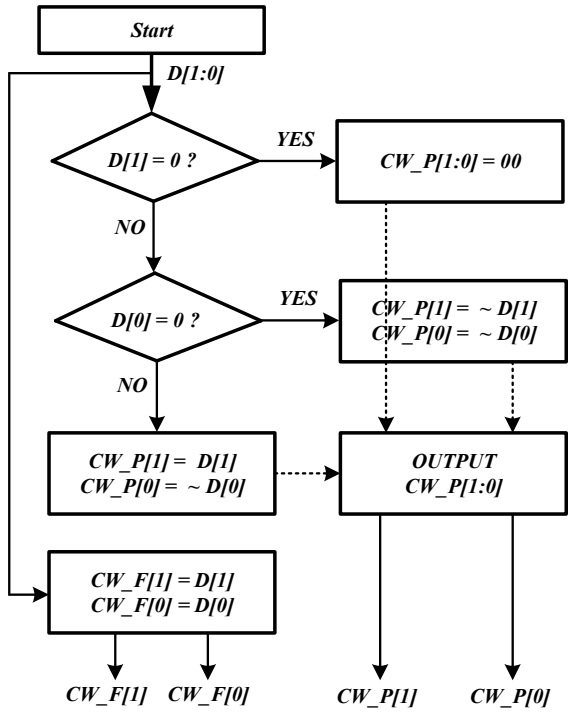

Figure 5. Workflow of logic synthesis of D [1:0].

Table 1. The division relationship between D [4:0] and SMMD.

D [1:0]		PSMMD	FSMMD	D [4]	D [3]	D [2]	OSMMD
Logical Synthesis				0	0	0	1
CW_P [1:0]	CW_F [1:0]			0	0	1	2
00	00	3	24	0	1	0	3
00	01	3	25	0	1	1	4
01	10	4	20	1	0	1	6
10	11	5	15	1	1	1	8

However, the delay time inside the SMMDs increases with the length of division chains, especially in MMDs based on the basic division unit cascade structure, which is determined by the inherent characteristics of the internal logic gates. In this type of MMD [17,18], the clock delay of the counter is not negligible as the division ratio changes. In the application of wide division ratios, the longer transient process of this type of clock driver is caused.

Assuming that the clock delay time of the N-stage 2/3 division unit is T_{dn}, the delay time is reduced to

$$\Delta T_{total} = \sum_{i=2}^{N-1} T_{di}$$

The simulation of the delay time of the SMMDs for cascaded 2~4 stage 2/3 dividers in the *tt* corner at 27 °C is shown in Figure 6. The output phase noise of the FSMMD is −145 dBc /Hz @ 1 MHz, which reduces the phase noise by 9 dBc/Hz compared to the situation without a retime, as shown in Figure 7. The delay time simulation results for SMMD (f_{CK} = 1.8 GHz) at different corners and temperatures are shown in Table 2. The delay time of SMMD has increased at a slow corner (100 °C), while it has reduced a few nanoseconds at a fast corner (0 °C). The phase noise deteriorates by 3.2 dBc/Hz (slow corner, 100 °C) and 2.9 dBc / Hz (fast corner, 0 °C), respectively, for FSMMD compared to −145 dBc/Hz @ 1 MHz (typical corner, 27 °C).

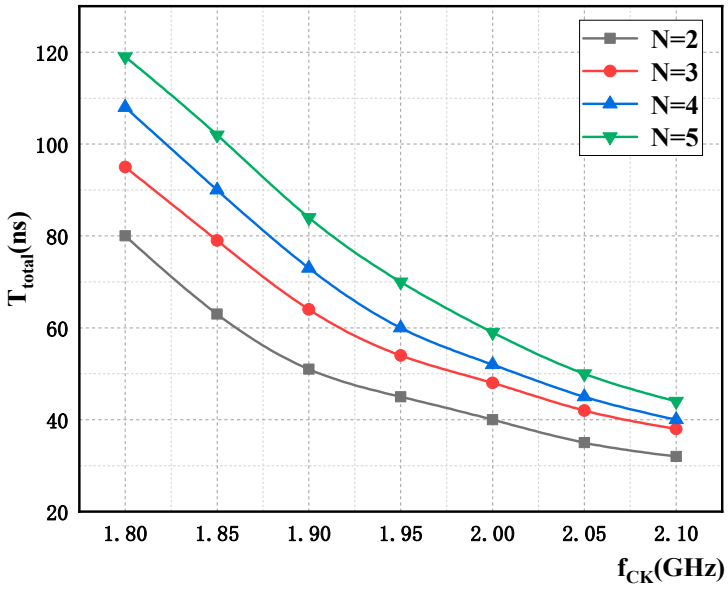

Figure 6. Delay time of SMMD.

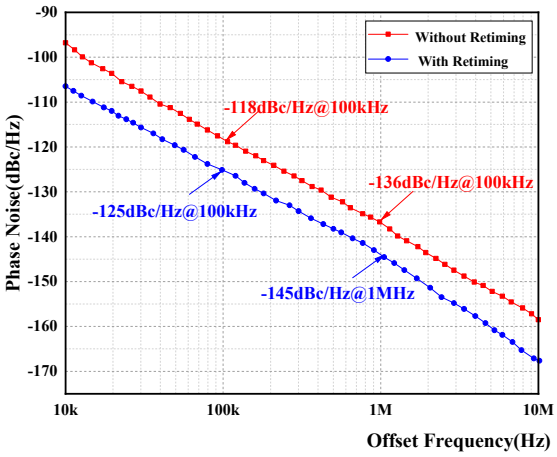

Figure 7. Phase noise of FSMMD.

Table 2. Delay time of SMMD (N = 5) at different corners.

f_{CK} = 1.8 GHz	Slow Corner, 100 °C	Typical Corner, 27 °C	Fast Corner, 0 °C
N = 2	87 ns	80 ns	75 ns
N = 3	102 ns	95 ns	90 ns
N = 4	115 ns	108 ns	103 ns
N = 5	126 ns	119 ns	114 ns

To verify the effect of MMD-based LVTW technology on improving the locking speed, we used 3-bit AFC for loop lock simulation. The reference clock frequency was 25 MHz, and the frequency resolution of VCO was 30 MHz/LSB, with N_{div} set to 75. The simulations were conducted with fixed M and variable M based on LVTW, as shown in Figure 8. Compared to fixed M, the lock time based on the variable was reduced by 23.9%. It is worth noting that the simulated values may be smaller than the theoretical values due to the high resource consumption caused by LVTW-based digital logic circuits in operation. Furthermore, the fact that ΔT_{delay} is not included in the derivation of T_{total} causes the actual AFC time to be larger as well.

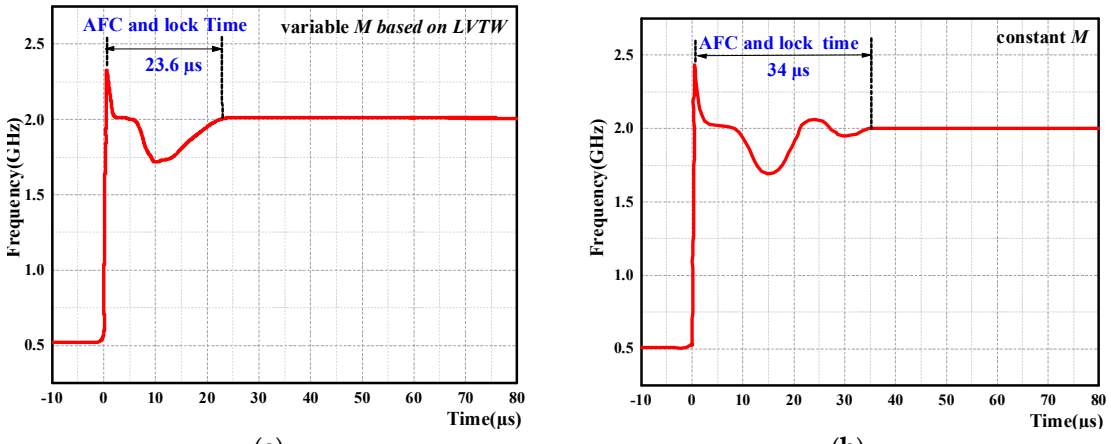

Figure 8. AFC and lock time with (**a**) variable M and (**b**) constant M.

3. Other Building Blocks

3.1. VCO

Due to the specific frequency division mechanism of MMD, the bandwidth requirement of VCO is not harsh. In MHz telecom applications, the VCO output frequency only needs to be maintained as a series of specific discrete frequencies. At the same time, attention should be paid to the power consumption and phase noise of VCO.

A schematic of VCO is shown in Figure 9 [19,20]. The required tuning frequency is easy to achieve, but the difficulty of the design lies in how to reduce the phase noise. In order to construct a small K_{VCO} and reduce the effect of the subtle jitter of V_{ctrl} on the phase noise of VCO, a 3-bit switch capacitor array is used. The design of variable capacitors must meet the requirements of overlapping frequency, which is also the basis for selecting the size of variable capacitors [21]. The cumulative MOS transistor variable capacitor has the lowest power consumption and phase noise among all variable capacitors provided by the foundry. Therefore, this variable capacitor was adopted in the LC-VCO design of this article. The high-pass filter used to avoid output signal attenuation is composed of R_1 and C_1. The K_{VCO} comparative simulation of single-channel and three-channel parallel structures with variable capacitors is shown in Figure 10. An inductance is used to suppress the second harmonic at the common source of the cross-coupled pair.

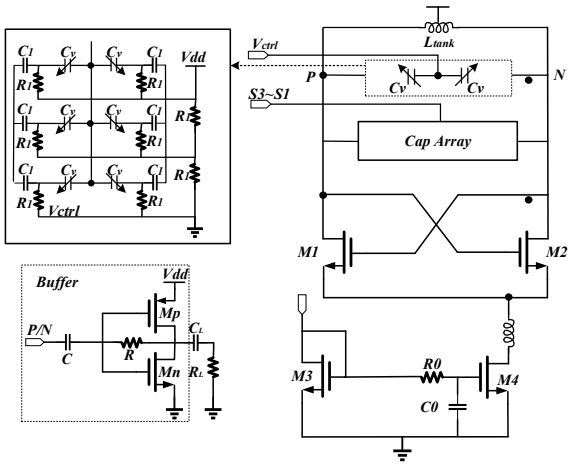

Figure 9. Schematic of VCO.

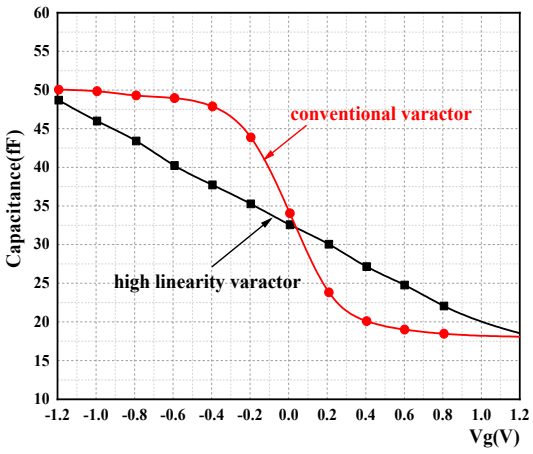

Figure 10. C-V curve between conventional and high linearity varactor.

3.2. CP

As shown in Figure 11, the programmable CP adopts a 4-bit binary weighted current switch structure, which outputs a total of 16 discrete current values from 30 µA to 0.5 mA.

The operational amplifier based on feedback structure enables both charge and discharge current mismatch and the spur level to be reduced effectively. M_8~M_{11} are used as switching tubes with an aspect ratio of 50:1 provided by the PFD with four differential inputs. The aspect ratio of M_{12}~M_{17} is 9:1, and they are controlled by the switch control words code [2:0] and code_N [2:0], and the switch control words are generated by UP, DN, CT1, and CT2 [22].

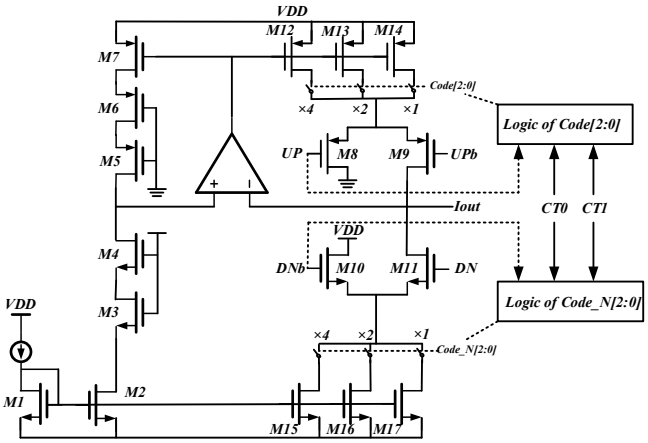

Figure 11. Schematic of CP.

The feedback mechanism introduced by the operational amplifier has advantages in the control of gate voltage of M_{12}~M_{13}, which can suppress current mismatch. On the other hand, the size of the transistors M_{12}~M_{17} in the charging and discharging branches should be carefully designed to reduce the mismatch. The simulation of the charge–discharge current mismatch of the programmable charge pump is shown in Figure 12. In addition, the simulation indicates that the charge–discharge current mismatch does not exceed 0.1% at a typical corner; meanwhile, it does not exceed 0.13% at the slow corner and 0.15% at the fast corner, respectively.

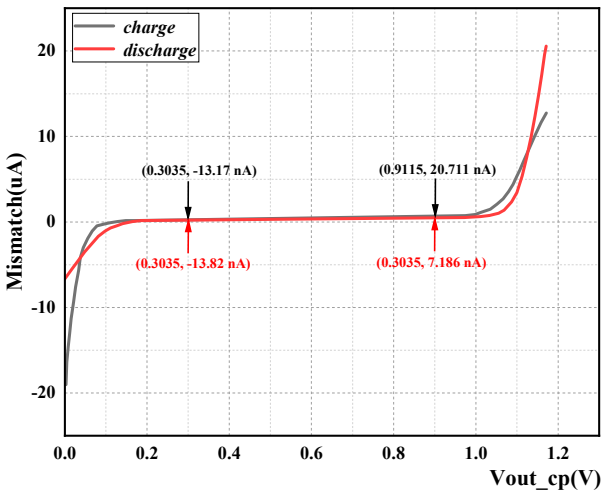

Figure 12. Current mismatch of CP.

4. Measurement Results

The proposed clock generator was fabricated in 0.18 µm CMOS technology. The layout and PCB for measurement are shown in Figures 13 and 14, respectively.

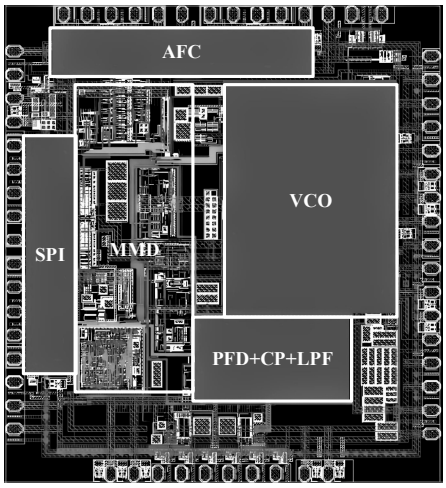

Figure 13. Layout of the clock generator.

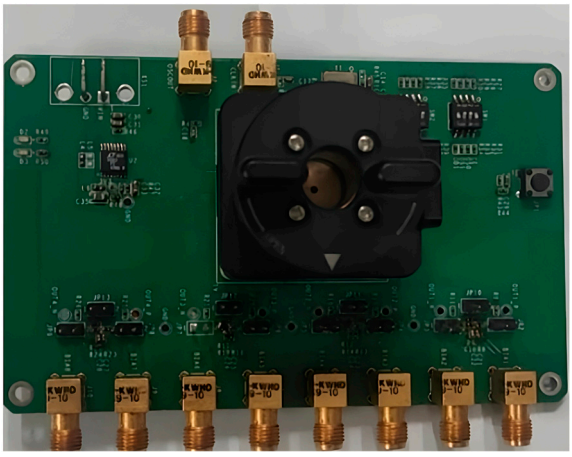

Figure 14. PCB for measurement.

The measurement setup is presented in Figure 15. The reference signal is provided by a crystal oscillator of 25 MHz, and power is supplied by a 1.3 V low dropout regulator (LDO). During the adaptive frequency calibration, the power management module provides 0.65 V for VCO to ensure that V_{ctrl} remains at the center of the frequency bands. The MMD division ratio selection signal is controlled by an external microcontroller unit (MCU). The pad O_PAD of the output stage is connected to the phase noise analyzer to measure the phase noise of the overall system. In addition, VCO_PAD and VCO_SIG are drawn from the VCO, respectively, to obtain the curve of tuning and V_{ctrl}.

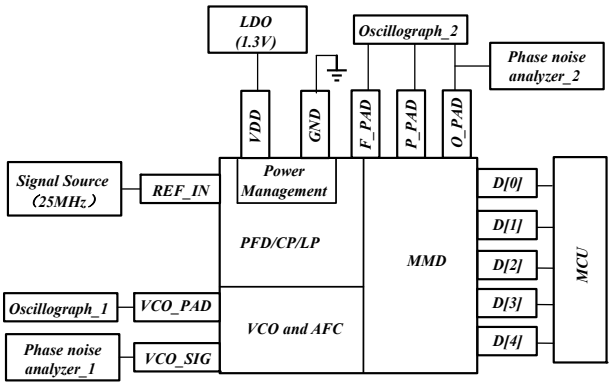

Figure 15. Measurement setup.

The VCO tuning curve shown in Figure 16 indicates that there is an overlap between adjacent frequency bands in different colors, which ensures the continuous frequency modulation of the VCO. The tuning frequency of VCO covers 1.79~2.05 GHz. Compared with the wide tuning range of VCO in other types of PLL systems, 1.8~2 GHz VCO meets the requirements of wideband design and simplifies the design of oscillators [23–25]. The output frequency of the clock generator is shown in Figure 17. Continuous clock frequency provided by a clock generator is not required for many communication systems. The proposed clock generator can generate 24 discrete clock frequencies covering 46.875~625 MHz, which meets the data transmission needs of communication systems such as GigE, HDTV, SATA, SONET, 10 G Fibre Channel, XGMII, etc. [26,27].

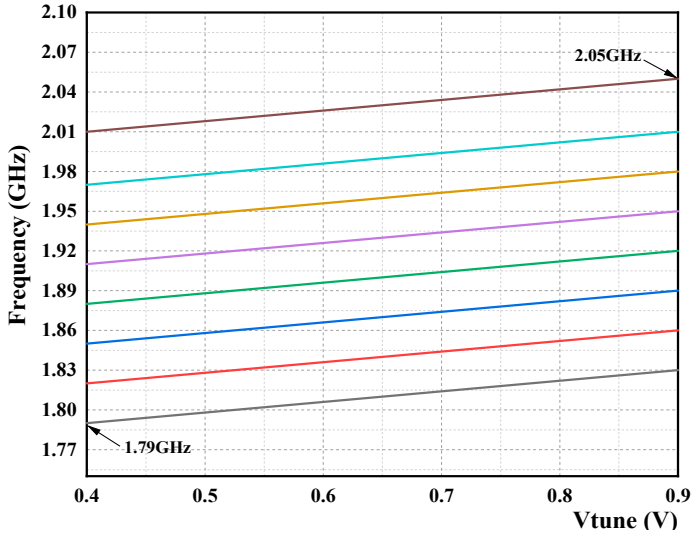

Figure 16. Tuning curve of VCO.

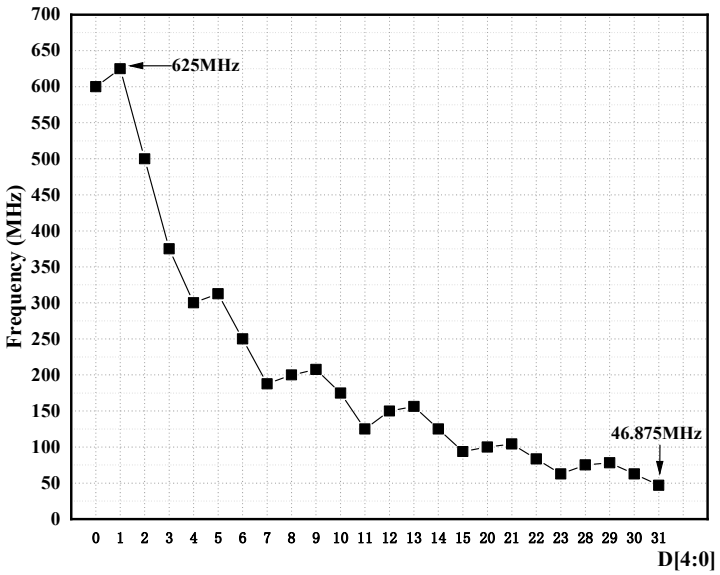

Figure 17. Output frequency of clock generator.

The input reference frequency of the clock generator is 25 MHz. After MMD is divided by 24, the output clock is 599.9 MHz. In addition, the transient result of V_{ctrl} is shown in Figure 18, which indicates that the loop lock time does not exceed 30 µs. The phase noise of the VCO is −120.39 dBc/Hz @ 1 MHz, as shown in Figure 19. In Figure 20, the phase noise of the overall PLL is −128 dBc / Hz at the frequency offset of 1 MHz, and the RMS jitter

integrated from 10 kHz to 20 MHz is 492 fs. Finally, a summary and comparison table of clock performance is given in Table 3.

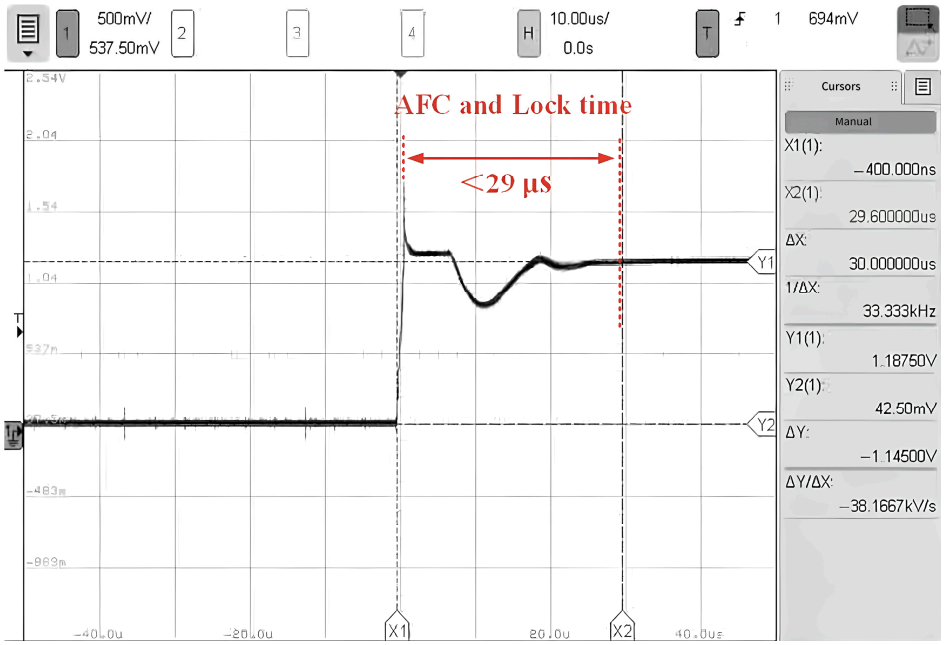

Figure 18. Measured transient results of V_{ctrl}.

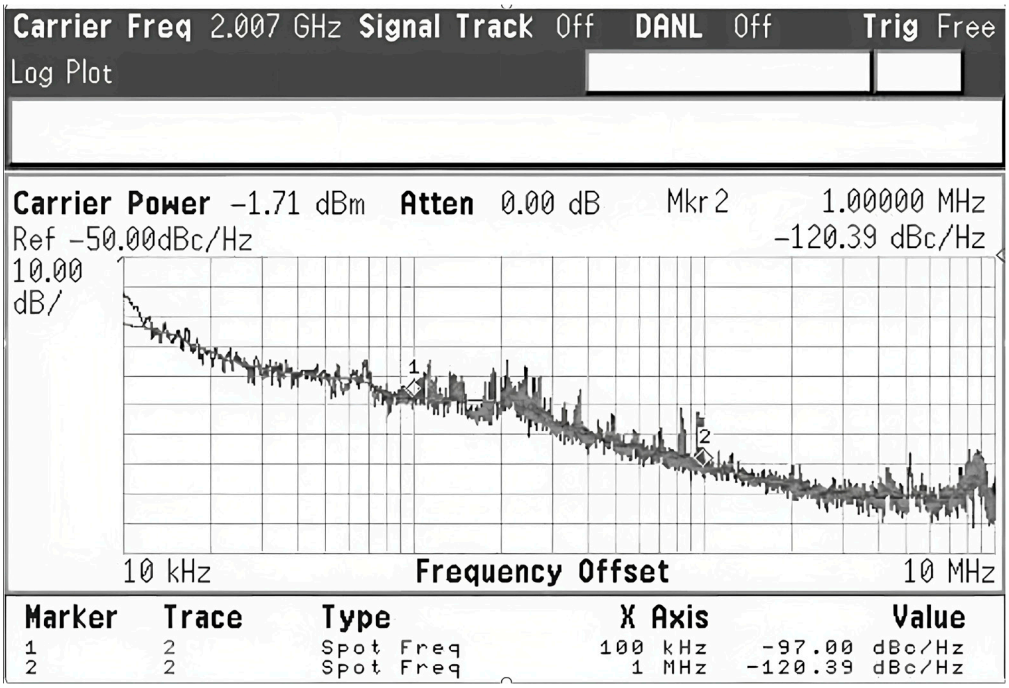

Figure 19. Measured phase noise of the VCO @ 2.007 GHz.

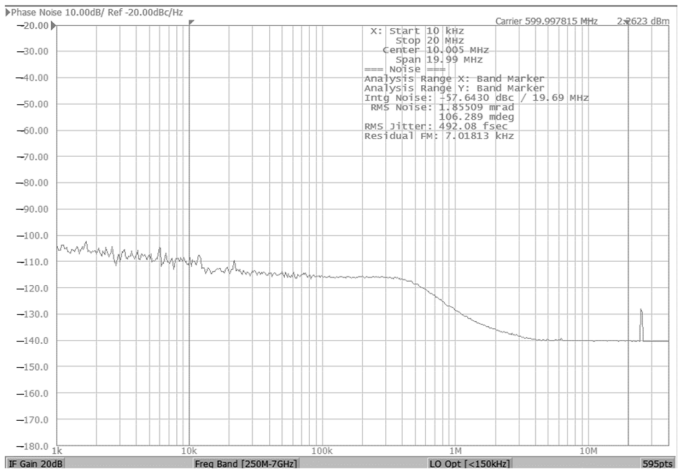

Figure 20. Measured phase noise of the PLL @ 600 MHz.

Table 3. Performance comparison.

	Process	VCO TR/ GHz	LO Output Range/GHz	Power/ mW	Ref. Freq./ MHz	Lock Time (Including AFC Time)	Out-Band PN @ 1 MHz (dBc/Hz)	FoM_T [1]
[6]	0.13 µm CMOS	1.9–3.8	1.9–3.8	15.36	40	<10.025 µs	<117.57 (f_c = 3.8 GHz)	NA
[7]	0.5 µm BiCMOS	1.15–1.75	1.15–1.75	54.6	13	50 µs (AFC)	−129 (f_c = 1.4 GHz)	−178
[10]	0.18 µm CMOS	2.3–3.7	0.05–4.8	94	10/20	<40 µs	−127 (f_c = 1.8 GHz)	−211.2
[14]	0.11 µm CMOS	1.5–2.4	0.09–0.77	20.28	6	90 µs 50 µs (AFC)	<100 @ 100 kHz	NA
This work	0.18 µm CMOS	1.79–2.05	0.047–0.625	30	25	<29 µs	−128 (f_c = 600 MHz)	−204

[1] $FoM_T = FoM - 20log[Tuning\ Range(TR)/10]$, $FoM = PN - 20log[(f_0/\Delta f) + 10log(P_{DC}/1mW)]$.

5. Conclusions

In this paper, a clock generator for MHz telecom application is proposed using a loop adaptive tuning structure based on LVTW technology and modified MMD. This structure adopts the method of reducing the feedback clock counting period to achieve a fast lock. Compared with the existing MMD, the improved MMD achieves the multi-protocol application under a unified architecture with its special internal structure and method of external controlling. The configuration method of external split ratio simplifies the configuration process. In addition, the feedback divider with variable division ratios improves the rate of VCO capture. This clock generator for MHz telecom application can operate over a temperature range of −45~125 °C and remains thermally stabilized. Under the temperature condition of 27 °C, due to the improvement in the loop adaptive architecture structure, the system configures integer or fractional division ratios of 1.875~25 for the clock generator. The clock generator provides a range of output frequencies of 46.87~625 MHz. With a maximum lock time of no more than 30 µs and jitter of no more than 500 fs, the proposed clock generator meets the clock frequency requirements of most communication systems.

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