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Soft-Error-Aware Radiation-Hardened Ge-DLTFET-Based SRAM Cell Design

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Abstract: In this paper, a soft-error-aware radiation-hardened 6T SRAM cell has been implemented using germanium-based dopingless tunnel FET (Ge DLTFET). In a circuit level simulation, the device-circuit co-design approach is used. Semiconductor devices are very prone to the radiation environment; hence, finding out the solution to the problem became a necessity for the designers. Single event upset (SEU), also known as soft error, is one of the most frequent issues to tackle in semiconductor devices. To mitigate the effect of soft error due to single-event upset, the radiation-hardening-by-design (RHBD) technique has been employed for Ge DLTFET-based SRAM cells. This technique uses RC feedback paths between the two cross-coupled inverters of an SRAM cell. The soft-error sensitivity is estimated for a conventional and RHBD-based SRAM cell design. It is found that the RHBD-based SRAM cell design is more efficient to mitigate the soft-error effect in comparison to the conventional design. The delay and stability parameters, obtained from the N-curve, of the Ge DLTFET-based SRAM cell performs better than the conventional Si TFET-based SRAM cell. There is an improvement of 305x & 850x in the static power noise margin and write trip power values of the Ge DLTFET SRAM cell with respect to the conventional Si TFET SRAM cell.

Keywords: germanium based dopingless tunnel FET (Ge-DLTFET); radiation-hardening-by-design (RHBD) technique; SRAM cell; single event upset (SEU)

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1. Introduction

Static random-access memory (SRAM) is an important component in lightweight satellites for space applications, owing to its high packaging density and better logic performance [1]. However, space contains highly energetic particles viz. protons, neutrons, α-particles, heavy ions, etc. When these particles strike on any digital circuit, electron–hole pairs are generated along the path they traverse [1]. These charges get accumulated at the sensitive node, thereby creating a transient voltage signal at that node. When the amplitude of the transient signal exceeds the switching threshold of the circuit, the stored data at that sensitive node gets altered. The phenomenon changes the logic state of the bit stored in the SRAM cell node, which is called single event upset (SEU) or soft error [2]. In the sub nanometer regime, the SRAM stability is more vulnerable to SEU [3–5]. Due to scaling of the technology node, the space of the transistor decreases, resulting in a reduced silicon/polysilicon/metal layer area, which makes the device more sensitive to radiation effect. This phenomenon further affects the multiple nodes of the circuit [6–8] due to the accumulated charge. Moreover, the SRAM functionality is affected due to the introduction of radiation. Hence, for the SRAM to work efficiently, it becomes necessary to remove this effect. In order to mitigate the SEU effect in the transistor itself, a method has been proposed

here. The same SEU may be viewed as tolerable or intolerable by the user depending on the desired reliability of the electronic device. In various research papers, many SEU removal techniques have been utilized to achieve a suitable radiation hardness for a device. Some of the ways to mitigate single-event upset are error detection and correction using codes, removing and reducing the radiation sources, radiation effect mitigation by layout and circuit design techniques [9]. A variety of techniques can detect and correct errors in SRAM arrays caused by ionizing particles or resulting from increasing process variations. This type of radiation mitigation technique adds redundancy to the system, which affects performance and takes up additional space. It increases the complexity of the circuit. It results in increasing delays in the circuit operation. Circuit or system redundancy is the most effective method for compensating for a single event upset. The most efficient redundancy strategies are also the costliest in terms of area and efficiency. When two or more similar circuit elements run simultaneously, i.e., same code at same time, this is called circuit redundancy. When a data mismatch is found in a dual-component system, the system must be restarted. The disadvantages of circuit redundancy include the additional space, power, and delay that redundant schemes entail. Moreover, in the approach involving the removal of radiation sources, single event upset can be minimized by reducing heavy particles. To minimize the SEU, pure material for the manufacturing and packing of integrated circuits (ICs) and be utilized. To reduce the SEU formed by particles, the careful selection of solders, mold and underfill compounds with low emissivity rates is critical. The BPSG (boron-doped phosphosilicate glass) being removed from the semiconductor process flow is the most efficient way of minimizing the single-event upset caused by neutron-induced 10B fission [10].

In recent studies, the soft-error performance of a 6T SRAM cell has been analyzed with sub-nanometer devices. It was found that the FinFET-based SRAM cell showed better immunity due to soft error in comparison with its conventional counterpart, the CMOS SRAM cell [11–13]. Moreover, in the literature, a technique called radiation hardening by design (RHBD) is used to eliminate the effect of SEU during circuit level implementation [14–16]. However, with the scaling of CMOS technology, nano-devices experience various challenges, such as short-channel effects (SCEs) and complex fabrication processes. Hence, the Tunnel Field-Effect Transistor (TFET) is emerging as a potential candidate for low-power VLSI technology and has replaced conventional MOSFETs due to its steeper subthreshold swing and low standby power [17–19]. However, TFETs suffer from a low ON current due to the use of indirect and large energy band gap material. TFET also suffers from a lower ION/IOFF ratio. These challenges restrict the aid of TFET for elevated-speed and extreme low power circuit purposes. In this manuscript, the above-mentioned problems have been considered. To achieve this, a device model of n-type and p-type germanium-based dopingless tunnel FET (Ge DLTFET) has been implemented. Due to the dopingless structure of the device, it offers a reduced minimal thermal cost, and it is also immune to process variability. In this manuscript, Verilog-A modeling of n-type and p-type Ge DLTFET has been organized. Compact modeling of the devices is achieved using 2D lookup tables. The calibrated characteristics of the device and the TCAD display a similar behavior. With respect to these results, our model has been validated. Then, a comparison of various performance parameters of Ge DLTFET has been carried out with conventional TFET. The compared results show that the performance of Ge DLTFET is far better than conventional TFET in terms of delay and stability parameters.

Moreover, in this manuscript, the presented Ge-DLTFET structure is utilized to analyze the 6T SRAM cell stability against the soft-error effect or SEU. Due to the use of germanium as source material, the Ge-DLTFET structure shows a low-energy band gap, which improves the device ON current (ION). The Ge-based DLTFET structure is also immune from variability issues due to the random dopant fluctuations (RDFs) [20]. Further, the dopingless (DL) structure simplifies the fabrication processes due to the use of intrinsic Si.

In brief, the paper analyzes the sensitivity of a Ge-DLTFET-based SRAM cell before and after the radiation effect and its mitigation technique. A radiation-hardening-by-design

(RHBD) technique has been employed to reduce the effect of SEU in the Ge-DLTFET-based SRAM cell.

This manuscript is divided into seven different sections. Section 2 explains the device structure and its parameters, Section 3 describes the impact of soft error on the 6T Ge DLTFET SRAM cell, Section 4 shows SEU mitigation using the radiation-hardening-by-design technique, Section 5 explains the delay analysis of 6T Ge DLTFET & TFET SRAM cells under various conditions, Section 6, a stability analysis using an n-curve has been performed for 6T Ge DLTFET & TFET SRAM cells, and Section 7 concludes the manuscript.

2. Device Structure and Simulation Parameters of Ge-DLTFET

Figure 1 shows the schematic cross-sectional view of Ge-source n-type DLTFET. The simulation parameters for both types of DLTFETs have been adapted from [20]. The details of the simulation parameters are summarized in Table 1 [20,21].

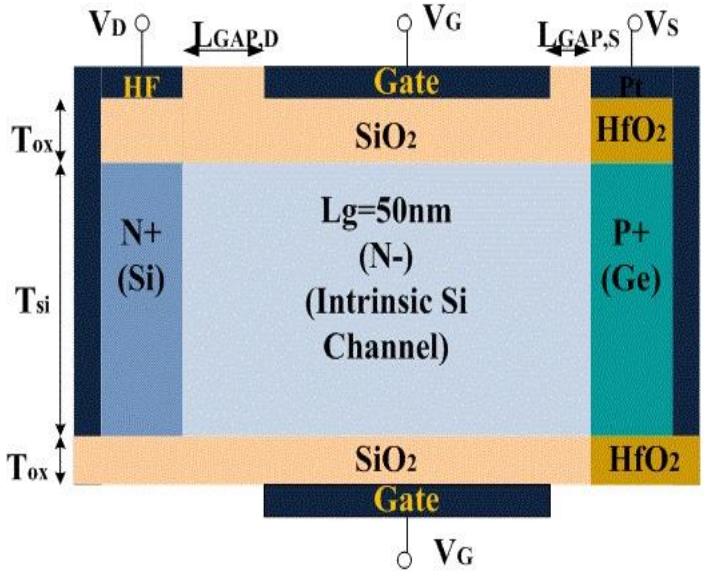

Figure 1. Cross-section view of Ge-Source n-type DLTFET.

Table 1. Simulation parameters for Ge DLTFETs.

Parameters	Ge DLTFET
Thickness of Si (T_{Si})	10 nm
Thickness of source dielectric	0.5 nm (HfO_2)
Thickness of drain dielectric	3 nm (SiO_2)
Channel doping (N_D)	10^{15} cm^{-3}
Source metal work function (Pt)	5.93 eV
Drain metal (Hafnium)	3.90 eV
Gate work function (ϕ_M)	4.50 eV
Distance between source (p+) and gate ($L_{Gap,S}$)	3 nm
Distance between drain (n+) and gate ($L_{Gap,D}$)	15 nm
Thickness of gate dielectric (T_{OX})	3 nm (SiO_2)
Length of gate (L)	50 nm

DLTEFTs employ the concept of charge plasma (CP) to create heavily doped source and drain regions. CP technique simplifies the fabrication of nano-devices in comparison to ion implantation and the diffusion process. The following two conditions must be satisfied while employing CP technique: (i) The work function of the source/drain metal electrodes must be less than that of the intrinsic silicon, i.e., $\phi_M = \chi_{Si} + \left(\frac{E_G}{2q}\right)$, where χ_{Si} is the electron affinity (χ_{Si} = 4.17 eV) and EG is the band gap energy of bulk silicon; (ii) The

silicon film thickness must be less than the Debye length, i.e., $L_D = \sqrt{\varepsilon_{Si} V_T / qN}$, where ε_{Si} is the dielectric constant of silicon, V_T is the thermal voltage, N is the concentration in the body, and q is the elementary charge [22,23]. For the creation of N+ source regions, platinum metal (Pt), having a work function of 5.39 eV, is used, and for the creation of the drain region, hafnium metal (Hf) is used.

The details of the simulation parameters for Ge-DLTFETs are included in Table 1.

TCAD simulations for the shown device structures are performed on a Silvaco ATLAS tool, and their V-I transfer characteristics are shown in Figure 2. Figure 2a depicts the transfer characteristic of n-type Ge DLTFET whereas Figure 2b shows the transfer characteristic of p-type Ge DLTFET. For the simulation of tunneling current, a nonlocal band-to-band tunneling (BTBT) model is used in this study. The potential profile along the entire path linked by tunnelling determines the inter-band tunneling current in the TFET. To estimate the tunnelling probability along with the tunneling direction, the Wentzel–Kramer–Brillouin (WKB) approximation model was used. The leakage current study was carried out using a drift-diffusion current transport model in which the Poisson's equation and carrier continuity equation are solved consistently. Additionally, the concentration-dependent Shockley Read Hall (SRH) generation and recombination model are also included.

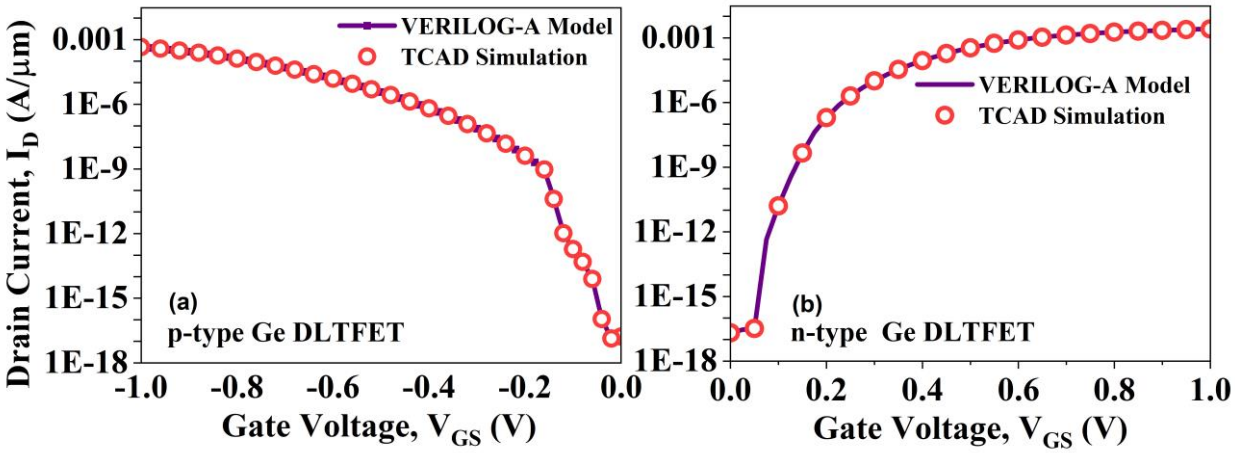

Figure 2. Transfer characteristic of (**a**) n-type Ge DLTFET and (**b**) p-type Ge DLTFET.

3. Impact of Soft Error on 6T Ge-DLTEFT SRAM Cell

In the analysis of the SRAM cell, the data were extracted from the Silvaco Atlas device simulation for n-type and p-type devices, such as C_{GS}, C_{GD}, I_D vs. V_D, in terms of lookup tables. Verilog codes, for both devices, are written with the help of lookup tables. This Verilog code describes the behavior of the proposed device in order to perform a circuit simulation of the SRAM cell using the SPICE tool. These steps are being followed due to the unavailability of SPICE models for modern devices, such as Tunnel FET, Ge DLTFET, etc. This device-circuit co-design approach helps analyze the circuit performance made from modern sub-nm.

In general, complex simulations with a large number of transistors put the constraints of computational resources, a long simulation period and convergence issues in TCAD (ATLAS Device Simulation Software 4.2.0.R., 2015) [24]. To mitigate the above-mentioned issues, the Verilog-A models of p-type and n-type GE DLTFETs have been introduced. The device for the circuit-level simulation of both Ge DLTFETs has been followed here. The C–V and I–V characteristics of the above devices are obtained from the TCAD simulation tool by adjusting the bias conditions throughout a broad range of operating voltages. The lookup tables are prepared by using the extracted characteristics of both devices, including I–V and C–V data. For various performance parameters, i.e., drain current (I_{DS}), gate-to-source capacitance (C_{GS}) and gate-to-drain capacitance (C_{GD}), as functions of (V_{GS}, V_{DS}) over a broad range of nominal voltage, the DC and small-signal simulations have been performed. The calibrated characteristics of p-type and n-type GE DLTFETs along with Verilog-A

models and TCAD simulations results are verified. It has been observed that the developed Verilog-A models of p-type and n-type GE DLTFETs are favorably matched with the TCAD simulation results.

The soft-error sensitivity of the SRAM cell of Ge DLTFET is investigated in this section. The data recovery prevention technique after a heavy ion attack is addressed. The 6T SRAM cell is designed using Ge DLTFET. The single-event upset problems have been mitigated by implementing the RC feedback loop. The delay before and after the radiation has been calculated.

In Figure 3, the impact of soft error on the 6T Ge-DLTEFT SRAM cell has been analyzed. Here, two cross-coupled inverters utilized n-type and p-type DLTFET. Transistors X_1 and X_2 are pull-up devices, whereas transistors X_3 and X_4 are pull-down devices, forming the cross-coupled inverters. Transistors X_5 and X_6 are the access devices. The access transistors are controlled by the word line (WL). The complementary bit lines BL and BLB are used to store the desired information to the storing nodes of the SRAM cell. When WL is high, the transistors X_5 and X_6 are ON, and data on BL and BLB gets transferred at the nodes Q and QB, respectively. When WL is LOW, both the transistors X_5 and X_6 are OFF, and nodes Q and QB retain their values until WL goes high.

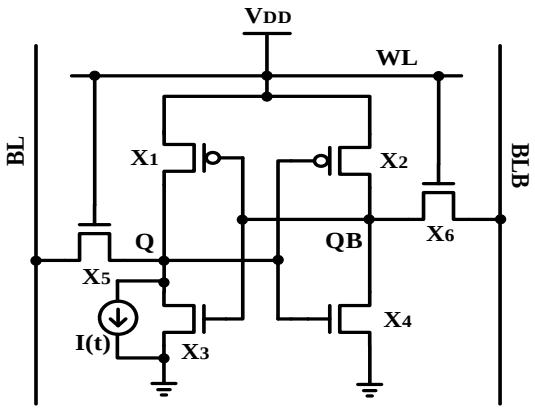

Figure 3. Standard 6T DLTFET SRAM cell.

To investigate the effect of SEU at the circuit level, a heavy ions strike can be modeled using a transient current pulse, which occurs for a very short period of time, as shown in Figure 3. This pulse represents the collected charges $Q_{collected}$ at node Q resulting from electron-hole pairs generated when heavy ion strikes at the respective node. The double exponential current model is widely used for determining the effect of SEU on circuit operations [25,26]. It is given by:

$$I(t) = I_0\{exp(-t/\tau_\alpha) - exp(-t/\tau_\beta)\},$$

where $I_0 = \frac{Q_{collected}}{\tau_\alpha - \tau_\beta}$ is the amplitude of the current pulse. τ_α and τ_β are the rising and falling time constants of the current pulse. For our analysis, I_0 is taken to be 5 mA, and τ_α and τ_β are taken to be 50 ps and 10 ps, respectively. Here, Q node is the impact node, so the current pulse is connected between node Q and the ground terminal. Let us say Q = 1 and QB = 0 and an ion strikes node Q at t = 0. The changes in the data stored at nodes Q and QB can be referred to as 1 to 0 upset at Q and 0 to 1 upset at QB. These effects are depicted in Figure 4. Therefore, SEU may cause a change in the state of an SRAM cell and, thus, degrades its performance. The transient voltage is observed at the above-described values of the I_0, τ_α and τ_β. For 1 to 0 upset at Q, due to the charge collected by the heavy ion attack, the voltage at the node of the drain of transistor X_3 is discharged to less than 0 V. This effect is shown in Figure 4a. For 0 to 1 upset at QB, the heavy ion strike causes a voltage shift "1" to "0" at node Q, which switches on transistor X_2 and turns off transistor X_4. Hence, the data or value stored at the node changes from "0" to "1". This effect is

shown in Figure 4b. It can be concluded from the above figure that after applying an exponential current source model at the drain of X_3, because of the radiation, the values at the storage node of DLTFET SRAM change. Hence the SRAM functionality is affected due to the introduction of radiation. The efficient working of the SRAM demands for this effect to be overcome. In this manuscript, a method has been suggested to mitigate the SEU effect at the transistor level itself.

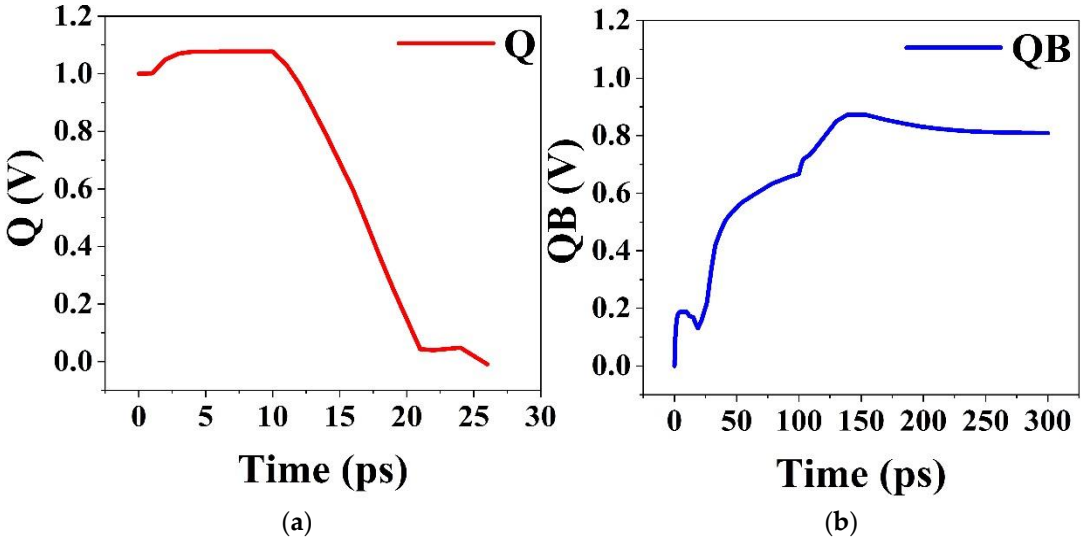

Figure 4. Output of GeDLTFET SRAM cell after strike of an ion at (**a**) node Q, and (**b**) node QB.

4. SEU Mitigation Using Radiation Hardening by Design Technique

To mitigate the effect of SEU, in the 6T Ge-DLTFET SRAM cell, the radiation-hardening-by-design technique has been employed. This technique uses two RC feedback paths, connected between the two cross-coupled inverters. The circuit for the 6T DLTFET SRAM cell, employing the RHBD technique, is shown in Figure 5. Here, R1 and R2 are chosen to be 50 Ohms, and C1 and C2 are chosen to be 10 pF. It has been assumed that logic 1 is stored at node Q, whereas logic 0 is stored at node QB.

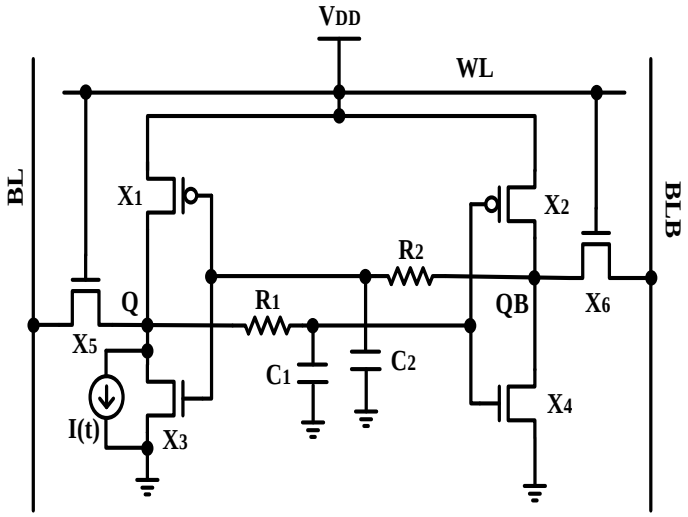

Figure 5. Radiation-hardened 6T Ge DLTFET SRAM cell.

The data recovery mechanism of the radiation-hardened Ge DLTFET SRAM cell is completed in two steps: (1) Due to the heavy ion strike at node Q, the voltage at node Q changes temporarily from '1' to '0'. Thus, X_4 transistor turns OFF for a short period of time.

The value of node Q deviates from '1' to '0' for a very short amount of time, as because of having the capacitor in feedback back path, the original value remains as it is. That keeps transistor X_1 always in an ON state. As a result, Q will revert to its original state of Logic 1. (2) Gain transistor X_4 turns back ON by restoring the data at node Q (from '0' to '1'). Thus, the data at node QB has also been recovered. The simulation result of the above circuit is shown in Figure 6. Figure 6 depicts the use of the RHBD technique on the 6T DLTFET SRAM cell, and it proves to be efficient enough to recover the data after a heavy ion strike. Hence, this section presents a method to relieve the SEU issue in Ge DLTFET SRAM cells.

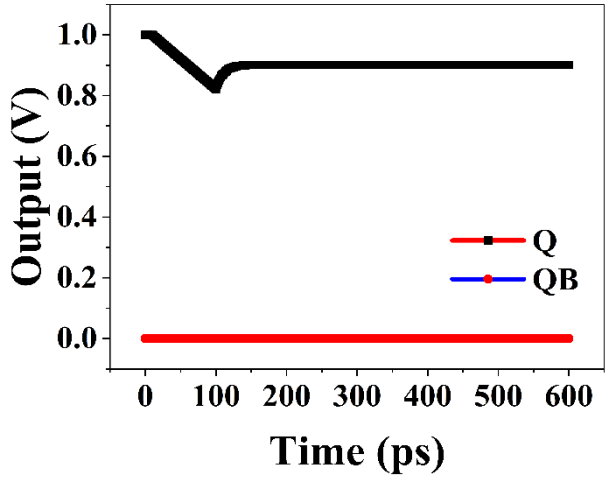

Figure 6. Output of RHBD-based Ge-DLTFET SRAM cell after strike of an ion at node Q and node QB.

5. Delay Analysis

The delay analysis of 6T Ge DLTFET has been conducted using the SPICE tool for various cases, such as before the introduction of radiation, after the introduction of radiation and when delaying the radiation-hardened cell. The delay obtained for our circuit has been compared with that in [27] and is shown in Figure 7. It has been found that the delay of the hardened 6T SRAM cell is higher when compared to a conventional 6T SRAM cell. This is because of the additional RC feedback path, which increases the delay of the circuit. The delay in the DLTFET-based SRAM has been decreased by 95.33% and 89% in comparison with DGTFET-based SRAM. Thus, using DLTEFT improves the delay performance of the SRAM compared to that of DGTFET [28].

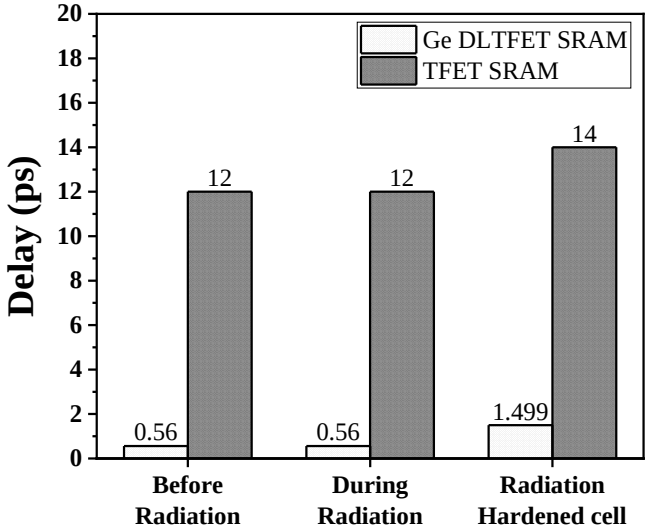

Figure 7. Delay of 6T Ge DLTFET and TFET SRAM cells under various conditions.

6. Stability Analysis Using N-Curve

The N-curve for the stability of an SRAM cell is obtained as given in [27]. The static voltage noise margin (SVNM) and static current noise margin (SINM) provide information regarding the stability of the SRAM cell during read operation, whereas write trip voltage (WTV) & write trip current (WTI) express the stability of the SRAM cell during the write operation [27,29]. The N-curve for conventional silicon TFET and Ge DLTFET-based SRAM cells is obtained and is recorded in Table 2. SVNM, SINM, WTV and WTI for both SRAM cells is calculated from their respective N-curves and is also shown in Table 2. There is an improvement in the SINM, WTV and WTI values of Ge DLTFET-based SRAM in comparison to a conventional Si TFET SRAM cell, whereas the SVNM value of the Ge DLTFET SRAM cell is lower.

The static power metrics, obtained from the N-curves of the SRAM cell, are called static power noise margin (SPNM) and write trip power (WTP) [9,10,30] and depict the stability of the SRAM cell during the read and write operation, respectively. For both SRAM cells, SPNM and WTV are calculated as the area covered by the N-curve above and below the horizontal axis, corresponding to a zero current value, respectively. The calculated SPNM and WTV values are given in Table 2. It is observed that the static power metric for the Ge DLTFET SRAM cell is better than that for the conventional Si TFET SRAM cell. Thus, there is a 305× & 850× improvement in the SPNM and WTP values of the Ge DLTFET based SRAM cell.

Table 2. Parameters obtained from N-curve for both SRAM cells.

Parameters	Conventional Si TFET-Based SRAM	Ge DLTFET-Based SRAM
SVNM	460 mV	150 mV
SINM	438.9 nA	434.4 µA
WTV	440 mV	580 mV
WTI	36.91 nA	29.45 µA
SPNM	2.98 µW	910 µW
WTP	347 nW	296 µW

7. Conclusions

In this paper, a radiation-hardened 6T SRAM cell has been implemented using Ge-DLTFET at a 50 nm technology node. As semiconductor materials are very sensitive to extreme radiation particles, especially at a lower technology node, due to the strike of high energy particles, the state of the SRAM cell gets changed. However, the employed RHBD technique prevents any change in the state of the SRAM cell, due to the SEU problem. RHBD is used to improve the soft-error performance or sensitivity of the 6T DLTFET SRAM cell. The implemented method proves effective in mitigating SEU but at the cost of an additional delay. Additionally, the delay parameter of the proposed SRAM cell using Ge DLTFET is improved with respect to that of a conventional Si-TFET-based SRAM cell. The static voltage current and power noise margins, obtained from the N-curves, are superior for our design, showing a better stability of the SRAM cell during read and write operations.

Author Contributions: P.R.: Resources, Supervision, Review and Editing. P.K.: Analysis and Investigation. M.P.: Supervision, Methodology, Review and Editing. P.D.: Original Draft Preparation, Interpretation of Results, Figure Preparation. K.C.: Supervision, Review and Editing. All authors have read and agreed to the published version of the manuscript.

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