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A *Ka*-Band Doherty Power Amplifier in a 150 nm GaN-on-SiC Technology for 5G Applications

Alessandro Parisi [1], Giuseppe Papotto [1], Claudio Nocera [1], Alessandro Castorina [1] and Giuseppe Palmisano [2,*]

[1] STMicroelectronics, 95121 Catania, Italy; alessandro.parisi@st.com (A.P.); giuseppe.papotto@st.com (G.P.); claudio.nocera@st.com (C.N.); alessandro.castorina@st.com (A.C.)
[2] Dipartimento di Ingegneria Elettrica Elettronica e Informatica (DIEEI), University of Catania, 95125 Catania, Italy
* Correspondence: giuseppe.palmisano@unict.it

Abstract: This paper presents a *Ka*-band three-stage power amplifier for 5G communications, which has been implemented in a 150 nm GaN-on-SiC technology and adopts a Doherty architecture. The amplifier is made up of a 50 Ω input buffer, which drives a power splitter, thanks to which it delivers its output power to the two power amplifier units of the Doherty topology, namely the main and auxiliary amplifier. Finally, the outputs of the two power amplifiers are properly arranged in a current combining scheme that enables the typical load modulation of the Doherty architecture, alongside allowing power combining at the final output. The proposed amplifier achieves a small signal gain of around 30 dB at 27 GHz, while providing a saturated output power of 32 dBm, with a power-added efficiency (PAE) as high as 26% and 18% at peak and 6 dB output power back-off, respectively.

Keywords: Doherty power amplifier; EM simulations; 5G; *Ka*-band; GaN; mm-wave; power-added efficiency

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1. Introduction

The 5G network is the key technology for the deployment of the next-generation communication systems. It envisages data rates of up to 100 Gbps, with ultra-low latency (i.e., lower than 1 ms), high reliability, and massive network capacity, with a simultaneous connection density higher than 1 M/km^2. This will enable a wide range of breakthrough applications under various environments, such as healthcare, home automation, etc. [1–3].

To support the stringent requirements of such applications, the 5G network relies on carrier frequencies in the *Ka*-band and allows extended bandwidth and alternative access techniques, such as beam division multiple access (BDMA) and massive MIMO [4]. Furthermore, highly spectral efficient modulation schemes have been adopted (e.g., 64-QAM OFDM modulation) by 5G communication systems, which lead to transmission signals with a high peak-to-average power ratio (PAPR), thus pushing the power amplifier (PA) to operate in a deeper output power back-off (OPBO) region. This scenario poses stringent requirements to the PA, which mainly sets the efficiency and linearity performance of the whole transceiver [5]. Specifically, increasing the efficiency of the PA while preserving linearity is mandatory in a 5G transceiver for both the reduction in the operating costs of the base stations and the enhancement in the battery lifetime of the handsets. Moreover, a high output power (i.e., in the range of a few watts) in the *Ka*-band is required to the 5G power amplifiers to increase the network coverage area.

The Doherty architecture is the best candidate for the implementation of mm-wave power amplifiers for 5G applications. A Doherty power amplifier (DPA) is made up of a main and an auxiliary amplifier and exploits load modulation to provide an optimum trade-off between efficiency and linearity.

In recent years, several mm-wave DPAs that were designed using CMOS and BiCMOS technology have been presented [6–8]. These works demonstrate the effectiveness of the Doherty architecture to guarantee linearity while preserving efficiency, but they exhibit an output power that is well below the typical requirements of 5G applications, leading to the request for high-order MIMO architectures. On the other hand, gallium nitride (GaN) is nowadays the reference technology for the implementation of high-power and efficient power amplifiers. Although, over-*W* output power mm-wave DPAs in GaN technology have been already demonstrated [9–14], these works suffered from a limited gain performance. This means that they require a high input power, thus transferring to the pre-amplifier design requirements, such as output power, linearity, and efficiency.

In this work, the design and characterization of a *Ka*-band DPA for 5G applications has been presented. The amplifier exploits a three-stage architecture and provides a small signal gain of around 30 dB at 27 GHz, while achieving a saturated output power, P_{SAT}, of 32 dBm with a power-added efficiency (PAE) as high as 26% and 18% at peak and 6 dB OPBO, respectively.

This paper has been organized as follows. Section 2 briefly discusses the Doherty operation, while Section 3 provides an insight on the GaN technology adopted and mainly deals with the DPA design and circuit solutions. Experimental results have been presented in Section 4, which also provides a comparison with the state of the art. Finally, conclusions have been drawn in Section 5.

2. The Doherty Operation

A Doherty power amplifier consists of a main and an auxiliary amplifier, which are properly arranged in a power-combining scheme to enable active load modulation and allow efficiency enhancement [15,16].

Figure 1a shows the well-known structure for the implementation of the Doherty architecture, which has been referred to as the current-combined DPA. The two current sources, I_M and I_A, represent the main and auxiliary amplifiers, respectively. The impedance-inverting network, which has been implemented through a quarter-wave transmission line with characteristic impedance Z_0, combines the power from both amplifiers into the load, R_L, and simultaneously downscales the impedance observed by I_M for optimum efficiency performance [15]. The load impedance of the main amplifier is modulated through the current of the auxiliary amplifier, as according to Equation (1):

$$Z_M = \frac{Z_0^2}{R_L\left(1 + \frac{I_A}{I'_M}\right)} \quad (1)$$

where I'_M is the current of the main amplifier that has been transformed via the impedance-inverting network. In the Doherty operation, the main and the auxiliary amplifier are usually operated in class AB and C [17–21], respectively. Therefore, a low (i.e., until OPBO) and a high (i.e., from OPBO to saturation) power region can be identified. In the low-power region, only the main amplifier is active and provides current to the load; in the high-power region, both amplifiers are active and load modulation properly occurs. Specifically, in the low-power region, according to Equation (1), the main amplifier output load is $Z_M = {Z_0}^2/R_L$ ($I_A = 0$), and its output voltage, V_M, linearly increases with the driving input voltage, V_i, until reaching its maximum value and, hence, its first peak of efficiency. As V_i increases, the auxiliary amplifier turns on and modulates the load impedance of the main amplifier to keep V_M to its maximum value and simultaneously increasing the output power. Once the output voltage of the auxiliary amplifier, V_A, reaches its maximum value, a second peak of efficiency occurs, which defines the saturation condition. Assuming a symmetrical Doherty configuration (i.e., the two amplifiers generating the same maximum current) Z_0 and R_L are to be set to R_{OPT} and $R_{OPT}/2$, respectively, where R_{OPT} is the optimum impedance of the amplifiers [20]. Figure 1b,c show the voltage and load impedance profile, respectively, versus the normalized input voltage for both amplifiers. It is worth noting that the load

impedance of the main amplifier is modulated from $2R_{OPT}$ to R_{OPT}, whereas its output voltage is kept constant at its maximum value thanks to the load modulation. On the other hand, the load impedance of the auxiliary amplifier changes from ideally infinity to R_{OPT}.

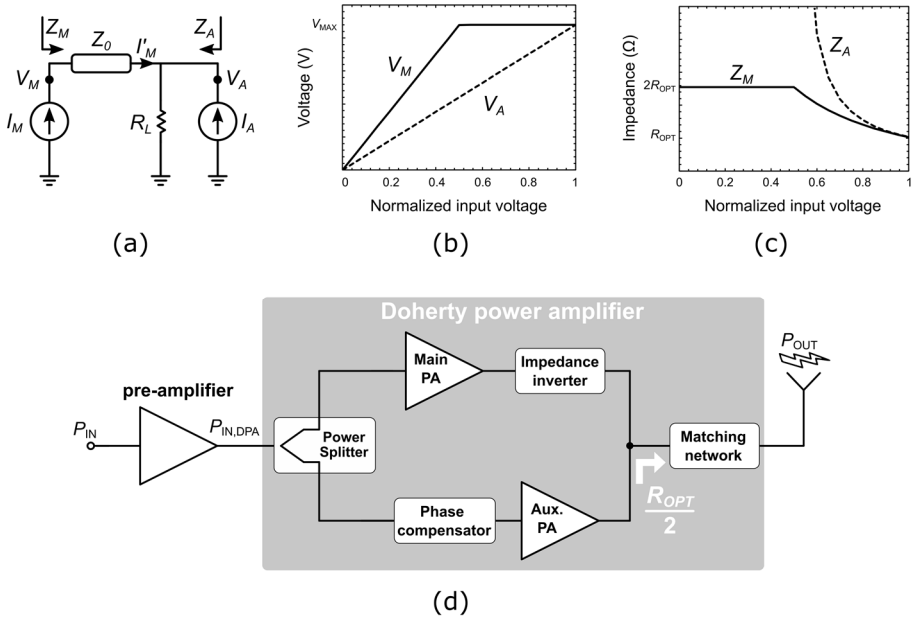

Figure 1. Doherty operating principle: (**a**) current combined structure, (**b**) corresponding voltages versus the normalized input voltage, (**c**) corresponding load impedances versus the normalized input voltage, and (**d**) simplified schematic of a Doherty power amplifier.

The simplified schematic of a DPA is shown in Figure 1d, which includes an input power splitter to drive both amplifiers, a phase compensator to compensate for the phase shift introduced by the impedance inverter, and an output matching network to transform the 50 Ω impedance of the antenna into the required Doherty load impedance (i.e., $R_L = R_{OPT}/2$).

3. Circuit Design

The proposed DPA was designed using GaN-on-SiC technology, which features a substrate thickness of 100 µm and provides high-electron-mobility transistors (HEMTs) with a gate length of 150 nm. These devices exhibit a transition frequency of 35 GHz, manage a power density of about 3 W/mm, and are defined via a scalable non-linear model qualified up to a 20 V operating drain voltage. As far as the back end of line (BEOL) is concerned, this technology provides two gold metal layers with a thickness of 1 µm and 4 µm, MIM capacitors with specific capacitance of around 215 pF/mm^2, and 50 Ω/square thin-film resistors. Moreover, it features through-wafer vias for low-inductance ground connections and air-bridge-based passive structures for optimum monolithic inductors.

A simplified schematic of the proposed *Ka*-band DPA is shown in Figure 2. It is based on a three-stage architecture, which allows a linear gain as high as 30 dB to be achieved. Specifically, the DPA is made up of a 50 Ω input buffer and two power units, namely the main and auxiliary PAs, which, in turn, are composed of a driver and a power stage. The input buffer supplies both the main and auxiliary branches by means of a proper power splitter connected to the driver inputs, whereas the power output terminals are arranged in a current combining scheme, which includes the impedance inverter for proper load modulation.

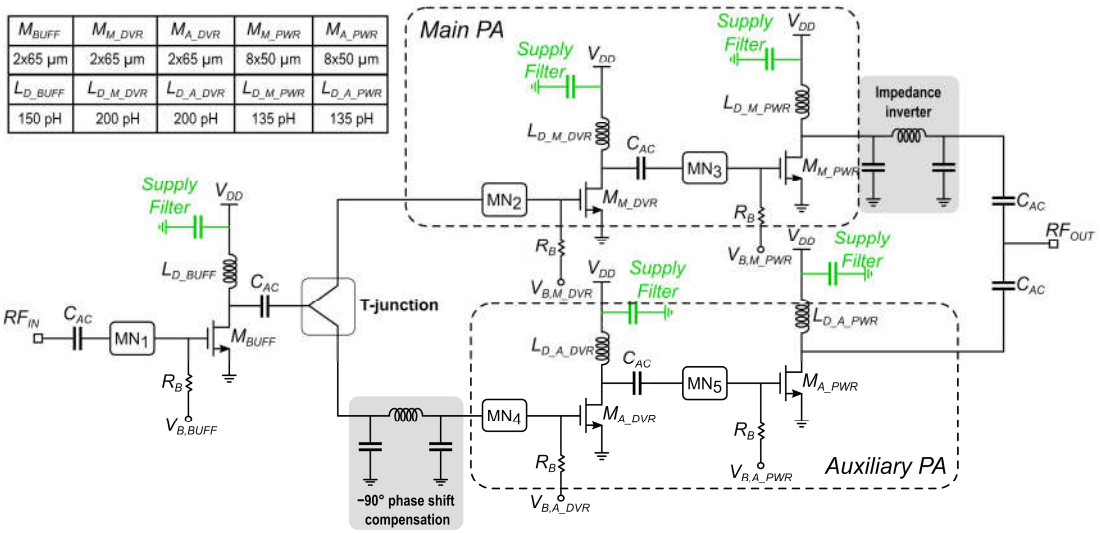

Figure 2. Simplified schematic of the proposed *Ka*-band DPA.

Distinct from the conventional implementation (see Figure 1d), here the output matching network that transforms the 50 Ω load into the impedance required by the Doherty architecture (i.e., $R_{OPT}/2$ in Figure 1d) [22] has been avoided. In this way, all the limitations related to this matching network in terms of power loss, area occupation, and bandwidth have been overcome. Figure 3 shows a 28 GHz load-pull simulation for a transistor whose gate width ranges from 200 to 600 µm. This simulation provides the optimum load resistance, R_{OPT}, and the corresponding output power, P_{OUT}, assuming a class AB operation.

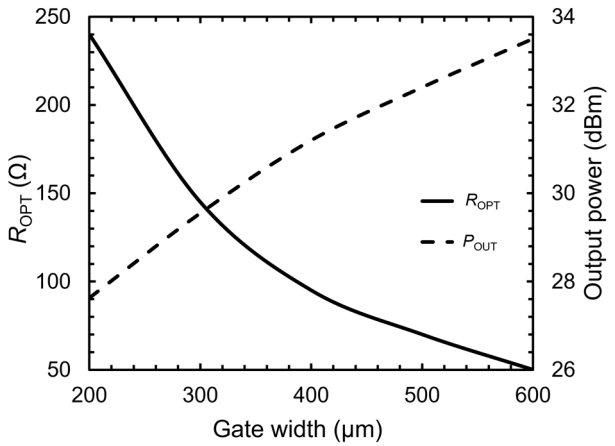

Figure 3. Load-pull simulations of a GaN transistor versus the gate width: optimum load resistance and delivered output power at 28 GHz.

It is important to note that only the imaginary part of the optimum load needs to be tuned to the operating frequency, whereas the real part is not appreciably affected by the frequency. As apparent, a transistor with a gate width of 400 µm needs an optimum load of 100 Ω, which allows the output matching network to be avoided. Accordingly, a 400 µm transistor with eight gate fingers, each of 50 µm, was used for both the main and auxiliary power stages, thus implementing a symmetrical Doherty configuration with the aim of achieving an OPBO of 6 dB. Neglecting impedance inverter losses and assuming a 31 dBm output power (see Figure 3) for each power stage, a maximum output power of 34 dBm is achieved. A gate width of 130 µm (i.e., 2 × 65 µm) was set for both the input buffer and driver stages as a fair trade-off between driving capability and power

consumption, with the aim of preserving PAE performance. Moreover, shunt inductors, L_D, are sized to absorb the residual drain parasitic capacitance of the transistors, which are not compensated through the interstage matching networks (MNs), thus improving the frequency performance. Although a symmetrical configuration, the main and auxiliary amplifiers differ in their class of operation. Specifically, the main PA stages are operated in class AB by setting the gate-source voltage to around −1.7 V, while the auxiliary PA stages are operated in deep class C with the gate-source voltage at around −2.2 V.

As far as the design of passive structures is concerned, a lumped-based approach was preferred over the distributed one, with the aim of reducing area occupation. Specifically, the impedance inverter at the output of the main power stage was implemented through exploiting a π network, whereas the power splitter was based on a T-junction architecture with a splitting factor of 1:1.5 for the main and auxiliary branches, respectively. Accordingly, a π network was included at the input of the auxiliary path to compensate for the 90° phase shift caused by the impedance inverter.

Figure 4 shows the passive circuitry of the designed DPA, which includes inductors, capacitors, through-wafer vias, and interconnections among components. All the inductors were designed by stacking the two metal layers available in the adopted technology, thus increasing the Q-factor. The layout of the overall amplifier was partitioned into four entries for EM simulation purposes, with the aim of accurately estimating interconnection parasitics and undesired coupling effects.

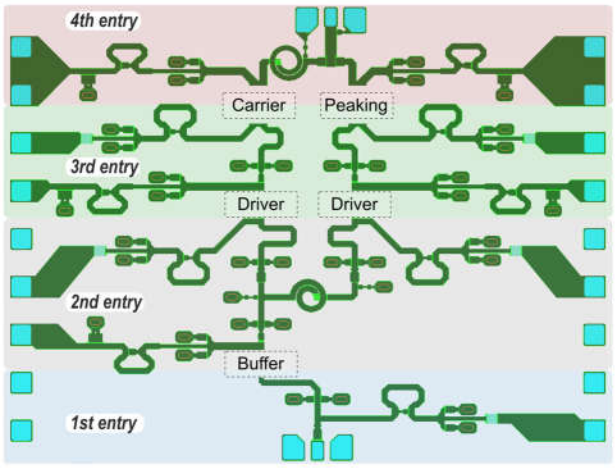

Figure 4. Passive circuitry of the Doherty power amplifier.

An S-parameter model of each entry of the EM simulator was extracted and embedded into the main schematic to finely tune transistor aspect ratios and matching networks for the optimum PA performance.

4. Experimental Results

Figure 5 shows the chip micrograph of the proposed *Ka*-band DPA, whose die size is 3.1 mm × 2.5 mm. Extensive on-wafer measurements were performed using a Cascade probe station to characterize the power amplifier. Specifically, bias voltages and mm-wave signals were directly probed on the die by means of dedicated on-chip pads.

For the sake of completeness, Figure 6 shows the adopted measurement setup, in which the mm-wave input signal is provided by a R&S SMW200A vector signal generator, whereas the amplifier output signal is delivered by means of a Keysight 87301C directional coupler to the Agilent E4417A power meter for power measurements and the Keysight UXA N9040B signal analyzer for spectrum analysis. All measurements were performed using a 20 V power supply under a continuous wave (CW) mode.

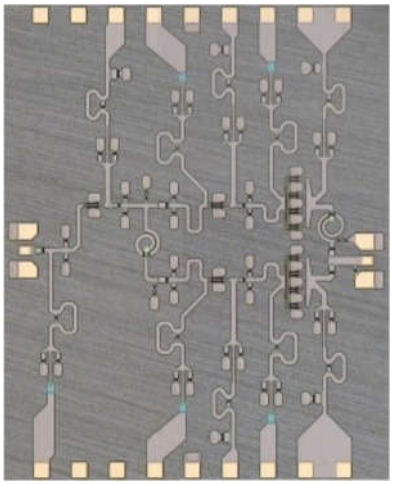

Figure 5. Chip microphotograph of the *Ka*-band DPA.

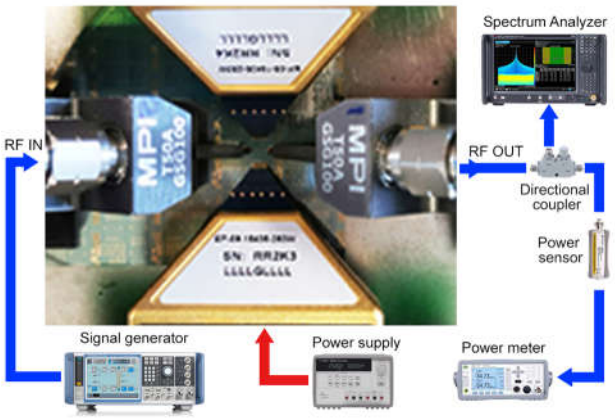

Figure 6. DPA measurement setup.

Figure 7 shows the measured S-parameters. As apparent from Figure 7a, good values of input (−S11) and output (−S22) return losses were achieved, which were both better than 10 dB at the operating frequency of 27 GHz. Moreover, the measured reverse isolation (−S12) was higher than 40 dB, and a small-signal gain (S21) as high as 30 dB was obtained, as shown in Figure 7b.

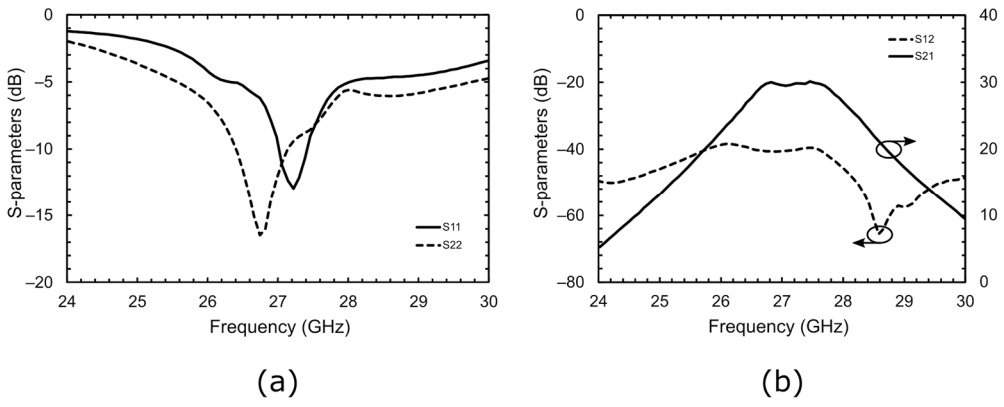

Figure 7. Measured S-parameters: (**a**) input (-S11) and output (-S22) return loss, and (**b**) small-signal gain (S21) and reverse isolation (-S12).

Figure 8 shows the measured output power and gain as a function of the input power at 27 GHz. As apparent, the proposed DPA delivered a maximum output power of about 32 dBm, while achieving linear and saturated gains as high as 30 dB and 22 dB, respectively.

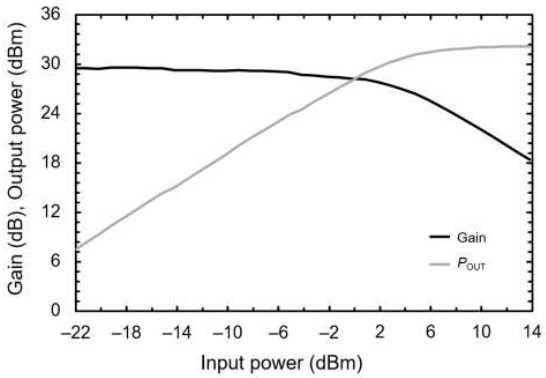

Figure 8. Measured P_{OUT} and gain as a function of P_{IN}.

Figure 9 compares the measured PAE at 27 GHz with the efficiencies of ideal class-A and class-B amplifiers, which have all been assumed with an equal PAE at P_{SAT}. A peak PAE of 26% was achieved while, thanks to the Doherty operation, the PAE at 6 dB OPBO was about 18%, which is higher by factors of 2.75 and 1.4 than the PAE of the ideal class-A and class-B PAs, respectively.

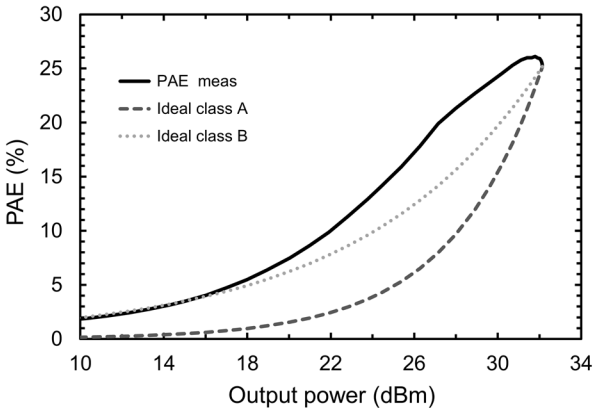

Figure 9. Measured PAE as a function of P_{OUT}, along with a comparison of efficiency between the ideal class-A and class-B PAs.

Figure 10 shows the measured saturated output power over a frequency range from 26 GHz to 28 GHz. The DPA exhibits a 1 dB bandwidth of around 1 GHz. The PAE for the 6 dB OPBO in the 1 dB bandwidth has also been shown; it is almost flat, being around 18%.

P_{SAT} was measured over all available samples (i.e., 30 samples) distributed on the same wafer for a statistical evaluation. The result is shown in Figure 11. As apparent, the average P_{SAT} and its standard deviation, σ, are around 31.8 dBm and 0.5 dB, respectively.

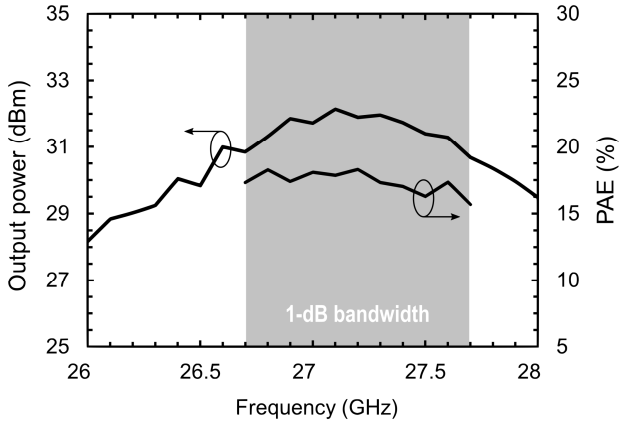

Figure 10. Delivered output power as a function of the frequency and 6 dB OPBO PAE over the 1 dB bandwidth.

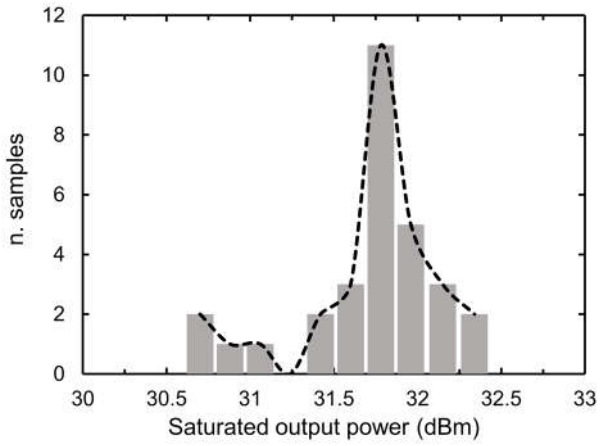

Figure 11. Distribution of the saturated output power over 30 samples.

The DPA was also characterized with a 64-QAM 5G NR downlink-modulated signal to assess its inherent linearity. This signal exhibited a PAPR of around 11 dB. The signal bandwidth was set to 20 MHz due to the frequency limitations of the available measurement setup. Figures 12 and 13 show the measured received constellation and normalized output power spectrum. An EVM and an ACPR lower than 5% and −32 dBc were achieved, respectively, with an average output power, $P_{OUT,AVG}$, of 19 dBm. Moreover, the proposed DPA met the 5G linearity requirements [23], i.e., an EVM < 8% and an ACPR < −28 dBc, with a $P_{OUT,AVG}$ of up to 21 dBm.

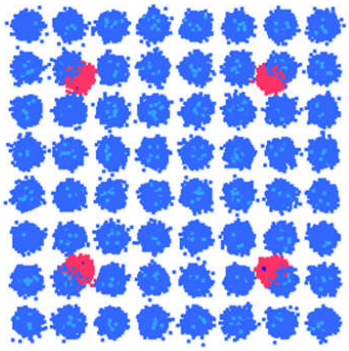

Figure 12. Measured received constellation at $P_{OUT,AVG}$ = 19 dBm.

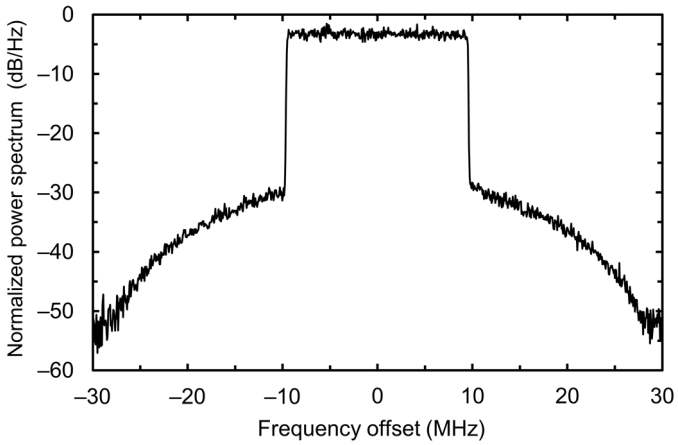

Figure 13. Measured normalized power spectrum at $P_{OUT,AVG}$ = 19 dBm.

Finally, Table 1 summarizes the DPA experimental results, while comparing them with the state-of-the-art *Ka*-band GaN works. A higher PAE performance has been reported by the authors of [12,13], while the authors of [9,11,12] achieved a higher output power level. However, all these works exhibited a much lower gain performance, which greatly increased their pre-amplifier requirements in terms of maximum output power, linearity, and efficiency, thus negatively affecting the system complexity and cost in addition to the overall transmitter performance.

Table 1. Performance comparison with the state-of-the-art *Ka*-band DPAs.

	[9]	[10]	[11]	[12]	[13]	This Work
Channel length [nm]	150 *	150 *	150 *	150 *	100 **	150 *
Frequency [GHz]	28	26	28	30	28	27
P_{SAT} [dBm]	34	32	35.6	36.5	33	32.1
Linear gain [dB]	20	13.6	15.8	15.7	13.7	30
Saturated gain [dB]	10	8	12	10	12.5	22
PAE_{MAX} [%]	22	21.7	25.5	31.8	36.2	26
PAE @ 6 dB OPBO [%]	15	20	22.7	27	30	18
V_{DD} [V]	20	24	24	24	12	20
Die size [mm^2]	15.6	5	4.3	3.5	6	7.75
FoM [W/mm^2]	0.05	0.09	0.77	1.1	0.64	1.5

* GaN-on-SiC; ** GaN-on-Si.

For a fair comparison, the following figure of merit (FoM), was used:

$$\text{FoM}\left[\frac{\text{W}}{\text{mm}^2}\right] = \frac{P_{\text{SAT}} \times G_{\text{SAT}} \times PAE_{\text{MAX}} \times PAE_{-6\text{dB}}}{die\ size}$$

As apparent, the proposed DPA offers the best trade-off between the performance parameters, such as power density, saturated gain, and PAE.

5. Conclusions

This paper presents a *Ka*-band Doherty power amplifier implemented in a 150 nm GaN-on-SiC technology. The amplifier is based on a three-stage architecture and was designed with the aim of providing both a high output power and a high gain with suitable PAE performance to properly address the crucial issues of 5G GaN PAs. Extensive on-wafer measurements were carried out, including a statistical analysis that proved the robustness of the DPA design. The amplifier delivers up to 32 dBm with a PAE of 26%, while guaranteeing an excellent saturated gain as high as 22 dB. Finally, measurements with a 5G-modulated signal were carried out, achieving an EVM < 8% and an ACPR < −28 dB, with an average output power of 21 dBm.

Author Contributions: Conceptualization, A.P., G.P. (Giuseppe Papotto) and G.P. (Giuseppe Palmisano); methodology, A.P., C.N. and G.P. (Giuseppe Papotto); validation, A.C., A.P. and G.P. (Giuseppe Papotto); formal analysis, A.P. and C.N.; investigation, A.P., C.N. and A.C.; writing—original draft preparation, A.P. and G.P. (Giuseppe Papotto); writing—review and editing, A.P. and G.P. (Giuseppe Palmisano); supervision, G.P. (Giuseppe Papotto); project administration, G.P. (Giuseppe Palmisano). All authors have read and agreed to the published version of the manuscript.

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