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A 110 GHz Feedback Amplifier Design Based on Quasi-Linear Analysis

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Abstract: The power gain and output power of millimeter-wave (mm-Wave) and terahertz (THz) amplifiers are critical performance metrics, particularly when the operating frequencies of amplifiers are near to the maximum oscillator frequency (f_{max}) of the transistor. This paper presents the design of a 110 GHz amplifier based on the quasi-linear method. The power gain can be boosted to maximum achievable gain (G_{max}) using a linear, lossless, reciprocal feedback network, though this leads to a simultaneous decrease in output power. Based on quasi-linear analysis, for an amplifier with G_{max} gain, when the K-factor is equal to 1, the output power is zero. To avoid the very low output power of amplifiers, a new approach is proposed to balance power gain and output power. A 110 GHz six-stage feedback amplifier was designed using the proposed approach and fabricated using 40 nm CMOS technology. The measured power gain is 26.5 dB, and the saturation output power is 13 dBm at 110 GHz.

Keywords: feedback amplifiers; maximum achievable gain; millimeter-wave integrated circuits; terahertz

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1. Introduction

Millimeter-wave (mm-Wave) and terahertz (THz) frequencies offer vast bandwidth and enable a variety of applications, including ultra-high-speed wireless communication, imaging, and medical sensing [1,2]. Amplifiers play a crucial role in transmitters (TXs) and receivers (RXs). Indeed, with the advancement of modern communication and imaging technologies, there is a strong demand for amplifiers operating in the W-band (75–110 GHz) and beyond [3]. For example, a broadband amplifier with cascaded stagger-tuned stages for 100+ GHz was realized in [4–6], introducing a 110–180 GHz broadband amplifier with 10 dB gain and a 70–110 GHz broadband amplifier with over 15 dB gain, respectively. However, when the operation frequency of an amplifier is very high, the gain of the intrinsic transistor is quite low [7,8]. So, previous research has focused on achieving high power gain in mm-Wave and THz.

One of the most useful methods of boosting power gain is to construct feedback networks [9–21]. As shown in Figure 1, the power gain of a two-port network can achieve the maximum achievable gain G_{max} by embedding feedback networks. The G_{max} is only related to the unilateral gain (U, Mason's invariant), which can be used as a figure of merit to compare any active two-port device. The relationship between the power gain and Rollet's stability factor (K-factor, K) and U has been researched [9,10,22,23]. The G_{max} is the peak value of G_{ma}; we can obtain the amplifier with a gain of G_{ma} or G_{max} via input and output conjugate matching [12].

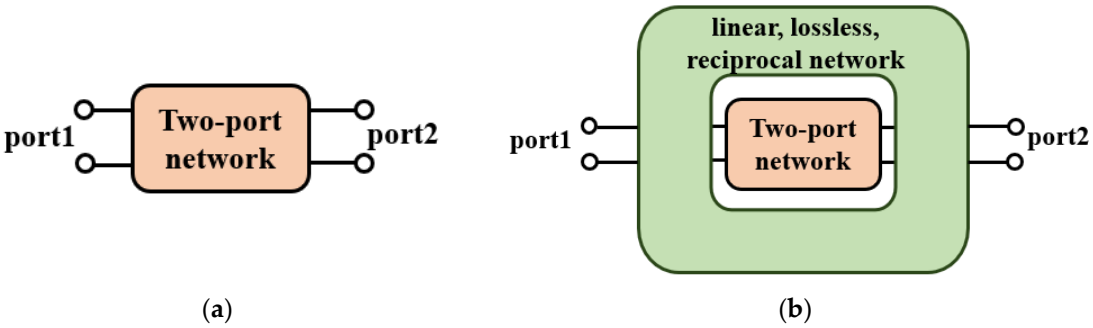


Figure 1. (**a**) Basic two-port network. (**b**) The two-port network of an embedded linear, lossless, reciprocal feedback network.

The work in [18] achieves G_{max} by boosting gain, but the saturation power is only 0.09 dBm at 247 GHz and −2.36 dBm at 272 GHz. A lossy capacitive over-neutralization technique was proposed to increase U for an amplifier with 14.3 dB of gain and only 1.5 dBm of saturation power [19]. For the feedback amplifier, embedding is used to boost gain and a power combiner is used to increase saturation power in [20,21], which explore inductive gain-boosting power amplifiers to achieve a higher saturation power while maintaining a high G_{max}. However, this paper does not propose a general method to balance gain and output power. Additionally, the saturation output power of amplifier is not well researched when it is boosted to G_{max}. Previous research studies focus on the gain in most cases; they ignore the change in output power when K = 1. To investigate this phenomenon, this paper analyzes a two-port network, and a set of formulas are derived based on a quasi-linear model. For feedback amplifiers, the relationship between power gain and K-factor and the relationship between output power and K-factor are all analyzed. These analyses reveal that G_{max} should not be the design target from the view of trade-off because the saturation output power degrades dramatically. Thus, a new approach is proposed to balance power gain and output power. With the proposed approach, a six-stage differential amplifier was designed and fabricated using 40 nm CMOS technology. The measured results demonstrate a power gain of 26.5 dB and saturation output power of 13 dBm at 110 GHz.

The structure of this paper is as follows: Section 2 presents an analysis of the gain of amplifiers, including the G_{ma}, U, and G_{max}. Section 3 analyzes the output voltage and power and analyzes the impedance matching and the sensitivity of G_{max} when K-factor is near to 1, which are all based on the quasi-linear method. Section 4 shows the feedback amplifier design methodology. Section 5 presents the proposed 110 GHz feedback amplifier, which utilizes a novel approach. Section 6 presents the measured results of the fabricated six-stage amplifier. Finally, Section 7 sums up the paper.

2. Gain of Amplifier

2.1. G_{ma}, and K-Factor

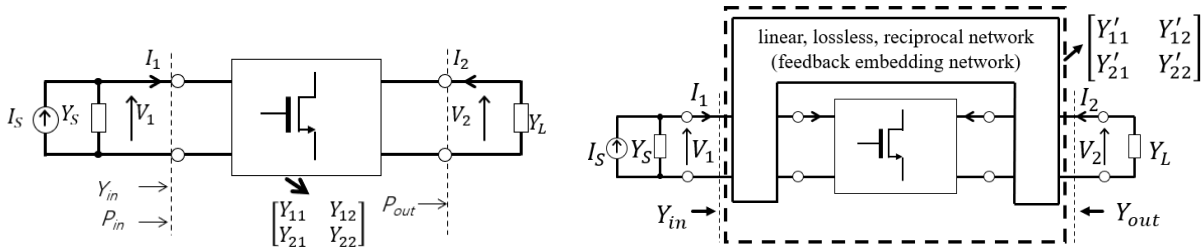
A mm-wave and THz amplifier can be modeled as a two-port network for quasi-linear analysis, as shown in Figure 2. Here, the transistor core is modeled as Y-parameters, and the current and voltage on both sides is I_1, V_1 and I_2, V_2. The input source is modeled as the current source I_S with source admittance Y_S. In addition, the load admittance is Y_L.

An amplifier with G_{ma} (maximum available gain, MAG) can be obtained via the simultaneous conjugate impedance matching of input and output if K > 1. For the two-port network, the G_{ma} is the ratio of the power delivered to the load to the power available from the source, and G_{ma} can be derived by the Y-parameters of the two-port network and K-factor, as shown in (1) [23]. This is achieved when input and output impedance matching are simultaneously realized. For an unconditional stable amplifier, its K-factor is more than 1, and only under such conditions can the G_{ma} can be defined. If the operation frequency is quite high and near to f_{max}, K $\geq$ 1 is generally satisfied because the gain of transistor is

low. The expression of K-factor is shown in (2) [24]. It is important to note that if K < 1, simultaneous conjugate impedance matching cannot be realized.

$$\mathrm{K} = \frac{2Re(Y_{11})Re(Y_{22}) - Re(Y_{12}Y_{21})}{|Y_{12}Y_{21}|} \tag{1}$$

$$G_{ma} = \left|\frac{Y_{21}}{Y_{12}}\right| \frac{1}{\mathrm{K}+\sqrt{\mathrm{K}^2-1}} \tag{2}$$



(**a**) (**b**)

Figure 2. (**a**) Quasi-linear model for amplifiers. (**b**) Quasi-linear model with feedback network for amplifiers.

2.2. Unilateral Power Gain

In electronics, U is a measure of the quality of transistors, which is given in (3) with Y-parameters [24]. The G_{ma} is equal to U when the transistor is unilateralized. Figure 2b shows an example of the quasi-linear model with a feedback network. The feedback embedding network is also modeled as Y-parameters; to distinguish it, it is represented by $[Y']$. The linear, lossless, reciprocal feedback network does not change the value of U [25].

$$U = \frac{|Y_{21} - Y_{12}|}{4(Re[Y_{11}]\cdot Re[Y_{22}] - Re[Y_{12}]\cdot Re[Y_{21}])} \tag{3}$$

2.3. Maximum Achievable Gain

G_{max} is the up limit of G_{ma}, which is shown in (4). The G_{ma} can be boosted to G_{max} via a linear, lossless, reciprocal feedback network. As (4) shows, G_{max} is only related with U, so it is also a figure of merit for a given two-port network. In other words, for a given two-port network, the G_{max} is invariant [25]. Additionally, if $U \gg 1$, G_{max} approaches to $4U$, and G_{max} is 6 dB larger than U. An amplifier with the power gain of G_{max} can be obtained by tuning the feedback network and conjugate matching the input and output impedance. When designing high-gain amplifiers, G_{max} gives the guideline for the gain capability at millimeter-wave (mm-Wave) and terahertz (THz) frequency.

$$G_{max} = \max(G_{ma}) = 2U - 1 + 2\sqrt{U(U-1)} \tag{4}$$

2.4. λ-Plane

Define λ in (5) so that G_{ma} can be shown by K and λ in (6). It is noted that λ is complex. The U of a two-port network can be written as a function of G_{ma} and λ, as shown in (7) [9].

$$\lambda = \frac{Y_{12}}{Y_{21}} \tag{5}$$

$$G_{ma} = \left|\frac{Y_{21}}{Y_{12}}\right| \frac{1}{\mathrm{K}+\sqrt{\mathrm{K}^2-1}} = \left|\frac{1}{\lambda}\right| \frac{1}{\mathrm{K}+\sqrt{\mathrm{K}^2-1}} \tag{6}$$

$$\sqrt{\frac{G_{ma}}{U}} = \left| \frac{\frac{1}{\lambda} - G_{ma}}{\frac{1}{\lambda} - 1} \right| (\mathrm{K} > 1) \tag{7}$$

Here, we only consider the unconditional stable (K > 1). Because U is invariant, G_{ma} can be boosted with the change in λ. In fact, given U and G_{ma}, (7) can be represented as a circle. The G_{ma}-circle will draw on λ-plane. The function of the G_{ma}-circle is shown in (8).

$$(\lambda_{re} - \frac{U-1}{UG_{ma}-1})^2 + \lambda_{im}^2 = \frac{(G_{ma}-1)^2}{(UG_{ma}-1)^2} \cdot \frac{U}{G_{ma}} \tag{8}$$

where λ_{re} and λ_{im} represent the real and imaginary parts of λ, respectively. The G_{ma}-circle cannot be drawn if K < 1. In order to draw the boundary of the cluster of the G_{ma}-circle, formulas (3) and (5) can be substituted into (1), and the K-factor can be expressed as (9):

$$\mathrm{K} = \frac{|\frac{1}{\lambda}|^2 + 2(U-1)Re\left(\frac{1}{\lambda}\right) + 1}{2|\frac{1}{\lambda}|U} = \frac{(\lambda_{re}^2 + \lambda_{im}^2) + 2(U-1)\lambda_{re} + 1}{2U\sqrt{\lambda_{re}^2 + \lambda_{im}^2}} \tag{9}$$

Figure 3 shows the G_{ma}-circle and boundary on the λ-plane. The λ-plane is employed for amplifier design. According to equation (7), G_{ma} is only related to λ and U, where U is a constant value. Hence, G_{ma} is solely dependent on λ. The curve of K = 1 is a teardrop shape as the unconditional stable range (K > 1) is inside the teardrop. All the G_{ma} values should exist in the K > 1 range. The larger G_{ma} is closer to the left apex of the curve. For the G_{max}, its G_{ma}-circle shrinks into a point. The maximum G_{ma} is realized at the leftmost point on the curve of K = 1, which is the G_{max}. The leftmost point is on the real axis [17]. Using the graphical approach, it is easy to figure out that G_{ma} can be boosted to G_{max} under two conditions: (1) if K = 1 and (2) if $\lambda_{im} = 0$ [12,13]. Readers who wish to know more can read reference [17].

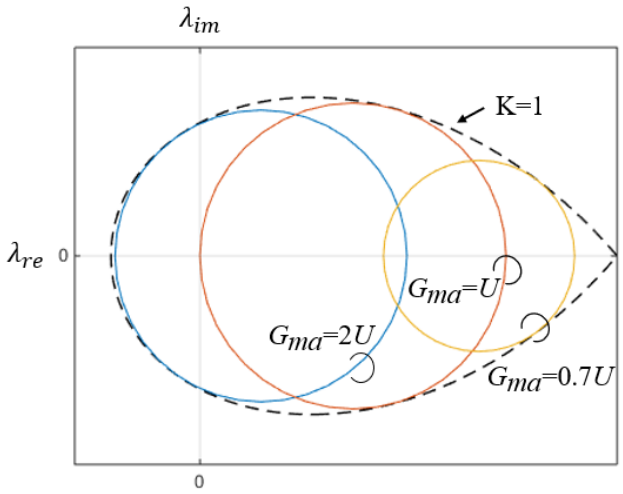


Figure 3. An example of λ-plane with the curve of K = 1, $G_{ma} = 2U$, $G_{ma} = U$, $G_{ma} = 0.7U$.

3. Discussion Based on Quasi-Linear Analysis

This section analyzes the linearity and saturation output power when the K approaches 1. Figure 2 is used in the quasi-linear analysis. The following discussion applies to any amplifier and is not limited to feedback amplifiers.

3.1. Output Voltage

Based on the above analysis, if an amplifier needs to achieve the gain of G_{ma} or G_{max}, simultaneous conjugate impedance matching is necessary for both. Based on the quasi-

linear analysis shown in Figure 2, if the simultaneous conjugate impedance matching is realized, the output voltage V_2 is shown in (10). The complete derivation of (10) is shown in Appendix A.

$$V_2 = \frac{-2Re(Y_{11})Re(Y_{22})Y_{21}}{|Y_{21}Y_{12}|(Y_{21}Y_{12} + |Y_{21}Y_{21}|(\sqrt{K^2-1}+K))\sqrt{K^2-1}} I_S \tag{10}$$

It can be observed that K = 1 is a pole for V_2. If the K-factor is near to 1, the V_2 must be very high, even with small source current I_s. However, V_2 cannot be very high because it is usually limited by the supply voltage of amplifier. Thus, we can predict that the linearity of amplifier will degrade greatly when the K is approaching 1.

3.2. Output Power

Thus, we can observe input and output power, which are shown as (11) and (12). Generally, the real part of Y_{22} is not zero. Thus, for a given I_S, the K-factor mainly affects the input and output power values. If K = 1, the input power P_{in} and output power P_{out} are zero. This means that the amplifier cannot absorb any power from the source and cannot deliver any power to the load either when K = 1. For a feedback amplifier, if the power gain is boosted to G_{max}, the input and output power are zero. Thus, G_{max} cannot be chosen for the design target.

$$P_{in} = Re\left(\frac{1}{Y^*_{S\_opt}}\right)|I_s|^2 = \frac{|Y_{12}Y_{21}|\sqrt{K^2-1}}{2Re(Y_{22})}|I_s|^2 \tag{11}$$

$$P_{out} = P_{in}G_{ma} = \frac{|Y_{21}|^2\left(K+\sqrt{K^2-1}\right)\sqrt{K^2-1}}{2Re(Y_{22})}|I_s|^2 \tag{12}$$

3.3. Impedance Matching

The real part of optimal source impedance Z_{S_opt} is shown as (13). It is zero when K = 1, so the optimal source reflection coefficient Γ_{S_opt} is located on the edge of the Smith chart, which is shown in Figure 4a. In cases where K < 1, achieving simultaneous conjugate impedance matching becomes impossible. This is illustrated in Figure 4b, which depicts S11 and VSWR during conjugate matching; the matching process is close to the edge of the Smith chart. As a result, impedance matching necessitates a high degree of precision. As a result, if the reflection coefficient is located on the edge of the Smith chart, impedance matching to 50 Ohm cannot be realized with lossless components; thus, a lossy impedance matching network must be used. If the power gain is very near to G_{max}, the Γ_{S_opt} is very near to the edge of the Smith chart; therefore, we can predict that impedance matching will be difficult to realize and that the impedance matching network will be quite narrow or lossy.

$$Re\left(Z_{in_{opt}}\right) = Re\left(Z^*_{s_{opt}}\right) = Re\left(\frac{1}{Y^*_{S\_opt}}\right) = \frac{|Y_{12}Y_{21}|\sqrt{K^2-1}}{2Re(Y_{22})} \tag{13}$$

3.4. Sensitivity of G_{max}

The sensitivity of G_{max} is analyzed by differentiating G_{ma} with respect to K, and it is found that G_{ma} is sensitive when K near to 1. We derivate the G_{ma} by K to see the slope. The result is shown in (14). It is divided into two terms; the right term is infinite when K = 1. Thus, the value of G_{ma} will be infinite when K = 1. Subsequently, it is impossible for gain to achieve G_{ma}; the gain will be limited by other conditions.

$$\frac{\partial G_{ma}}{\partial K} = \frac{\partial}{\partial K}\left(\left|\frac{Y_{21}}{Y_{12}}\right|\frac{1}{K-\sqrt{K^2-1}}\right) = \frac{1}{K-\sqrt{K^2-1}}\frac{\partial}{\partial K}\left(\left|\frac{Y_{21}}{Y_{12}}\right|\right) + \left|\frac{Y_{21}}{Y_{12}}\right|\frac{\partial}{\partial K}\left(\frac{1}{K-\sqrt{K^2-1}}\right) \tag{14a}$$

$$= \frac{1}{K - \sqrt{K^2 - 1}} \frac{\partial}{\partial K} \left(\left| \frac{Y_{21}}{Y_{12}} \right| \right) - \left| \frac{Y_{21}}{Y_{12}} \right| \left(\frac{1}{K - \sqrt{K^2 - 1}} \right)^2 \left(1 - \frac{K}{\sqrt{K^2 - 1}} \right) \quad (14b)$$

Figure 5 shows the slope of G_{ma} when K is near 1. G_{ma} degrades dramatically when K is slightly deviating from the 1. This means that G_{max} is also very sensitive. Our analysis revealed that the gain should not be boosted to G_{max}. Instead, a trade-off between power gain and output power is proposed.

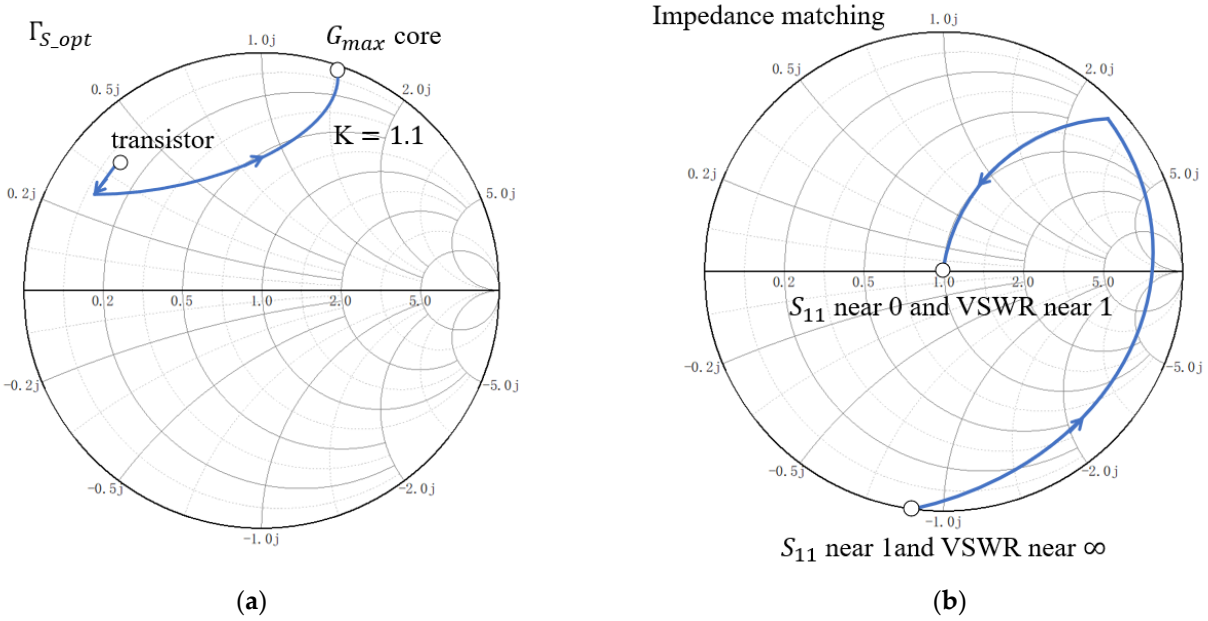


Figure 4. (**a**) The optimal source reflection coefficient Γ_{S_opt} on the Smith chart. (**b**) The S_{11} and VSWR in the process of impedance matching.

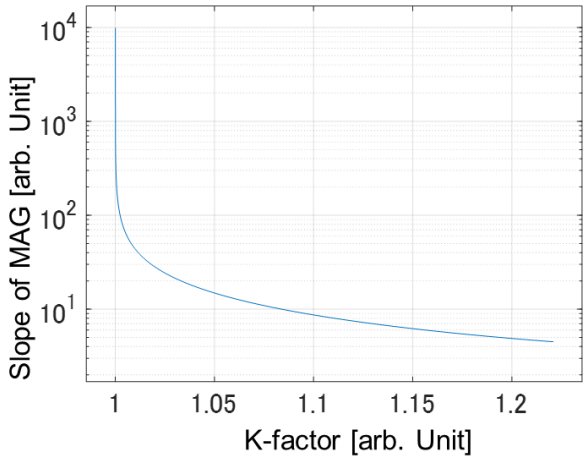


Figure 5. The slope of G_{ma} versus K-factor. The value becomes infinite when K = 1.

4. Feedback Amplifier Design Methodology

4.1. Boost the Power Gain

Several topologies of the feedback network can boost the power gain to G_{max} [12–16]. Here, we use the topologies in Figure 6 as an example. Figure 6 shows equivalent single-ended and differential topologies. The feedback admittance *-jB* for the single-ended topology is equivalent to the *jB* for the differential configuration. Here, a comprehensive design theory for amplifiers is taken into account, including the consideration of stability. The amplifiers of the proposed two topologies are unconditionally stable. Regarding the two-

port network, in this example, the embedding structure is parallel and cascade embedding. Cascade embedding, which is formed by TL_1 and TL_2, can expand the scope of movement on the λ plane. In the single-ended topology, a series of connections involving the inductor and capacitor forms the negative parallel feedback susceptance $-jB_f$. By the equivalent analysis of the two topologies, the cross-coupling of two capacitors forms parallel embedding, and the parallel feedback susceptance is reversed to jB_f. We assume that the source and load impedance are simultaneous conjugate impedance matching so that the power gain is G_{ma}. The design process is demonstrated on a six-stage amplifier in Section 5. An NMOS (32 μm/40 nm in size) is created via a 40 nm bulk CMOS process. The f_{max} of the NMOS is about 275 GHz. The design frequency is 110 GHz. The U is 8.9 dB.

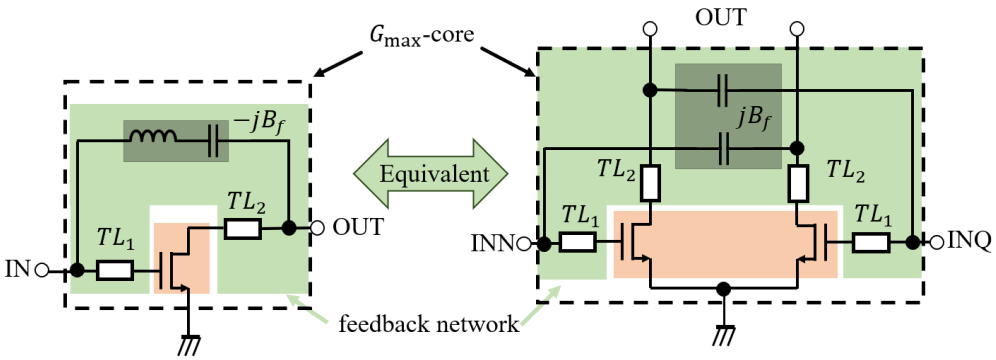


Figure 6. Single-ended and differential topology for boosting the power gain to G_{max}.

It is convenient and intuitive to design a feedback network on the λ plane [10,17]. The power gain of single-ended and differential intrinsic transistors can also be boosted to G_{max} core via the feedback network. Figure 7 shows the gain boosted on the λ plane. Each capacitor and inductor on the feedback network can change the point location. The change in feedback network can be reflected on the λ plane via the following formula: $\lambda = Y_{12}/Y_{21}$. We can judge the G_{ma} of an amplifier by analyzing how far the point of G_{ma} is from the point of the G_{max} core. G_{ma} is 8.8 dB without a feedback network, and the G_{max} is 14.6 dB.

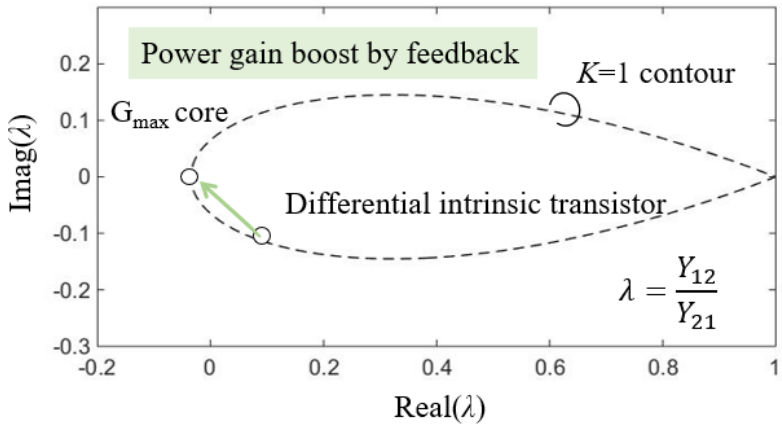


Figure 7. Gain boosted shown on the λ plain at 110 GHz.

4.2. PG Product

We have analyzed the method used to boost the power gain. The current and voltage will increase faster when K is near to 1 until they reach the limit. Naturally, based on the above analysis, the output power is the next object to be discussed.

Using quasi-linear analysis and BSIM4 model analysis, simulate the saturation power. The quasi-linear analysis is formulated utilizing Y-parameters, while the BSIM4 model is a form of the SPICE model. Distinct modeling approaches account for the variance between the quasi-linear analysis and the BSIM4 model. The BSIM4 model takes the physical

characteristics of the transistor into greater consideration. The simulation transistor has a channel length of 40 nm, and its total width is 32 µm when the multiplier is 4. Figure 8 shows the simulation result at 110 GHz, and the result using the BSIM4 transistor model is also shown for comparison. As predicted by (17) and (19), the saturation output power drops very quickly when K is approaching to 1. As the value of K deviates from 1, the saturation output power exhibits a relatively consistent stability. As depicted in Figure 8, under the same conditions, the saturation output power of the BSIM4 model is higher than that of the quasi-linear model. Nevertheless, when K approaches the vicinity of 1, both model outputs experience a rapid decrease in output power.

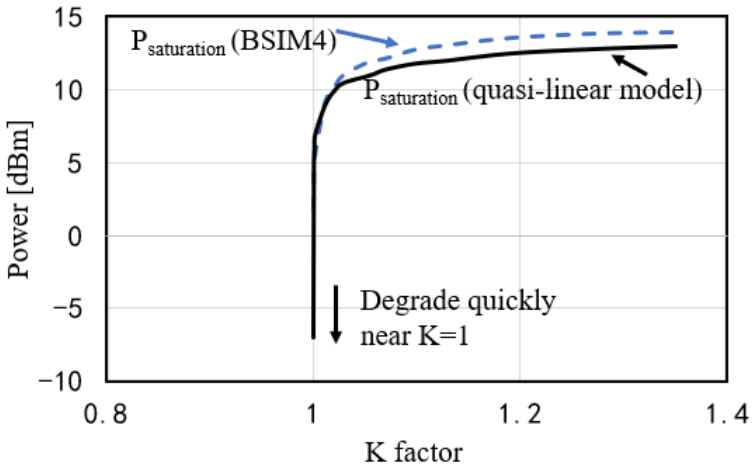


Figure 8. Simulated saturation output power versus K-factor at 110 GHz.

Based on the discussion above, it is not wise to boost the power gain very near to G_{max}, so we would like to discuss the trade-off between the gain and output power. In order to create a more accurate representation of the actual situation, the simulation is based on a large signal with the differential topology. The saturation power versus G_{ma} is drawn in Figure 9. The parallel slashes are the contour lines of the $P_{saturation}(\text{dBm}) + G_{ma}(\text{dB})$ product (PG product), the step of which is 10. The PG products on the same contour lines are equal, and their calculation formulas are shown in the figure. A substantial PG product is attainable only when both $P_{saturation}$ and G_{ma} values are elevated. Through assessing the PG product, we can effectively achieve a balance between $P_{saturation}$ and G_{ma}. Furthermore, the PG product can be calculated with varying coefficients based on the actual circumstances.

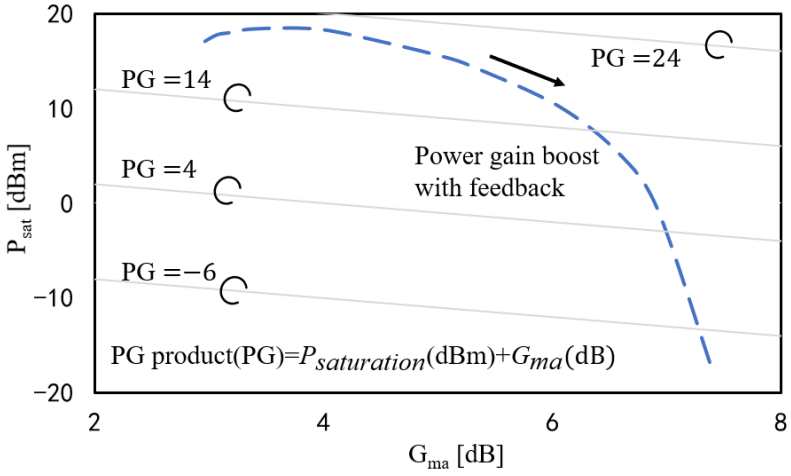


Figure 9. Saturation output power versus G_{ma}. The parallel slashes are the contour lines of the PG product.

If the PG product is considered as a kind of figure of merit (FoM), the gain boosting can be observed from a different angle. The gain boosting is relatively light on the left side of the cure, and the PG product does not suffer large decreases. The PG product decreases quickly when the gain boosting becomes heavy.

The closer the K-factor gets to 1, the higher G_{ma} is. For the design of the amplifier, the K-factor should be near to 1 but not too close. For the output power, we do not want the PG product to degenerate when the gain is boosted. Thus, from the view of output power management, the curve that shows when the PG product starts to decrease is the design target. Here, the curve simulated with BSIM4 should be used.

5. Six-Stage Feedback Amplifier

5.1. The Last Output Stage

The former stage should provide enough power for the latter stage. In the proposed six-stage amplifier, the total width of the transistors in the last three stages is gradually increasing. Generally, the design of the last stage is particularly important. Its output power and stability can heavily affect the performance of the entire amplifier. Given that the purpose of this stage is to deliver sufficient output power, in accordance with the PG product, we need to compromise some gain values. The size of the transistor is 32 µm/40 nm, with a total of 32 fingers and a multiplier of 4.

Figure 10a illustrates the variation in G_{ma} and saturation output power as the feedback capacitor changes, where C_f represents the feedback capacitor. Due to the wide range of saturation output power variations, a coefficient of 4 is applied to G_{ma} in order to ensure result coherence, resulting in the formula PG product = $P_{saturation}$(dBm) + 4 × G_{ma}(dB). Figure 10b shows the PG products versus different feedback capacitors. With a cross-coupling capacitor of 15.7 fF, there is a maximum PG product, making it suitable for constructing the feedback network. When the feedback capacitor is 15.7 fF, the calculated G_{ma} is 5.8 dB, with a saturation output power of 15 dBm at 110 GHz. At this point, the saturation power does not experience a rapid decrease, indicating the effectiveness of our design.

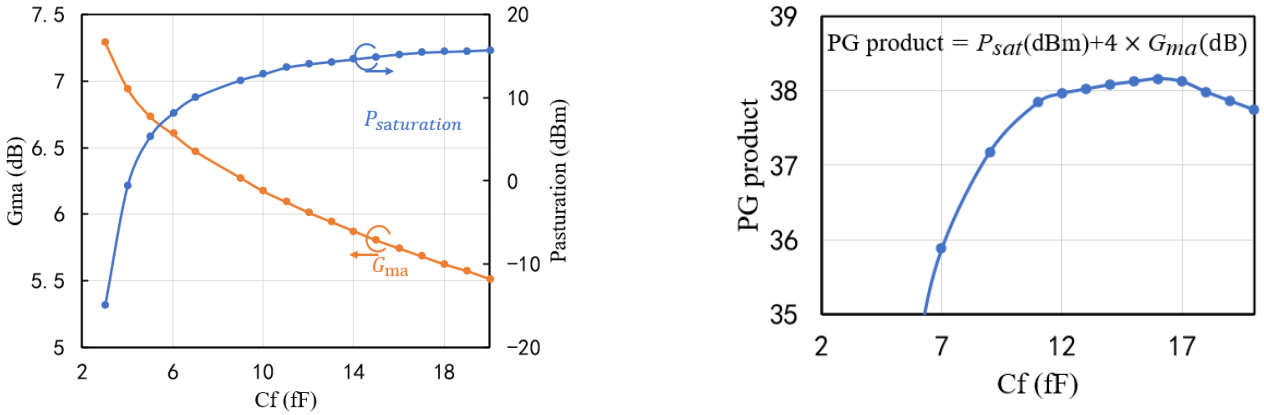


Figure 10. (**a**) The G_{ma} and saturation output power versus feedback capacitors. (**b**) PG products versus different feedback capacitors.

5.2. The Entire Amplifier

A 110 GHz feedback amplifier was designed using the proposed approach. The main targets for designing the amplifier include the output power and gain. The size of the output stage transistor determines the output power, while the number of stages affects the gain of the amplifiers. The design is based on the trade-off between power gain and output power, as quantified by the PG product. Figure 11 shows a schematic of the proposed amplifier; it consists of six pseudo-differential stages. Based on the equivalent relationship

between the single-ended and differential topologies from Section 4.1, two single-ended circuits form the pseudo-differential NMOS pair. The feedback network is embedded onto the pseudo-differential pair using cross-coupling capacitors. All stages use the λ plane approach to enhance gain and balance output power according to the PG product. The cross-coupling capacitors are linear, lossless, reciprocal feedback networks, which are used to move the G_{ma} point on the λ plane. There are three terms for why the feedback network only uses the capacitors in the proposed structure. First, from Section 4.2, the G_{max} is not the target of boosting gain. It is not necessary nor wise to achieve G_{max} accurately. Second, the feedback capacitor can provide sufficient moving range on the λ plane in the process of the proposed amplifier design. Third, the inductor will occupy a large area in the layout. In order to control the area of the amplifier chip, we only select the capacitor to form a feedback network.

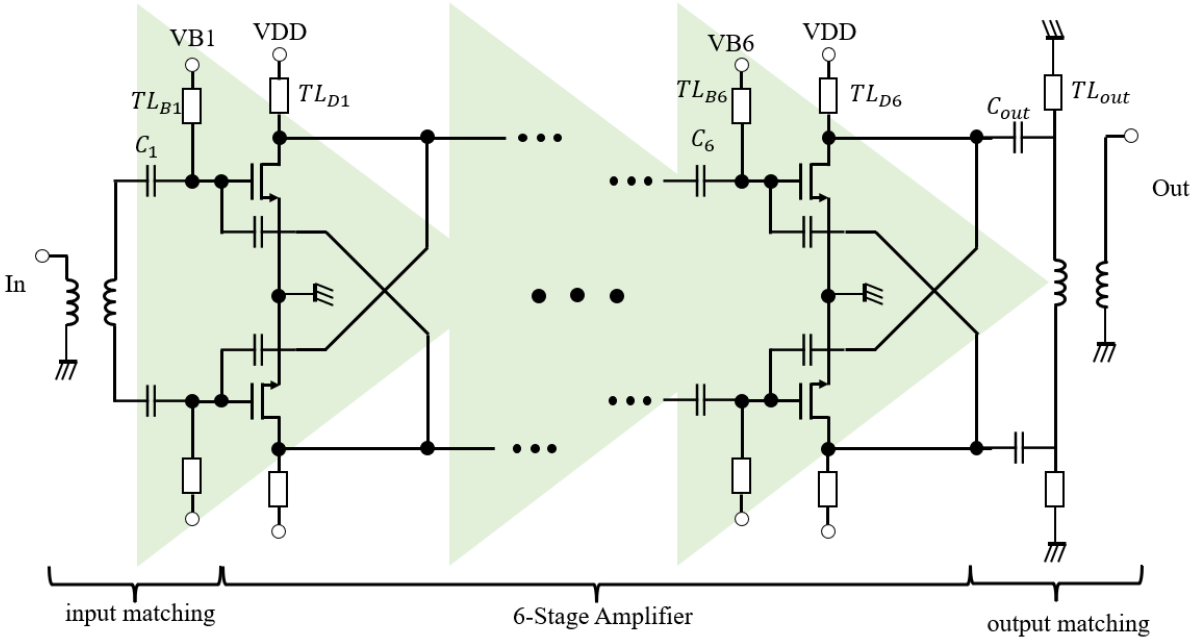


Figure 11. Schematic of the amplifier that balances power gain and output power.

The capacitor between the two stages of amplifier and transmission line TL_B constitutes the inter-stage matching; for example, C_6 and TL_{B6} constitute the inter-stage matching between the fifth and sixth stages. By tuning inter-stage matching, we can moderate the K-factor and output power of every stage. Additionally, this capacitor can also isolate the DC current. The supply voltage VDD is 1 V, and VB is 0.75 V. The gate and drain terminal voltage of the transistor are tuned and controlled by a transmission line with a characteristic impedance of 50 ohm.

The proposed amplifier design is separated into two parts. The first three stages are seized for gain where the NMOS size is 16 µm/40 nm, and the last three stages are seized for output power, where the NMOS sizes are 32 µm/40 nm, 64 µm/40 nm, and 128 µm/40 nm, respectively. Thus, the goals of the feedback networks for the two parts are also different. For the first three stages, the feedback capacitor is 4.6 fF in simulation. The fourth and fifth stages have a feedback capacitor that is 13.6 fF. The sixth stage of the amplifier utilizes a feedback capacitor with 15.7 fF.

The input and output impedance matching networks are also included in the design schematic shown in Figure 11. The transmission line TL_{B1}, capacitor C_1, and balun constitute the input matching. The output matching consists of three parts, namely C_{out}, parallel transmission lines TL_{out}, and balun.

6. Measurement

The proposed amplifier was fabricated via a 40 nm 10-Metal CMOS process and occupies an area of 820 µm × 950 µm (0.779 mm^2). Its micrograph is shown in Figure 12. The chip was measured on wafer. The input and output were probed using the Cascade Infinity WR8 waveguide probe. Keysight PNA-X and VDI mm-Wave extender were used to measure the S-parameters. The measured result includes the input and output pads. The measured and simulated results of the S-parameters are shown in Figure 13. The peak gain is 26.5 dB at 112 GHz. S_{11} is −18.5 dB at 102 GHz, and S_{22} is −12.8 dB at 118 GHz. The measured bandwidth is 14 GHz (from 104 GHz to 118 GHz). Due to the decreases in input, output matching, balun, and transmission lines, the peak of S_{21} is 7.8 dB lower than the simulated S-parameters.

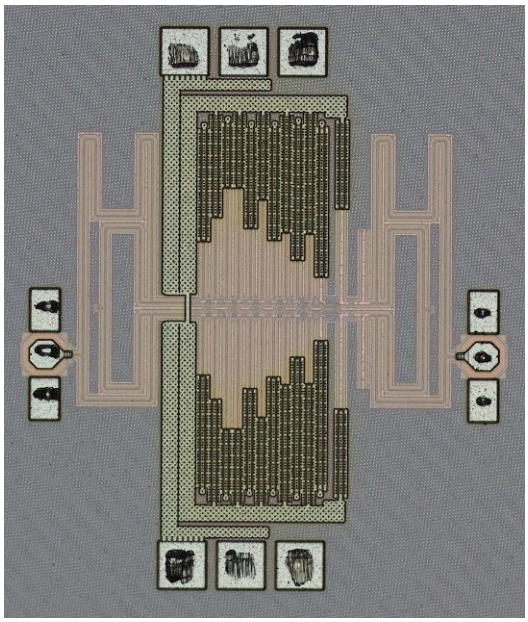


Figure 12. Photo of the proposed amplifier's chip.

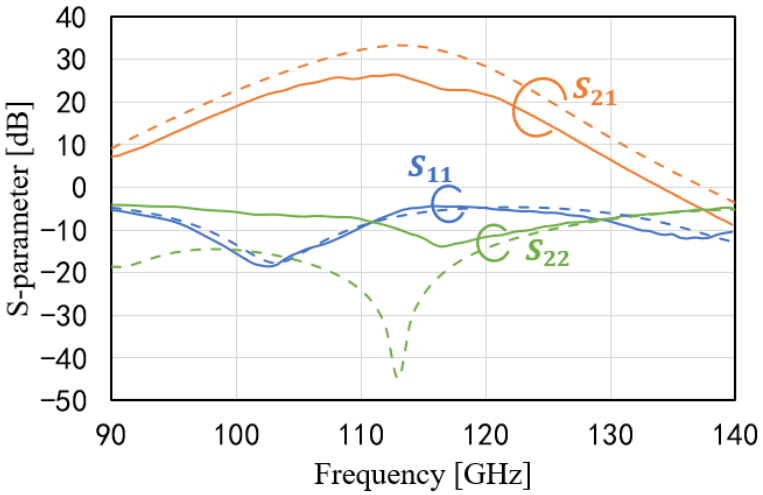


Figure 13. The measured and simulated S-parameters of the designed amplifier. The simulated parameters are represented by dashed lines, and the measured parameters are represented by solid lines.

The output power was measured using a power meter (Keysight PM5). As Figure 14 shows, the measured saturation power is 13 dBm, and the measured DC power consumption is 182 mW. Although the simulated circuit characteristics and actual circuit

characteristics are different. The measured results demonstrate the effectiveness of the proposed design approach in achieving a trade-off between power gain and output power. Table 1 summarizes the measured results in this work and shows a comparison with other state-of-the-art amplifiers.

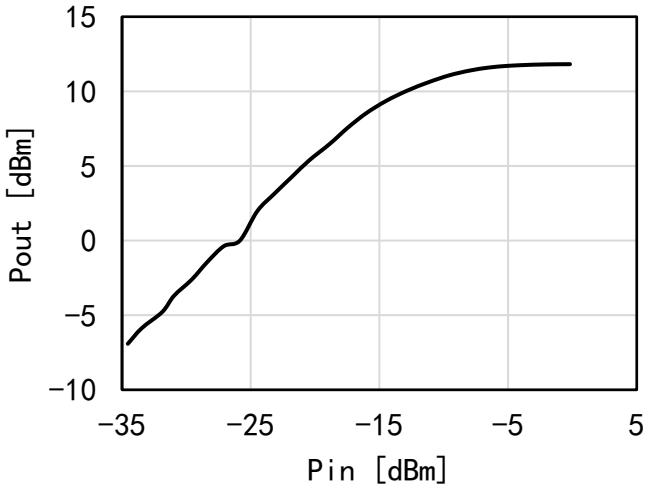


Figure 14. The measured output power.

Table 1. Performance summary for the proposed amplifier and comparison with state-of-the-art amplifiers.

Reference	This Work	[20]	[21]	[26]	[27]	[28]
Technology	40 nm CMOS	65 nm CMOS	28 nm CMOS	65 nm CMOS	130 nm BiCMOS	65 nm CMOS
Topology	Differential six-stage cascade	eight-stage cascade	Differential four-stage cascade	three-stage CS *	Full differential two-stage	Differential three-stage CS *
Frequency (GHz)	110	200	132	95	114	95
Gain (dB)	26.5	19.5	22.5	20	18.5	20.5
Saturation power (dBm)	13	9.4	8	13	11.8	13.4
Bandwidth (GHz)	104–118	195–209	121–143	92.5–98.5	N/A	88–100
Area (mm^2)	0.779	0.92	0.0265 **	0.11	0.35	0.025 **
DC power (mW)	182	732	N/A	74	231	170

* CS: Common-Source. ** Chip core area (excluding the pads).

7. Conclusions

For this paper, a 110 GHz six-stage CMOS power amplifier was designed and measured, considering the trade-off between power gain and output power. The power gain of the amplifier was discussed based on quasi-linearity analysis. We found that there are many demerits if the power gain is boosted to the G_{max}. To overcome the drawback of the G_{max}-core design method in the design power amplifier, a design approach based on the $P_{saturation} \times G_{ma}$ product was proposed so that a suitable trade-off between power gain and output power could be realized. To demonstrate the design method, a 110 GHz six-stages CMOS amplifier was designed. The fabricated amplifier realized a small-signal-power-gain of 26.5 dB and a saturation output power of 13 dBm at 110 GHz. The proposed amplifier is expected to have applications in mm-Wave and THz radar and communications systems.

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Data Availability Statement: All data used for this work can be made available upon reasonable request by contacting the corresponding author.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Based on Figure 2, the output current I_2 can be expressed as (A1a) and (A1b), which are based on Y-parameter.

$$I_2 = Y_{21}V_1 + Y_{22}V_2 \tag{A1a}$$

$$I_2 = -V_2Y_L \tag{A1b}$$

where V_2 is the output voltage and Y_L is the load admittance. Then, V_2 can be solved as (A2)

$$V_2 = \frac{-Y_{21}}{Y_L + Y_{22}}V_1 \tag{A2}$$

It is easy to know $V_1 = I_S/(Y_S + Y_{in})$, so the V_2 can be express as (A3).

$$V_2 = \frac{-Y_{21}}{Y_L + Y_{22}} \times \frac{I_S}{Y_s + Y_{in}} \tag{A3}$$

The input admittance Y_{in} can be expressed the formula as shown in (A4). If it is substitute into (A3), the V_2 can be expressed as (A5).

$$Y_{in} = Y_{11} - \frac{Y_{12}Y_{21}}{Y_L + Y_{22}} \tag{A4}$$

$$V_2 = \frac{-Y_{21}}{(Y_s + Y_{11})(Y_L + Y_{22}) - Y_{21}Y_{12}}I_S \tag{A5}$$

When the simultaneous conjugate impedance matching is realized, the source impedance and the load impedance are labeled with Y_{S_opt} and Y_{L_opt}, respectively, which are shown in (A6a) and (A6b) [25],

$$Y_{S\_opt} = \frac{Y_{21}Y_{12} + |Y_{12}Y_{21}|(\mathrm{K} + \sqrt{\mathrm{K}^2 - 1})}{2Re(Y_{22})} - Y_{11} \tag{A6a}$$

$$Y_{L\_opt} = \frac{Y_{21}Y_{12} + |Y_{12}Y_{21}|(\mathrm{K} + \sqrt{\mathrm{K}^2 - 1})}{2Re(Y_{11})} - Y_{22} \tag{A6b}$$

where $Re(Y_{11})$ and $Re(Y_{22})$ are the real part of Y_{11} and Y_{22}. If $Y_S = Y_{S\_opt}$ and $Y_L = Y_{L\_opt}$, then (A6a) and (A6b) are substituted into (A5). By some algebraic calculation, (A7) can be obtained finally.

$$V_2 = \frac{-2Re(Y_{11})Re(Y_{22})Y_{21}}{|Y_{21}Y_{12}|(Y_{21}Y_{12} + |Y_{21}Y_{21}|(\sqrt{\mathrm{K}^2 - 1} + \mathrm{K}))\sqrt{\mathrm{K}^2 - 1}}I_S \tag{A7}$$

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